
Frank Alberto SUN Microsystems, Inc., session chair
David McGregor DuPont iTechnologies
Bill Balliette 3M Electronic Solution Division
John Andresakis Oak-Mitsui Technologies, LLC
Cindy Gretzinger Sanmina-SCI, Owego
Bob Greenlee Merix Corporation
Lance P. Riley Unicircuit, Inc.
Steve Patrick Benchmark Electronics, Inc.
John Grebenkemper NonStop Enterprise Division, Hewlett-Packard Company
Istvan Novak SUN Microsystems, Inc.
Abstract

At DesignCon 2002, a TecForum titled "Thin PCB Laminates for Power Distribution: How Thin Is Thin Enough?" brought together five representative OEMs, three PCB fabricators, and three material suppliers to answer these questions: How thin is thin enough? When will these thin laminates be needed? Will the industry be ready? Since then there has been progress in the available laminates, in their agency approval status, and in the experience collected with them.

This TecForum reviews the thin laminate availability in 2004.
Background

DesignCon 2002
High-Performance System Design Conference

TecForum HP-TF2
Thin PCB Laminates for Power Distribution
How Thin is Thin Enough?

Presenters:
Ben Beker  AMD
Rick Charbonneau StorageTek
Valerie St. Cyr (*) SUN Microsystems, Inc
Bob Greenlee  Merix Corporation
John Grebenkemper Compaq Computer Corporation
Jason Gretton Aromat Corporation (a Matsushita company)
James Howard Sanmina Corporation
Kang Hsu  Wus Printed Circuit Co. Ltd.
David McGregor DuPont iTechnologies
Istvan Novak (*) SUN Microsystems, Inc.
Joel S. Peiffer 3M
Robert Sheffield Nortel
Thin Laminate Nomenclature

The diagram represents the dielectric thickness in mils for different categories:

- **Fine Line**
  - Min: 2.00
  - Nom: 3.00
  - Max: 4.00

- **Thin**
  - Min: 1.00
  - Nom: 2.00
  - Max: 3.00

- **Very Thin**
  - Min: 0.30
  - Nom: 0.70
  - Max: 1.00

- **Ultra Thin**
  - Min: 0.10
  - Nom: 0.20
  - Max: 0.30

- **Extra Thin**
  - Min: 0.01
  - Nom: 0.05
  - Max: 0.10

DesignCon 2004, TF09
DuPont Electronic Technologies
Thin and Very Thin Laminates

David R. McGregor
DesignCon 2004  February 2, 2004
Planar Capacitor Thin Laminates

Available Laminates

18* and 25 μ unfilled laminates

14 and 25 μ filled laminates

* Developmental
Impact of Thin Laminate on SMT Capacitor Removal

• High Speed Video board made conventionally and with 25 micron unfilled polyimide laminate.
• Removed over 400 bypass capacitors on thin laminate board.
• Board operated identically without these capacitors when using the thin laminate (Active devices worked as designed, radiated EMI improved, signal noise reduced).

Conventional Board with SMT Caps

Board with thin laminate and SMT Caps Removed
Thinner Dielectric Reduces Impedance

Courtesy of Sun Microsystems
Interra™ HK 111436R

Courtesy EIT

Courtesy Merix
Unfilled Thin Laminate: Inter™ HK 04

Physical Properties:
D. R. McGregor

- **Dielectric:** Polyimide
- **Peel Strength:** 10 pli
- **CTE:** 25 ppm/°C
- **Water Absorption:** 0.8% (100% RH for 48 hours)
- **UL Flammability:** UL94 V-0
- **RTI, mech/elec:** 200° C / 240° C
- **Dissimilar Materials w/FR-4:** Complete. This test not required for fabricator.
- **Debond/Delam:** This test required to be done by each fabricator.

Electrical Properties:

- **Dielectric Constant:** 3.4
- **Capacitance Density:** 0.8 nF/in² (measured at 1 MHz)
- **Dissipation Factor:** 0.003 (measured at 1 MHz)
- **Breakdown Voltage:** 6000 Volts/mil
- **HiPot Voltage:** >1500 Volts DC
Unfilled Thin Laminate: Interra™ HK 04

Temperature Coefficient of Capacitance for Interra(tm) HK 04

Percent Change (%)

Temperature (degree C)

-55 -35 -15 25 45 65 85 105 125

-4.00 -3.00 -2.00 -1.00 0.00 1.00 2.00 3.00 4.00

Moisture and Insulation Resistance Interra(tm) HK 04 [ohm]

HK04 Dry HK04 85/85

Moisture Effect on Dk

Dielectric Constant [-]

815 1280 1894 2551 3226 3909 4596 5286

3.0 3.2 3.4 3.6 3.8 4.0 4.2 4.4 4.6 4.8 5.0

Equivalent capacitance [F]

3.0E-08 3.2E-08 3.4E-08 3.6E-08 3.8E-08 4.0E-08

1.0E+05 1.0E+06 1.0E+07 1.0E+08

Measurement artifact

Courtesy of Sun Microsystems

D. R. McGregor

DesignCon 2004

February 2, 2004
Filled Thin Laminate:  
Interra™ HK 10

**Physical Properties:**

- **Dielectric:** Polyimide with Barium Titanate Filler
- **Peel Strength:** 8 pli
- **CTE:** 46 ppm/°C
- **Water Absorption:** 0.7% (100% RH for 48 hours)
- **UL**
  - **Flammability:** UL94 V-0
  - **RTI:** 130° C
  - **Dissimilar Materials w/FR-4:** Pending.

**Electrical Properties:**

- **Dielectric Constant:** 10
- **Capacitance Density:** 2.2 nF/in² (measured at 1 MHz)
- **Dissipation Factor:** 0.01 (measured at 1 MHz)
- **Breakdown Voltage:** 3100 Volts/mil
- **HiPot Voltage:** 250 Volts DC
Filled Thin Laminate: Interra™ HK 10

Temperature Coefficient of Capacitance for Interra(tm) HK 10

Moisture and Insulation Resistance Interra(tm) HK 10 [ohm]
Filled Very Thin Laminate: 
Interra™ HK 11

**Physical Properties:**
- Dielectric: Polyimide with Barium Titanate Filler
- Peel Strength: 13 pli
- Water Absorption: 0.5% (100% RH for 48 hours)
- UL
  - Flammability: UL94 V-0
  - RTI: 130° C
  - Dissimilar Materials w/FR-4: Pending.

**Electrical Properties:**
- Dielectric Constant: 11
- Capacitance Density: 4.5 nF/in² (measured at 1 MHz)
- Dissipation Factor: 0.02 (measured at 1 MHz)
- Breakdown Voltage: 2500 Volts/mil
- HiPot Voltage: 100 Volts DC
Filled Very Thin Laminate:
Interra™ HK 11

Capacitance Response with Increasing Frequency

Measurement artifact

Courtesy of Sun Microsystems
Planar Capacitor Highlights

- Excellent overvoltage protection
- High capacitance density
- Low impedance
- Reduced EMI
- Excellent peel strength
- Frequency Response
- Significant product history
- Commercial products

- Unfilled > 6000 V BDV
  > 1500 V HiPot
- HK 11 = 4.5 nF/in² (0.7 nF/cm²)
- All > 6 pli
- Capacitance stable with frequency
- HK 04 built on Pyralux® AP technology
- 3 commercial laminates; 1 in development
Summary

• Planar capacitor laminates are commercial products offering superior overvoltage protection, high capacitance density, reduced impedance, and high reliability.
Ultra-Thin, Loaded Epoxy Materials for Use as Embedded Capacitor Layers

Bill Balliette
3M - Austin
(512) 984-7324
wmballiette@mmm.com
Why Embedded Capacitance?

1. Performance
2. Space
3. Cost
## Reasons for Embedded Capacitance

<table>
<thead>
<tr>
<th>Potential Benefits</th>
<th>Performance</th>
<th>Space</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Faster signaling/Reduce power bus noise</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reduce design time &amp; redesigns</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Eliminate capacitors</td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Reduce layer count</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Enable DS to SS assembly</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reduce via count</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Simplify rework</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Reduce board size, thickness</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reduce assembly time</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Enable decoupling w/back-side heat sinks</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reduce weight</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reduce opportunities for damaged components</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Improve PWB panel utilization</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reduce EMI</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
</tbody>
</table>
Thin-Film Capacitor Technology

- Capacitance per unit area (C/A) is proportional to $k$ and inversely proportional to $t$.
- Vary C/A by varying thickness ($t$) or dielectric constant ($k$).
# 3M™ Embedded Capacitor Material

## Key Properties

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitance /area</td>
<td>5.5 nF/in2*</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td>16</td>
</tr>
<tr>
<td>Dielectric loss @ 1GHz</td>
<td>0.03</td>
</tr>
<tr>
<td>Resin system</td>
<td>Epoxy, ceramic filler</td>
</tr>
<tr>
<td>Freq., Voltage, Temperature</td>
<td>Meets X7R</td>
</tr>
<tr>
<td>Dielectric Strength</td>
<td>~130V/um</td>
</tr>
<tr>
<td>Breakdown Voltage</td>
<td>&gt;100V**</td>
</tr>
<tr>
<td>Copper Thickness</td>
<td>35 um</td>
</tr>
<tr>
<td>Flammability Rating</td>
<td>94V-0</td>
</tr>
</tbody>
</table>

* For 16 um dielectric thickness. Thinner dielectrics in development

** Higher breakdown voltages in development
Impedance Comparison

Self-Impedance Magnitude at J501

Impedance magnitude [ohm]

Frequency [Hz]

2 mil
1 mil
0.3 mil

3M (8 um)

Bare board

Impedance and EMC Characterization

APEX '01
January 2001
Power Bus Noise on Test Vehicle

- Traditional decoupling capacitors are not effective at frequencies above 1 GHz
- 3M has excellent performance to 5 GHz

Data from NCMS Embedded Decoupling Capacitance Project Report - 12/00
Power Bus Noise
(Time Domain - 50 MHz)

Data from NCMS Embedded Decoupling Capacitance Project Report - 12/00
Radiated Emissions Comparison

Close-Field Radiation J501-J603

Relative radiation field [dB]

-4.0E+01
-6.0E+01
-8.0E+01
-1.0E+02
-1.0E+02
1.00E+06  1.00E+07  1.00E+08  1.00E+09

Frequency [Hz]

2 mil
1 mil
0.3 mil

3M (8 um)

Bare board

Impedance and EMC Characterization
### Examples of Embedded Capacitance Replacing Discretes

<table>
<thead>
<tr>
<th>Design</th>
<th>Discrete Capacitance Removed (nF)</th>
<th>Embedded Capacitance (nF)</th>
<th>Ratio of Removed to Embedded</th>
<th>% of Total Discrete Capacitance Removed</th>
</tr>
</thead>
<tbody>
<tr>
<td>EDC TV1</td>
<td>330 (33 \times 0.01 \mu F)</td>
<td>105</td>
<td>3.1</td>
<td>100%</td>
</tr>
<tr>
<td>OEM A</td>
<td>12,600 (126 \times 0.1 \mu F)</td>
<td>300</td>
<td>42.0</td>
<td>NA</td>
</tr>
<tr>
<td>OEM B</td>
<td>6,310 (62 \times 0.1 \mu F)</td>
<td>210</td>
<td>30.0</td>
<td>&gt;60%</td>
</tr>
<tr>
<td>OEM C</td>
<td>3,180 (29 \times 0.1 \mu F)</td>
<td>~300</td>
<td>~10.6</td>
<td>&gt;75%</td>
</tr>
<tr>
<td>OEM D</td>
<td>52,900 (529 \times 0.1 \mu F)</td>
<td>1969</td>
<td>26.9</td>
<td>&gt;75%</td>
</tr>
</tbody>
</table>
Benefits of Embedded Capacitance for Power-Ground Decoupling

- Lowers impedance of power distribution system
- Dampens board resonances
- Reduces noise on power plane
- Reduces radiated emissions
- More effective than discrete capacitors for decoupling high frequencies. Can replace large numbers of capacitors in high speed digital designs
## Environmental Testing

<table>
<thead>
<tr>
<th>Test</th>
<th>Property</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>High Temp (125°C)</strong></td>
<td>Capacitance</td>
<td>No Change (1000 hrs)</td>
</tr>
<tr>
<td><strong>Thermal Cycle</strong></td>
<td><strong>Thermal Shock</strong></td>
<td><strong>Capacitance</strong></td>
</tr>
<tr>
<td><strong>High Humidity</strong></td>
<td>(85°C/85% RH)</td>
<td><strong>Capacitance</strong></td>
</tr>
<tr>
<td><strong>TMA (T260)</strong></td>
<td><strong>Dissipation Factor</strong></td>
<td><strong>Life</strong></td>
</tr>
<tr>
<td><strong>THB</strong> (85°C/85%RH/15 V)</td>
<td><strong>Life</strong></td>
<td><strong>Life</strong></td>
</tr>
<tr>
<td><strong>ESD</strong> (2-25 kV)</td>
<td><strong>Capacitance/D.F.</strong></td>
<td><strong>No change</strong></td>
</tr>
<tr>
<td><strong>Bend Test</strong></td>
<td><strong>Capacitance</strong></td>
<td>No change (200 cycles)</td>
</tr>
<tr>
<td><strong>Multiple Reflow (3X)</strong></td>
<td><strong>Capacitance</strong></td>
<td><strong>No change</strong></td>
</tr>
</tbody>
</table>

*Returned to pre-test level after bake*
## UL Testing

<table>
<thead>
<tr>
<th>Test</th>
<th>Property</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Laminate</td>
<td>Flammability</td>
<td>94V-0</td>
</tr>
<tr>
<td>Laminate</td>
<td>Solderability Limits</td>
<td>288C/30 sec</td>
</tr>
<tr>
<td>Laminate</td>
<td>Relative Thermal Index</td>
<td>130C</td>
</tr>
<tr>
<td>Board (Merix)</td>
<td>Flammability</td>
<td>94V-0</td>
</tr>
<tr>
<td>Board (Merix)</td>
<td>Max Operating Temp</td>
<td>130C</td>
</tr>
</tbody>
</table>
PCB Processing - 1

- Compatible with all rigid and flex PCB processing (including laser ablation)

- Material handling is most significant issue (compares to bare 2 ounce copper)

- A sequential lamination process is recommended
  - Pattern 1\textsuperscript{st} side copper
  - Laminate patterned side to another layer of prepreg
  - Pattern 2\textsuperscript{nd} side copper
PCB Fabrication - 2

- If a sequential lamination process is utilized, there are no design limitations

- Many high end fabricators have successfully fabricated numerous prototype lots
  - Over 25 board designs have been manufactured by a dozen fabricators for 17 different OEMs
  - Additional fabricators have demonstrated process capability
Conclusion

• 3M Embedded Capacitance Material offers a high capacitance density of 5.5 nF/in². (Future products will offer even higher capacitance density.)

• Delivers many electrical benefits when used for power-ground decoupling

• Compatibility with fabrication has been demonstrated multiple times

• The product is available for sale, has UL approval, and can be manufactured in volume

For more information:
http://www.3m.com/us/electronics_mfg/microelectronic_packaging/
Performance of Polymeric Ultra-thin Substrates For use as Embedded Capacitors: Comparison of Unfilled and Filled Systems with Ferroelectric Particles

John Andresakis, Takuya Yamamoto, Pranabes Pramanik
Oak-Mitsui Technologies, LLC
Nick Biunno
Sanmina-SCI Corporation

DesignCon 2004
February, 2004
Product Design

Construction

12 µm

\{ 12 micron Polymer Dielectric \}

16 µm

\{ 16 micron Polymer Dielectric with Hi-Dk Filler \}

(16 µm with Filler is under development)

16 µm

\{ 16 micron Polymer Dielectric \}

24 µm

\{ 24 micron Polymer Dielectric \}

-Standard Copper thickness is 35 µm
### Electrical Properties

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Condition</th>
<th>Unit</th>
<th>24µm</th>
<th>16µm</th>
<th>12µm</th>
<th>8µm</th>
<th>16µm-Filler</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitance</td>
<td>1GHz</td>
<td>nF/cm²</td>
<td>0.14</td>
<td>0.23</td>
<td>0.31</td>
<td>0.45</td>
<td>1.75</td>
</tr>
<tr>
<td>Dk</td>
<td>1GHz</td>
<td>N/A</td>
<td>4.4</td>
<td>4.4</td>
<td>4.4</td>
<td>4.4</td>
<td>30.0</td>
</tr>
<tr>
<td>Df</td>
<td>1GHz</td>
<td>N/A</td>
<td>0.015</td>
<td>0.015</td>
<td>0.015</td>
<td>0.016</td>
<td>0.019</td>
</tr>
<tr>
<td>Dielectric Thickness</td>
<td>Nominal</td>
<td>Micrometer</td>
<td>24</td>
<td>16</td>
<td>12</td>
<td>8</td>
<td>16</td>
</tr>
</tbody>
</table>
## Physical Properties

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Condition</th>
<th>Unit</th>
<th>24µm</th>
<th>16µm</th>
<th>8&amp;12µm</th>
<th>16µm-Filler</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tg</td>
<td>DMA</td>
<td>Celsius</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>Peel Strength</td>
<td>As received</td>
<td>lb/in</td>
<td>8.0</td>
<td>8.0</td>
<td>8.0</td>
<td>6.0</td>
</tr>
<tr>
<td>Young’s Modules</td>
<td>JIS 2318</td>
<td>GPA</td>
<td>4.8</td>
<td>5.8</td>
<td>7.2</td>
<td>NA</td>
</tr>
<tr>
<td>Tensile Strength</td>
<td>JIS 2318</td>
<td>MPa</td>
<td>180</td>
<td>180</td>
<td>180</td>
<td>NA</td>
</tr>
<tr>
<td>CTE (x,y)</td>
<td>IPC TM650</td>
<td>PPM</td>
<td>23</td>
<td>23</td>
<td>28/23</td>
<td>TBD</td>
</tr>
<tr>
<td>Breakdown</td>
<td>1kV/sec</td>
<td>V</td>
<td>&gt;5000</td>
<td>&gt;4000</td>
<td>&gt;4000</td>
<td>TBD</td>
</tr>
<tr>
<td>Insulation Reliability</td>
<td>85C/85%/35V</td>
<td>hr</td>
<td>&gt;1000</td>
<td>&gt;1000</td>
<td>&gt;1000</td>
<td>&gt;1000</td>
</tr>
</tbody>
</table>

NA- Not Applicable since material is not self supporting
**PWB Manufacturing Process**

**Thin Substrate without Particles**
1. Pre-Clean
2. Dry Film lamination
3. Expose Image
4. Pattern etching (Both sides)
5. Black Oxide or Alternative

**Thin Substrate with Particles**
1. Pre-Clean
2. Dry Film lamination
3. Expose Image (Pattern/Blanket)
4. Pattern etching (One side)
5. Black Oxide or Alternative
6. Laminate Prepreg/Cu to Imaged Side
7. Pre-Clean
8. Dry Film Laminate
9. Expose Image (Both Sides)
10. Pattern Etching (Both Sides)
11. Black Oxide or Alternative
PWB Manufacturing Process

DIMENSIONAL CHANGE: COMPATIBLE WITH FR-4 CORE

12 µm CAPACITOR
Summary of Unfilled Substrates (approx. 1200 panels)

- Substrates Processed at 10 Major PCB Facilities
- Standard I/L Processing
- Results
  1. No loss due to jams
  2. No “blow out” of Clearance holes
  3. No separation from border pattern
  4. 99+ % Yield (due to material issues) at Hi-Pot (500 Volts)
  5. Both Vertical Racked Black Oxide and Alternative Oxide used successfully
- PWBs available from ZBC™ Licensed Fabricators

ZBC™ - Is a trademark of HSCI
Summary of Filled Substrates(<110 panels)

- Substrates Processed at 2 Major PCB Facilities
- Standard I/L Processing with additional steps
- Results
  1. No loss due to jams
  2. No “blow out” of Clearance holes
  3. No separation from border pattern(Cu to edges)
  4. 100 % Yield at Hi-Pot (100 Volts) (limited quantity)
  5. Both Vertical Racked Black Oxide and Alternative Oxide used successfully
  6. Registration between buried and outer core layers on subassembly critical

- PWBs available from ZBC™ Licensed Fabricators

ZBC™ - Is a trademark of HSCI
Availability

- 12,16 and 24 micron unfilled materials are commercially available
- 1 oz. Copper is standard and can be delivered quickly (other copper weights will take longer initially until inventory established)
- 8 micron unfilled and 16 micron filled materials available for testing (commercially available by 2Q04)

Cost/ft²

- Quotes available upon request
- Competitive with other sub 1 mil materials
- Price reductions in future based on production optimization and reduced raw material prices.
Reliability Tests

- Dielectric Withstanding Voltage: 500V Passed, No failure
- T-260 Time to Delamination: 12 µm - 6.3min, 24 µm - 5.2min
- Blind Via Plating Defects: No defects found
- Thermal Solder Shock (288ºC)– 10x: No defects found
- Liquid-Liquid: 24 µm 4.2%(500 cycle)
- IST Testing: Passed 500 Cycles

Approvals

- Unfilled 12, 16 and 24 micron materials are UL approved (94VO, 130 Operating Temp.)
- PCB Shops submitting their UL samples (2 already submitted)
- Telcordia samples being prepared
- 8 micron unfilled and 16 micron filled materials are in for UL approval
PWB Electrical Performance (Self Z)

Significant Reduction on Impedance

![Graph showing impedance vs. frequency for different thicknesses of material with and without BaTiO3.](image)
PWB Electrical Performance (Transfer Z)

Significant Reduction on Impedance

Transfer Z Profiles at 1" Separation

Transfer Z High Frequency Response

Data Courtesy of Sammna-SCI Corp.

- 8 micron
- 16 micron with BaTiO₃
Significant Reduction of EMI

MPU (40MHz) is mounted on the other side of the board.

SMA connector
Vcc(3.3V)

MPU

4 LAYER BOARD

P.P 0.6mm

P.P 0.6mm

Capacitor Core
AND CONVENTIONAL CORE

8 µm, 16 µm Filled

24 micron core
12 micron core

DIFFICULT FREQUENCY RANGE TO REDUCE NOISE BY DISCRETE COMPONENTS

CONDUCTED EMISSION NOISE (dBuV)

FREQUENCY OF NOISE (MHz)
## Comparison Summary

### Unfilled Substrates Versus Filled Substrates

<table>
<thead>
<tr>
<th>Property</th>
<th>Unfilled Thin Substrates</th>
<th>Filled Substrates</th>
</tr>
</thead>
<tbody>
<tr>
<td>Impedance Reduction/lower noise</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>Electric Strength/ High Potential Testing</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>Ease of PCB Processing</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>Cost of Substrate/Raw Board</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>Cost of Assembled Board</td>
<td>?</td>
<td>?</td>
</tr>
</tbody>
</table>
Conclusion

- Thinner Power Distribution Planes are required for improved Impedance Performance at high frequency
- New Substrates have demonstrated excellent electrical performance and physical properties.
- They are compatible with PWB processing; a truly “drop in” material.
- Materials are commercially available from Licensed Fabricators
- The use of Embedded Capacitance can simplify PCB lay-out and reduce the number of prototypes required.
- The Technology can Improve System Price/Performance by
  - Reducing Discrete Caps
  - Reducing PWB size
  - Increasing Functionality
- Substrates Filled with Ferroelectric Particles have better performance, but result in higher cost PWBs
- Additional work is ongoing to
  - Improve PWB manufacturing process of filled substrates
Thin and Very Thin Core Laminates: Processing and Reliability

Cindy Gretzinger
Inner Layer Engineering Manager – Owego Division

Chad Kormanek
Materials Engineer – Owego Division
Topics of Discussion

- Manufacturability
  - Thin Core Material Experience
  - Thin Core Processing Capabilities
  - Material UL Status
- Reliability
  - Thermal Analysis –T260
  - Interconnect Stress Testing (IST)
    - Test Equipment
    - Test Design
  - Assembly Rework Simulation
    - Solder Float Testing
    - Multiple Pass Through Reflow
Manufacturability:
Thin Core Material Experience

ZBC-2000®: 2 mil thick material

- Over 10 years experience in processing
  - >10 million square feet processed
  - Known & established material in the market


- Quality Controlled:
  Patented: 9 US Patents, 22 Foreign Patents
  Common standards guarantee quality and consistency of material.
  Material testing and qualification program.
  Web site being established for sharing of BC™ information.
  Fully tested, high frequency electrical performance of BC materials.
Manufacturability:
Thin Core Material Experience

- **< 0.5 mil Cores – Very Thin - Ultra Thin**
  - Oak Mitsui BC12™ (12 micron core)
  - Oak Mitsui 8 -10 micron cores
  - 3M C-Ply (8 micron core)

- **0.6 mil Core – Very Thin**
  - Oak Mitsui BC16™ (16 micron core)

- **1 mil Core – Thin**
  - ZBC-1000™ (25.4 micron core)
  - Oak Mitsui BC24™ (24 micron core)
  - Dupont HK04 (25 micron core)

- **2 mil Cores – Fine Line**
  - ZBC-2000® (2 mil [50.8 micron] core)
# Manufacturability: Thin Core Processing Capabilities

## Table of Thin Core Processing Capabilities as Compared to a ZBC-2000 Baseline

<table>
<thead>
<tr>
<th>Process</th>
<th>ZBC-1000</th>
<th>24 Micron Non-Reinforced</th>
<th>16 Micron Non-Reinforced</th>
<th>8-12 Micron Non Reinforced</th>
</tr>
</thead>
<tbody>
<tr>
<td>PreClean/Lamination</td>
<td>Thin core equipment required – no leaders</td>
<td>Thin core equipment required – no leaders</td>
<td>Thin core equipment required – Laminate one side at a time</td>
<td>Thin core equipment required – Laminate one side at a time</td>
</tr>
<tr>
<td>Expose</td>
<td>Standard process</td>
<td>Standard process</td>
<td>Standard process</td>
<td>Standard process</td>
</tr>
<tr>
<td>Develop, Etch, Strip</td>
<td>Thin core equipment required – no leaders</td>
<td>Thin core equipment required – no leaders</td>
<td>Thin core equipment required – leaders required</td>
<td>Thin core equipment required – leaders required</td>
</tr>
<tr>
<td>Post Etch Punch</td>
<td>Front/Manual Unloading Required</td>
<td>Front/Manual Unloading Required</td>
<td>Front/Manual Unloading Required</td>
<td>Front/Manual Unloading Required</td>
</tr>
<tr>
<td>AOI</td>
<td>Standard process</td>
<td>Standard process</td>
<td>Standard process</td>
<td>Standard process</td>
</tr>
<tr>
<td>Oxide</td>
<td>Horizontal or vertical acceptable</td>
<td>Horizontal or vertical acceptable</td>
<td>Horizontal or vertical acceptable, support needed in baskets</td>
<td>Horizontal or vertical acceptable, support needed in baskets</td>
</tr>
<tr>
<td>Lay Up</td>
<td>Standard process</td>
<td>Standard process</td>
<td>Modified Handling</td>
<td>Modified Handling</td>
</tr>
</tbody>
</table>
Manufacturability: Thin Core Processing Capabilities

Thin Core Conveyor Transport

**Manufacturability:**

**Thin Core Processing Capabilities**

**Dimensional Stability**

<table>
<thead>
<tr>
<th></th>
<th>Repeatability – Width</th>
<th>Repeatability – Length</th>
<th>Movement Deviation – Width (from baseline)</th>
<th>Movement Deviation – Length (from baseline)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZBC-2000 (Baseline)</td>
<td>+/- 1.0 mils</td>
<td>+/- 0.5 mils</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>FaradFlex BC24 µm</td>
<td>+/- 0.7 mils</td>
<td>+/- 0.7 mils</td>
<td>- 0.07 mils/in</td>
<td>0.02 mils/in</td>
</tr>
<tr>
<td>Faradflex BC16 µm</td>
<td>+/- 0.8 mils</td>
<td>+/- 0.6 mils</td>
<td>- 0.06 mils/in</td>
<td>- 0.02 mils/in</td>
</tr>
<tr>
<td>Polyimide 25 micron</td>
<td>+/- 0.9 mils</td>
<td>+/- 1.0 mils</td>
<td>-0.07 mils/in</td>
<td>0.04 mils/in</td>
</tr>
</tbody>
</table>

**Based on one Commercial Part Number, 24 layer board**
**Manufacturability: Thin Core Processing Capabilities**

<table>
<thead>
<tr>
<th></th>
<th>ZBC 2000 (50 micron)</th>
<th>Interra HK04 (25 micron)</th>
<th>Farad Flex BC24 (25 micron)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Foreign Material</td>
<td>Rework 6.1%</td>
<td>Rework 28%</td>
<td>Rework 7.7%</td>
</tr>
<tr>
<td></td>
<td>Scrap 0.6%</td>
<td>Scrap 2%</td>
<td>Scrap 0%</td>
</tr>
<tr>
<td>Material Damage</td>
<td>Scrap 2.6%</td>
<td>Scrap 8.0%</td>
<td>Scrap 3.8%</td>
</tr>
<tr>
<td>Core Material</td>
<td>90.7%</td>
<td>62%</td>
<td>88.5%</td>
</tr>
<tr>
<td>First Pass Yield</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Core Material</td>
<td>96.8%</td>
<td>90%</td>
<td>96.2%</td>
</tr>
<tr>
<td>Second Pass Yield</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Yields are based on one Commercial part number with 2 Thin cores
Manufacturability:
Thin Core Processing Capabilities

Foreign Inclusion Testing
The higher the inclusion rate, the longer the processing time in AOI & increased chance of scrap at Electrical Test.
Manufacturability: Material UL Status

- ZBC-2000 – Approved
- ZBC-1000 – Approved
- Oak-Mitsui FaradFlex:
  - BC12 – Approval March 04
  - BC16 – Approval March 04
  - BC24 – Approval March 04
- DuPont Interra HK04 - Approved
Reliability: Thermal Analysis - T260

Thermal Mechanical Analysis TMA

- Measure expansion of a sample (X, Y, or Z) as a function of temperature

- Measure % Z-axis Expansion from 50º C to 260º C

- Time to Delamination at 260º C

- No Failures found on any Thin Core Materials to date

- Goal: Further test the thermal reliability of Thin Laminates to induce possible failures on the Thin cores using phenolic materials and TMA up to 288º C
Reliability:
Interconnect Stress Testing (IST)
Test Equipment

- Test the reliability of PTH and innerlayer post to barrel connection over a period of thermal cycles
- Thermal cycles are made using DC current to heat up the coupon and air cooling to reduce the temperature.
- Resistance changes are checked through the PTH and across the post to barrel connection
- Testing is coupon design dependant
IST Testing

- IST Test Design: 8 layer Sun Test Vehicle and 26 layer Commercial Part with two Thin Core Layers, 24 layer Commercial Part with four Thin Core Layers.

- Results: IST cycles average the same as with standard FR4 layers. No failures found at the Thin core layers.

- Further Testing: Test through hole reliability by using Phenolic Materials and new Coupon Designs to induce failures on the Thin Core Layers
  - Final board thickness of ~ 0.095” (18 Layers)
  - Heater cores positioned at the 4/5 and (n-3)/(n-4) layers
Reliability: Assembly Rework Simulation

- Solder Float Testing
  - 6 x Solder Shock Blind Vias
  - 6 x Solder Shock Through Holes
  - No failures on testing done to date

- Further Testing
  - Solder Shock Testing with Phenolic Materials
  - Multiple Pass - 8x Through Reflow
  - Process at a local assembly shop in a 10 zone convection oven
Reliability: Assembly Rework Simulation

- 6x Solder Float Testing on Through Holes

ZBC-1000

Faradflex 16 µm

Faradflex 24 µm

Dupont 25 µm
Reliability: 
Assembly Rework Simulation

- 6x Solder Float Testing on Blind Vias

ZBC-1000

Faradflex 24 µm

Faradflex 16 µm

Dupont 25 µm

## Test Summary

<table>
<thead>
<tr>
<th>Test Description</th>
<th>ZBC-2000</th>
<th>ZBC-1000</th>
<th>FaradFlex</th>
<th>Dupont HK04</th>
</tr>
</thead>
<tbody>
<tr>
<td>6x Through Hole Solder Shock</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td>IPC 6012 Cross section review</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6x Blind Via Solder Shock</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td>IPC 6012 Cross section review</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dielectric Thickness per Cross Section within +/-10%</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td>T-260 (&gt;4 min)</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td>IST Testing</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td>Core Level Hi-pot Testing 100 Cores (100V/sec ramp; 500 V max)</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td>Finished Circuit Level Hi-pot 50 circuits (100V/sec ramp; 500 V max)</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
</tbody>
</table>
Thin Core Processing Summary

- Sanmina-SCI is capable of manufacturing Thin Cores down to 8 µm.
- Sanmina-SCI has extensive experience with ZBC-2000 (>10,000,000 core square feet produced)
- Reliability testing indicates that Thin Cores packages are as thermally reliable as the dicy cured FR4 material
- Initial yield data suggests a difference in foreign material inclusion rates between the suppliers
- Initial yield data suggests a higher rate of material damage on the 24 µm material
- Sanmina-SCI is continuing comparison testing of the materials for reliability and material yield improvements

This work was performed under support of the U.S. Department of Commerce, National Institute of Standards and Technology, Advanced Technology Program, Cooperative Agreement Number 70NANB8H4025
Introduction

• At DesignCon 2002 reported on:
  – 3M C-Ply: 8 µm BaTiO₃ filled epoxy
  – DuPont: thin BaTiO₃ filled polyimides

• Since then, have gained experience with:
  – Oak-Mitsui FaradFlex: 12 µm epoxy/polymer
  – 16 µm version of 3M’s C-Ply
  – DuPont HK-4: 25 µm polyimide
  – DuPont HK-10: 25 µm BaTiO₃ filled polyimide
  – DuPont HK-11: 12 µm BaTiO₃ filled polyimide

• Future work planned with:
  – Oak-Mitsui BC16T: BaTiO₃ filled epoxy/polymer
Thin Laminate Board Builds

• NIST AEPT test vehicles (TV1-C and TV2-C)
• Two emulators with the C-Ply material:
  – Nortel high-speed emulator
  – Hewlett-Packard iPaq emulator boards
• Impedance test boards for Sun with C-Ply and DuPont HK materials.
Thin Laminate Board Builds

• As interest has grown, we have built prototypes and production boards with both filled and non-filled materials for customers.

• Materials used in combination with Isola, MEM, and Nelco materials, some with embedded resistors.

• These thin laminates stretch the capability of our equipment but also improve our ability to process standard materials.
Processing Challenges

• Differences between filled and non-filled materials:
  – Filled laminates require subpart processing
  – Non-filled materials generally able to withstand etcher spray pressure, so both sides can be etched simultaneously.
  – Thin, filled dielectric materials have a lower breakdown voltage, and so must be HiPot tested at a lower voltage.
Processing Challenges

- Non-filled laminates may be more difficult to convey through an etcher than filled laminates
  - With filled laminates, the copper is completely left on one side of the panel, which provides extra support
  - With non-filled laminates, depending on the panel layout, there may be “fold” lines in the etched panel
  - May be necessary to use leader boards when processing very thin unfilled materials
Processing Challenges

• Conveyor systems must be well-maintained
  – Misplaced rollers or guide fingers can be disastrous
  – Can use thin “dummy” panels to check conveyors
  – Rolled-annealed copper has more surface tension than reverse treat copper foil, so may adhere more as it goes through pinch rollers

• Autolaminator maintenance is critical
  – Balance tension of the top and bottom rolls
  – Once the equipment is set up correctly for thin materials, standard product will also run trouble-free
Processing Challenges

• For post-etch punch and AOI optical systems may need to adjust contrast between the copper and the dielectric. Handling also key.
• Scaling may vary for different stackups
  – No fiberglass reinforcement to constrain movement
  – Ultra-thin materials tend to move with adjacent materials
  – Once determined, scaling is generally stable
Processing Challenges

• Train technicians to handle thin materials as they would film

• At electrical test, may need to make adjustments for extra capacitance and reduced dielectric withstanding voltage of loaded materials
UL Qualification and IPC Standards

• UL qualification:
  – 3M C-Ply (complete)
  – DuPont HK4 (complete)
  – Oak-Mitsui FaradFlex (in process)

• IPC board performance standard for embedded passives virtually complete
  – We hope to incorporate it into IPC 6012
Summary

• OEMs are showing greater interest in thin and very thin laminates for performance, size EMI improvements

• Process challenges can be met with:
  – Good equipment that is well maintained
  – Technicians that are well trained
  – Minor process adjustments

• The capability to process very thin materials makes standard thickness material processing easier and more robust
Unicircuit Thin Laminate Experience
Materials Utilized:

- 3M C-Ply
- Gould Upilex
- Nelco N4000-6
- Polyclad 371
Manufacturing Issues & Lessons Learned:

- Artwork modifications
- Material stabilization
- Transportation approach for .001 & .002 cores
- .002 cores with 2oz Cu
- Hipot testing
- Lamination
- Thermal stress testing
- IST testing
OEM Product Deployment:

- Raytheon
- Lucent
- Agilent
- MIT
- Motorola SPS
- Rockwell Collins
Summary:

• End item performance data is very closely held by OEM’s and is considered to be confidential and proprietary.

• Products are being deployed in a number of different market sectors.

• Robust manufacturing guidelines have been established.

• In process and final yield data supports that the product is mature, and is production worthy.
CM Challenges Related to Thin and Ultra Thin Core Laminates <= 1 Mil
February 2nd, 2004
Considerations for Processing 1 Mil Boards

- Incoming Inspection
- Cross-sectional Analysis
- Handling
- Storage
- Fixturing
- Thermal Profiling
- Testing
- Final Packaging
- Integration
Typical Profile for Processing this Size/Type Assembly
As received Sample, note condition of 1 mil Core

As received sample, through 1 HASL process.
As received sample through 1 HASL process
As received sample, polyimide to copper interface
1 X solder float sample, note 1 core movement

1 mil core, 1X solder float, note movement
1X solder float, polyimide to copper plate

1X solder float, polyimide to plate interface
1X solder float, copper to copper interface
3 X solder float, note the position of polyimide
3 X solder float polyimide to plating interface
Closer view of Polyimide to copper interface
6 X Solder Float, Polyimide To Plated Copper

6 X solder float polyimide to copper
6 X Solder Float, note 1 mil Core interface region

6X solder float CU / Polyimide & CU interface
Nickel / Gold Via

Nickel / Gold vias, note condition of the I/L
Polyimide to copper plating

HASL'd via. Polyimide to copper interface
What do we know and where do we go?

- 1 mil Material has been in use for many years
- Application to PCBs recent event
- 250 plus units processed at BEI without failure related to 1 mil
- IST testing from Multiple suppliers indicate acceptable reliability
- Long term reliability studies for assembled product not complete
- HALT / HASS type testing recommended for assembled units
Thin Laminates and Power Plane Noise

John Grebenkemper, Ph.D.
Hewlett-Packard Company
February 2, 2004
Laminate Thickness & Noise

• Reduced Laminate Thickness Decreases Noise
  - Increased capacitance between planes
  - Decreased distribution inductance
  - Reduced distribution impedance

• Reduced Laminate Thickness Increases High Frequency Loss
  - Increases electric field between power and ground planes
  - Increases high-frequency current in conductors
  - High-frequency loss increases due to $I^2R$
  - Increased loss damps noise faster
Calculation of Power Plane Noise

- Simulated board physical design parameters
  - Board size: 3 by 6 inches
  - Separation between power and ground planes: 4 mils
  - Assumed dielectric loss tangent: 0.01
  - Assumed relative permittivity of dielectric: 4
  - Copper power and ground planes
    - Conductivity of copper: $58 \times 10^6$ Siemens/meter
  - Noise source is 2 ns pulse with a 200 ps risetime
  - RMS Noise averaged across entire board
Spacing Between Power And Ground Planes

- Decreasing the spacing between the power and ground planes can substantially reduce the noise
  - Slope ~10 dB/decade above 1.5 mil spacing
  - Slope ~20 dB/decade below 1.5 mil spacing
  - A 0.3 mil spacing has 16 dB less noise than a 4 mil spacing
Laminate Thickness Test Board

- Processor daughter card
  - MIPS R14K processor @ 550 MHz
  - 9 Secondary cache SRAM’s @ 275 MHz

- Laminate thickness between power & ground modified
  - Standard FR-4 type material, 3 mil thickness
  - 3M C-Ply material, 0.3 mil thickness, \( \tau = 16 \)

- Measurements made on 1.5 volt I/O power distribution
High-Frequency Bypass Capacitors

- Bypass capacitors used in test vehicle
- Capacitors distributed around the board
- Mounting sites for 0603 capacitors designed to minimize ESL

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Value</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>2.2 μF</td>
<td>8-pin IDC</td>
</tr>
<tr>
<td>15</td>
<td>0.1 μF</td>
<td>0603</td>
</tr>
<tr>
<td>15</td>
<td>1000 pF</td>
<td>0603</td>
</tr>
<tr>
<td>15</td>
<td>100 pF</td>
<td>0603</td>
</tr>
</tbody>
</table>
Noise Reduction Using C-Ply 8µm Dielectric

- Blue: 3 mil FR-4
- Red: 0.3 mil C-Ply
- Green: 0.3 mil C-Ply with no HF bypass capacitors

High frequency noise is substantially reduced
- Insufficient low frequency capacitance when no HF bypass capacitors used
Total Noise Power

- Integrate noise power over frequency
- Compute the relative change in noise power
- Bypass capacitors do not provide much benefit with C-Ply material
- 13 dB reduction in noise with no HF bypass capacitors between FR-4 and C-Ply Laminates

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>FR-4 With No HF Bypass Capacitors</td>
<td>+6.8 dB</td>
</tr>
<tr>
<td>FR-4 With HF Bypass Capacitors</td>
<td>0.0 dB</td>
</tr>
<tr>
<td>C-Ply With No HF Bypass Capacitors</td>
<td>-6.5 dB</td>
</tr>
<tr>
<td>C-Ply With HF Bypass Capacitors</td>
<td>-7.1 dB</td>
</tr>
</tbody>
</table>
Conclusions

• Decrease the laminate thickness to reduce the noise on printed circuit board power planes
• May be able to eliminate some of the HF bypass capacitors
Frequency Dependent Capacitance and Inductance of Thin and Very Thin Laminates

Istvan Novak
Signal Integrity Senior Staff Engineer
Volume Server Products
Outline

Laminates measured
Test board construction
Extracted absolute capacitance:
Extracted relative capacitance
Extracted inductance
Conclusions
Thin Laminates in Test Boards

• DuPont’s Interra™ HK04: three 25um laminates with one and two-ounce RA and ED Cu; two 50um laminates with one and two-ounce RA Cu, one HKXX14 laminate with one-ounce Cu
• Oak-Mitsui FaradFlex™ unreinforced epoxy: 24um, 16um and 12um laminates with one-ounce RA Cu
• Matsushita glass-reinforced epoxy laminates: ZBC2000™ and ZBC1000™ with one-ounce Cu
• 3M C-Ply™ 24um, 12um, 8um unreinforced filled epoxy, one-ounce Cu
Test Board Top View
Open/Shorted Board Impedance

HK042536R

Impedance magnitude, phase bare [ohm, deg]

Impedance magnitude, phase short [ohm, deg]
Shorted Board Inductance
Capacitance of Open Boards

Capacitance [F]

- Frequency [Hz]
- Capacitance [F]

- ZBC2000
- HK045036R
- HK045072R
- HK042536E
- HK042536R
- HK042572R
- ZBC1000
- BC24
- CPly24
- BC16
- HK1014
- BC12
- CPly12
- CPly8

February 2, 2004
DesignCon 2004, TF09
Istvan Novak
Capacitance of 2-mil Boards

Capacitance of 2-mil bare laminates [F]

- ZBC2000
- HK045072R
- HK045036R

Frequency [Hz]
Capacitance of 1-mil Boards

Capacitance of 1-mil bare laminates [F]

- CPIy24
- BC24
- ZBC1000
- HK0425
Capacitance of <1-mil Boards

Capacitance of <1-mil bare laminates [F]

Frequency [Hz]
Relative Change of Capacitance

Percentage change of capacitance [%]

Frequency [Hz]

-20
-18
-16
-14
-12
-10
-8
-6
-4
-2
0
1.E+5 1.E+6 1.E+7 1.E+8

HK04, HK10
BC12
others
Inductance of Shorted Boards (1)

- Inductance [H]
  - Values range from \(0.0 \times 10^0\) to \(1.0 \times 10^{-11}\)

- Frequency [Hz]
  - Values range from \(1.0 \times 10^6\) to \(1.0 \times 10^9\)

- Graph showing inductance values for different boards:
  - ZBC2000
  - HK045036R
  - HK045072R
  - HK042536E
  - HK042536R
  - HK042572R
  - ZBC1000
  - BC24
  - CPly24
  - BC16
  - HK1014
  - BC12
  - CPly12
  - CPly8
Inductance of Shorted Boards (2)

Inductance [H]

Frequency [Hz]

0.0E+00
1.0E+11
2.0E+11
3.0E+11
4.0E+11
5.0E+11
6.0E+11
7.0E+11
8.0E+11
1.0E+7
1.0E+8

ZBC2000
HK045036R
HK045072R
HK042536E
HK042536R
HK042572R
ZBC1000
BC24
CPly24
BC24
CPly12
BC16
HK1014
BC12
CPly8

Inductance of Shorted 2-mil Boards

Inductance of 2-mil shorted laminates [H]

HK045072R
HK045036R
ZBC2000

Frequency [Hz]
Inductance of Shorted 1-mil Boards

Inductance of 1-mil shorted laminates [H]

- HK042572R
- HK042536R
- ZBC1000
- BC24
Inductance of Shorted <1-mil Boards

![Graph showing inductance of 1-mil shorted laminates](image)

- **Inductance of <1-mil shorted laminates [H]**

  - **Frequency [Hz]**
    - 1.E+6
    - 1.E+7
    - 1.E+8
    - 1.E+9

  - **Laminates**
    - BC12
    - BC16
    - CPLy8
    - CPLy12
    - HK1014
Conclusions

Capacitance of bare boards drops with frequency
-3%/decade for resin laminates
<1%/decade for polyimide
Inductance of shorted boards
varies with copper/laminate thickness
drops with frequency