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Characterizing and Modeling the Impact of Power/Ground Via Arrays on Power Plane Impedance

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Abstract

In this paper, the impact of power/ground via arrays on power plane impedance is studied. 8 x 8 via array structures are characterized and the results are compared to full-wave field simulation using HFSS. These results show that the impedance and effective inductance is a strong function of location within the array. The lowest impedance is found on the array perimeter and the impedance is several times higher in the array center. The impact antipad size and dielectric thickness on the plane impedance and inductance is examined using parameterized models.

Author Biography

Jason Miller is currently a Staff Engineer at Sun Microsystems where he works on ASIC IO cell development, ASIC packaging, interconnect modeling and characterization, and system simulation. Jason received his Ph.D. in Electrical Engineering from Columbia University.

Istvan Novak is a signal-integrity senior Staff Engineer at Sun Microsystems. Besides signal integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for Sun servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF and analog circuits, and system design. He is a Fellow of IEEE for his contributions to the fields of signal-integrity, RF measurements, and simulation methodologies.

Jim DeLap is an Applications Engineer specializing in the High Frequency products including HFSS and Ansoft Designer. Prior to working at Ansoft, he has designed many products ranging from millimeter-wave mixers and antennas to integrated radios in the 30-60 GHz range. He earned his BSEE from the University of Lowell, Lowell, MA, his MSEE from the University of Virginia, Charlottesville, VA, and has worked for companies such as Millitech Corporation, Raytheon, and Agilent Technologies.

Introduction

This paper examines the impact of via arrays on the electrical characteristics of power/ground planes. Via arrays can be found underneath a package where the power/ground connections to the printed circuit board (PCB) are made using multiple power and ground vias. Package designers often incorporate multiple parallel vias to minimize the inductance incurred in connecting to the board power planes. With increasingly tight ball pitches, this results in a very dense pin or ball grid array field. The antipads associated with these via connections will perforate the plane region underneath the package, often to such an extent that only a thin web of metal exists underneath the package. Smaller antipad diameters can help to mitigate this effect but multilayer boards require a certain minimum antipad diameter to be manufacturable. As a consequence of these perforations, the power plane pair impedance can be significantly altered by the via array [1]. It has also been shown that the effective inductance of a plane pair increases with the density of the via array [2].

In this paper, we study the impact of different physical parameters on the power plane impedance and effective inductance. There are three parts to this paper. In the first part, the impedance of a test board consisting of an 8 x 8 array of vias is measured. These results are then correlated to full-wave electromagnetic field solution using HFSS [3]. In this second section we examine the simulation environment and the validity of various simplifying assumptions (e.g. losses). Lastly, the model is parameterized and by sweeping some of the physical parameters of the array such as antipad diameter and dielectric thickness we study the impact of the array's physical dimensions on the power plane impedance.

1. Measurement Results

A number of test boards were designed and fabricated which all had in common a 8 x 8 via array of alternating power/ground vias centered on a 2.5" square plane pair. Figure 1 shows a top view of the array illustrating the staggered arrangement of the power/ground vias. Power vias are identified by filled circles inside the hollow via cylinders. The openings in the power-ground plane pair are created by overlapping antipads. Here the antipad diameter is 58 mils and the via center-to-center distance is 50 mils, respectively. Each via pair can be uniquely identified using the row and column identifiers shown in Figure 1. For example, (A1,B1) corresponds to the via pair located in the bottom left hand corner. The matrix is fully symmetric; thus, (A1,B1) has the same geometry and environment as (G8,H8). Figure 2 shows a cross section of the top portion of the structure. The via diameter is 22 mils and the plated through holes (PTH) have a wall thickness of about 1.3 mils. The dielectric thickness is 8 um.

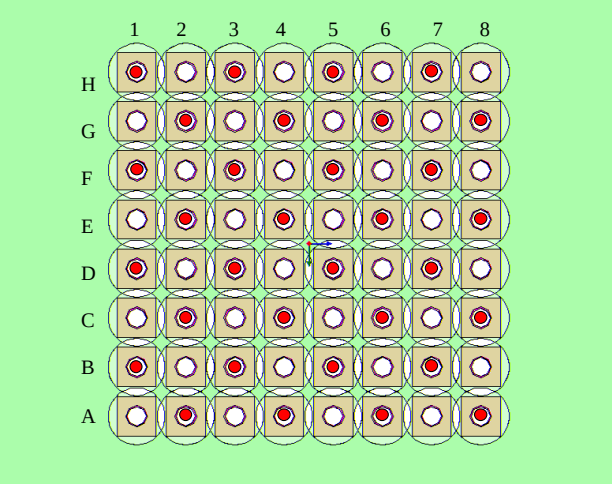

Figure 1: Via matrix arrangement. The array is centered on a 2.5" square plane pair that is not shown.

An HP 4396B vector network analyzer (VNA) was used to measure the self-impedance magnitude and phase from 100 kHz to 1.8 GHz. With the board secured on its side, semirigid coaxial probes were used to contact the via pairs from opposite sides of the board. A full-two port calibration was performed. The power/ground via pairs were then measured as a function of pair location. Real and imaginary S_{21} measurement data were processed and the corrected self-impedance magnitude and phase was obtained [3]. In this arrangement, the parasitics associated with the via are in series with the source and load impedances. If the via impedance is small compared to the 50 ohm environment, its contribution can safely be ignored.

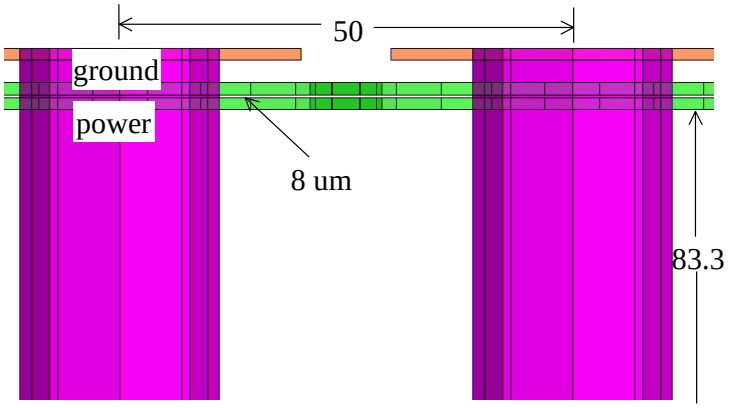

Figure 2: Side view of the test structure showing the a pair of vias, the plane pair and top via pads. The units are in mils unless otherwise noted. The copper weight is 1 oz.

Figure 3 plots the impedance measured on the diagonal of the matrix from the corner (A1,B1) to the center (D4,E4). Also shown for reference is the measured impedance at a stand-alone via pair that is outside of the array surrounded by a solid plane pair. Up to about 10 MHz the locations show similar self-impedance profiles as the impedance is dominated by the static capacitance of the plane pair. Above 10 MHz, the impedance

profiles diverge signifcantly; the plane perforation pushes the series resonance lower and increases the plane equivalent inductance. The largest impedance change within the array is observed one step in from the corner location. Thereafter, the impedance changes are smaller. In fact, the final two measurment pairs near to the center are overlapping on this scale.

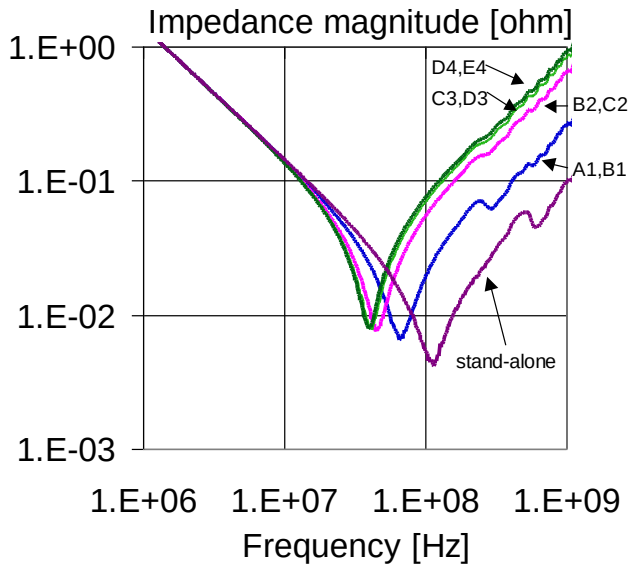

Figure 3: Measured impedance profiles at via pairs on the diagonal starting with (A1,B1) progressively moving towards the center (D4,E4).

Figure 4a plots the measured equivalent inductance ($L = Im[Z]/\omega$) at the via pairs moving diagonally from the corner via pair to the center of the array. The measured equivalent inductance at the stand-alone via pair is shown as reference. The inductance is found to be a strong function of location within the array. Figure 4b plots the ratio of the equivalent inductances at the via pairs, measured along the diagonal, to the inductance at the stand-alone via pair. The equivalent inductance within the array is found to vary by as much as 4X.

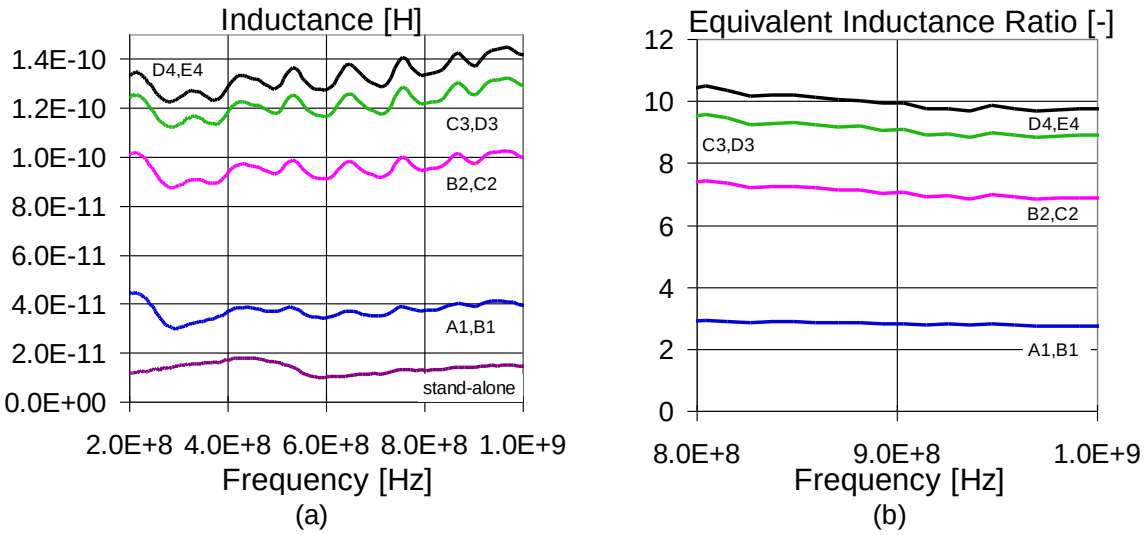

Figure 4: (a) Measured equivalent inductance at via pairs on the diagonal starting with (A1,B1) progressively moving towards the center (D4, E4). (b) Ratio of the equivalent inductance at via pairs along the diagonal of the array relative to the stand-alone via pair.

By measuring rows AB, BC, CD, DE across each column (1-8) and taking advantage of the symmetry of the structure, it is possible to obtain a plot of the impedance and inductance of the entire array. Figure 5a and Figure 5b plot the impedance and equivalent inductance of the array at 500 MHz, respectively. Moving in from the array perimeter, the impedance magnitude and equivalent inductance are found to increase sharply towards the array center. The highest impedance, in the center of the array, is found where the plane pair is heavily perforated on all sides by the antipad cutouts. The

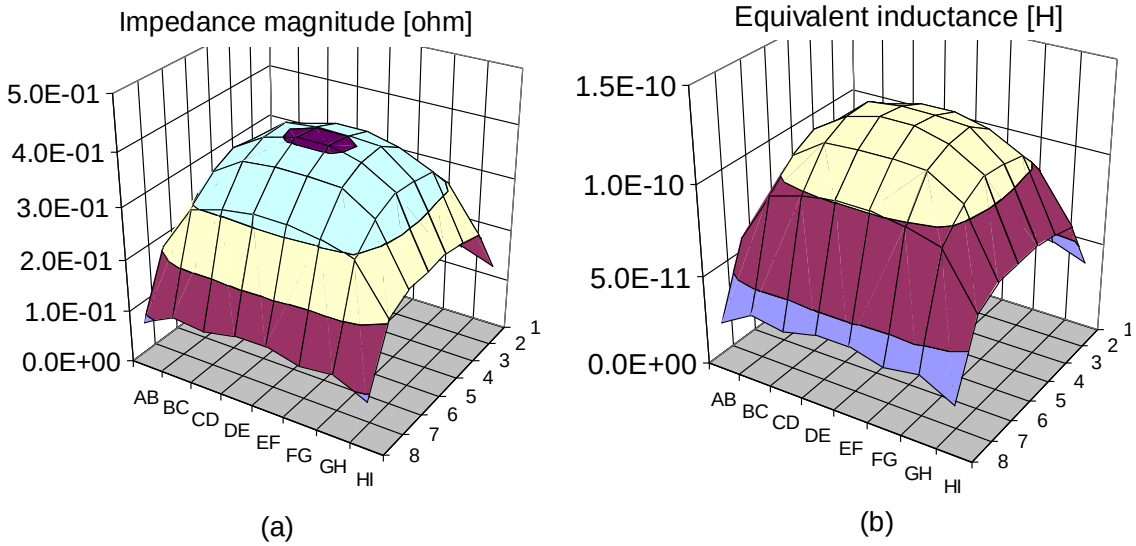

Figure 5: (a) Plot of measured impedance magnitude of the entire array at 500 MHz. (b) Plot of the equivalent inductance of the entire array at 500 MHz.

lowest impedance is found at the corners of the array where the plane is solid on two sides.

2. Simulation Results

Ansoft HFSS [4], a 3D full-wave electromagnetic field simulator, was used to extract the S-parameters of the entire via array. Lumped gap ports of 50 ohms were defined at each of the via pad pairs, on the top and bottom of the test board, and the two-port S-parameters were calculated for each pair. An absorbing boundary was used to simulate the open nature of the problem and to insure negligible energy is reflected back towards the structure. In order to properly capture the antipad overlap, the antipad was modeled with 30 facets, very closely approximating the true area overlap. Real and imaginary S_{21} solver data was then processed and the corrected impedance magnitude and phase information was obtained using the same procedure as above. Figure 6a and Figure 6b compare the impedance measured and simulated at the corner and center of the array, respectively. The dielectric materials in these simulations were assigned a loss tangent of 0.02. Overall, excellent agreement is obtained between the measurement and simulation. The resonance at about 170 MHz, more pronounced in the corner of the array, was not captured by the simulation and remains to be understood.

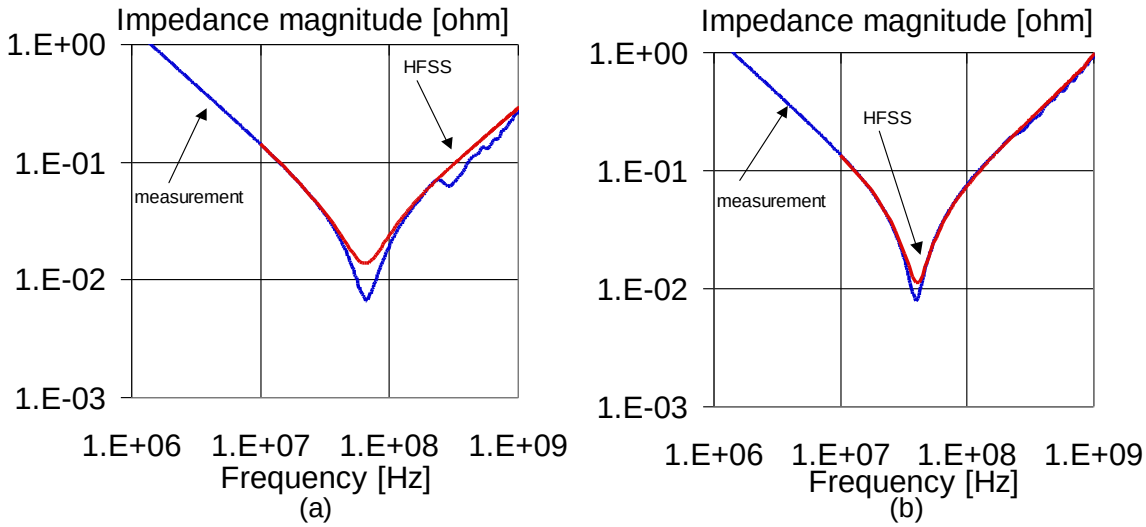

Figure 6: (a) Measured and simulated impedance data at a via pair located at the corner of the array (A1,B1) and (b) located at the center of the array (D4,E4).

Without internal metal meshing, currents are forced to flow on the surface which represents the high frequency current distribution. By meshing both internally and on the surface of the metal, it was found that meshing the surface was sufficient to capture the impedance in the frequency range of interest. Figure 7a and Figure 7b compare the impedance measured and simulated with and without meshing the internal metal for locations (A1,B1) and (D4,E4), respectively. The right hand corner of Figure 7a shows a zoomed in region of the impedance profile from 100 MHz to 1 GHz. The simulated data with and without internal meshing yield very similar impedance profiles.

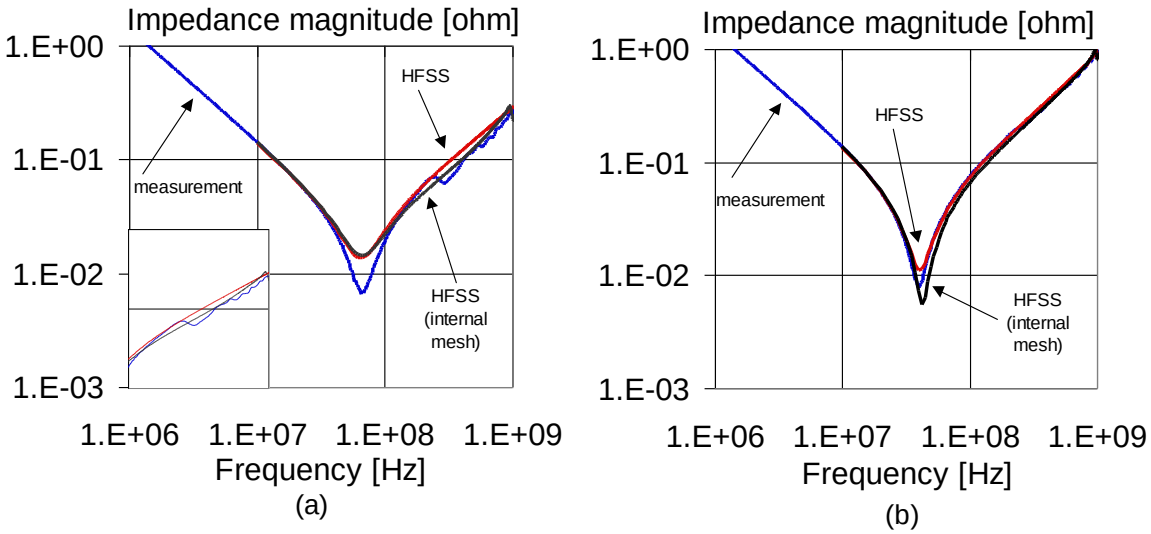

Figure 7: (a) Measured and simulated impedance data at a via pair located at the corner of the array (A1,B1) and (b) at the center of the array (D4,E4). Simulations were performed with and without internal meshing.

Finally, we look at the impact of dielectric loss on the correlation with measurement results. Figure 8a and Figure 8b show the simulation results with and without dielectric loss for locations (A1,B1) and (D4,E4), respectively. As expected, eliminating dielectric loss from the simulation results in resonances that are sharper with a higher Q-factor. Aside from that feature, the profiles with and without dielectric loss are quite similar.

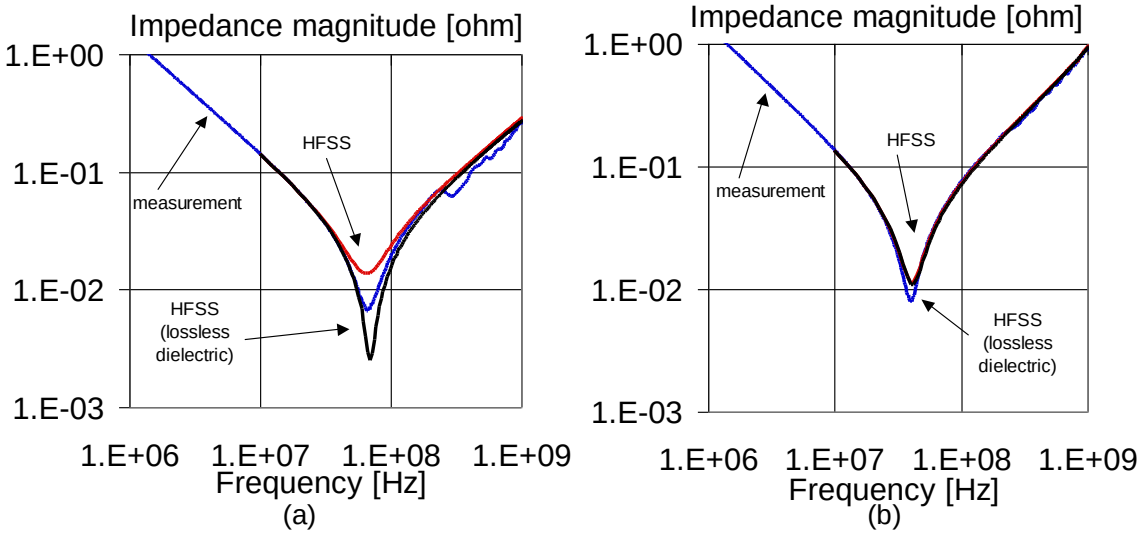

Figure 8: (a) Measured and simulated impedance data at a via pair located at the corner of the array (A1,B1) and (b) at the center of the array (D4,E4). Simulations were performed with and without dielectric loss.

3. Parameterization

3.1. Antipad Diameter

By parameterizing the antipad diameter in the field solver, it is possible to examine the impact of antipad overlap on the impedance and equivalent inductance as a function of location within the array. Figure 9 plots the equivalent inductance of the locations (A1,B1) and (D4,E4) as a function of antipad overlap. In this geometry, an antipad overlap of zero means that the antipad diameter is 50 mils. For the two pair locations the inductance at 250 MHz, 500 MHz, 750 MHz and 1 GHz was compared. At all frequencies, the plots show that the inductance at the two locations increases sharply when the antipad overlap is positive. A positive value for the antipad overlap implies that the via center-to-center spacing is such that there is an overlapping opening in the power and ground planes. On a linear-linear scale the equivalent inductance at all frequencies points overlap. Figure 10 shows the same graph as Figure 9, except on a log-linear scale. This graph more clearly shows that in the case of negative overlap, the inductance does increase as the antipad diameter increases although not as sharply as when there is positive antipad overlap.

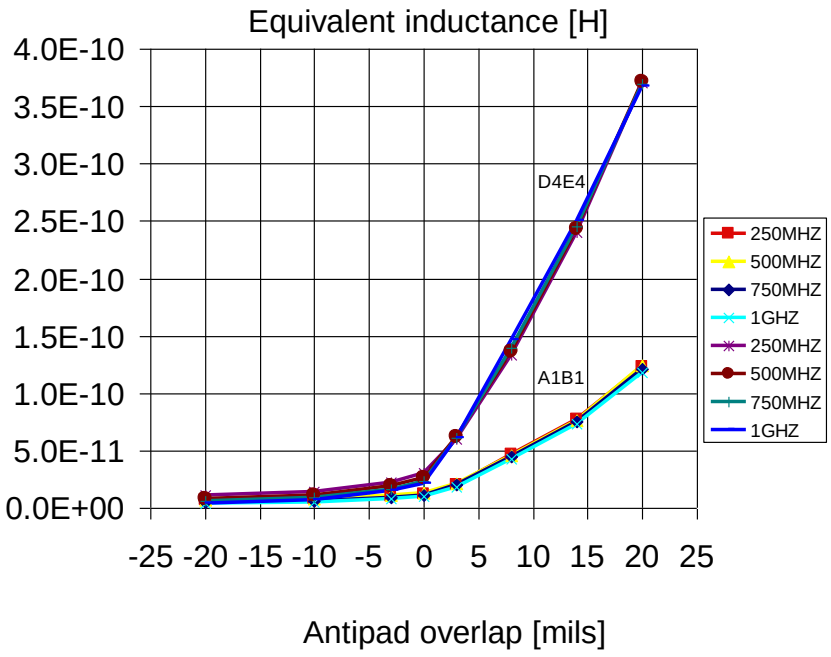

Figure 9: Simulated equivalent inductance at the corner via pair (A1,B1) and (D4,E4) as a function of the antipad overlap.

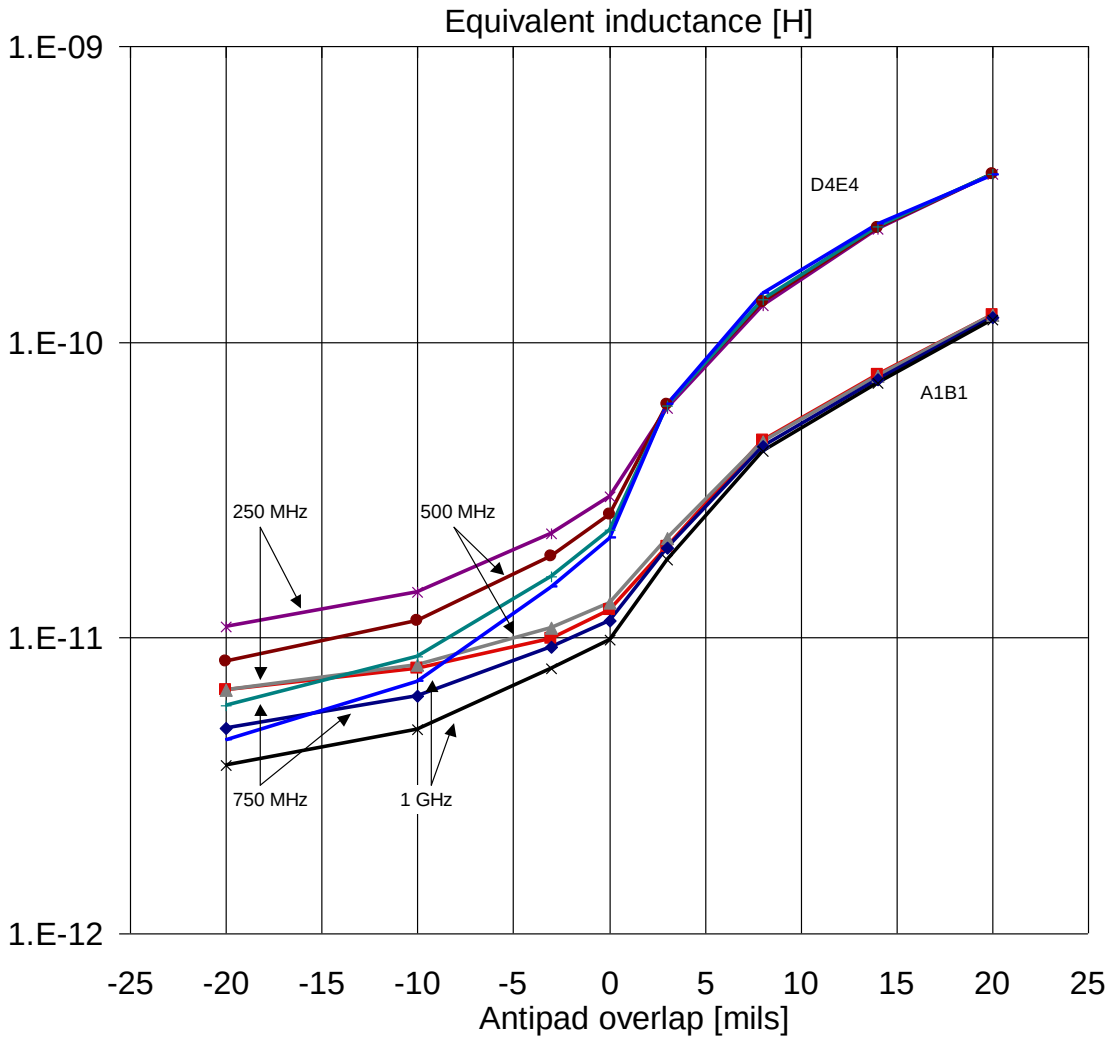

Figure 10: Simulated equivalent inductance at the corner via pair (A1,B1) and (D4,E4) as a function of the antipad overlap on a log-linear scale.

Figure 11 plots the ratio of the inductance at (D4,E4) over the inductance at (A1,B1), at 250 MHz, 500 MHz, 750 MHz and 1 GHz. The plot shows that with positive antipad overlap the center via pair locations will have much higher inductance than the perimeter vias. Conversely, with negative antipad overlap, the ratio of the inductances of the center vias to the perimeters vias asymptotically approaches one. At lower frequencies (e.g. 250 MHz), the ratio approaches one more slowly probably due to current spreading.

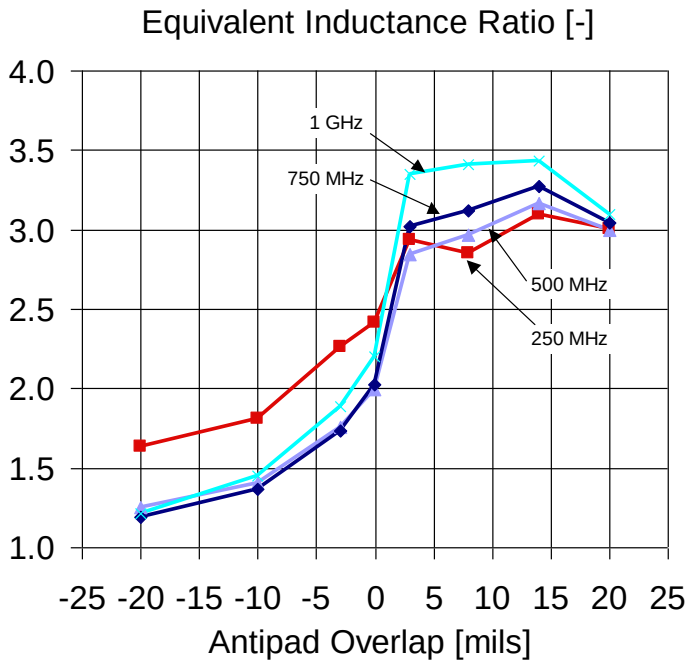

Figure 11: Ratio of the inductance at (D4,E4) to (A1,B1) at 250 MHz, 500 MHz, 750 MHz and 1 GHz as a function of antipad overlap.

3.2. Dielectric Thickness

In the previous section it was found that across a wide range of frequencies, the equivalent inductance is a strong function of antipad diameter, particularly in the case of positive antipad overlap. In addition, it was found that the antipad overlap helps to determine how the impedance varies across the array. These simulations were performed with a fixed dielectric thickness of 8 um. This section examines the impact of dielectric thickness on these conclusions.

Figure 12 plots the simulated equivalent inductance at the corner via pair (A1,B1) and (D4,E4) as a function of the antipad overlap for a 8 um, 24 um, and 100 um thick dielectric. The plot is generated for 500 MHz because it exhibited the smoothest impedance profile. Higher amplitude resonances are observed at other frequency points for the 24 um and 100 um thick dielectrics due to the lower loss of the power plane pair. Looking at Figure 12 we see that for a given negative antipad overlap, the dielectric thickness will increase the inductance at both locations in the array. This indicates that for the range of dielectric thicknesses studied the plane inductance dominates for small antipads. As the antipad overlap increases, the inductance profiles converge for the center and perimeter locations, indicating that the antipad inductance dominates the plane inductance.

Figure 13 plots the ratio of equivalent inductance of the 24 um and 100 um thick dielectrics to the 8 um thick dielectric at the (A1,B1) and (D4,E4). Again, these results are plotted at 500 MHz only. This plot shows graphically what was stated above. Namely, that for positive antipad overlap the dielectrics yield approximately the same

equivalent inductance. One conclusion that can be drawn from this is that increasing the antipad size reduces the benefits of using thinner dielectrics to reduce the power plane impedance. Notice that the ratio is slightly larger than one for the corner location with the 100 um dielectric. This indicates that with the 100 um thick dielectric the plane inductance is becoming a fraction of the antipad inductance. With even thicker dielectrics the profile in Figure 13 would become flatter as plane inductance dominates across a wider range of antipad diameters.

Since the plane inductance increasingly dominates as the antipad size shrinks, we expect an inductance ratio that's proportional to the difference in the loop area introduced by the larger plane separation. For example, moving from a 24 um thick dielectric to a 100 um thick dielectric should increase the inductance by about a factor of four. Figure 13 shows an increase of about a factor of three. This discrepancy is a consequence of the inductance profiles as a function of frequency (for a given antipad size) being non-monotonic at certain frequencies due to resonances, making it difficult to make a comparison. The comparison point of 500 MHz was chosen because the inductance profile was well-behaved across the range of dielectrics and antipad sizes.

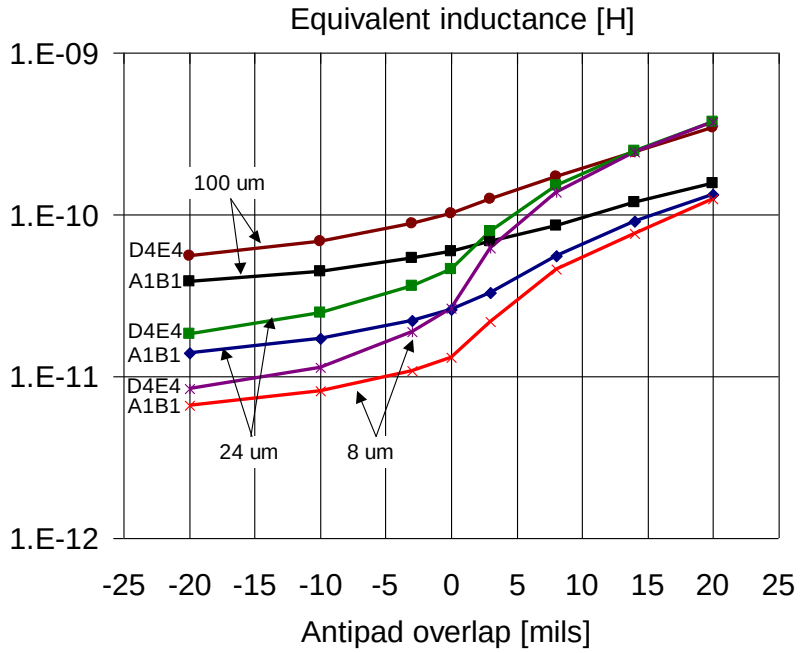

Figure 12: Simulated equivalent inductance at the corner via pair (A1,B1) and (D4,E4) as a function of the antipad overlap for a 8 um, 24 um and 100 um thick dielectric.

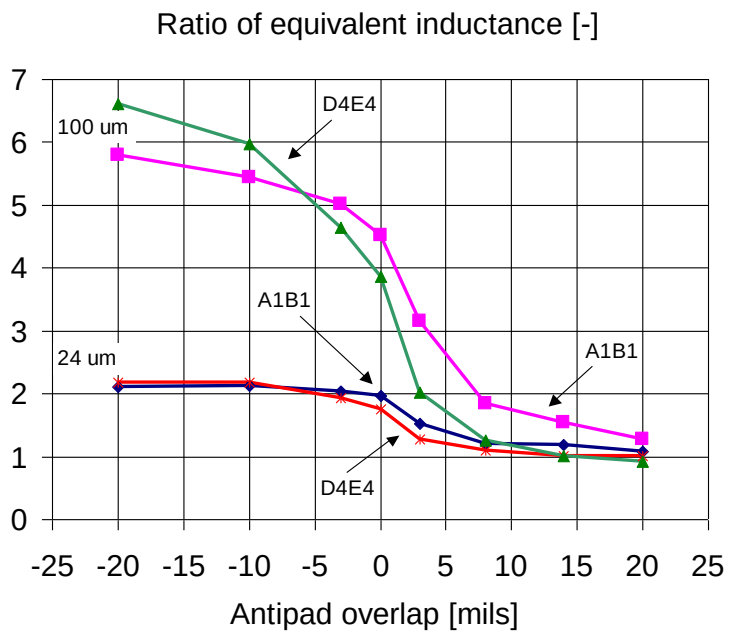

Figure 13: Ratio of equivalent inductance of the 24 um and 100 um thick dielectric to the 8 um thick dielectric at (A1,B1) and (D4,E4).

In Figure 11 it was shown for the 8 um thick dielectric that as the antipad overlap increases there is more impedance variation across the array. Figure 14 examines the sensitivity of the impedance variation to the dielectric thickness. The graph plots the ratio of the inductance at (D4,E4) to (A1,B1) at 500 MHz as a function of antipad overlap and dielectric thickness. The plot shows that thinner dielectrics materials will demonstrate more impedance variation as the antipad size is increased while using a thick dielectric will minimize this variation. (Here "thin" and "thick" dielectrics are relative to the antipad radius.) One way of looking at this is that the electromagnetic fields in the dielectric material will not be perturbed by the antipad cutout providing its radius is small relative to the thickness of the dielectric.

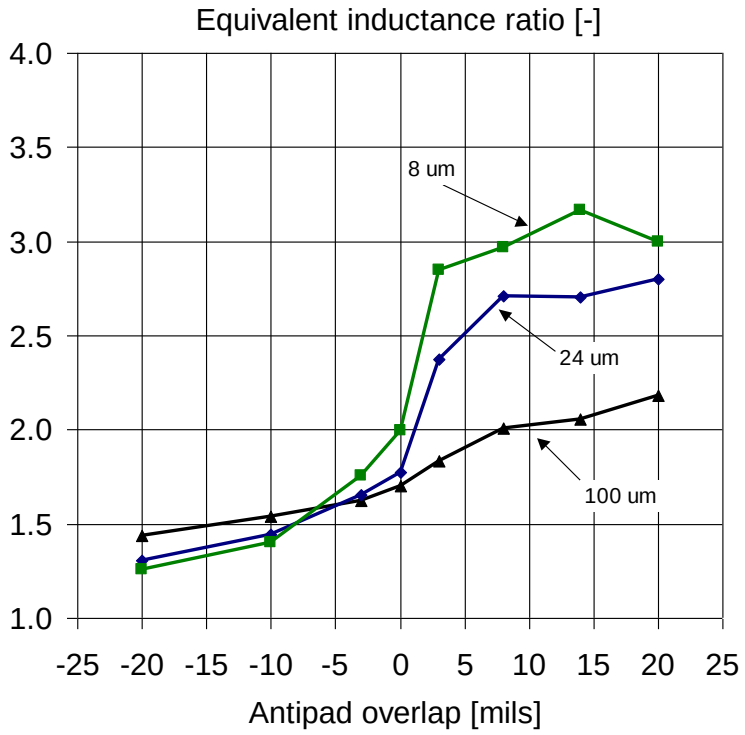

Figure 14: Ratio of the inductance at (D4,E4) to (A1,B1) at 500 MHz as a function of antipad overlap.

Conclusions

A via array structure was measured and analyzed using HFSS. Very good correlation was achieved between measurement and simulation. The measurement and simulation data show that the impedance measured across the array varies with location. Vias on the outside of the array have the lowest impedance and the impedance was found to increase sharply towards the array center. This variation can be reduced by using thicker dielectrics and decreasing the antipad size.

Simulation results showed that the impedance is a strong function of antipad size. Positive antipad overlap was found to dramatically increase the impedance for both the center and perimeter vias. This indicate that antipads in power/ground via arrays should not overlap so that impedance is reduced and a more uniform impedance is maintained across the array.

The simulations revealed that negative antipad overlap causes the plane inductance to dominate the antipad inductance over a large range of dielectric thicknesses. It was also shown that antipad diameter does help to shape the impedance profile even with negative antipad overlap. However, the antipad size matters less and less as the thicker dielectrics are used. Conversely, with positive antipad overlap the differences between the dielectric thicknesses are less important as the antipad inductance dominates. This suggests that the benefits of using thinner dielectrics to reduce the power plane impedance will be tempered by the relative proportion of antipad inductance.

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