Characterizing and Modeling the Impact of Power/Ground Via Arrays on Power Plane Impedance

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Agenda

- **Introduction & goals**
- Measurement results
  - Test board design
  - Measurement set-up
  - Single pair measurements
  - Full array measurements
- Simulation results
  - Simulation conditions
  - Measurement correlation
- Parameterization
  - Antipad diameter
  - Dielectric thickness
- Summary

Introduction

- Via arrays can be found underneath a package where the P/G connections to the PCB are made using multiple power and ground vias.
- With multiple P/G vias and increasingly tight ball pitches, this results in a very dense pin or ball grid array field.
- Antipads perforate the plane region underneath the package, often to such an extent that only a thin web of metal exists.
- Smaller antipad diameters can help to mitigate this effect but multilayer boards require a certain minimum antipad diameter to be manufacturable.
- As a consequence of these perforations, the power plane pair impedance can be significantly altered by the via array.

Goals

- Measure and model the impedance of via array with good measurement to simulation correlation.
- Examine the dependence of the impedance and effective inductance on the antipad size and location in the array.
- Through model parameterization, understand the dependence of the array impedance on the array geometry.

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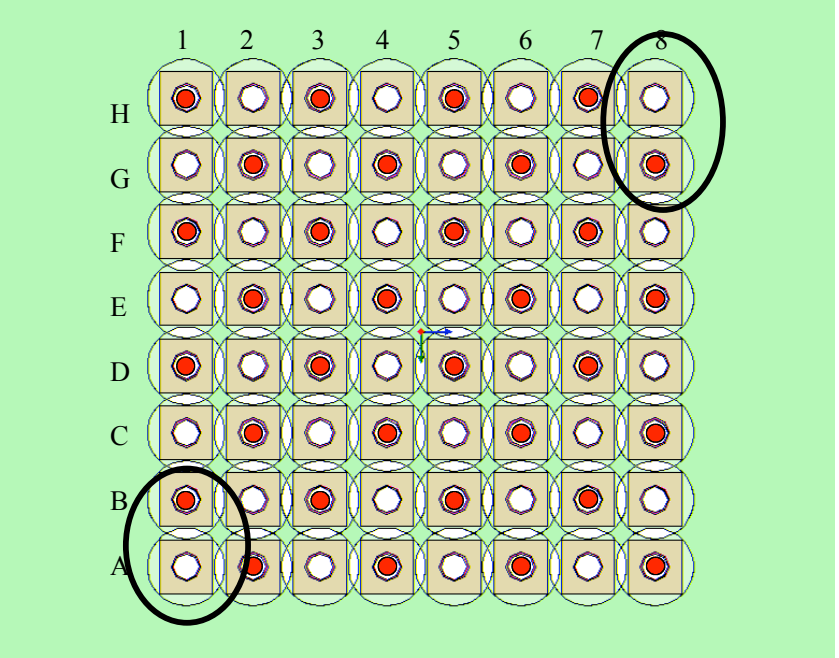
Test board design

- Consists of four 8 x 8 via arrays with alternating P/G vias on a 2.5” x 10” board
- Board stackup utilizes only a single P/G plane pair
- Suite of test boards which vary geometrical parameters, e.g. dielectric thickness.

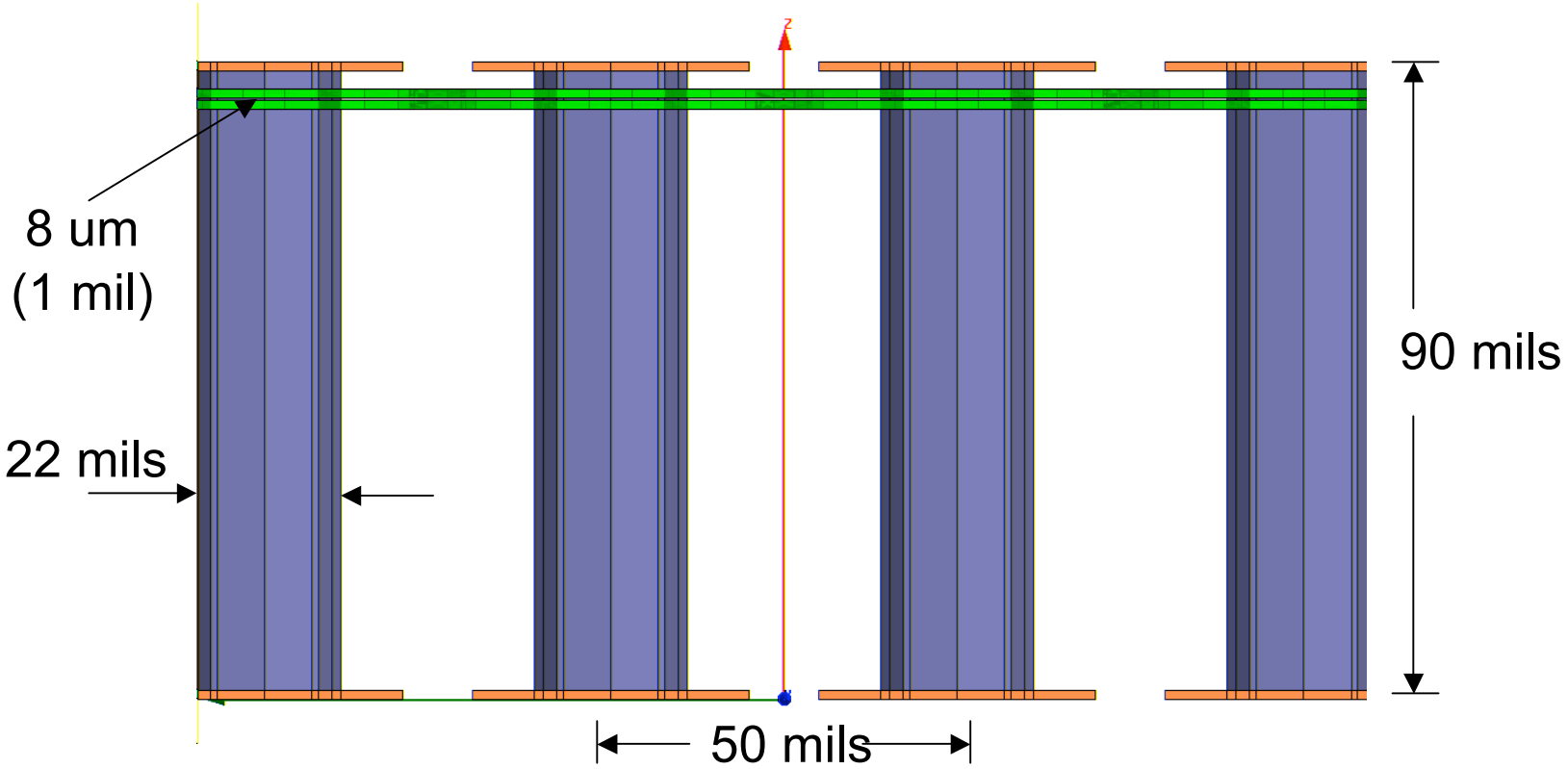
Test board design

- Power vias are identified by filled circles inside the hollow via cylinders.
- Openings in the power-ground plane pair are created by overlapping antipads.
- Each via pair can be uniquely identified using the row and column identifiers shown.
- E.g., (A1,B1) corresponds to the via pair located in the bottom left hand corner.
- The matrix is fully symmetric; thus, (A1,B1) is the same as (G8,H8).



Top view of the 8 x 8 via array arrangement

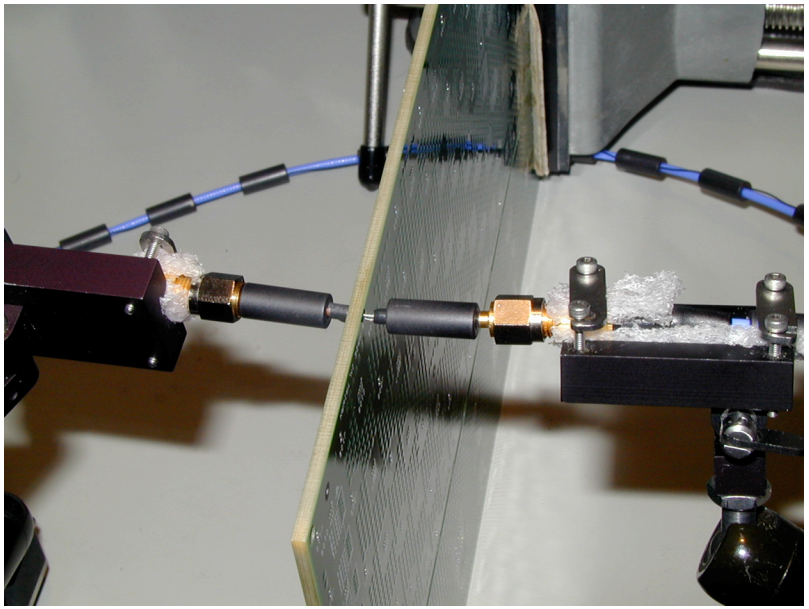
Test board design



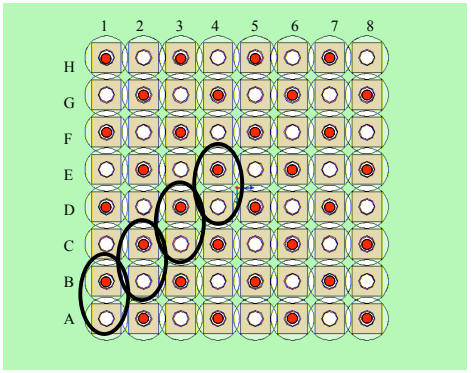
Side view of the test structure showing the vias, plane pair, and top and bottom via pads

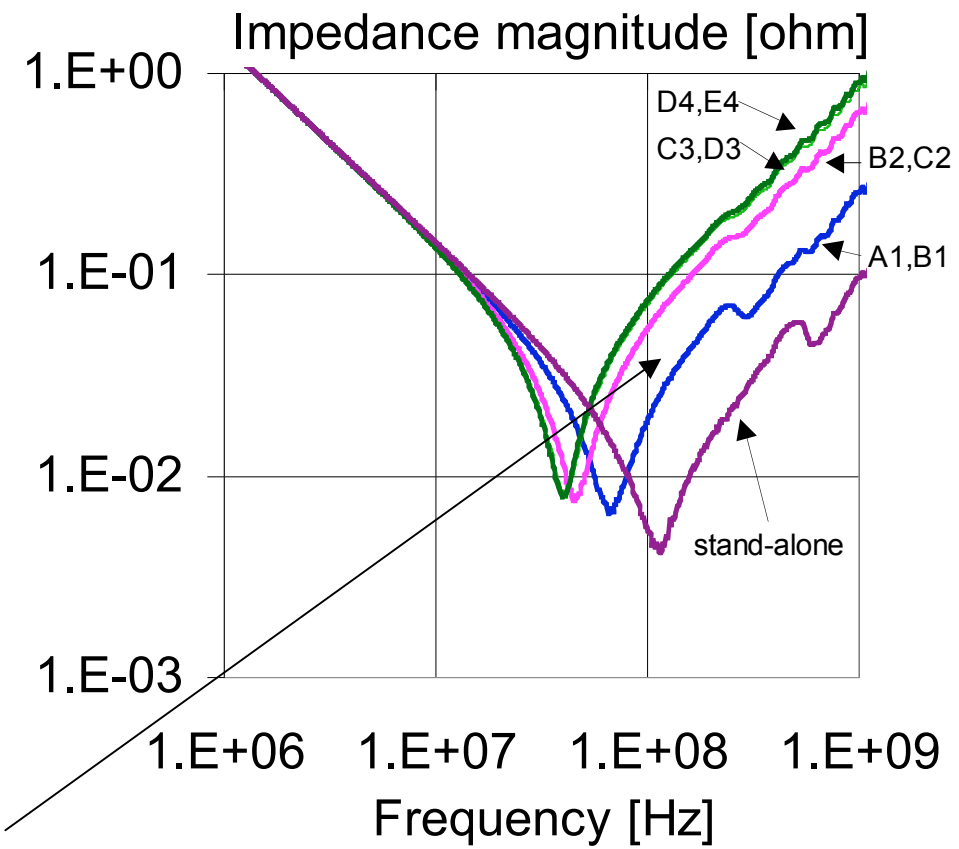
Measurement set-up

- HP 4396A VNA, 100 kHz-1.8 GHz
- Full two port calibration
- Semirigid coaxial probes on opposite sides of the board



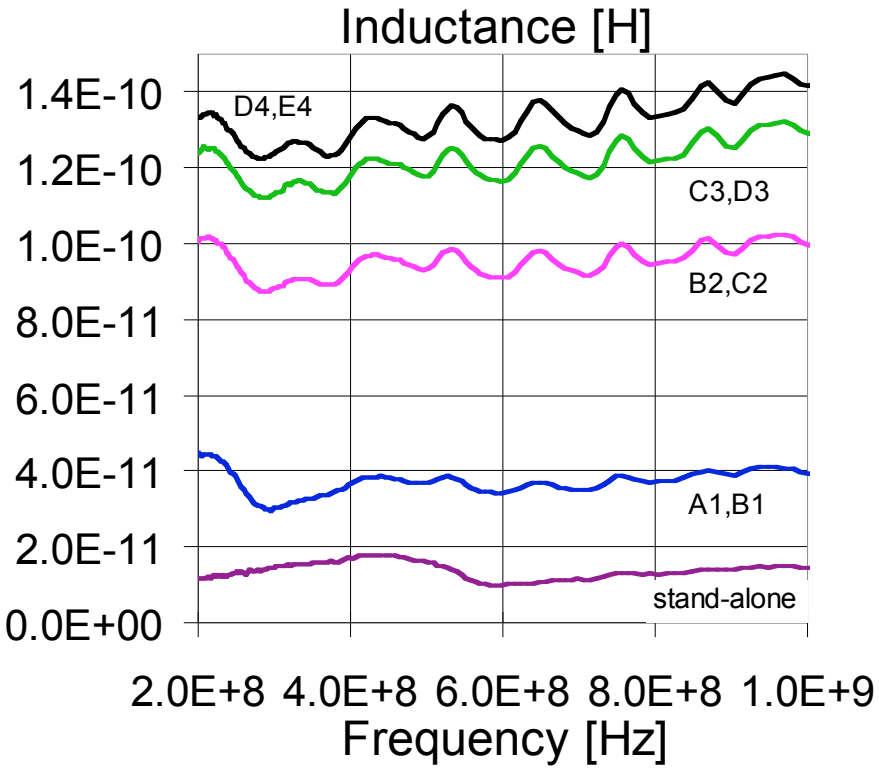
Single pair measurements



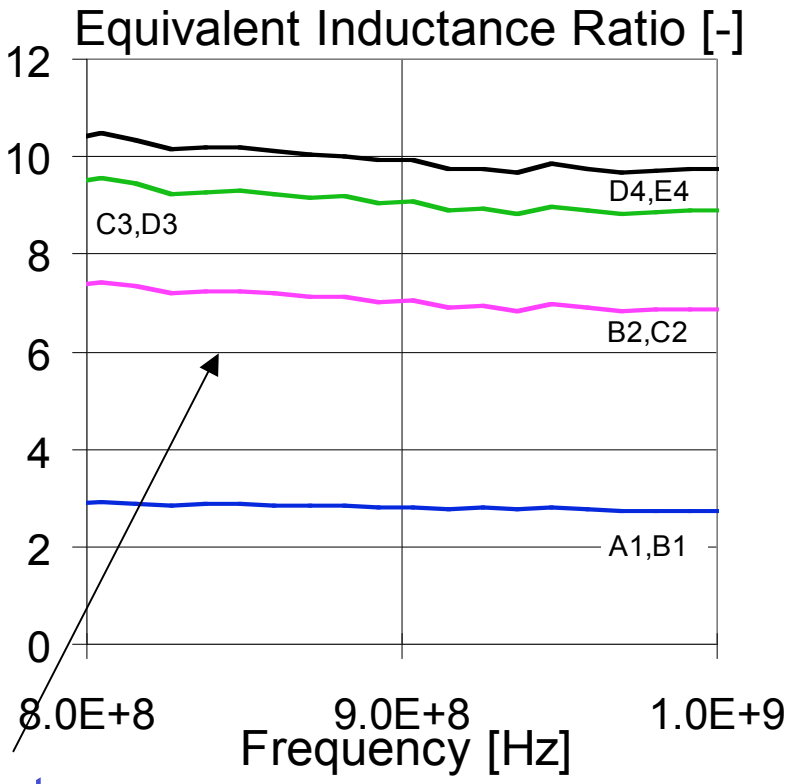


impedance increases moving towards the array center

Single pair measurements



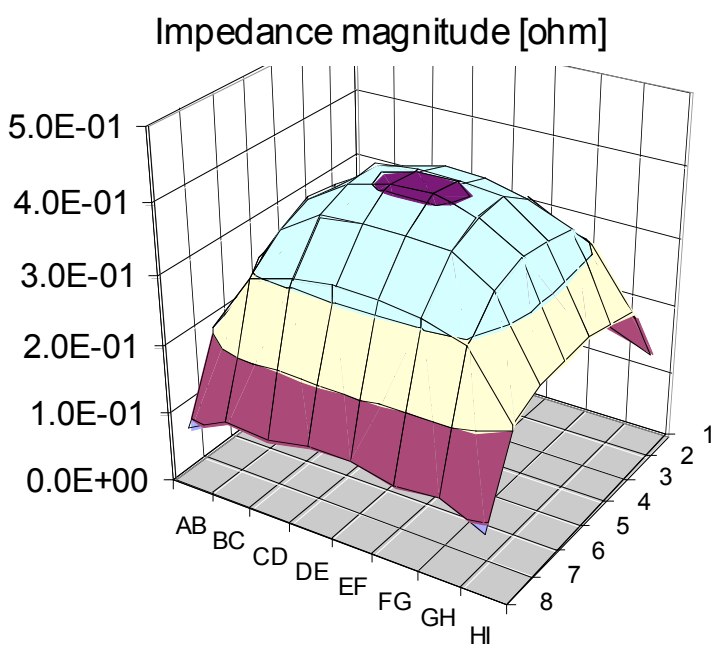
(a)



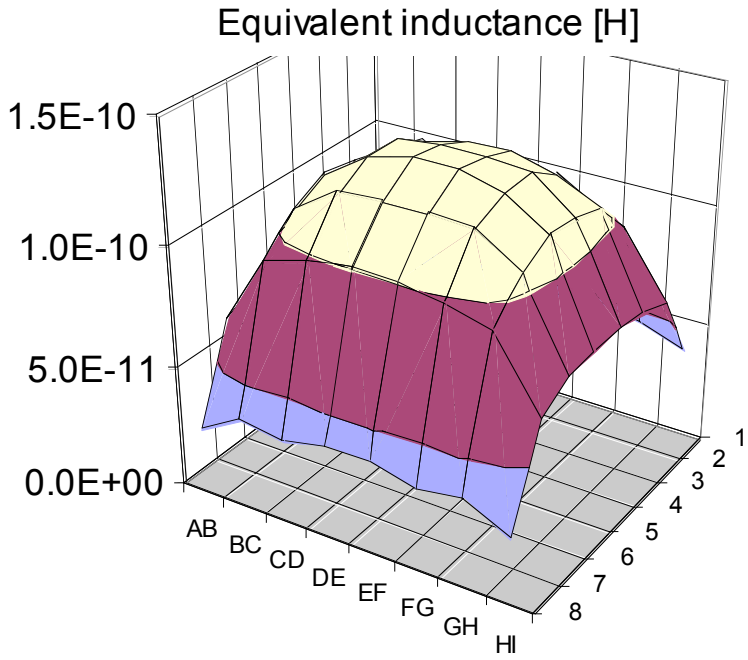
(b)

inductance increases moving towards the array center

Full array measurements



(a)



(b)

Measured impedance magnitude of the entire array at 500 MHz

Measured inductance of the entire array at 500 MHz

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  - **Measurement correlation**
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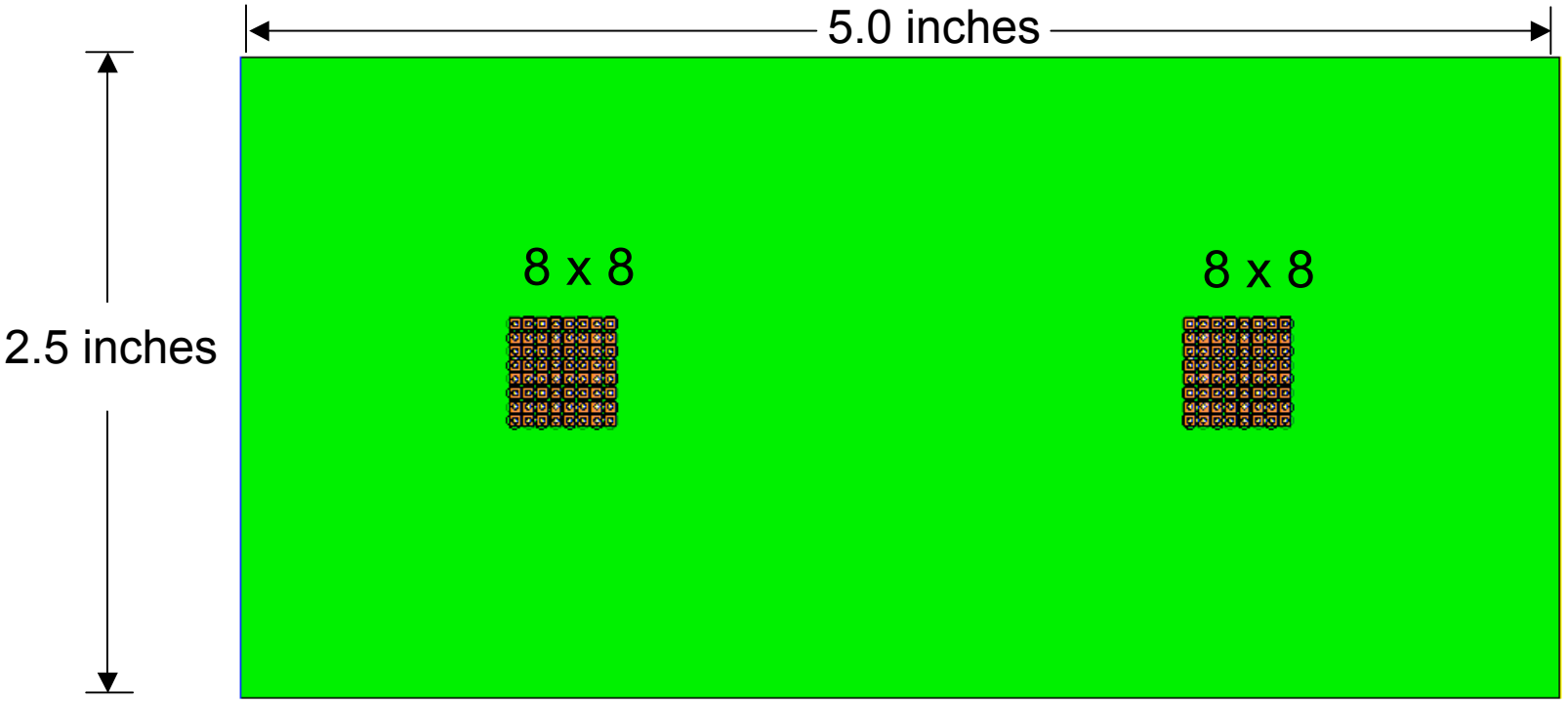
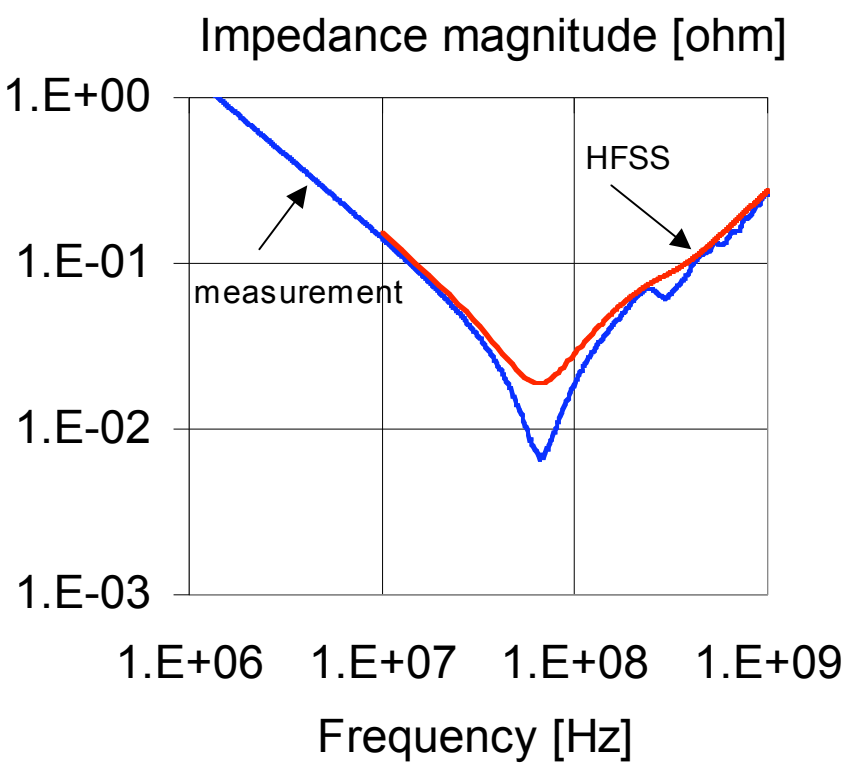
Simulation conditions

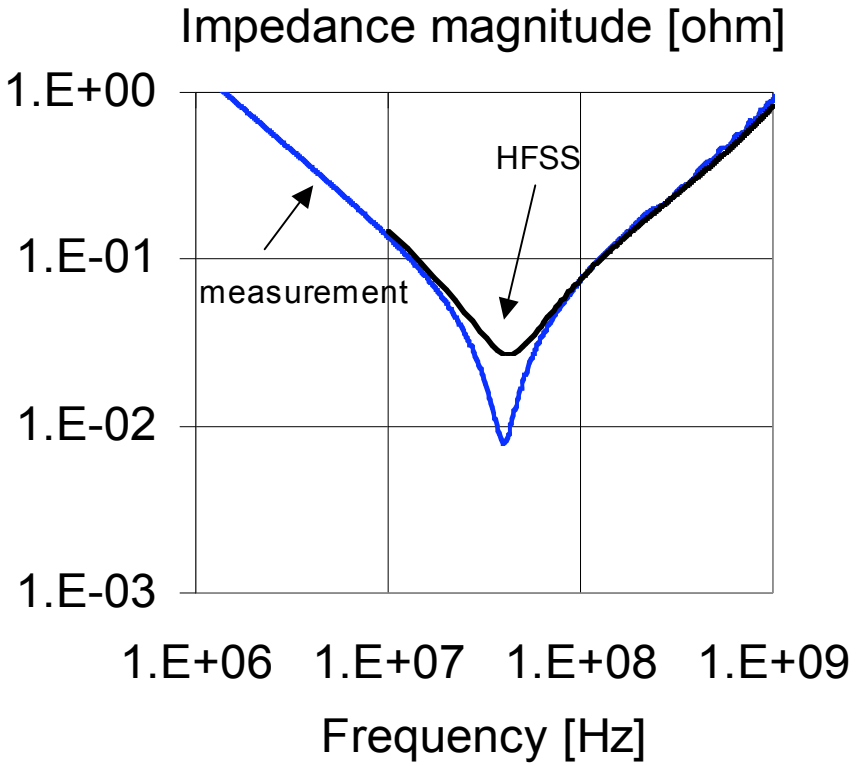
- Ansoft HFSS 9.2.1, 3D full-wave EM field solver
- Fully parameterized project
- 2.5” x 5” board with 128 vias simulated



Measurement correlation

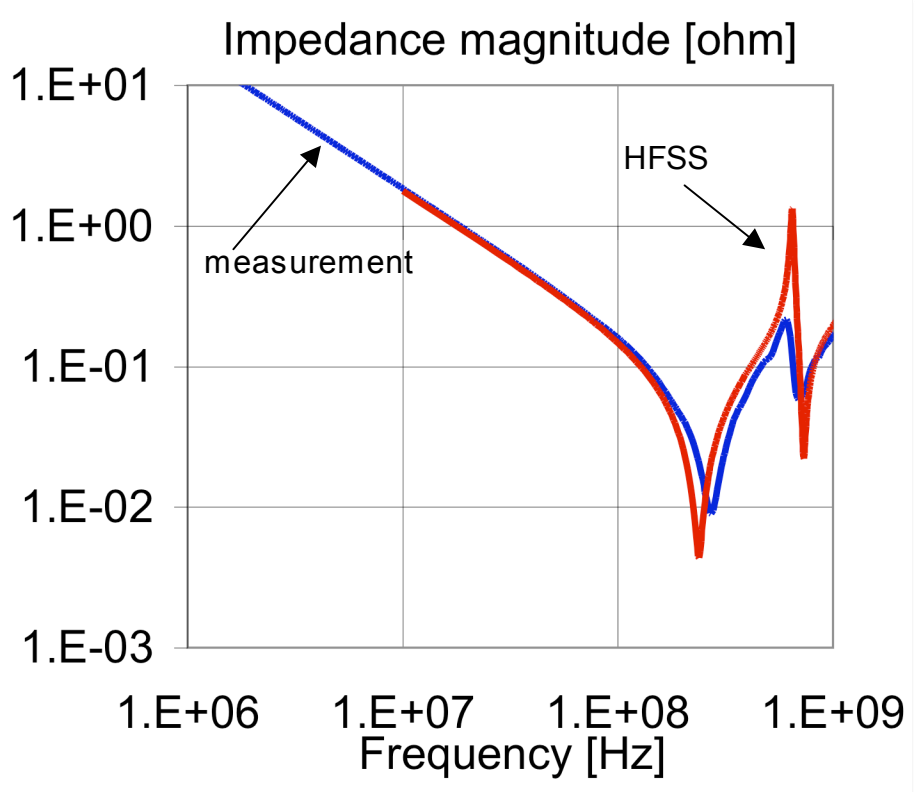


Measured and simulated results at a1b1 for a 8 um dielectric

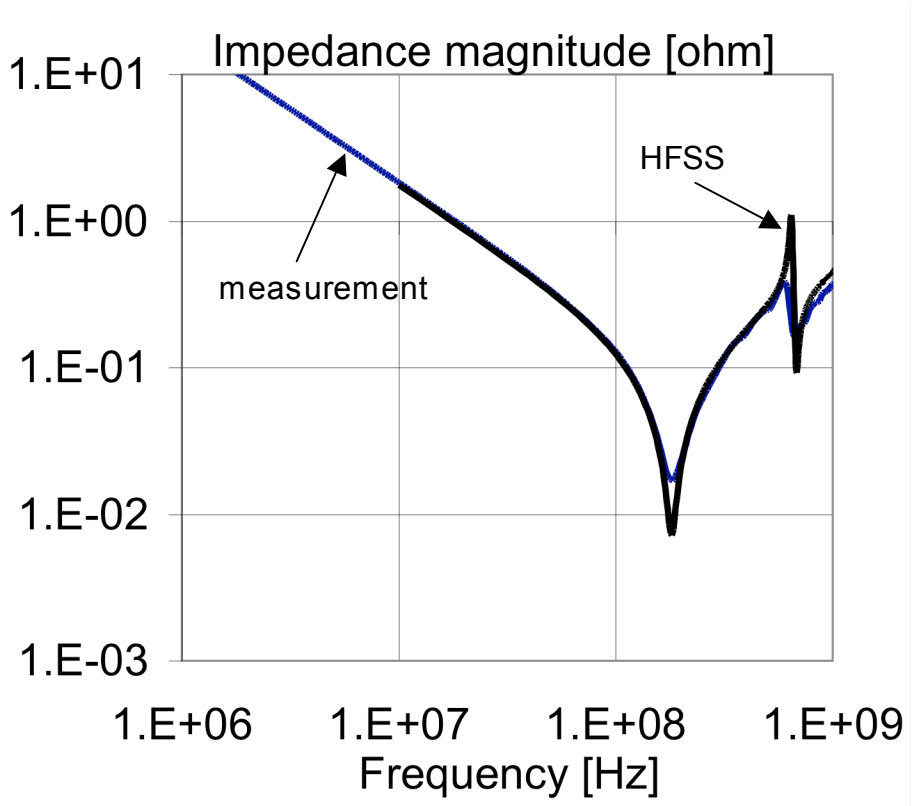


Measured and simulated results at d4e4 for a 8 um dielectric

Measurement correlation



Measured and simulated results at a1b1 with a 1 mil thick dielectric



Measured and simulated results at d4e4 with a 1 mil thick dielectric

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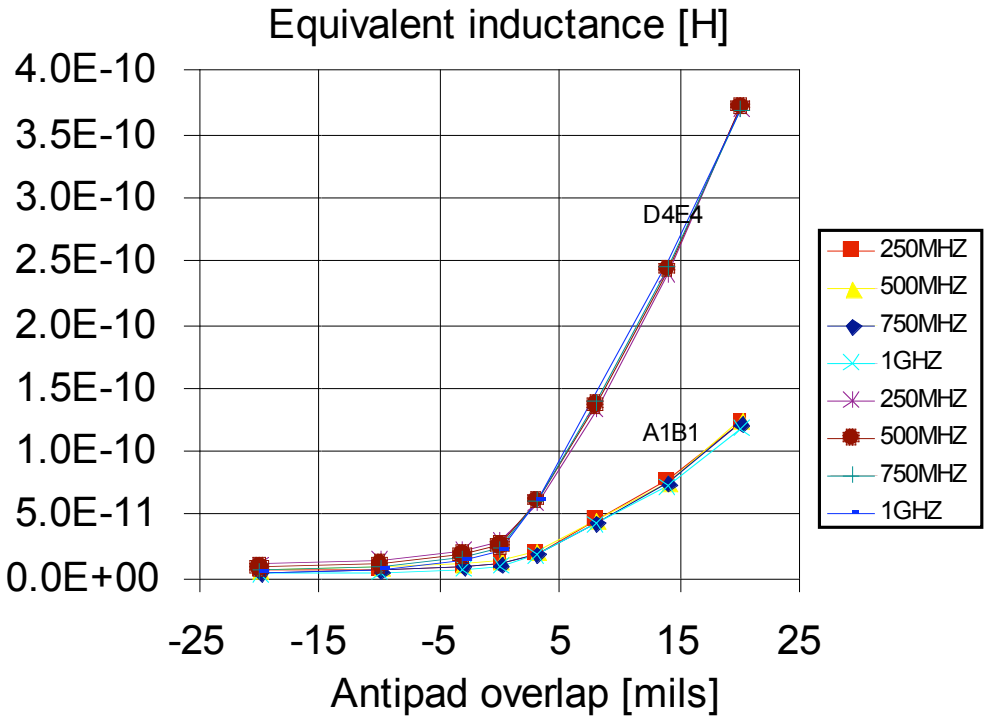
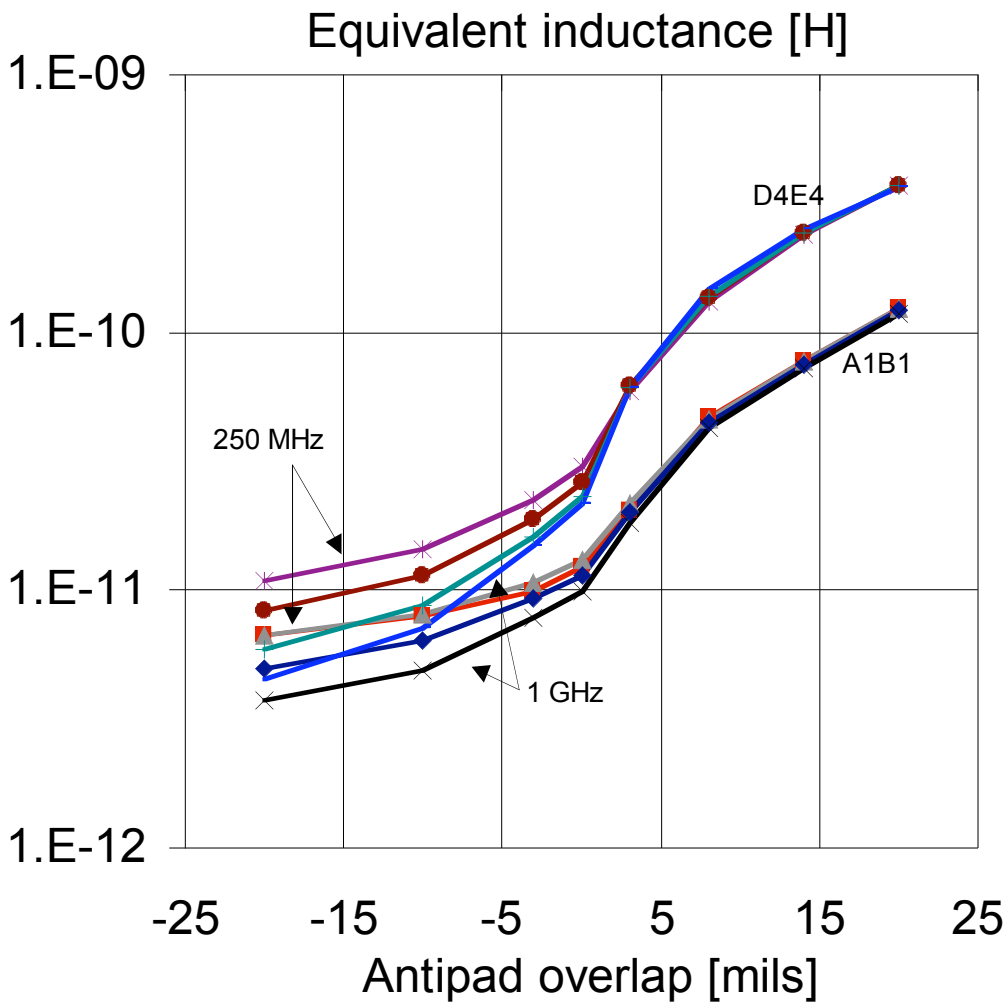
Antipad diameter parameterization

- Antipad overlap of zero means that the antipad diameter is 50 mils.
- Positive antipad overlap implies that the via center-to-center spacing is such that there is an overlapping opening in the power and ground planes.
- On a linear-linear scale the inductance is fairly flat for negative antipad overlap.

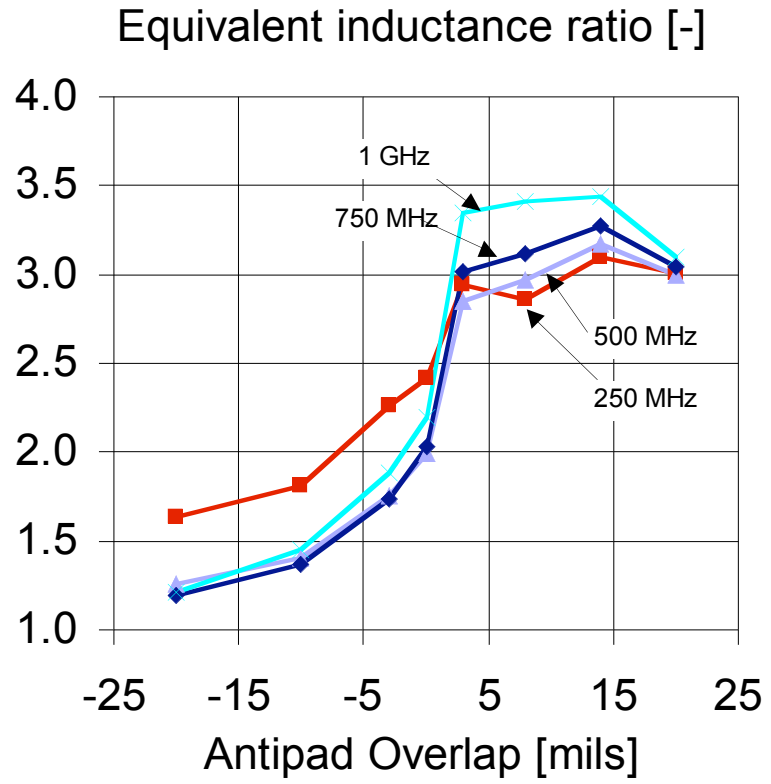


Antipad diameter parameterization



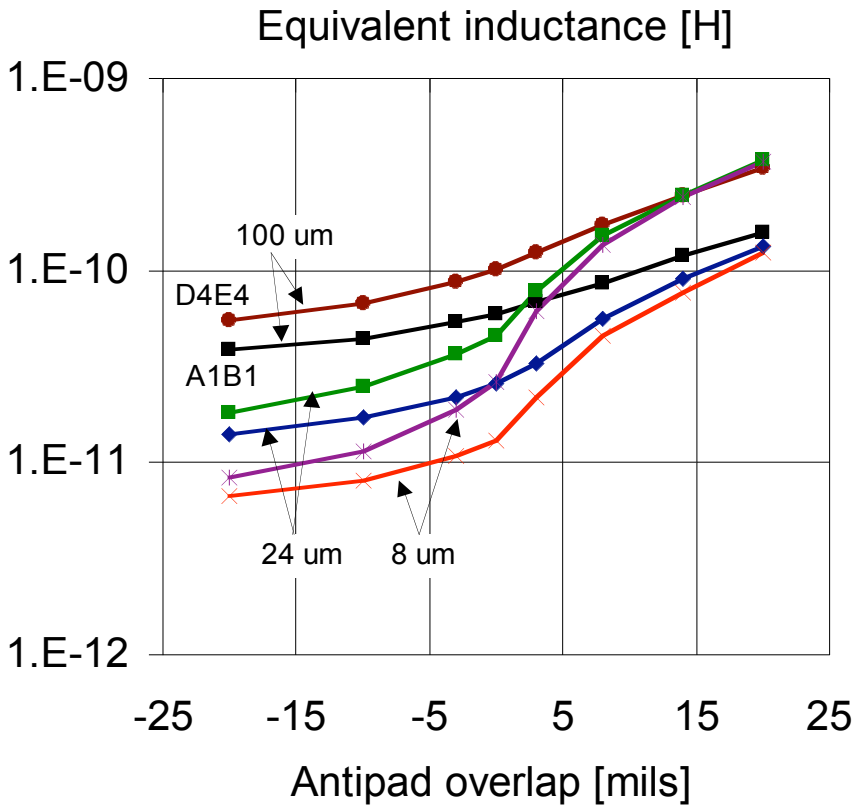
Antipad diameter parameterization

- Plots the **ratio** of the inductance at (D4,E4) over the inductance at (A1,B1) as a function of frequency.
- With positive antipad overlap the center via pair locations will have much higher inductance than the perimeter vias.
- With negative antipad overlap, the ratio of the inductances of the center vias to the perimeters vias asymptotically approaches one.



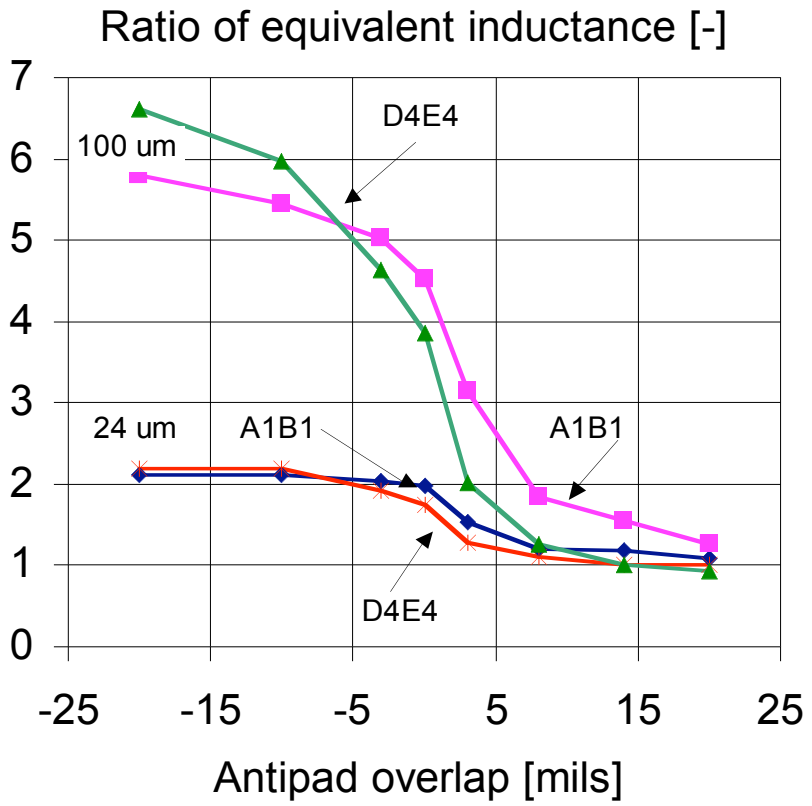
Dielectric thickness parameterization

- Plots the simulated equivalent inductance at (A1,B1) and (D4,E4) as a function of the antipad overlap for a 8 um, 24 um, and 100 um thick dielectric.
- 500 MHz had the smoothest impedance profile.
- For a given negative antipad overlap, increasing the dielectric thickness will increase the inductance at both locations in the array.
- As the antipad overlap increases, the inductance profiles converge for the center and perimeter locations, indicating that the antipad inductance dominates the plane inductance.



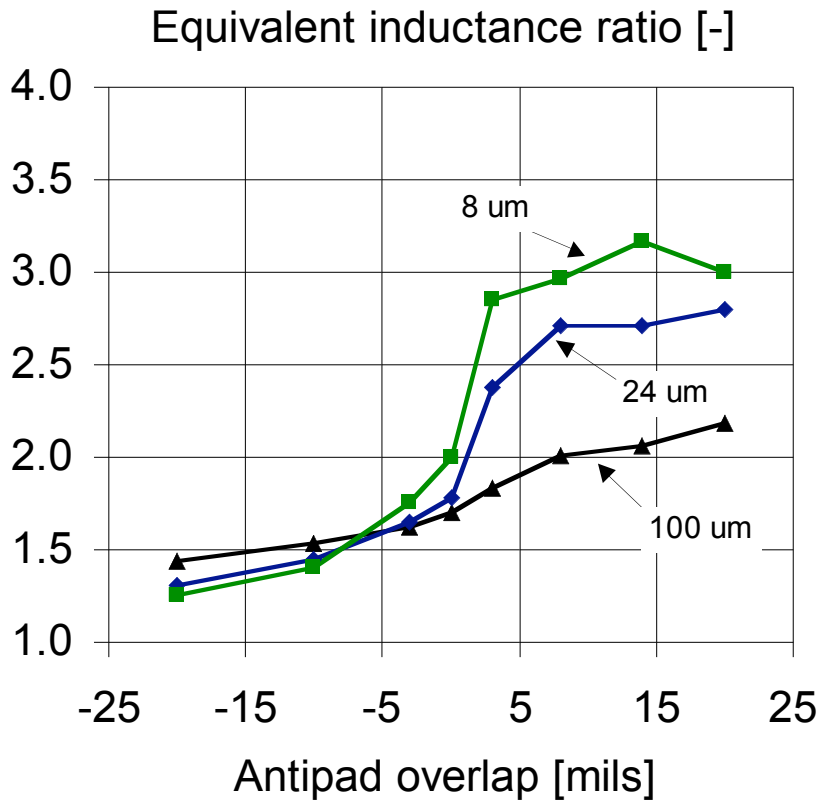
Dielectric thickness parameterization

- Plots the **ratio** of equivalent inductance of the 24 um and 100 um thick dielectrics to the 8 um thick dielectric at (A1,B1) and (D4,E4).
- Shows that for positive antipad overlap the dielectrics yield approximately the same equivalent inductance.
- Antipad diameter matters less and less with thicker dielectrics.

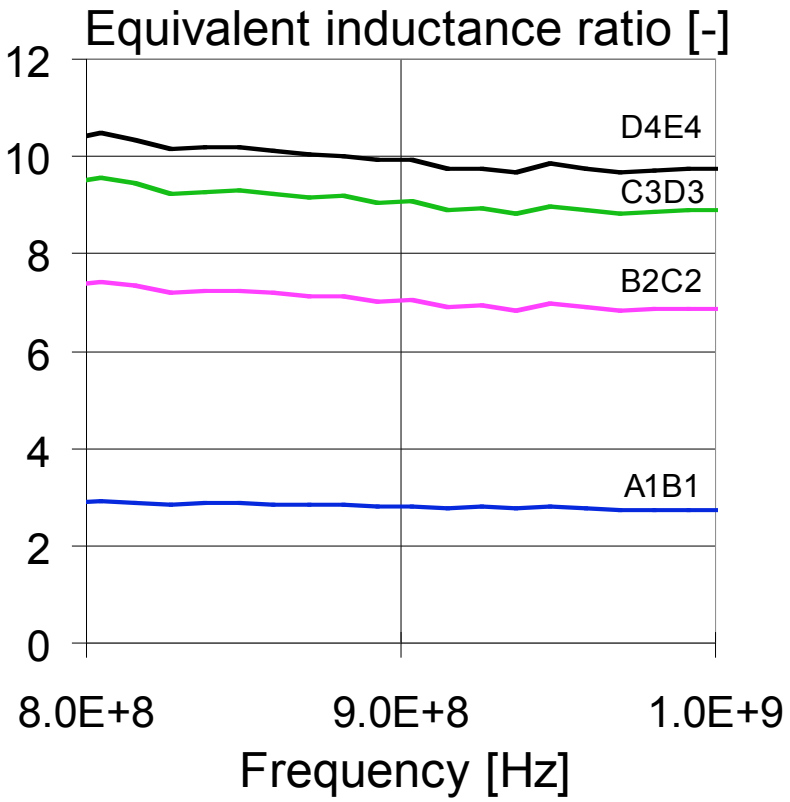


Dielectric thickness parameterization

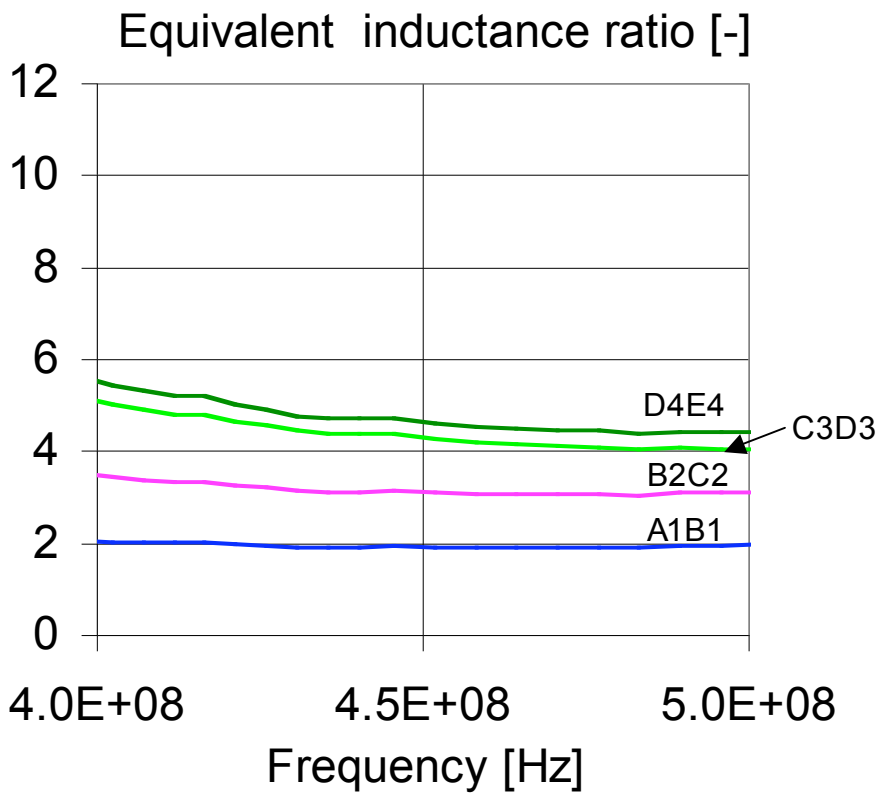
- Plots the **ratio** of the inductance at (D4,E4) to (A1,B1) at 500 MHz as a function of antipad overlap and dielectric thickness.
- Shows that thinner dielectrics materials will demonstrate more impedance variation.



Dielectric thickness parameterization



Measured inductance ratio for 8 um thick dielectric



Measured inductance ratio for 25.4 um thick dielectric

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Summary

- Excellent correlation was achieved between measurement and HFSS simulation.
- The measurement and simulation data show that the impedance measured across the array varies with location. Vias on the outside of the array have the lowest impedance and the impedance was found to increase sharply towards the array center.
- This variation can be reduced by using thicker dielectrics and decreasing the antipad size.

Summary

- Positive antipad overlap was found to dramatically increase the impedance for both the center and perimeter vias.

- This indicate that antipads in P/G via arrays should not overlap so that impedance is reduced (and a more uniform impedance is maintained across the array).

Summary

- Antipad size matters less and less as thicker dielectrics are used. Conversely, with positive antipad overlap the differences between the dielectric thicknesses are less important as the antipad inductance dominates.

- This suggests that the benefits of using thinner dielectrics to reduce the power plane impedance will be tempered by the relative proportion of antipad inductance.

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