DesignCon 2005

TecForum TF7

Inductance of Bypass Capacitors

How to Define, How to Measure, How to Simulate

Session organizer and chair:

Istvan Novak SUN Microsystems, Inc.

Presenters:

Zhiping Yang Cisco Systems Inc.
Leigh Wojewoda Intel Corp.
Larry Smith SUN Microsystems, Inc.
Hideki Ishida SANYO Electric Co., Ltd.
Masayuki Shimizu Taiyo Yuden Co., Ltd.

Abstract

Have you ever wondered why the same size bypass capacitor is listed with different inductance from different vendors? Do you want to know how some of the major OEMs want the inductance to be determined? Are you interested in knowing how major capacitor vendors measure the inductance? This TecForum will give an overview of how OEMs (Cisco, Intel, SUN) model capacitors, what are the important contributors to a capacitor's inductance in a real design, as well as how capacitor vendors (Sanyo, Taiyo-Yuden) do the testing. Participants who want a dialog with the presenters, can attend the panel discussion "Bypass capacitors: how to determine their inductance?"

Part I. Inductance of bypass capacitors, how to define, how to measure, how to simulate

Zhiping Yang, Cisco Systems Inc., 170 West Tasman Dr.,
San Jose, CA 95134, zhiping@cisco.com, 408-525-5690
Zhiping Yang, Senior Signal Integrity Engineer, Data Center, Switching, Wireless (DSW) Technology Group, Cisco Systems. His work is focused on signal integrity and power integrity in high-speed digital system design. His current responsibilities include the power integrity methodology development for Die/Package/Board co-design, signal integrity design and analysis for ASIC, package and PCB board, and UHS (Ultra-High-Speed) differential signaling for backplane application. He holds a Ph.D. degree in EE from the University of Missouri-Rolla.

Sergio Camerlo, Cisco Systems Inc., 170 West Tasman Dr. San Jose, CA 95134, Scamerlo@cisco.com, 408-527-1378
Sergio Camerlo, Director, Engineering, Data Center, Switching, Wireless (DSW) Technology Group, Cisco Systems. Mr. Camerlo's current organization is strongly focused on high-speed interconnects and advanced packaging technology and its application to the next generation products. Mr. Sergio's work on signal, timing, power integrity, and high-speed backplanes layout engineering has been successfully applied to several products currently in production. Mr. Camerlo is also chairing the Cisco Switching Patent Committee and is actively involved with the industry and academia to foster the development of new high-speed interconnects and packaging materials and methodologies.

Abstract

For any capacitors on the PCB board, its performance at the frequencies above the series resonant frequency is limited by its parasitic inductance associated with itself and PCB board mounting structures. How to define, measure and simulate the capacitor inductance is the topic of this paper.

Currently there are several capacitor component vendors and EDA tool vendors on the market, but there is no standardized way to define, measure and simulate the ESL (equivalent serial inductance) of the capacitor. Because of inconsistence in the ESL definition and application, it is hard to compare the performance of capacitors from different vendors and correlate the simulation results from different simulation tools.

In this paper, the authors looked at different elements of the inductance associated with capacitors on the PCB board and proposed an ESL definition based on physics and EDA tool interfaces. The reasons why it is very difficult to accurately define the ESL independence of the capacitor mounting structures and why the ESL is frequency-dependent are explained. Based on the ESL definition, the authors proposed a lab measurement method to extract the ESL of the capacitor on the PCB. In the end, the authors showed how significant the accuracy of the individual capacitor inductance has on the impact of the complete PCB through simulations.

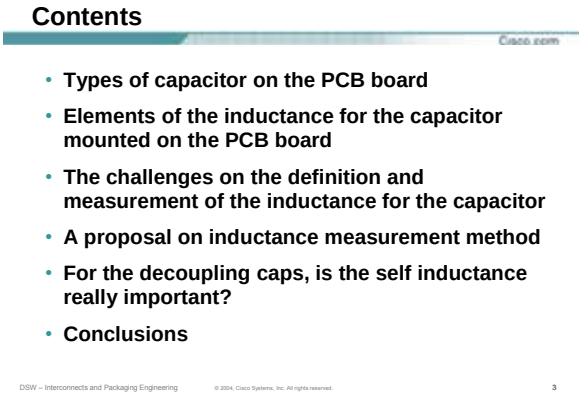
Background

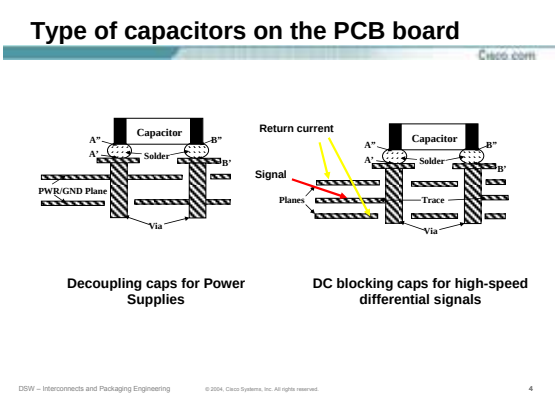
There are mainly two types of capacitor applications for digital circuits. The first one is power decoupling capacitors which are used for removing AC noises on the power delivery systems. The other one is DC blocking capacitors which are mainly for clock and other DC balanced high-speed signals.

Power integrity issues are more and more critical in high-speed designs with ever-increasing speed, frequency and power, as well as decreasing circuit dimensions and power levels. In order to solve and manage the power integrity issues at the design stage, the electronic industry is looking for solutions from the EDA tool vendors. As a key component in the power distribution system, decoupling capacitor plays a very important role in damping the high-frequency noises in the power delivery system. In order to accurately predict the performance of the complete power delivery system, EDA tools require accurate capacitor models in the simulation. The accuracy of the EDA tool simulation results partly depend on the accuracy of the capacitor models provided by capacitor vendors.

Because of the different capabilities within different EAD tools, the definition of the capacitor models may vary. For example, some EDA tools could handle the capacitor mounting structures within the tools itself so the capacitor models do not need to include the mounting structures. Some EDA tools can only handle plane structures, so its capacitor models include both capacitor itself plus the typical mounting structures.

For capacitor vendor, due to the lack of the standardized method to extract the capacitor model, each vendor uses its own way to measure/characterize the capacitor model. It is very hard to compare the capacitor performances between different vendors.





Elements of the inductance for capacitors on the PCB

In order to understand the elements of the inductance associated with capacitors on the PCB, it is better to understand the current path which goes through the capacitor. As what is shown in the following figure. The current path for the decoupling capacitor is from the power plane-> power via->power trace->power pad -> solder ball -> capacitor itself-> solder ball -> ground pad -> ground via -> ground plane. The current path for the DC blocking capacitor is a little bit complicated, but very similar. It is from the signal trace -> signal via-> signal trace on top -> capacitor pad-> solder ball -> capacitor itself ->solder ball -> capacitor pad -> signal trace on top -> signal via -> signal trace -> current return planes for signal trace.

Elements of the inductance for the caps on PCB

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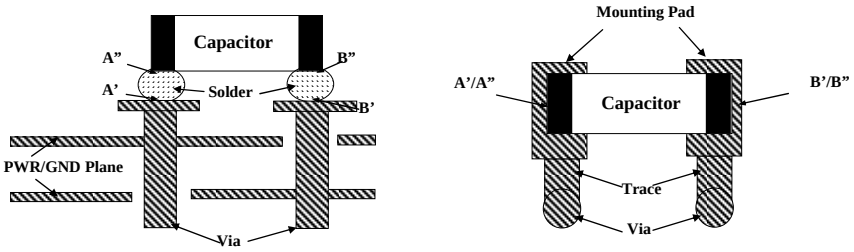


The current path (associated inductances) with different types of capacitor:

Decoupling cap: Power/Ground plane+Vias+Traces-on-top-layer+Pads+solders+capacitor
DC-blocking cap: Signal/return+Vias+Traces-on-top-layer+Pads+solders+capacitor

The partial inductances are associated with the elements of the current path. Some partial inductances are calculated and included in EDA tool. Some partial inductances are from the input component library which is generated by lab measurement or E/M simulators. For the above reason, it is beneficial for capacitor vendors, EAD tool vendors and board designer to have a clear boundary/definition of the capacitor ESL. Based on our experience with the EDA tools and board design experience, it makes sense to let the ESL of the capacitor only include the solder balls and capacitor itself. The rest of the components of the inductance should be handled by EDA tools.

Challenges with definition and measurement of the capacitor inductance

Besides the partial self-inductances we mentioned in previous section, there are also some mutual inductances between the partial self-inductances. Since the ESL of capacitor is from the capacitor vendors, and the mounting inductance is from the EDA tools, it is difficult to include the mutual inductance in the simulation since the mutual inductance is heavily dependent on how the capacitor is mounted on the board. For that reason, it is better to have the capacitor vendor measurement structure as close as possible to the real board application.

The typical MLCC (Mutil-Layer Ceramic Capacitor) is composed of mutil-layer power-ground planes within the capacitor body. At low frequency, the current is evenly distributed across every layer of the power/ground planes. If the individual plane pairs are modeled separately with the reset mounting structures on the PCB board, it is easy to see that different plane pairs have the different loop inductance. As we know that high-frequency current will flow more on the least inductance path, the current distribution within the capacitor itself will vary according to the height of the capacitor. Since the top power/ground pair has the largest inductance, it has the least current flowing through. For the same reason, the bottom power/ground pair has the largest current flowing through. Exactly how current is distributed across the total height of the capacitor is a function of the capacitor height, distance from capacitor to power/ground planes and the interested frequency.

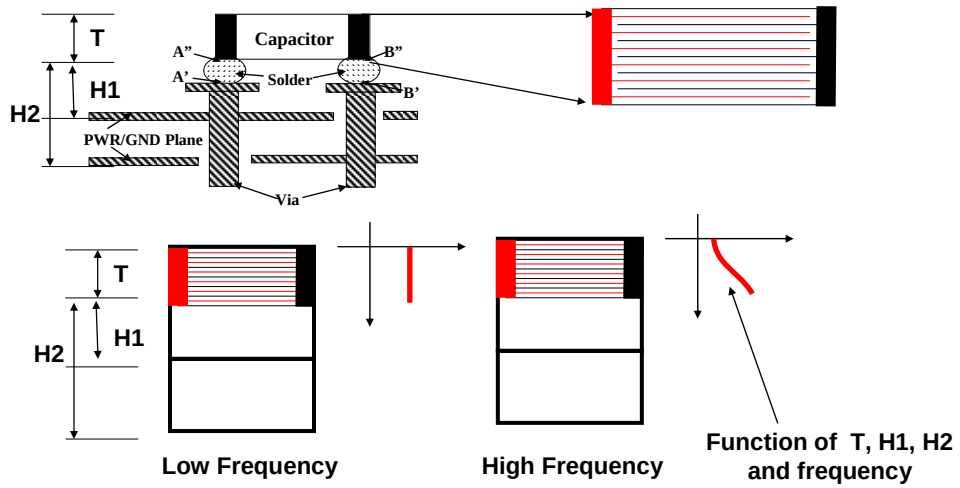
The challenges on defining and measuring the inductances the caps

- Where should the partial inductances be separated between the EDA tool vendors and Capacitor vendors?
- There are couplings between each components of the inductance. The couplings make the total inductance to not be simple addition.
- Inductance is associated with current distribution. At different frequencies, the current distribution will vary internal & external of the capacitor.

Examples:

- L_total=(L_planes+L_vias+L_traces+L_pads+L_solder)+(L_capacitor)+/-2*M_mutuals
- Mutual inductance is complicated and its value varies with the ways of capacitor mounting structures.

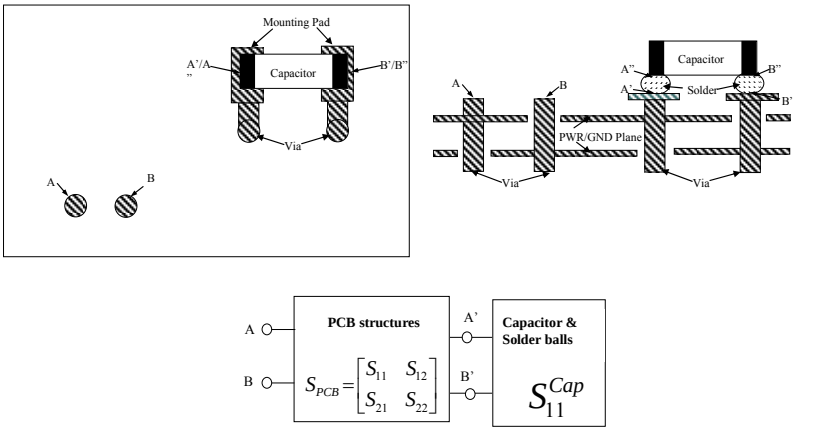
Example of current distribution at different frequencies



A proposal on how to measurement the capacitor ESL in the lab

It is desired to have the exact same or similar capacitor mounting structures on the capacitor ESL measurement board and the real application. As shown in the following picture, the capacitor should be mounted as close as possible to the real application.
Two sets of VNA measurement should be performed on the above test structures. First measurement is two-port VNA measurement before the capacitor is soldered on the board. One port is placed on the capacitor pads, and the other port is placed on the observation point A-B. It is recommended to use micro-probe station to perform such measurement. In order to enhance the measurement accuracy for non-50 test structure, some special measurement techniques are desired and necessary. The inaccuracy of this measurement could cause some unstable result in the final calculation. The second measurement is performed on port A-B with the capacitor is soldered on the board. The technique by using two-port S21 to get self-impedance is recommended. The details about this technique can be found in [1]. By using the equations on the following figure, the complete impedance profile of the capacitor can be extracted.

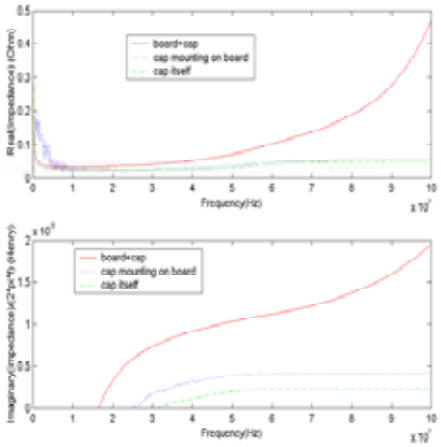
A proposed to measure the capacitor plus solder inductance



Equations and results

$$S_{11}^{AB} = \frac{S_{11} - (S_{11} * S_{22} - S_{12} * S_{21}) * S_{11}^{Cap}}{1 - S_{22} * S_{11}^{Cap}}$$

$$S_{11}^{Cap} = \frac{S_{11}^{AB} - S_{11}}{(S_{11}^{AB} - S_{11}) * S_{22} + S_{12} * S_{21}}$$

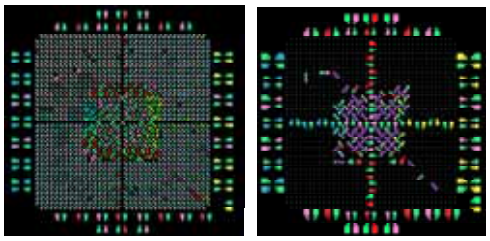


The VNA measurements are performed with HP 875ES/85047A with the help of the Micro-probing station GTL4060 from Gigatest Lab. The micro-probe is 40A-SG1250-EDP from Picoprobe. The VAN is calibrated through CS-11 calibration Substrate. Some test results are shown on the above figure. From the capacitor impedance, the frequency-dependent ESL can be easily obtained.

How significantly does the ESL accuracy of decaps impact the system simulation results?

In order to evaluate the impact of the ESL of decaps on the performance of the power delivery system, a real power delivery system was used. The real system board is shown in the following figure. The numbers of different sized capacitors and the corresponding power supplies are also shown. Total four simulations were performed and only the ESL of the 0402 and 0603 capacitors varied. In the first simulation which is the base case, the ESL of the 0402 capacitor is 0.8nH and ESL of the 0603 capacitor is 0.9nH. In the second simulation case, the ESL of 0402 keeps the same, but the ESL of the 0603 is 0.7nH (22% of reduction). In the third case, the ESL of the 0402 keeps the same, but the ESL of the 0603 capacitor is 0.45nH (50% reduction). In the fourth case, both the ESLs of 0402 and 0603 capacitors are reduced to half.

Is the accuracy of decap inductance really critical to your design?



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Capacitor values and connections

Voltage	0402 cap	0603 cap	0805 cap
Core	60	36	12
I/O_1	6	20	4
I/O_2	7	21	7
I/O_3	6	21	5

Simulation cases:

1. L_0603=0.9nH, L_0402=0.8nH
2. L_0603=0.7nH, L_0402=0.8nH
3. L_0603=0.45nH, L_0402=0.8nH
4. L_0603=0.45nH, L_0402=0.4nH

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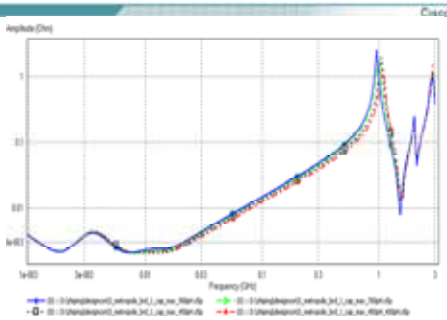
The total impedance profiles are shown in the following figures. The results show the total impedance variations are 4%, 11% and 18% for case #2, #3 and #4. If the impact from the 0402 and 0603 capacitor are calculated separately for this test board, we can get that the ESL of 0603 capacitor has error-transfer-rate about 22% (11%:50%) and the ESL of 0402 capacitor has error-transfer-rate about 14% ((18%-11%):50%). The reason why 0402 has lower error-transfer-rate is due to the fact that it has more capacitors (60 total) than 0603 (36 total).

Simulation Results



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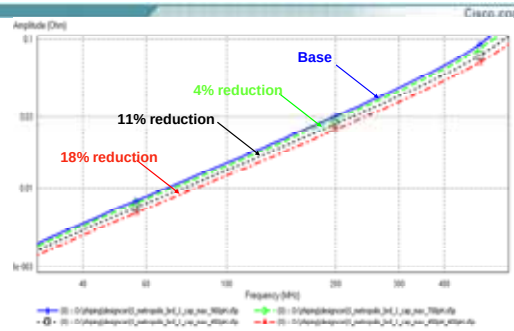
Simulation Results



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Conclusions

As a summary, the standardized ESL definition for the capacitor is desired for high-speed digital circuit design and simulation. In the reality, the partial inductance is only valid and accurate for a certain structures, so it makes it hard to define and extract a universal and accurate ESL value for different capacitor mounting structures. For the same reason, it is recommended to have the capacitor placement on the ESL measurement board as close as possible to the real application.

Acknowledgement

The authors would like to thank Dr. Wheling Cheng, Syed Huq and Vinu Arumugham for helpful discussions and support. John Fisher and Gurpreet Hundal performed the measurement on the test board. Their contribution to this paper is greatly appreciated.

References

[1] I. Novak, "Probes and Setup for Measuring Power-Plane Impedances with Vector-Network Analyzer," Proceedings of the 1999 DesignCon High-Performance System Design Conference, Feb. 1-4, 1999, Santa Clara, CA, pp. 201-215.

Part II. Measurements and Modeling of Microprocessor Decoupling Capacitors

Leigh Wojewoda, Intel Corp., Leigh.e.wojewoda@intel.com
Leigh Wojewoda joined Intel in 1997 and has worked since then in the Assembly Technology Development division in Chandler, AZ. Leigh Wojewoda is a Senior Packaging Engineer and currently manages an electrical measurement lab. She is responsible for development and characterization related to microprocessor packaging. The lab is also active in demonstrating new measurement techniques and correlating measurement results with various Intel suppliers. Leigh holds a BS in Engineering Physics and a MS in Mechanical Engineering from the University of Arizona. Contact her at leigh.e.wojewoda@intel.com.

Michael J Hill, Intel Corp., Michael.j.hill@intel.com
Michael J. Hill is a Sr. Electrical Packaging Engineer at Intel Corporation in Chandler, Arizona. He has been with the Electrical Analysis and Design group working on power delivery analysis and metrology development since 2002. Prior to coming to Intel, Michael was involved in the development of a high density active microwave phased array for use in medical applications, and later on the development of wireless networking hardware and measurement systems. These systems focused on medium and low gain antenna characterization utilizing spherical near-field scanning techniques. Michael is a member of the IEEE Microwave Theory and Techniques Society, Etta Kappa Nu, and Tau Beta Pi. He holds B.S., M.S. and Ph.D. degrees in Electrical Engineering from the University of Arizona. Michael can be reached by email at: Michael.j.hill@intel.com

Abstract

This paper presents an overview of the measurements and models used by Intel to characterize microprocessor decoupling capacitors. This paper will discuss measurements and modeling of multi-layer ceramic capacitors using an LRC lumped element model. A technique for highly repeatable inductance, resistance and capacitance measurements will be described. A procedure for inductance modeling and prediction using Ansoft Q3D Extractor™ will also be presented, along with examples of measurement to model correlation. Applications of the technique will be discussed. The applications include results of inductance measurements from semi-high volume scenarios and characterization of a recently introduced capacitor.

Introduction

Multi-Layer Ceramic Capacitors (MLCC) are a critical element in the design of power delivery networks of microprocessor packages. Accurate modeling and prediction of decoupling capacitor behavior is crucial due to short design cycle times. Stable and repeatable characterization techniques are required to ensure consistency of capacitor parameters. Once correlation is established between modeling and measurement methods, predictions can be trusted for more complex or even non-measurable cases, such as CPU packages with complicated current flows.

Because capacitors are an integral element in power delivery design, a robust characterization method is required. When establishing a characterization method for capacitors, many options are available. Various options were examined prior to establishing the measurement technique described in this paper. There were many opportunities for trade-offs between model complexity and ease of use. The following criteria were considered during the methodology development.

- Various families of capacitors were used within Intel. This meant that the characterization technique had to be extendable to a large number of capacitor types.
- Users of characterization data and models had differing levels of expertise. Because of this, the measurement and modeling tools had to be easy to understand and apply.
- Measurement correlation had to be established at other labs within Intel. This required that the measurement technique was stable and repeatable before transferring the procedure to other measurement sites.
- Finally, a further constraint was added by supplier needs. The technique had to be simple and fast enough for use in a semi-high volume measurement scenario.

This paper will discuss measurement and modeling techniques developed in response to the concerns listed above. Applications of the technique will also be discussed, including results of inductance measurements from semi-high volume scenarios. Finally, the impact of applying incorrect capacitor models as they relate to measurement techniques will be discussed utilizing a recently introduced capacitor as an example.

Measurement

Test Fixture

One of the early challenges of microprocessor capacitor measurements was issues with the existing test fixture. The existing test fixture was comprised of a two layer PCB design where the capacitor was assembled between the signal and ground of a 50 Ohm transmission line. A further description of the PCB test fixture may be referenced in a previous publication [1]. Several issues were identified with this test fixture: variation in test fixtures, relevance of inductance data, and extensions to advanced capacitors.

The first issue, variation in test fixtures, was a result of using test fixtures designed by different sources. Although the fixtures were similar, differences in inductance measurements were attributed to small differences in test fixture design. The second issue, relevance of inductance data, was also related to the fixture design. The existing fixture design was not similar to the actual design implementation on a microprocessor package. Because of this, the measured inductance of a capacitor on a test fixture did not directly apply to a package design. A further discussion of increased capacitor inductance due to layout has been discussed in past publications [2]. Finally, the PCB design rules did not have the capability to route the fine pitch features necessary for advanced capacitors.

The Universal Capacitor Test Vehicle (UCTV) was created by Intel to address these issues. The UCTV was designed to measure package capacitors in a consistent way. Figure 1 contains an illustration of a test site on the UCTV. The UCTV contains test sites for various capacitor form factors and is manufactured using a build-up process similar to the process used for Intel's microprocessor packages. Each capacitor is measured on a two layer structure, representing a simplified power/ground design. Measurement of the capacitor parameters includes both capacitor and package contributions. Although the capacitor inductance can be de-embedded, it is not typically of interest in this usage. The measurement represents realistic package contributions, which can become significant in the case of the advanced capacitors. The inductance of capacitor and fixture can be modeled using Ansoft Q3D Extractor™. The modeling technique will be discussed Section VI.

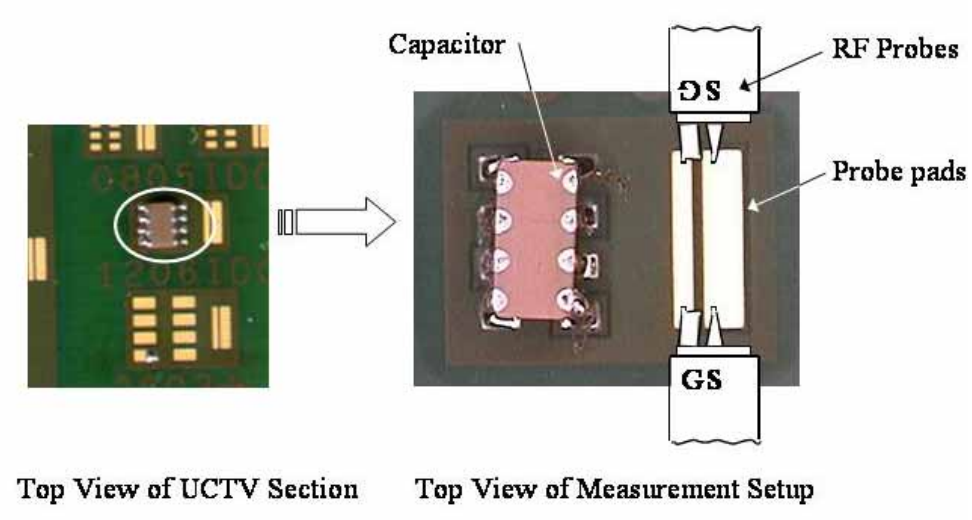

Figure 1. The Universal Capacitor Test Vehicle

Measurement Setup

The measurement setup is illustrated in Figure 2. The setup utilizes a 2 port Vector Network Analyzer (VNA) measurement. The capacitor and test fixture are connected in a shunt configuration between the two ports. Contact to the board is made with 250 um pitch SG/GS RF probes. An SOLT technique is used for calibration. The frequency range of 30 kHz to 3 GHz is typically sufficient to capture the resonance frequency observed in the transmitted S Parameters (S12 or S21). Although all reflected and transmitted S Parameters (S11, S12, S21 and S22) are downloaded from the VNA, only the S21 parameter is used during the data fitting process. Only the S21 data is used because the measurement sensitivity of S11 and S22 is generally poor for measured impedances typically seen with decoupling capacitors.

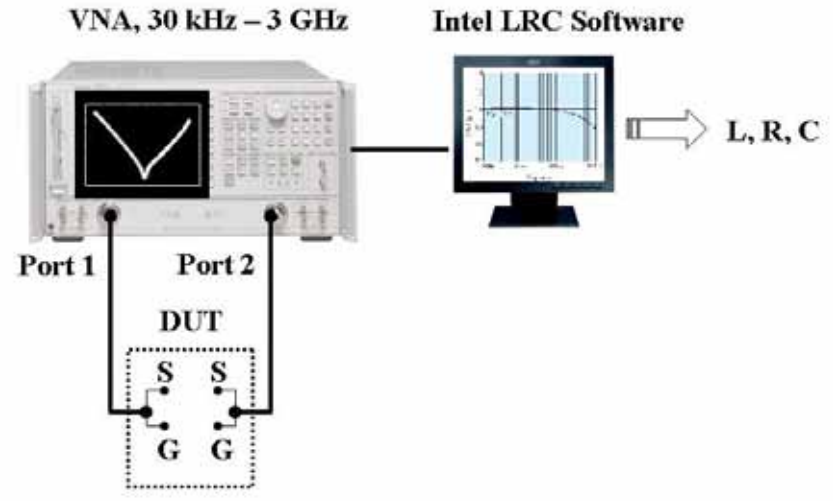

Figure 2. Inductance Measurement Setup

Lumped Element Model

The equivalent circuit for this measurement is illustrated in Figure 3. The capacitor and package assembly is represented as a lumped element model consisting of inductive, resistive and capacitive elements. The elements of this model are constant, frequency independent values.

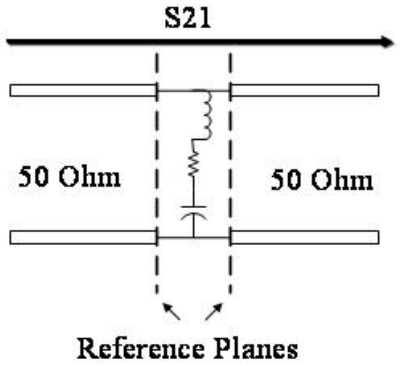

Figure 3. Lumped Element Model of Capacitor

Values for L, R and C are obtained by comparing the measured S21 curve to a theoretical curve. In the earliest measurement attempts, the values of L, R and C were manually adjusted until a user judged the fit "sufficient". Studies were completed to determine how much variation a single operator could introduce by the use of manual fitting techniques. Measurements were completed on capacitors with inductances ranging from 500 pH to 900 pH. It was determined that a single operator could add as much as a 25 pH discrepancy solely due to variations in manual curve fitting.

A second study was completed to examine the measurement repeatability. This type of experiment is useful to predict stability of the system, which is crucial for measurement correlation with other sites. The study examined data collected over a period of several days by three operators, each fitting the data manually. The output of the study was a tolerance which bounded the expected measurement variation. Historically, the labs at Intel have defined tolerance bounds on a measurement technique using a 6 sigma confidence level.

The results of the study are listed in Table 1. The error bound for an inductance measurement was +/- 13%. This would indicate that the technique could not reliably distinguish (with 6 sigma confidence) between a capacitor with an inductance of 112 pH and one with an inductance of 146 pH. For measured values of resistance, the error bound was even larger.

Parameter	Nominal Value	Pre-Automation Measurement Error Bound
L	129 pH	+/- 13%
R	8.5 mOhm	+/- 34%
C	0.1902 uF	+/- 16%

Table 1. Measurement Error Bounds Before Automated Data Fit Technique

Automated Data Fitting Technique

The need to improve the measurement technique was driven by the results in Table 1. A +/- 13% error in inductance characterization was not sufficient to resolve the effect of design changes in either the capacitor or package. The major source of error was determined to be discrepancies from individual users manually fitting the data. Software was developed to standardize the curve fitting technique. The software used the complex values of S21 to calculate L, R and C in the following three equations.

$$L = \frac{j(j - j \cdot s21 - C \cdot R \cdot \omega + 25 \cdot C \cdot s21 \cdot \omega + C \cdot R \cdot s21 \cdot \omega)}{C \cdot (s21 - 1) \cdot \omega^2} \quad (1)$$

$$R = \frac{-j(1 - s21 - 25 \cdot j \cdot C \cdot s21 \cdot \omega - C \cdot L \cdot s21 \cdot \omega^2)}{C \cdot (s21 - 1) \cdot \omega} \quad (2)$$

$$C = \frac{j(s21 - 1)}{\omega(-R + 25 \cdot s21 + R \cdot s21 - j \cdot L \cdot \omega + j \cdot L \cdot s21 \cdot \omega)} \quad (3)$$

The algorithm has been described in a previous publication and will only be summarized briefly in this paper [3]. The algorithm fits C at low to midrange frequency values. The value for C is then used to find L and R. L is fit at points above the resonant frequency. R is fit at points near the resonant frequency. This method was selected purposely over a least-squares approach to avoid excessive influences by higher order parasitics that would results in poor first order model values.

Quantification of Data Fit Improvement

Once the automated data fit algorithm was implemented, the error bounds were again quantified. Table 2 contains a comparison of error bound pre and post automation. The inductance error bound dropped from +/- 13% to +/- 3%.

Although the error was reduced, the error bound for R was still relatively high. It should be noted that the extraction of R is dependent on the depth of the resonance. Smaller values of R become increasingly difficult to measure with this technique. The same measurement technique was repeated on a different capacitor with an ESR of 50 mOhm. The technique yielded an error bound of +/- 5% for a mean value of 50 mOhm.

Parameter	Nominal Value	Pre-Automation Measurement Error Bound	Post-Automation Measurement Error Bound
L	129 pH	+/- 13%	+/- 3%
R	8.5 mOhm	+/- 34%	+/- 11%
C	0.1902 uF	+/- 16%	+/- 3%

Table 2. Comparison of Error Bounds With and Without Automated Fit Technique

Measurement Error Modeling

The repeatability study demonstrated the ability to reproduce a measurement and allowed a bound to be placed on the error of a typical measurement with multiple operators. The next step was to investigate the contribution of the measurement system alone. This section describes a modeling procedure used to determine the best accuracy that could be expected from the measurement system.

The sensitivity of the extraction to various system non-idealities was studied. This was accomplished by creating a model to quantify the amount that the extracted values of L, R and C could be perturbed by the measurement system. Figure 4 shows an error model of the measurement system. The model of the measurement system included the VNA, probes and cables. The VNA element included errors related to uncertainty in S21 magnitude, uncertainty in S21 phase, dynamic range, source power, IF bandwidth, averaging and frequency stability. The probe error elements were represented by series L and R terms. A transmission line with loss and variable impedance was added. Finally, R, L and C elements were added to represent the capacitor under test. In Figure 4, the capacitor parameters are labeled R_{DUT}, L_{DUT} and C_{DUT}.

To estimate the impact due to the various errors, model sweeps were performed. VNA, probe and transmission line errors were varied for given values of R_{DUT}, L_{DUT} and C_{DUT}.

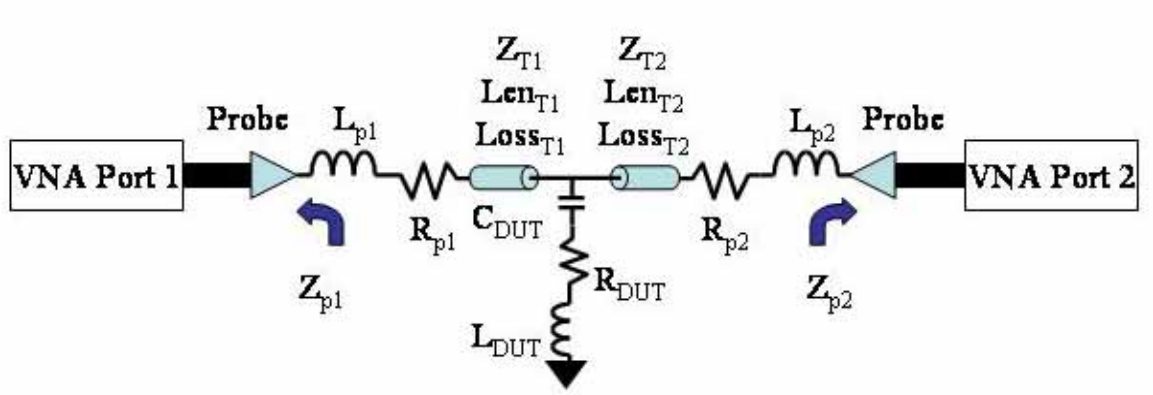

Figure 4. Error Model of Measurement System

The fitting algorithm was then used to extract L, R and C from the perturbed model data. The extracted values were compared to the R_{DUT}, L_{DUT} and C_{DUT} values in the model to determine a percent error. The error data was implemented in a reference table. The impact of the non-idealities is reported by the LRC fitting software package along with the extracted values of L, R and C.

Measurement Applications

Semi-High Volume Inductance Data

The measurement technique described in Section IV was transferred to several capacitor suppliers. Monitors for L, R and C were implemented in a semi-high volume scenario. A typical sampling plan selected a given number of capacitors from different manufacturing lots. The measurements provided a mean value and standard deviation representing the manufacturing distribution. Estimations of the manufacturing distribution may be found by applying the "Sigma Rule". The width of a normal distribution of data can be approximated by six standard deviations. For production ready capacitors, typical variations of inductance were found to be approximately +/-15% for a single supplier. When capacitors were procured from two suppliers, it was possible for bimodal distribution to be present. In this scenario, variations of +/-30% have been observed.

Bimodal inductance distributions may occur when capacitors have differing critical dimensions. Two of these critical dimensions are shown in the cross section in Figure 5. The dimension labeled "cover layer" is the height from the base of the capacitor body to the first internal capacitor plate. The dimension labeled "solder fillet" is the height from the capacitor base to the capacitor land on the package. Cover layer thickness, as well as other dimensions, may vary between different manufacturers, causing a skew in measured inductance.

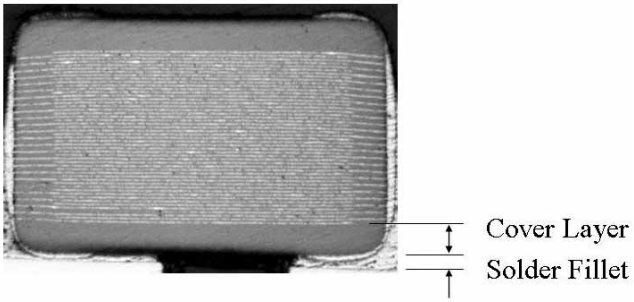

Figure 5. Cross Section of an MLCC

Inductance Modeling Using Ansoft Q3D

The measurement technique described in Section VI has been well correlated to inductance models in Ansoft Q3D Extractor™. This section will describe the modeling procedure and provide correlation values between model and measurement.

Inductance Modeling Procedure in Ansoft Q3D

The inductance modeling procedure makes use of Ansoft Q3D Extractor™ and the layout extraction tool, AnsoftLinks™. In the modeling procedure, two elements are created, the package test structure and the capacitor. The first element, the model of the test structure, can easily be created with AnsoftLinks™. AnsoftLinks™ can be utilized to extract a three dimensional model directly from the layout database.

The second element of the model is the decoupling capacitor. The modeling technique utilizes a simplified representation of a capacitor, shown in Figure 6. In Ansoft Q3D Extractor™, the capacitor is modeled as a conducting sheet. For good model correlation, critical dimensions of the capacitor must be accurately represented. The height of the simplified conductor model must reflect the cover layer and solder fillet dimensions. Other dimensions of interest include the capacitor internal plane size. For multi-terminal capacitors, the width of the electrodes is required for model construction.

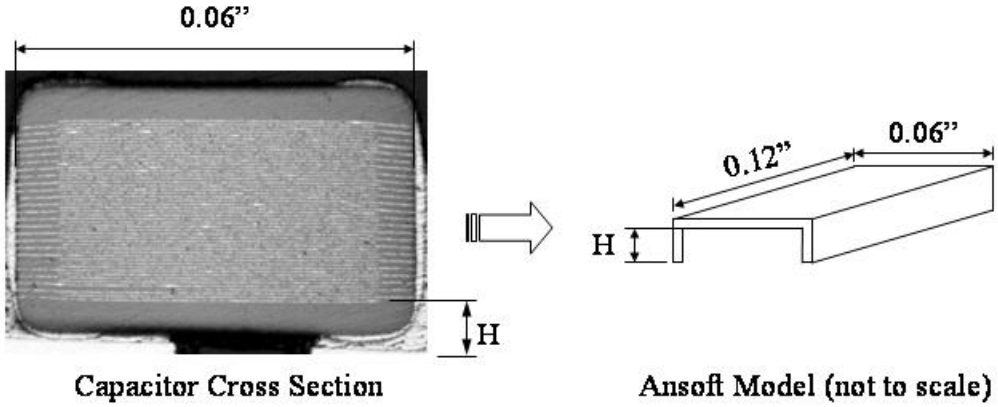

Figure 6. Example of Ansoft Model of 0612 2 Terminal Capacitor

In the final step of model construction, the capacitor and package models are combined. To simulate the model, sink and source terminals are drawn to represent the probe pads. A model of a multi-terminal capacitor and test structure is illustrated in Figure 7.

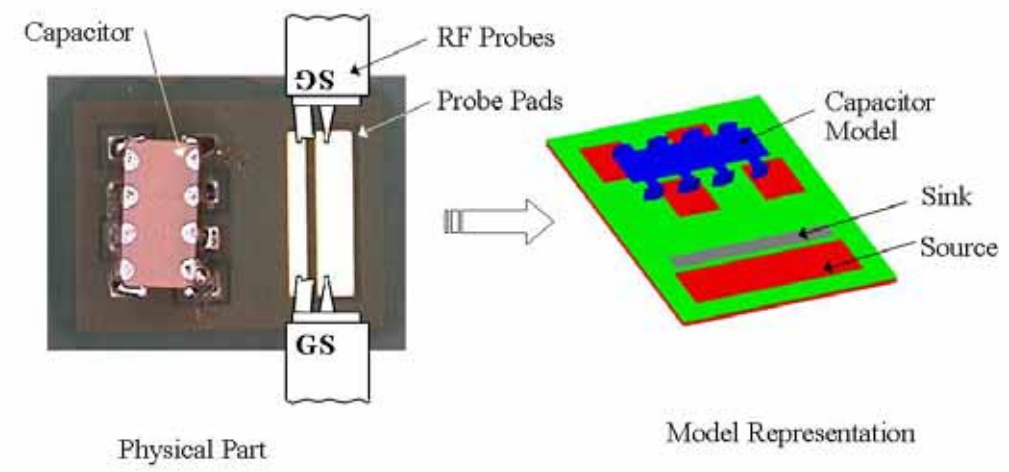

Figure 7. Physical Capacitor and Test Structure and Model

Model to Measurement Correlation

Table 3 lists the results of model to measurement correlation for several types of capacitors. Measurements were completed following the automated data fit routine described previously. Models were constructed using dimensions obtained from cross sectioning the actual part after measurements were completed. Model to measurement comparisons using techniques described in the paper repeatedly show correlation of 10% or better.

Cap Type	Modeled L (pH)	Measured L (pH)	Correlation
0306, 2 Terminal	142	131	8%
0805, 8 Terminal	109	99	10%
1206, 2 Terminal	536	520	3%

Table 3. Comparison of Modeled and Measured Inductance

Recently, software tools have been developed by Intel to address full wave capacitor characterization methods [4]. The modeling technique described in this paper cannot predict frequency dependent behavior or account for currents flowing in the upper layers of the capacitor. However, the established modeling to measurement agreement of 10% is much better than the manufacturing variations observed. As mentioned previously, manufacturing variations of 30% have been observed, thus placing a practical limit on the value of more sophisticated modeling methods.

Example of Inaccurate Characterization

An interesting application of the techniques described in this paper is the evaluation of a recently introduced capacitor. The capacitor, which will be referred to as Capacitor A, is shown in Figure 8. The datasheet for Capacitor A specifies an inductance of 1 pH in a decoupling usage. This claim was investigated using two fixtures provided by the manufacturer.

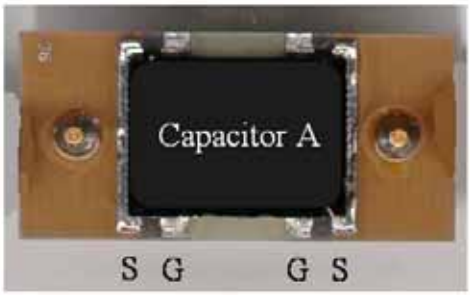

Figure 8. Capacitor A on a Test Fixture

An explanation of feedthrough and decoupling capacitor configurations is required to understand Capacitor A's 1 pH inductance specification. Figure 9 illustrates the difference between a capacitor in a decoupling configuration and one in a feedthrough configuration. In a decoupling configuration, an appropriate capacitor model is L, R and C elements in shunt between the two ports, as described in Section IV. A capacitor in a feedthrough configuration may be more correctly represented by a Tee filter. An equivalent circuit for a simple Tee filter is shown in Figure 9.

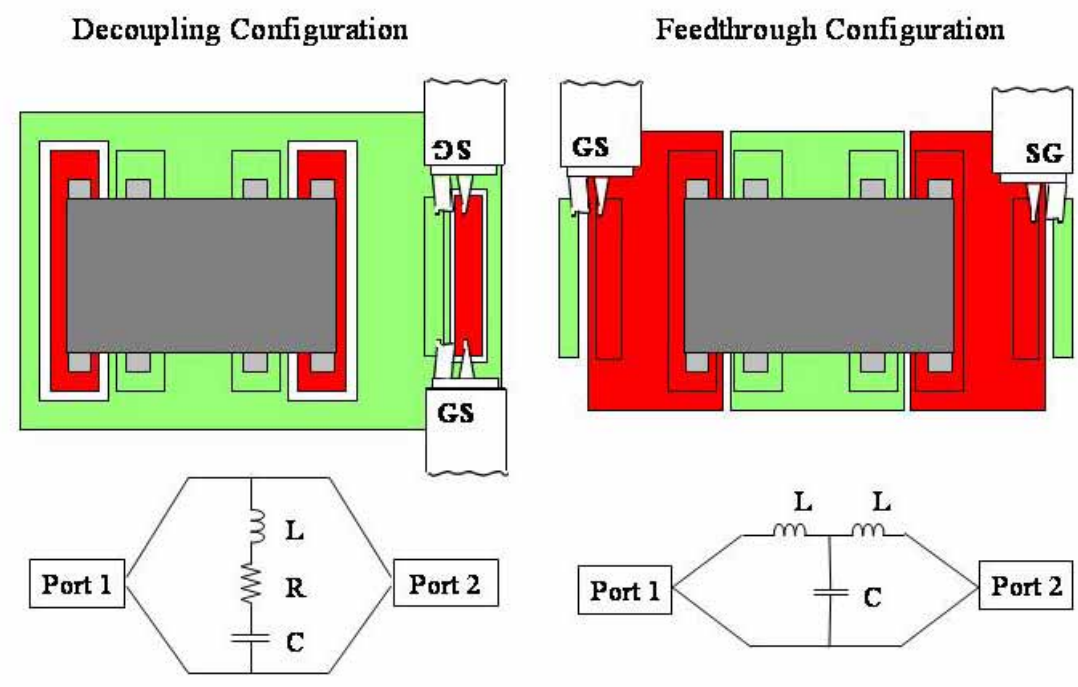

Figure 9. Capacitor A in Feedthrough and Decoupling Configurations

When the incorrect decoupling model was applied to the feedthrough measured data, unrealistic inductance values were generated, as shown in Figure 10, Graph B. This was because the decoupling curve could not be made to overlap the feedthrough data. Thus, by incorrectly applying the series LRC model to the feedthrough cap, an erroneous 1 pH value was found. This illustrates the importance of implementing and understanding the correct model when fitting capacitor data.

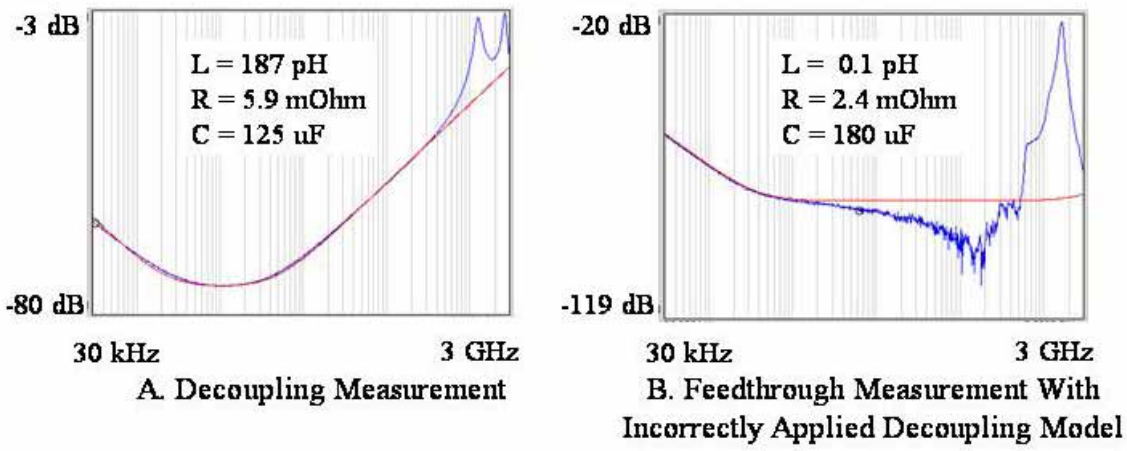

Figure 10. Capacitor A Decoupling and Feedthrough Measurements

Table 4 contains a comparison of modeled to measured inductance values for Capacitor A. On a 2 layer PCB style decoupling test fixture, a correlation of 7% was obtained between model and measurement. No package style decoupling fixtures were available for measurement. However, model predictions show an inductance of 222 pH for Capacitor A on the UCTV.

Fixture Type	Modeled L (pH)	Measured L (pH)	Correlation
Decoupling, PCB	201	187	7%
Decoupling, Package	222	NA	NA

Table 4. Capacitor A Inductance Values on Decoupling Style Fixtures

Conclusions

This paper described capacitor measurement and modeling techniques in relation to practical applications, such as semi-high volume measurements. The reproducibility of Intel's capacitor characterization method was examined and correlated to the modeling procedure. Finally, this paper illustrated a case of improper model usage, which led to incorrect results.

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[3] Michael J Hill, Leigh Wojewoda, "Capacitor Parameter Extraction – Techniques and Challenges," Intel Technology Symposium, Fall 2003.
[4] Joong-Ho Kim, et al,. "Characterization of Discrete Decoupling Capacitors for High-Speed Digital Systems," *Proc. 54th Electronic Components and Technology Conference*, pp 259 – 265, June 2004.

Part III. MLC Capacitor Parameters for Accurate Simulation Model

Larry D Smith, Sun Microsystems, Inc.
Larry D Smith received the BSEE degree from Rose Hulman Institute of Technology in 1975 and the MS degree in Material Science from the University of Vermont in 1983. After joining IBM in 1978, he worked in the areas of reliability, characterization, failure analysis, power supply and analog circuit design, packaging and signal integrity at Sun Microsystems since 1996. His current area of concentration is design of power distribution systems and reduction of simultaneous switch noise.

Abstract

Low impedance power distribution systems (PDS) must be designed by CAD tools to insure that a low and flat target impedance (i.e. 1 mOhm) is met over a wide frequency range. Accurate models for Multilayer Ceramic (MLC) capacitors are required for simulation. Traditional resistance, inductance and capacitance (RLC) models do not exhibit the frequency dependent effects that are observed when the capacitors are mounted on a low inductance PCB or test fixture. A transmission line model for the capacitors gives more accurate simulation results. Model parameters are extracted from S21 measurements of the capacitor mounted on a low inductance fixture.

Introduction

Today's power distribution systems for computer applications are often required to meet a 1 mOhm target impedance. This is driven by the need to supply 100 watts or more at about 1V to micro processors, memory and communication chip sets. CAD systems are used to design low target impedance PDSs in order to insure that a flat impedance is met over a wide frequency range [1]. Accurate analysis of the PDS requires accurate simulation models for the major PDS components. The traditional series RLC model is often used to simulate MLC capacitors but it does not exhibit the frequency dependent effects that are observed with hardware measurements. A more sophisticated simulation model is required [2, 3, 4, 5]. MLC capacitors used for decoupling or bypass in applications in computer systems are usually mounted on low inductance pads connected to power planes that provide a low impedance environment. Measurement techniques that produce accurate data for extraction of capacitor model parameters are needed.

Traditional model inaccuracies

The impedance vs frequency of a measured 1uF X5R 0603 size capacitor is shown in Figure 1. Also shown is a simulated series RLC model for the capacitor with parameters chosen for the best fit match. At frequencies below series resonance, capacitance value (*Cap*) is the dominant parameter. The impedance minimum at series resonance is determined by the equivalent series resistance (*ESR*) value. The frequency of the minimum is determined by the inductance and capacitance according to the formula

$$f_0 = \frac{1}{2\pi\sqrt{ESL \cdot Cap}} \tag{1}$$

where *ESL* is the equivalent series inductance. But after choosing *Cap, ESR* and *ESL* for the best match at low frequency and at series resonance, there is a poor match at higher frequency. This is because *ESL* and *ESR* at frequencies above series resonance are a function of frequency. The frequency dependent

effect is observed when the capacitor is mounted in a low inductance fixture such that the internal inductance of the capacitor is not dominated by the inductance of the mount.

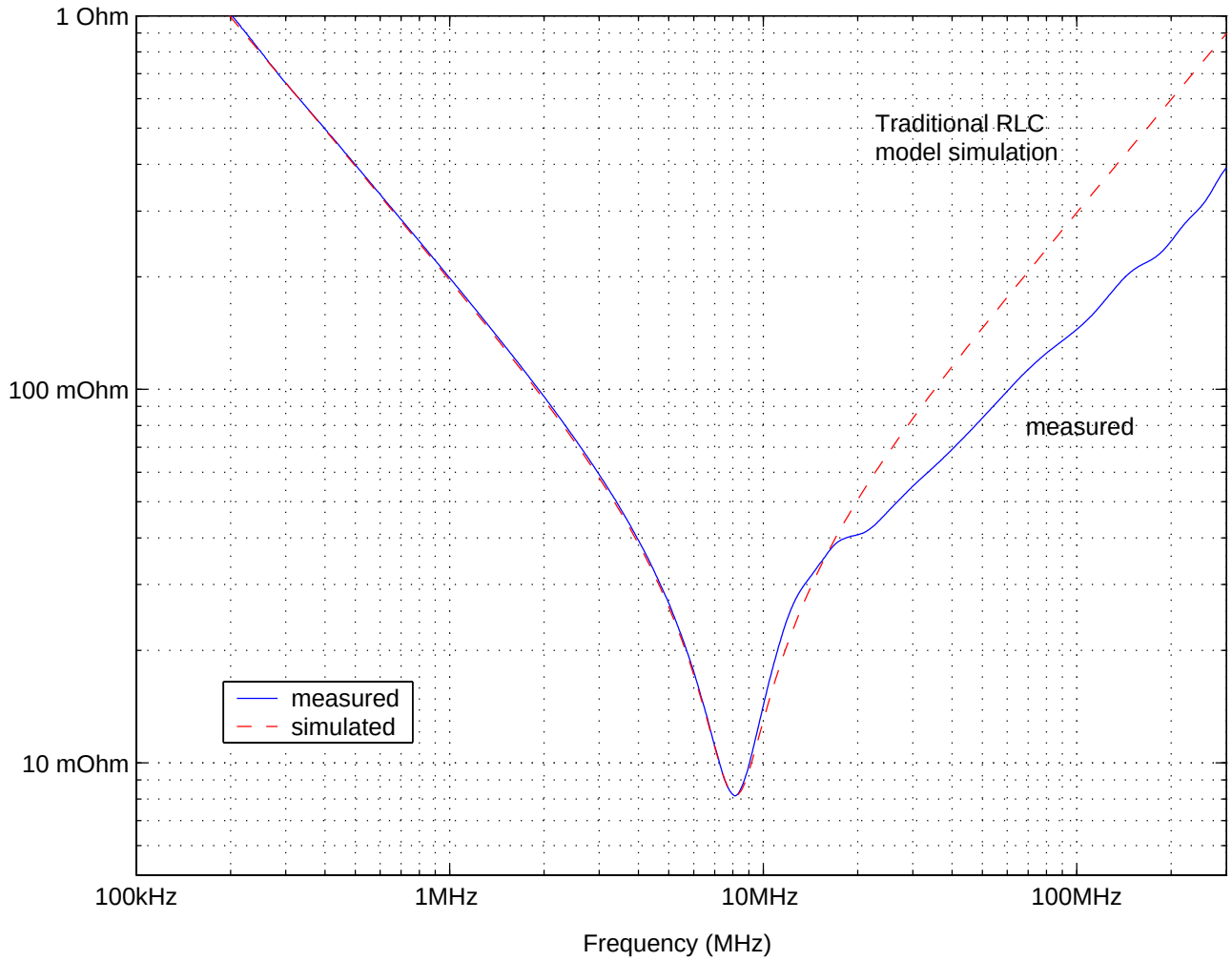

Figure 1: Measured and simulated results for 1 uF 0603 MLC capacitor. A series RLC model is simulated with R=8.2 mOhms, L=746 pH and C=801 nF. The traditional model gives poor matching above series resonance.

The low inductance pads on low impedance power planes in computer PDS applications provide such an environment. From a computer product perspective, a low inductance mount is highly desirable because it extends the effective range of the capacitor to higher frequency and fewer capacitors are required to accomplish the same decoupling performance. It is important to measure and model capacitors in an environment similar to their use conditions in order to gather model parameters that will be used for PDS simulation. A sufficiently accurate model will be able to capture the frequency dependent nature of *ESR* and *ESL* in a way that the simple series RLC model cannot.

Capacitor construction

The construction of an MLC capacitor, which is the basis for a more accurate model is schematically shown in Figure 2, together with the top power plane layers of a printed circuit board (PCB). The diagram is almost to scale in that the thickness between the PCB power planes and the distance between the top power plane and the capacitor is much less than the height of the capacitor. These PCB design features minimize the mounting inductance and are important for extending the frequency range where the capacitor is effective for decoupling applications. There is often a ceramic filler plate or coating [5]

in the bottom of the capacitor that is used to make the height of consistent with capacitors of the same body size but different capacitance values. The filler plate may be a large contributor to the intrinsic inductance of the capacitor.

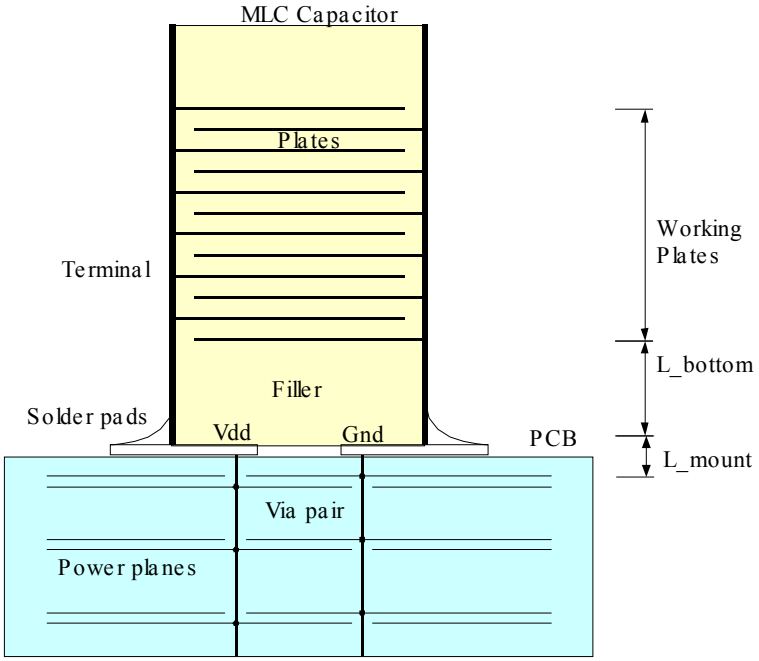

Figure 2: Construction of MLC capacitor mounted on PCB fixture. Inductance is associated with the working plates, the filler plate and the mount.

Further up and away from the PCB power planes is the working portion of the capacitor where many conductive and dielectric plates are stacked up for the purpose of charge storage. The number and thickness of the ceramic plates and the effective dielectric constant determines capacitance value. The number, thickness and conductivity of the conductive layers are the dominant factors that determine the *ESR* of the capacitor. The capacitance and *ESR* are primarily determined within the working plate region of the capacitor.

Inductance however is a function of the path or loop that the current takes as it makes it's way from the PCB power plane to ground plane. Inductance is associated with the magnetic field which is concentrated inside the loop where current flows. It is increased by increasing the loop dimensions and decreased by minimizing the area of the loop. Important dimensions in this loop include the horizontal distance between PCB vias and mounting pads and the length of the capacitor between terminals. The important vertical dimensions include the distance between PCB power planes, via height to the surface of the PCB, solder pads and terminal geometries, the thickness of the capacitor filler plate, and the height of the working plates within the capacitor. Capacitor values near the maximum capacitance for a given body size tend to be completely full of working plates whereas capacitors of lesser value may have a larger filler plate and have their working plates concentrated near the center of the body. Lesser valued capacitors may also have thicker dielectric plates of the same dielectric constant material.

The ESL of the capacitor is therefore determined not only by the dimensions of the working plates but also by the dimensions of the filler plate, mounting structures and PCB vias and power planes. The inductance discussion is complicated by the concepts of self inductance, partial inductance, mutual inductance and interactions of magnetic fields throughout the entire PCB and capacitor structure. The

ESL as defined in equation (1) above is the equivalent series inductance that is a property of the entire loop of the current path. The entire loop must be considered in any PDS simulation. Measurement of capacitor parameters to be used in simulation requires the inductance of the fixture to be backed out so that the parameters are not highly influenced by the inductance of the fixture. The inductance of the PCB mounting structure must be quantified and added back into simulations of the PDS in order to achieve accurate results.

Capacitor model

A transmission line circuit model has been proposed that mimics the construction of MLC capacitors and mounting structures as discussed in the previous section. The topology of the model is shown in Figure 3. The capacitance of the working plates is represented by capacitors that are effectively in parallel at low frequency (C_p). The *ESR* is mostly in the conductive plates and is represented by the resistors (R_p) which are also effectively in parallel at low frequency. Because of the many thin ceramic dielectrics and relatively wide dimensions of the conductive plates, the inductance associated with the horizontal plates is very small.

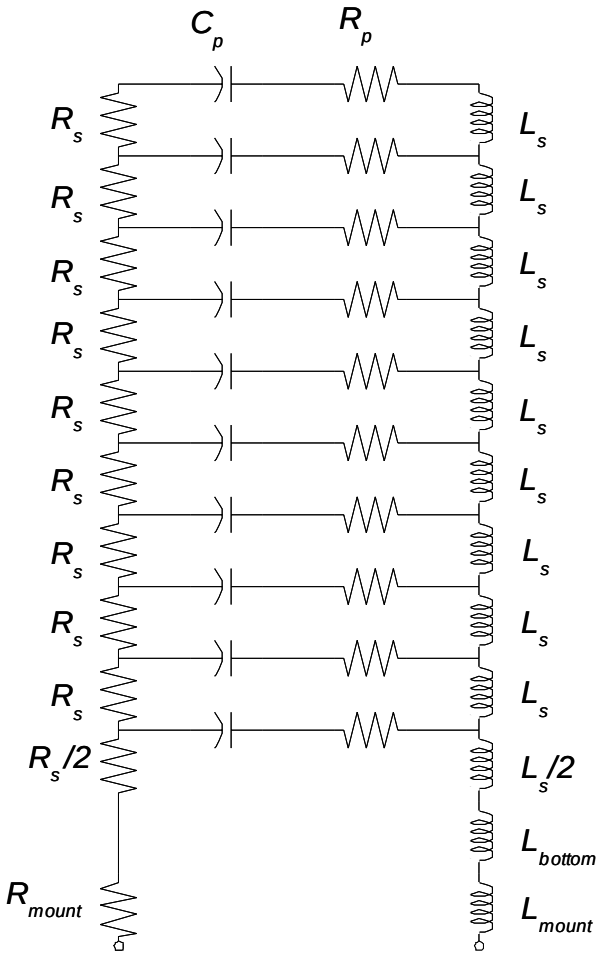

Figure 3: Transmission line circuit model for MLC capacitor.

The dominant inductance of the capacitor is associated with the vertical dimensions and mount. L_{bottom} is the inductance assigned to the portion of the loop near the filler plate. The loop area is further increased as current proceeds up the terminals past the working plates of the capacitor. These vertical inductances are in series and are designated L_s. The comparable series resistance is designated R_s. The frequency dependent nature of the capacitor can be envisioned by considering the relationship between the vertical and horizontal components of this model. At low frequency below series resonance, the relatively high reactance of the capacitance $1/(j\omega C)$ dominates over the reactance of the series inductance $j\omega L$.

At high frequency (above series resonance) the impedance roles of the inductance and capacitance reverse. The relatively high reactance of the L_s inductors dominates and impedes current from reaching the capacitance that is higher up the ladder. The effective inductance of the capacitor is diminished. At high frequency there are effectively fewer R_p resistors in parallel so the *ESR* of the capacitor increases above series resonance. This is a qualitative explanation for frequency dependent nature of capacitors on low inductance mounts. This phenomenon can only be observed when the fixture plus filler plate inductance (L_{mount} + L_{bottom}) is less or much less than the intrinsic inductance of the capacitor which is associated with the working plates (sum of L_s).

At series resonance, the vertical inductors and horizontal capacitors behave like a ¼ wavelength lossy transmission line with the high impedance open circuit at the end appearing to be a low impedance at the PCB pads. This property enables the calculation of the circuit parameters shown in Figure 3 [6].

Model to hardware correlation

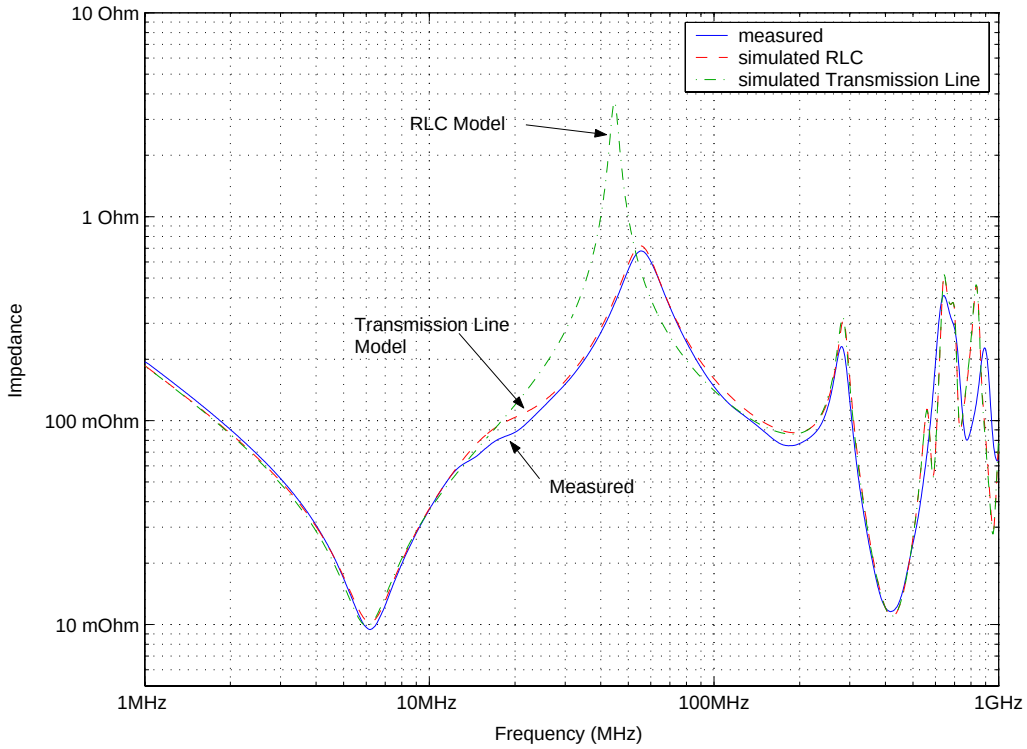

Figure 4: 1 uF capacitor mounted on PCB. Measured impedance and simulated results of the RLC and transmission line models are shown.

Figure 4 shows the measured impedance vs frequency for the 1 uF capacitor of Figure 1 mounted on PCB power planes with a low inductance mount. Also shown in the figure is the simulated results of the series RLC capacitor model and the transmission line capacitor model. Both capacitor models correctly

predict the impedance minimum at about 6 MHz associated with series resonance but at higher frequency the two simulations diverge. The peak at about 60MHz is due to the inductance of the mounted capacitor in parallel resonance with the capacitance of the PCB power planes.

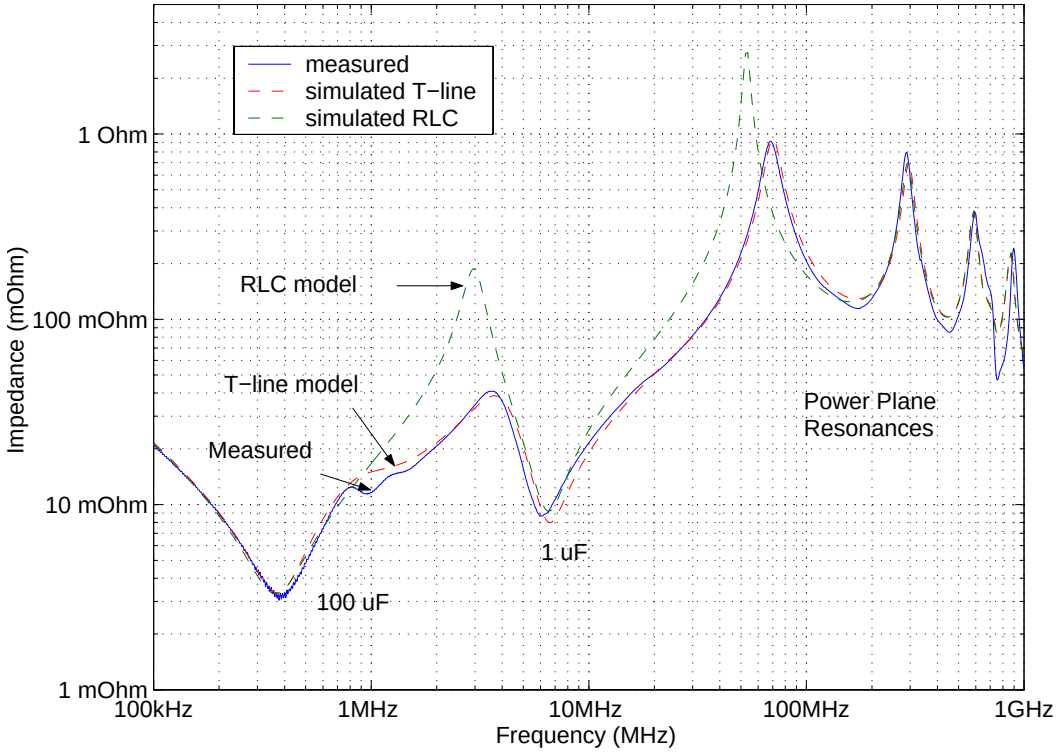

Figure 5: A 1uF and a 100 uF capacitor mounted on PCB. Measured and simulated results are shown.

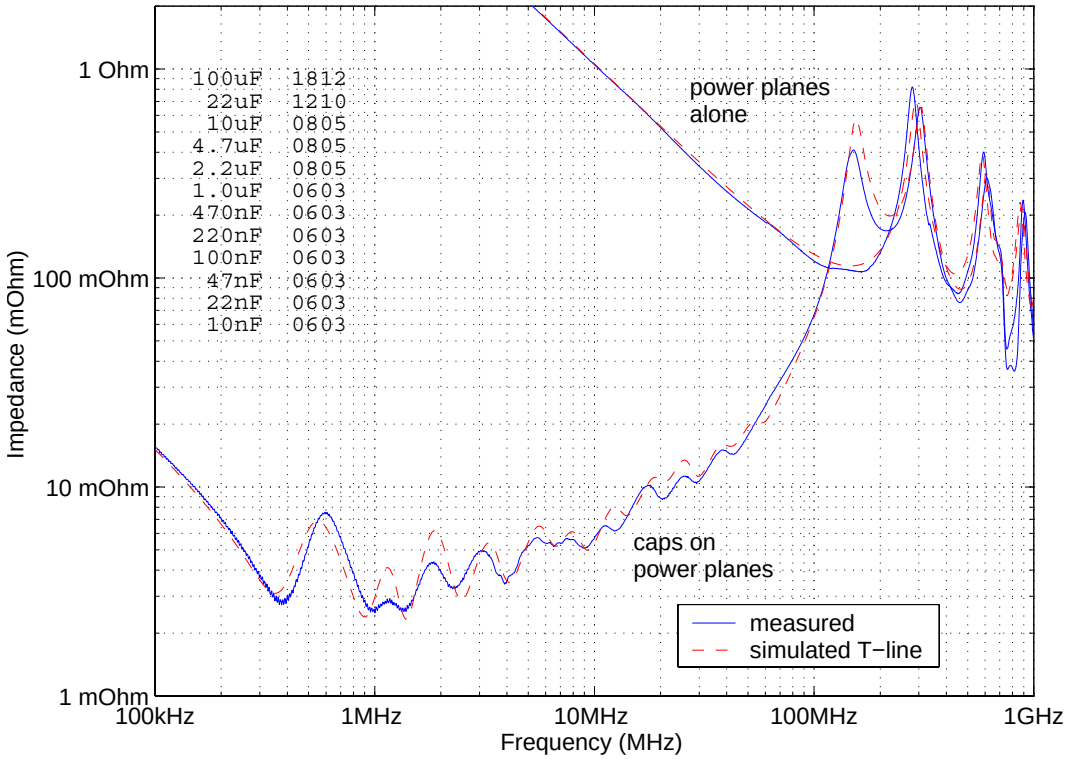

Figure 6: A dozen capacitor values mounted on PCB.

The transmission line capacitor model correctly predicts this resonant peak better than the traditional series RLC model because of the reduction of *ESL* and increase in *ESR* of the mounted capacitor at frequencies above series resonance. The power plane impedance, including cavity resonance effects, have been modeled according to the techniques described in [7].

Figure 5 compares the measurement of two capacitors mounted on power planes to simulation results for RLC and transmission line capacitor models. Once again, the resonant peaks are predicted better by the transmission line capacitor model because of the frequency dependent effects. Figure 6 shows the measured and simulated curves for a dozen capacitors mounted on power planes. As more capacitors of different values are added, it is possible to meet a target impedance less than 1 mOhm up to 50 Mhz or more. The most accurate results come from the more complex capacitor models. Careful capacitor measurements must be made to develop the parameters for such models.

Measurement of Transmission Line Parameters for Capacitor Model

As mentioned above, capacitors must be measured on very low inductance fixtures in order to observe the frequency dependent nature of *ESL* and *ESR*. The inductance of the fixture should ideally be much less than the intrinsic inductance of the capacitor. A VNA is used to measure the S21 parameters of the capacitors in a way similar to that described in [8]. Port 1 forces current from essentially a 50 Ohm current source into the capacitor. Port 2 measures the voltage at some point along the current path from port 1. The measured S21 data is easily converted to impedance. Three data points are required along the impedance vs frequency curve to determine the parameters of Figure 3.

1- a point one decade below series resonance determines the capacitance
2 - a point at the series resonance minimum determines *ESR* and *ESL*
3 - a point a decade above series resonance determines the high frequency L.

A fourth point is required to obtain the fixture inductance. This is the same measurement but the capacitor is replaced with a shorting bar that has dimensions similar to that of the capacitor DUT. Figure 7 shows the measurement of a 1 uF capacitor and shorting bar.

Fixture

The fixture used to measure the data in Figure 7 is shown in Figure 8, with and without a capacitor mounted. Figure 9 shows the full size of the fixture. This simple fixture is a pair of 50 Ohm coaxial cables with SMA connectors for the VNA. The DUT capacitor is soldered across the continuous 50 Ohm transmission line as shown in Figure 10. A “through” calibration is performed before attaching the DUT. The port 1 transmission line is the current source and the port 2 transmission line senses the voltage at the DUT. A shorting bar soldered into the DUT position gives S21 data for the shorted fixture that is consistent with 83pH inductance. Other fixtures have been tried but it is difficult to achieve inductances below 100pH. This fixture however may not be appropriate for a measurements in a production environment. Further work is required to develop fixtures that are sufficiently low in inductance to exhibit the frequency dependent nature of capacitors and also be consistent with the manufacturing environment. Details concerning the extraction of capacitor parameters from the 3 measured data points on the capacitor impedance profile together with the fixture inductance are given in [7]

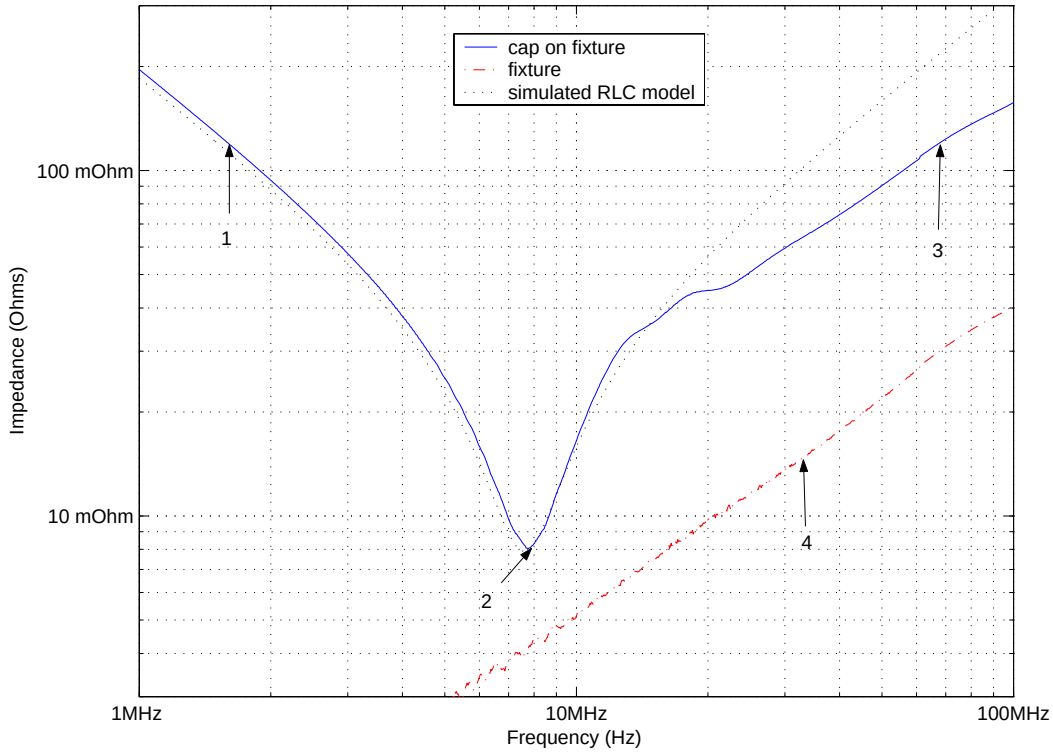

Figure 7: Measurement results for 1 uF capacitor and shorted fixture. Four data points are required to determine the parameters for Figure 3.

Figure 8: Low inductance measurement fixtures without (top) and with (bottom) a capacitor mounted as the DUT.

Figure 9: Low inductance wire fixture used to measure MLC capacitors.

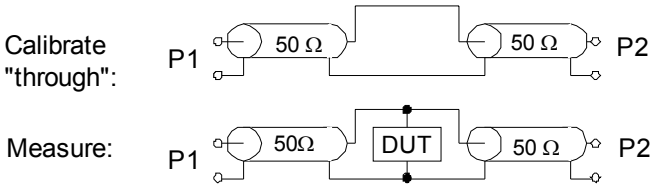

Figure 10: Schematic diagram of the calibration and measurement of the device under test (DUT, capacitor).

Conclusion

A transmission line model which is more accurate than the traditional RLC model has been developed for MLC capacitors. Simulation results correlates well with hardware measurements of multiple capacitors mounted on low inductance PCBs. Model parameters are gathered from S21 measurements of capacitors mounted on low inductance fixtures. The fixture inductance must be known so it can be backed out of the capacitor measurements. Further work is required to develop low inductance fixtures suitable for a manufacturing test environment.

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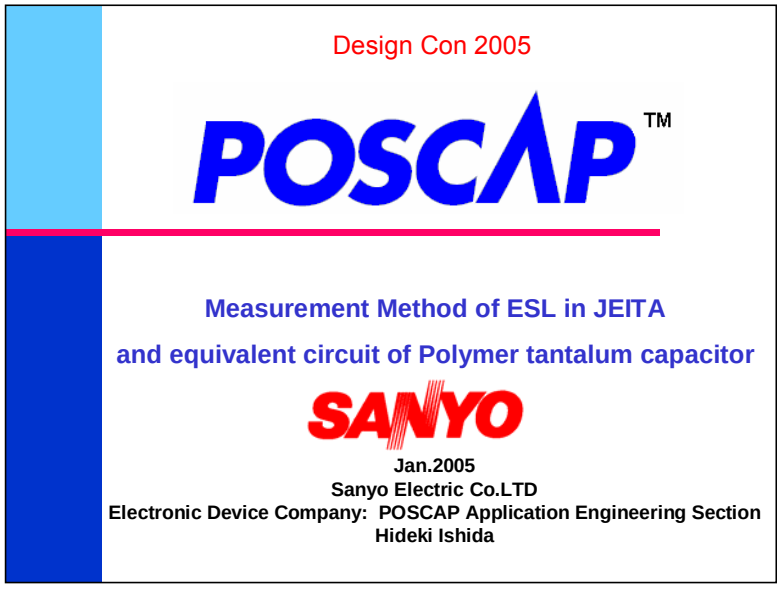
Part IV. Measurement Method of ESL in JEITA and Equivalent Circuit of Polymer Tantalum Capacitors

Hideki Ishida, SANYO Electric Co., Ltd.

Hideki Ishida started to work for SANYO in 1985 and he joined development team of polymer tantalum capacitors named "POSCAP" in 1998. Currently, he is an application engineering manager of POSCAP. Hideki is also a leader of the working group of the measurement method of ESR and ESL in JEITA.

Abstract

This presentation is about consideration of accurate and stable measurement method of capacitors' ESL. It is the trend on recent design of power supply for CPU to combine various types of capacitors. One of the important things from capacitor manufactures' stand point to support well-balanced power supply design which prevents from voltage drop at load change and ringing, is to provide accurate ESL value and help designers to come up with the most appropriate combination of capacitors' impedance. Currently standardized measurement method of capacitors' ESL hasn't been established yet and they still can see the difference by each manufacture. In an activity of JEITA, we got good progress on the method and the accomplishment will be finally reported in March 2005.



Agenda

SANYO Electric Co. Electronic Device Company

Topic 1: Measurement Method of ESL in JEITA

(1) Organization of JEITA

(2) History and Road Map of Standardization

(3) Measurement Method Details

(4) Our Progress

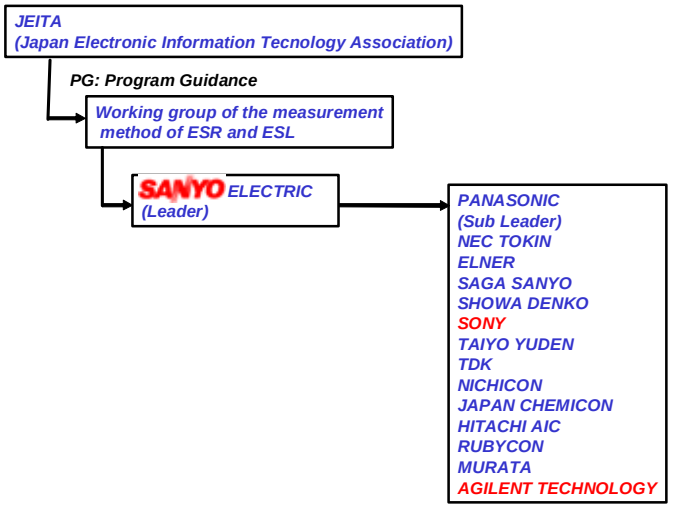
Topic 2: equivalent circuit of Polymer tantalum capacitor

(1) Equivalent circuit of POSCAP

Measurement Method of ESL in JEITA

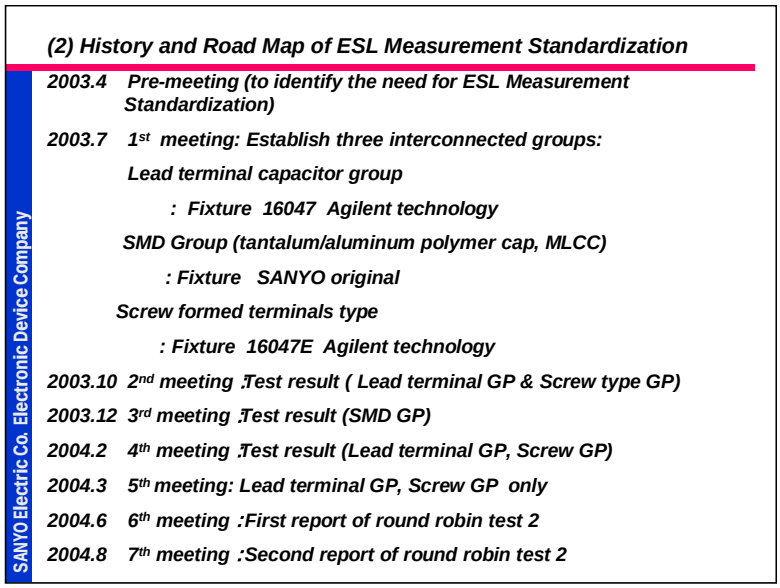
(1) Organization of JEITA

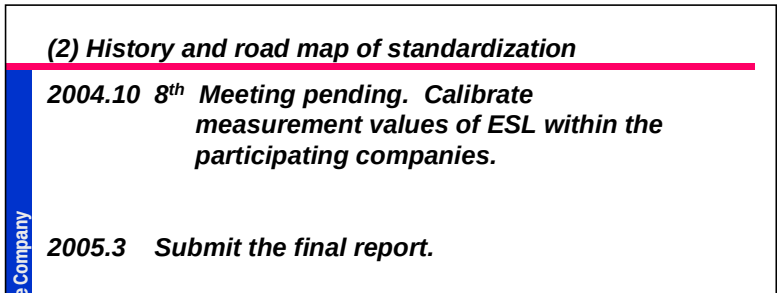
SANYO Electric Co. Electronic Device Company



JEITA is the IEC partner association/ that creates industrial standards in Japan.

This PG or “task group”/ has been established as the common research topic/ of the entire passive component industry. The group’s goal is to be adopted by IEC, and become the world’s standard.

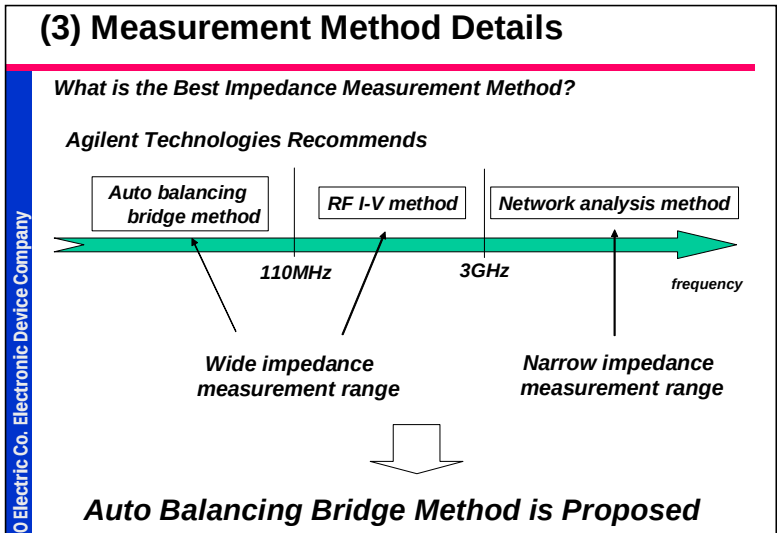




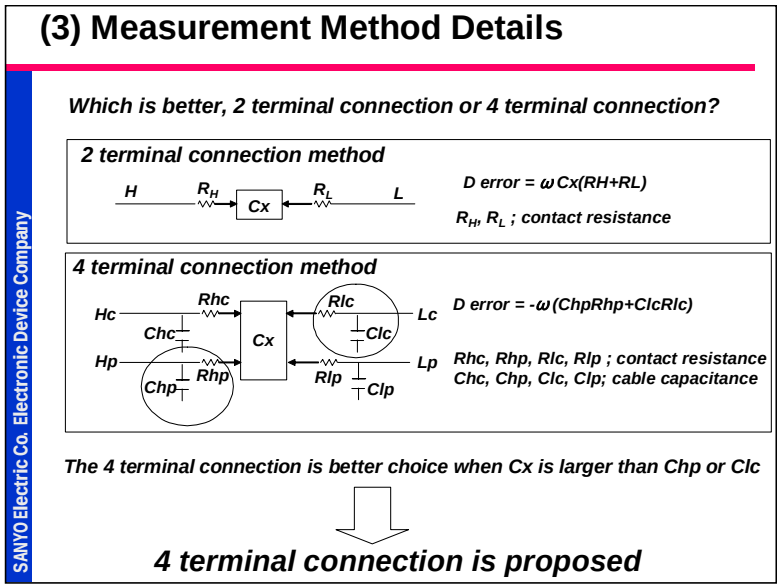
So far, we have held 7 meetings, for measurement standardization of ESR and ESL. We have divided into three groups by capacitor terminal shapes, and discussed the measurement method and fixture. Capacitors with capacitance values NOT in the "uF" range are excluded from this task group. We discussed the measurement method by putting an emphasis on the ability to duplicate measurement values. We used a round robin measurement method in which several companies tested the exact same capacitors with their own measurement equipment. Ideally, a STANDARD that has an absolute ESL value can be established, so all companies can calibrate their measurement machinery. Thus the ESL value claimed by each company will have a true, accurate value.

But in fact, measurement machine manufacturer has a measurement STANDARD for capacitance, and inductance values are calculated from the phase and impedance of this STANDARD. One method for determining ESL value was to use a measurement STANDARD and measurement fixture that is given by measurement machine maker. Unfortunately, the maker of this machine could not guarantee that the values were accurate. This issue was made worse by the fact that the machine manufacturer stated that the fixture does not exist.
We felt that Sanyo, as a leading capacitor manufacturer, needed to come up with a method to accurately measure ESL.
Sanyo designed the fixture for the SMD type. For the lead wire type, we modified the existing fixture, which is not designed for measuring ESL, by inserting a spacer in between the terminals of a capacitor. Screw formed type fixture also needs to be developed from scratch. Concerning the SMD type and lead wire type fixture, we submitted the rough draft in October '04, and the final report will be in March, 2005. Regarding the screw formed terminal type fixture, we are also planning to submit a report, with the cooperation and leadership of the maker of the measurement machine.

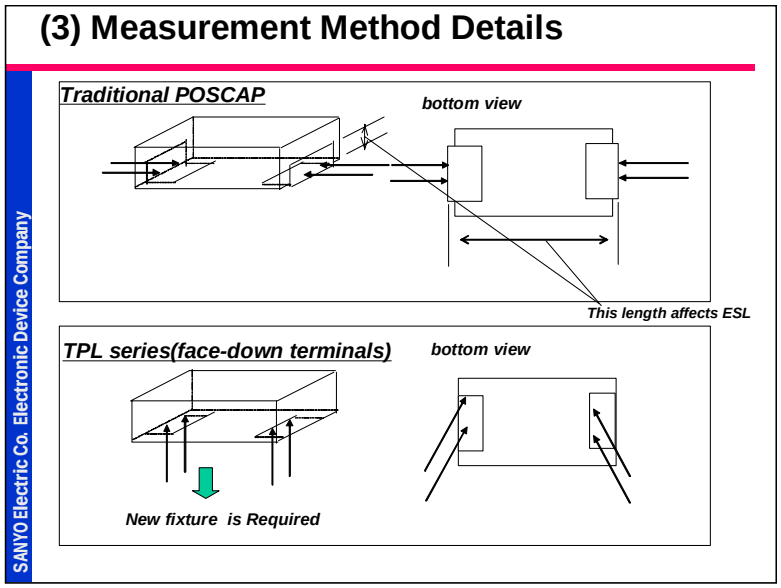
Measurement Method Details



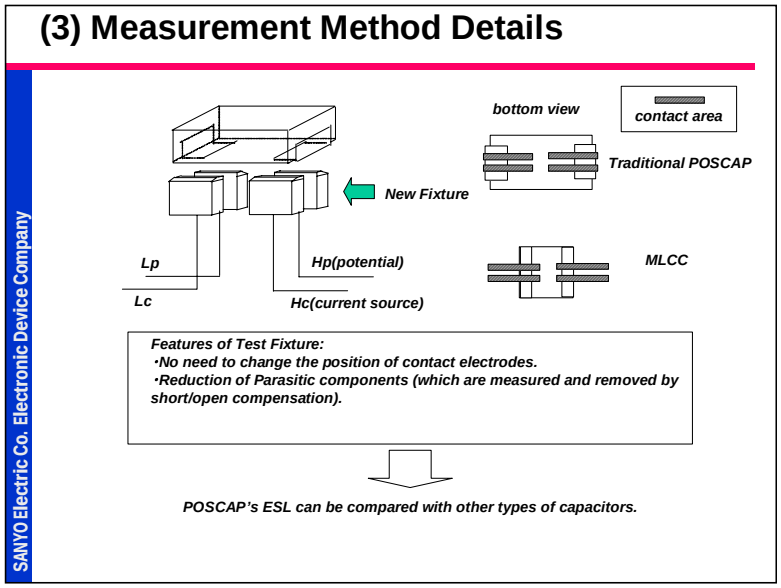
In the standardization of measurement, we have decided to follow the recommendation of Agilent Technologies, K.K., the maker of measurement machines. According to Agilent's recommendation stated in this slide, measurement accuracy differs by measurement frequency. Therefore, it is important to choose the right method based on the frequency. When measuring capacitors with capacitance in the "uF-range" we employed "auto balance bridge method" as the measurement method, and "Impedance Analyzer" as the measurement machine, because the resonance frequency of the capacitor that we are measuring is in the range of 20kHz to a few mHz. End users sometimes have to use Network Analyzers when measuring the entire circuitry. For small capacitance MLCCs, used with GHz solutions, network analyzers are the only measurement method as impedance analyzers cannot detect such High resonant frequency capacitors. Furthermore, Agilent stated that Network Analyzers can destroy the component itself, and due to the large impedance of the measuring board compared to the capacitor, it is too inaccurate to measure nH-range ESL.



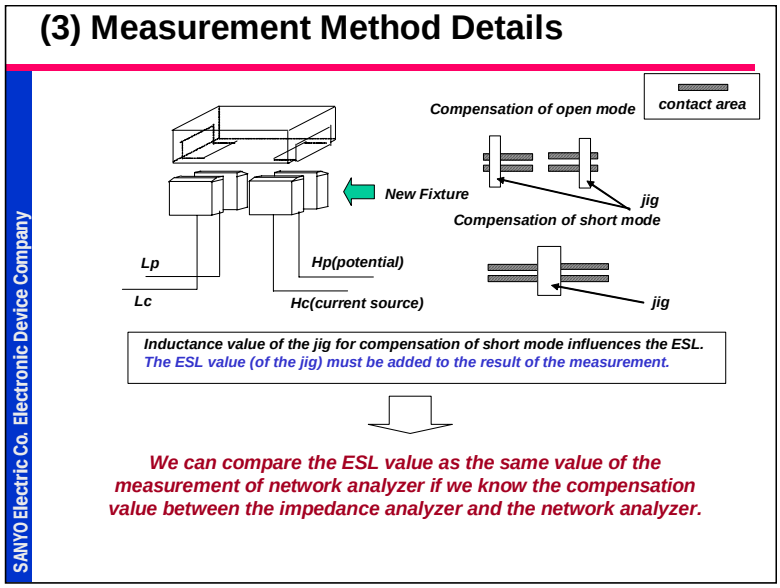
Two kinds of measurement methods for measurement fixtures are recommended by Agilent. In order to measure ESR accurately, the contact resistance between the fixture and the capacitor must be minimized. Since the 4 terminal method is better in reducing resistance, we employed the 4 terminal connection method.



This slide shows the problem when measuring conventional SMD type capacitors. The measured value of ESL differs from the measuring points. In order to obtain a consistent value, it is important to fix the measuring point. In the actual usage of SMD devices, contact is made at the bottom. Accordingly, Sanyo came up with the fixture that has 4 terminals, and at the same time makes contact from the bottom side. This fixture has been provided to JEITA for the use of all participating members. This fixture is anticipated to become the standard fixture by JEITA.



One of the advantages of this fixture is the capacitor that has a different contact shape, such as large capacitance MLCCs can also be measured in the same condition as conventional SMD capacitors. EIA proposed measuring MLCCs with a network analyzer. However, we believe MLCCs in the "uF" range can be measured with an impedance analyzer by taking the correlation between the measured values from both methods.



When measuring the ESL value with an "Impedance Analyzer", in order to initialize the measurement conditions, "open and short mode compensation" must be carried out each time. The problem with this operation is the ESL value of the jig for the short mode. ESL is subtracted from the measured value during the short mode compensation. The value of this subtracted ESL must be as small as possible and the absolute ESL value of the jig of short mode /needs to be added to the measured value./ The length between the measurement fixtures / is determined to be exactly 1 mm. Therefore, /a modification of the fixture becomes necessary / when there is a need to measure a capacitor with the size of less than 2mm/ in outer size.

Our Progress

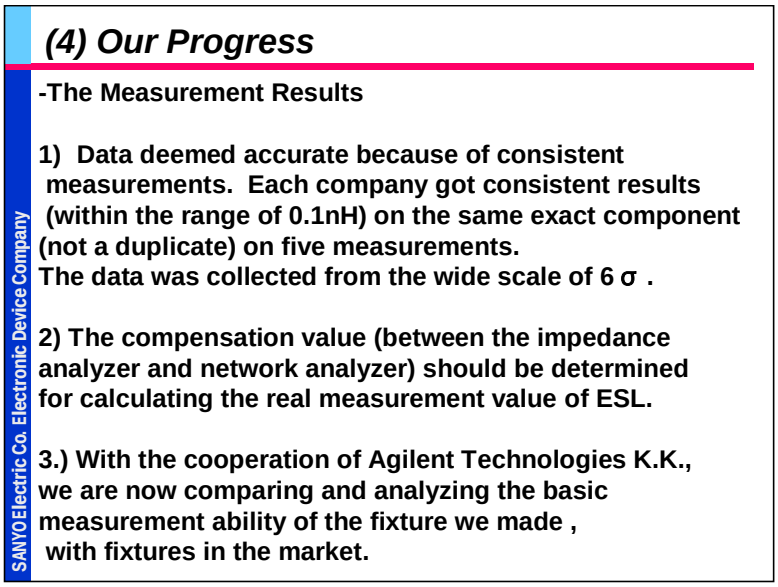
Measurement SAMPLE : SANYO (No.1 ~ No.5) 2.5V220uF (7.3x4.3x1.8)

NAME	SANYO					PANASONIC					NEC TOKIN					SHOWA DENKO				
No.	1	2	3	4	5	1	2	3	4	5	1	2	3	4	5	1	2	3	4	5
1st	1.86	1.85	1.88	1.82	1.90	1.85	1.81	1.86	1.80	1.89	1.81	1.80	1.83	1.78	1.86	1.85	1.83	1.87	1.81	1.90
2nd	1.86	1.84	1.88	1.83	1.90	1.87	1.84	1.88	1.82	1.91	1.82	1.80	1.83	1.78	1.86	1.86	1.83	1.87	1.81	1.90
3rd	1.85	1.84	1.88	1.82	1.89	1.86	1.83	1.88	1.80	1.90	1.79	1.77	1.81	1.76	1.83					
4th	1.84	1.83	1.87	1.79	1.87	1.86	1.84	1.89	1.81	1.91	1.82	1.80	1.84	1.78	1.86					
5th	1.85	1.85	1.88	1.82	1.90	1.85	1.81	1.86	1.79	1.89	1.81	1.78	1.82	1.77	1.85					
Ave	1.85	1.84	1.88	1.82	1.89	1.86	1.83	1.87	1.80	1.90	1.81	1.79	1.83	1.77	1.85	1.86	1.83	1.87	1.81	1.90
σ	0.01	0.01	0.01	0.01	0.01	0.01	0.02	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.00	0.00	0.00	0.00

Measurement SAMPLE : SANYO (No.1 ~ No.5) 2.5V220uF (7.3x4.3x1.8)

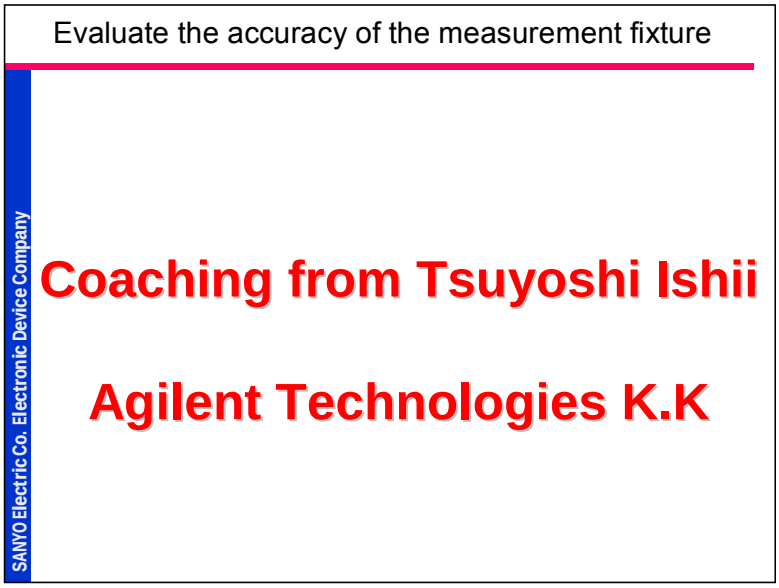
Name	TDK					TAIYO YUDEN				
No.	1	2	3	4	5	1	2	3	4	5
1st	1.86	1.84	1.86	1.82	1.89	1.86	1.84	1.86	1.81	1.90
2nd	1.86	1.84	1.87	1.81	1.90	1.87	1.84	1.86	1.82	1.89
3rd	1.86	1.85	1.86	1.81	1.90	1.85	1.84	1.86	1.81	1.89
4th	1.87	1.84	1.86	1.81	1.90	1.86	1.84	1.87	1.82	1.89
5th	1.86	1.84	1.87	1.81	1.90	1.85	1.84	1.87	1.82	1.90
Ave	1.86	1.84	1.86	1.81	1.90	1.86	1.84	1.86	1.82	1.89
σ	0.00	0.00	0.01	0.01	0.01	0.01	0.00	0.00	0.00	0.00

This is ONE example of the measurement results. The data was collected from the wide scale of 6σ. Each company got consistent results within the range of 0.1nH on five measurements. The data is deemed to be accurate enough because of these consistent measurements.

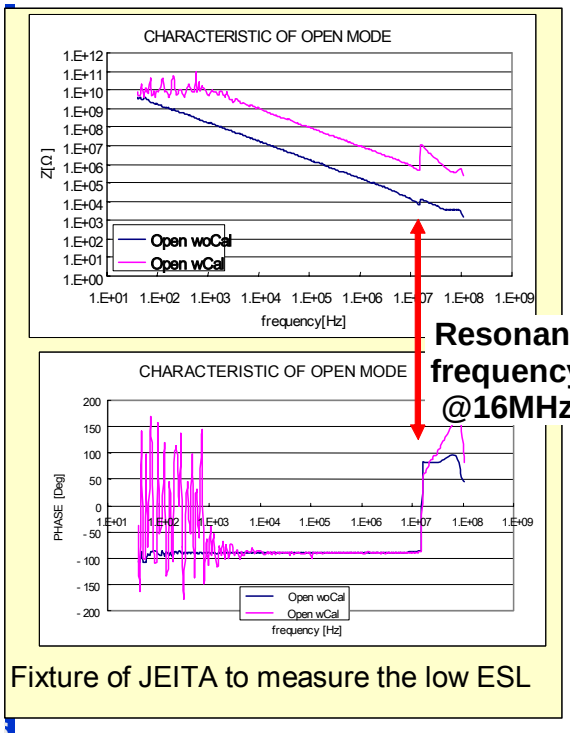


Data deemed accurate because of consistent measurements. Each company got consistent results (within the range of 0.1nH) on the same exact component (not a duplicate) on five measurements. The data was collected from the wide scale of 6 σ. The compensation value (between the impedance analyzer and network analyzer) should be determined for calculating the real measurement value of ESL. With the cooperation of Agilent Technologies K.K., we are now comparing and analyzing the basic measurement ability of the fixture we made, with fixtures in the market.

Evaluate the accuracy of the measurement fixture

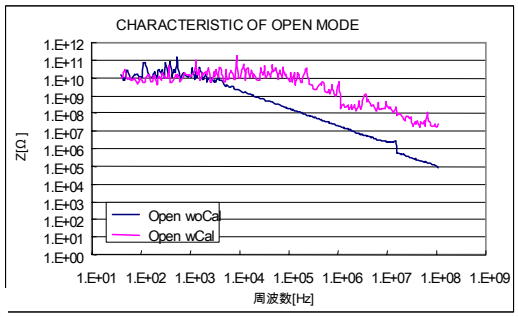


Frequency characteristics of coefficient of Open mode



Fixture of JEITA to measure the low ESL

Resonant frequency @16MHz

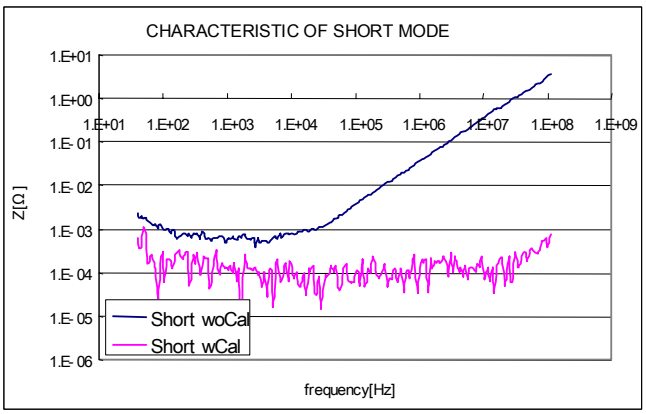


Previous fixture:16044A

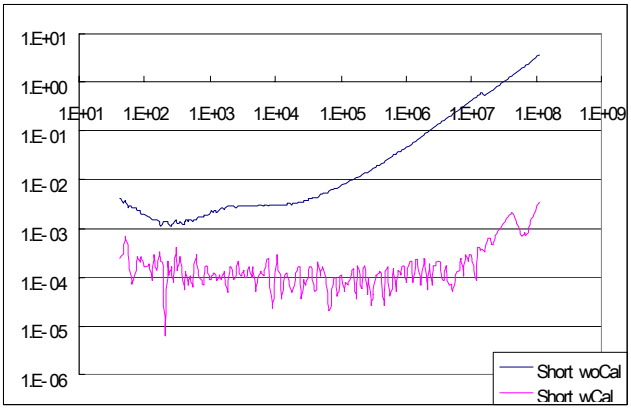
Because of the guard plate between High pole and Low pole, capacitance of the open mode coefficient decrease.

In the case of open mode compensation, infinitely large impedance value is needed ideally. In this test, test result of JEITA fixture is not good compared with previous fixture. But this value is not effective compared with the short mode compensation. Open woCAL: measurement result of open mode without calibration. Open wCAL : measurement result of Open mode with calibration.

Frequency characteristics of coefficient of short mode



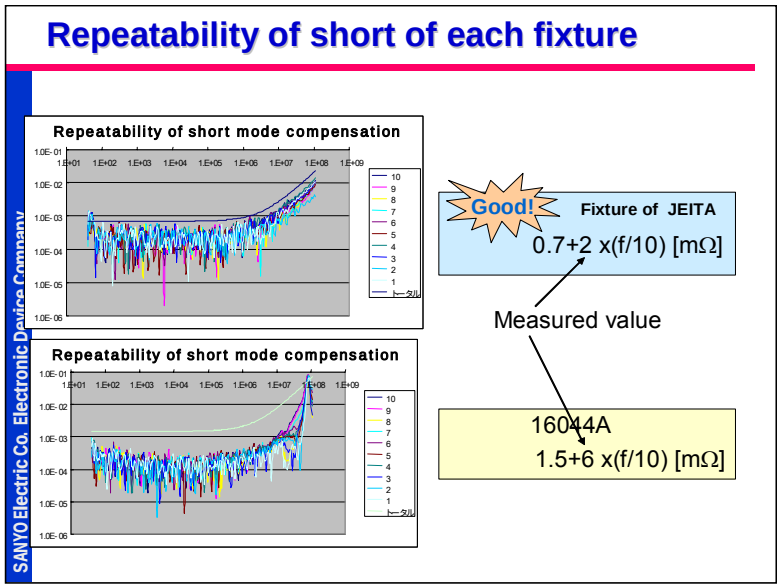
Fixture of JEITA to measure the low ESL



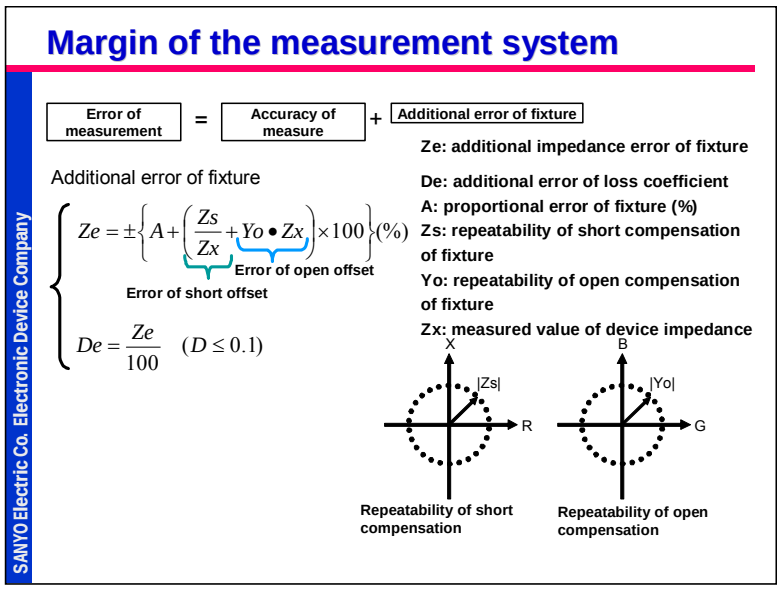
16044A

Measured value of each fixture is same (1 time).

Measured value after calibration of each fixture is almost same. But the issue of measuring the ESL value is the repeatability of fixture.

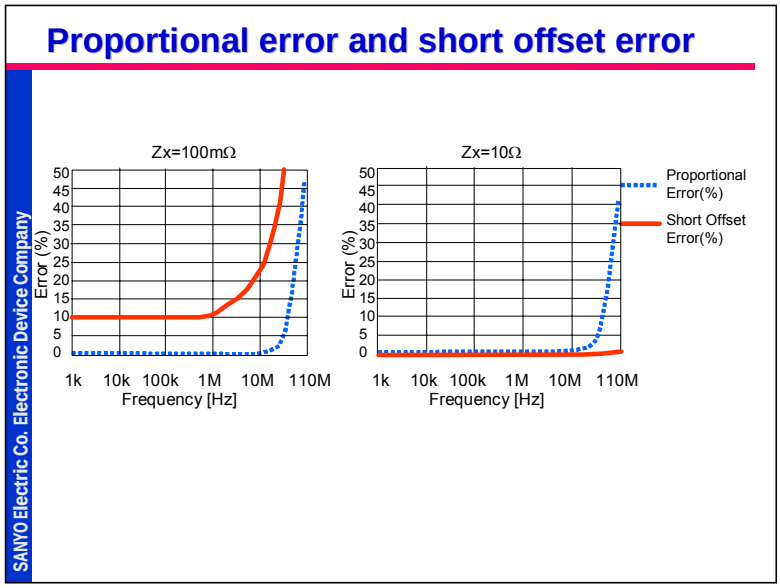


Measurement result of JEITA fixture is better than previous fixture. If the frequency of measurement point of ESL is 10MHz, JEITA fixture: 2.7mohm (0.04nH), previous fixture: 7.5mohm (0.12nH).

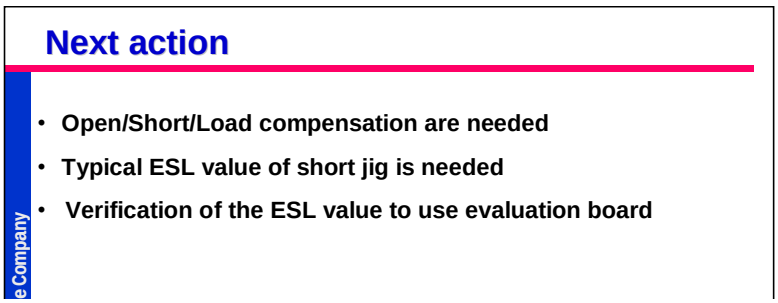


Measurement accuracy is sum of instrument's accuracy and test fixture's additional error The term, proportional error (A), was derived from the error factor, which causes the absolute impedance error to be proportional to the impedance being measured. Conceptually, it is dependent upon the stability of each element of the fixture's equivalent circuit model. The term, Zs/Zx ×100, is called short offset error. This term affects the absolute impedance error, by adding an offset. Short repeatability (Zs) is determined from the variations in multiple measurements of the test fixture in short condition. After performing short compensation, the measured values of the short condition will distribute around 0 in the complex impedance plane. The maximum value of the impedance vector is defined as short repeatability. The larger short repeatability is the more difficult it is to measure small impedance values. In essence, short repeatability is made up of a resistance and an inductance part, which become larger as the frequency becomes higher. The term, Yo•Zx ×100 is called open offset error. If the same analysis is carried out with admittance, then it can be concluded that this term also affects the absolute admittance error, by adding an offset.

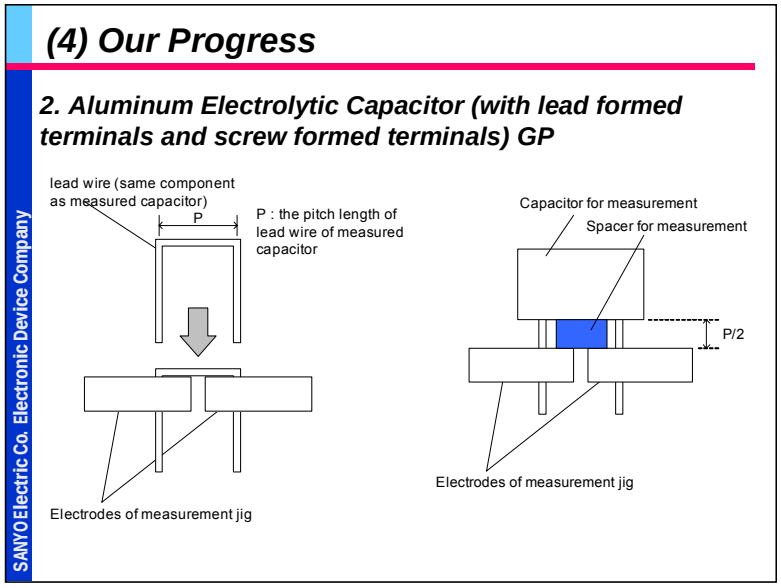
Open repeatability (Yo) is determined from the variations in multiple measurements of the test fixture in open condition. The maximum value of the admittance vector in the complex admittance plane is defined as open repeatability. The larger open repeatability is, the more difficult it is to measure large impedance values. Open repeatability is made up of a resistance and a capacitance part, which become larger as the frequency becomes higher.



In the figure above, the relationship between proportional error, short offset error and frequency are shown when measuring low impedance. Notice that when the measured impedance is less than 100 mΩ, short offset error influences the entirety of the test fixture's additional error. When the DUT's impedance is 100 mΩ and the test fixture's short repeatability is 10 mΩ, the short offset error will be 10%. Since the proportional error is minimal in low frequencies, the additional error will be 10% as well. For the additional error of test fixtures, up until now, it was common to just specify the proportional error (A). As shown in the 10Ω measurement case (same figure down below), if the measured impedance is large in comparison to the test fixture's short repeatability, then short offset error can be ignored completely. This is the reason why open and short offset error was not specified previously. Test fixtures that are only specified with proportional error in this accessory guide are due to this reason. On the contrary, for measured impedance from 1Ω to 10 kΩ proportional error (A) alone is sufficient to express the test fixture's additional error.



Lead formed terminal



This is the case of lead formed terminal group. This group has the special cancellation method of the ESL value of the jig. In this case, short mode compensation should be executed by using the same lead wire, that is used in the measured capacitor. It is shown in the picture on the left side of this slide. The pitch (p) is equal to the lead pitch of the measured capacitor. Notes: In this short mode compensation, the Inductance factor of lead wire, that has an equal length to the terminal pitch, is entirely subtracted. In order to offset the excessive inductance subtracted value, when measuring the capacitor, it needs to be elevated by a height of half the distance of P in the terminal pitch. During the actual capacitor measurement, by employing this elevated measurement method, we believe that we can arrive at Comparable values. The spacer that has the height of p 2 (p divided by 2) should be created to balance the length of the two lead wires, to ensure accurate measurement.

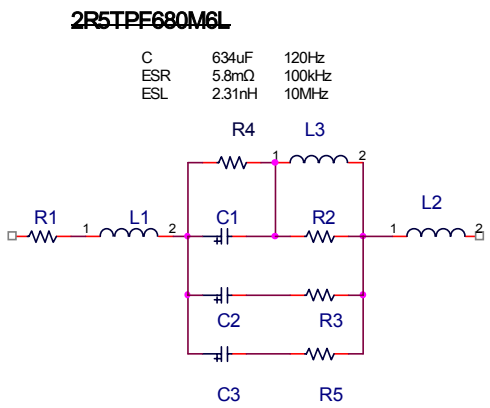
Table 1. Comparison of calculated and measured ESL from the output ripple of DC-DC Converter:

Size of Component (the pitch between terminals)	Calculated ESL	Measurement Result of Company A	Measurement Result of Company B
φ 6.3× 6L(2.5mm)	3.16nH	2.67nH	2.53nH
φ 8× 12L(3.5mm)	4.69nH	4.36nH	4.44nH

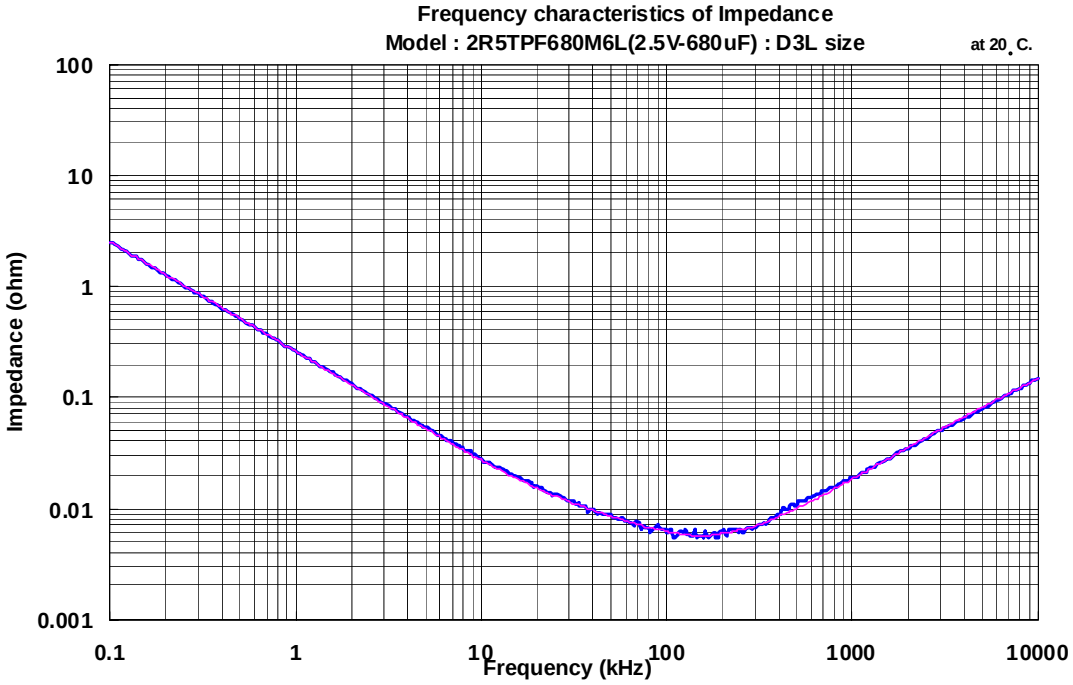
Measurement Condition : Buck Type, 7 ~ 15Vin, 5Vout, f=200 ~ 800kHz
Measurement Result : Average of n=3pcs.
Measurement Unit : nH at 10MHz
Measurement Equipment : Company A ; 4194A, Company B ; 4192A
Measurement Jig : 16047C

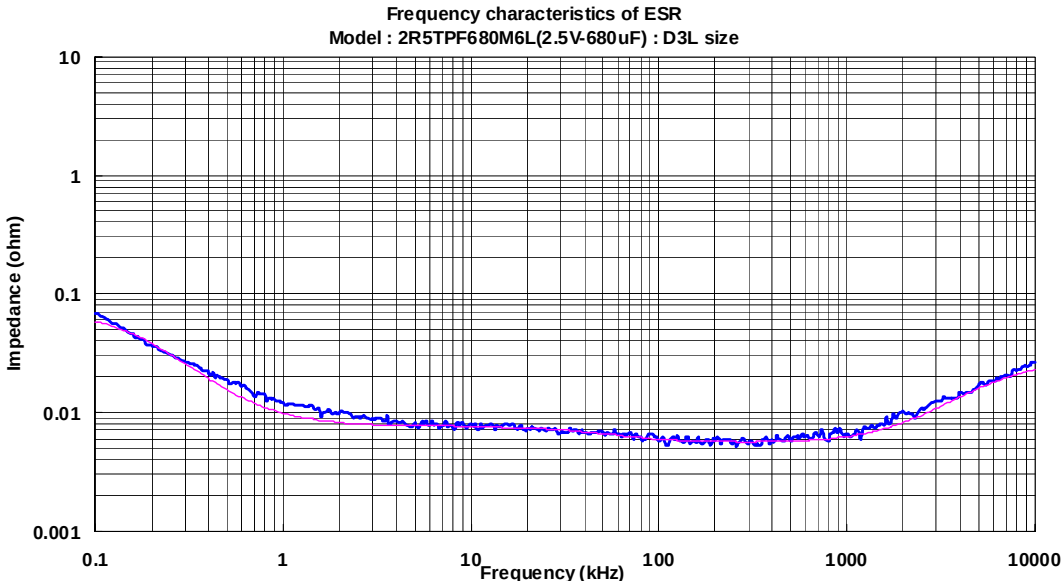
We prepare the back style dc/dc converter circuit board to measure and simulate the ESL value of each capacitor. The measurement value and simulated value is not so different. We believe that the measured value by impedance analyzers is reliable enough to use as a reference for the circuit constant.

Equivalent circuit of Polymer tantalum capacitor, correlation



R1	5.6mΩ
R2	200mΩ
R3	30Ω
R4	14.7 kΩ
R5	25mΩ
L1	1.35 nH
L2	0.8nH
L3	0.65nH
C1	438uF
C2	30uF
C3	175uF





Part V. Measurement ESL/ESR of the Passive Components and Compensation of the Fixtures

Masayuki Shimizu, Taiyo Yuden Co., LTD
shimizumasa@jty.yuden.co.jp, 81-027-360-8328
Masayuki Shimizu received Electrical Engineering B.E. degree from the Electrical and Electronics engineering department Saitama University, he was entered TAIYO YUDEN since 1995,and he was engaged in EMC component simulation and evaluation technology. Most recently being occupied in as an engineer of capacitor products development and evaluation technologies on Taiyo Yuden Central R&D Laboratories.

Satoshi Kazama, Taiyo Yuden co., LTD
kazama@jty.yuden.co.jp, 81-027-360-8328
Satoshi Kazama received B.E. degree from Niigata University in 1986 and Ph.D. degrees from Tohoku University in 2002. He joined YAIYO YUDEN Company in 1986. He is a member of the IEEE of the U.S. and The IEICE of Japan. His research interests include electromagnetic compatibility and microwave components.

Toshio Hiraoka, Taiyo Yuden co., LTD
thiraoka@t-yuden.com,408-573-4150 ext.22
Toshio Hiraoka received Electrical Engineering B.E. degree from the Tokyo University of Science in 1997. He joined TAIYO YUDEN in 1997. Most of his research was regarding multilayer capacitor (MLCC) product manufacturing including ceramic materials development and electrical characteristic evaluation. In 2003, he transferred to TAIYO YUDEN San Jose office as a Field Application Engineer for passive components.

Abstract

Recently, various Low ESL/ESR capacitors have been developed to improve decoupling characteristics for a voltage regulator and voltage circuit, as being accompany the advance of a high-speed semi-conductors. The ESL of a MLCC (Multi Layer Ceramic Capacitor) level was 1nH in the past, but it was been improved below 100pH presently [1]. It is necessary to subtract residual component except the capacitor for measuring capacitor's ESL/ESR with accuracy [2][3][4]. In this paper, we are reporting how much can it decrease as using short compensation method against an available fixtures or measuring printed circuit board.

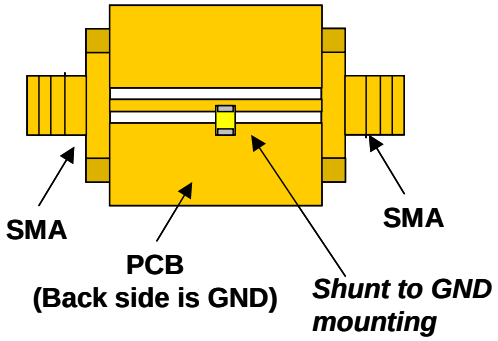
Introduction

It is becoming more important to improve decoupling characteristics for AC and DC current in the power supply circuit, since the IC operation and the noise frequency of CPU and GPU is becoming higher. MLCCs are often used for the power supply of IC and IC packages, because it's suitable for downsizing. Basically, the characteristic of a capacitor is expressed by capacitance, equivalent series resistance (ESR), and equivalent series inductance (ESL). First, reviewing measurement method for generic 2 terminal MLCC. Then reporting about an examination of the fixture compensation for current low ESR/ESL capacitors.

Capacitor Measurement using S-parameter

Typical measurement using 2port PCB fixture

As one of the general methods [3] of measuring ESR/ESL of a capacitor, it can be calculated from S21 characteristic, which is getting from a DUT mounted PCB like Figure8. In this case, the characteristic impedance of the line is being designed to be 50 ohm. And S-parameter data of the DUT connected in parallel between signal and GND are converted into the impedance characteristics from a formula (Eq.1). (Refer to 2.6 in detail)



$$Z_{DUT} = \frac{S_{21}}{2(1 - S_{21})} Z_0 \qquad \text{------ (Eq.1)}$$

Figure1.General capacitor test PCB and Z transformation formula

But, that structure is not suitable for multi-terminal electrode components except for 2 terminal parts. And it's difficult to make an equivalent circuit that it shows large variations in measurement data since the PCB is soldered to SMA connectors. Therefore, in recent years, the measurement using the probe station and high frequency probe of Figure2 is in use.

Probe Station

Cascade Micro-tech Probe(GSG-500)

Figure2.Probe Station and the edge of the probe

2-port test fixture for the Feed-thru MLCC

One of the low ESL capacitors is a feed-thru capacitor. The outer structure will be as shown Figure3. The feed-thru capacitor has two outer signal electrodes and two outer GND electrodes. Figure4 will show the inner structure and current flow model. The DC current flow through the outer signal electrode and the inner signal pattern from IN to OUT, and AC current flow to the PCB GND divided equally between the two outer GND. So the ESL of the feed-thru capacitor is decreased by dividing the current. Then, it cannot be measured by a general PCB fixture such as Figure1 and so we made a measurement PCB for feed-thru capacitor like Figure5.This fixture was designed for using probe-system, which is based on a coplanar wave-guide with bottom GND. This PCB has 0.45mm line width and 0.102mm gap.

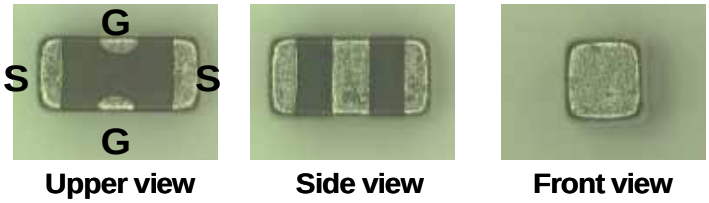


Figure3.Feed Thru Capacitor (0603 case size with 1uF,BJ)

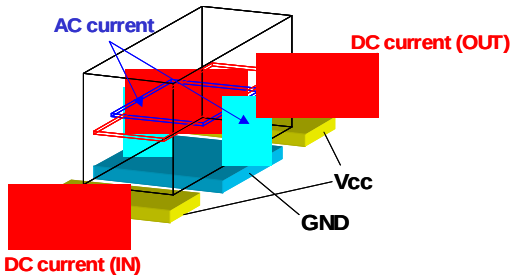


Figure4.Inner structure of the Feed Thru Capacitor

CPW PCB design
-Size: 10mm*30mm
-Material : BT resin(CCL-HL870)
-dielectric constant : 3.5
-dielectric loss : 0.003
-thickness : 0.4mm
-Surface treatment : Au flash
-Metal thickness : 15um

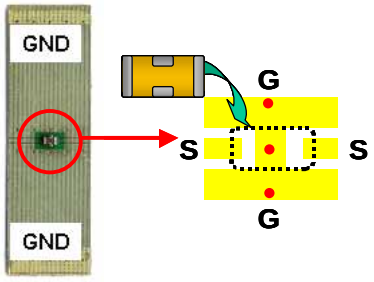


Figure5.CPW fixture with bottom GND for the Feed Thru Capacitor

The DUT S-parameter was measured with the two-port measurement method with a HP8753D (Option 1D5) VNA at room temperature. It was calibrated in full two port calibration by a Cascade impedance standard substrate (ISS) The measurement frequency range was set to 0.03MHz to 3GHz with 801 points and IF Bandwidth was set to 100Hz. The feed-thru capacitors were mounted on a CPW PCB with soldering, which was placed on a Cascade Micro-tech probe station. The connections to the DUT were made with 2 pieces 500um pitch GSG-probes.

This measurement compared to the case where it was mounted by making it rotate 90 degrees as shown on Figure6 for the study of the influence on ESL by mounting direction. The ESL was calculated from the each capacitance and SRF (self resonance frequency). Figure7 shows the measured impedance characteristics and the property.

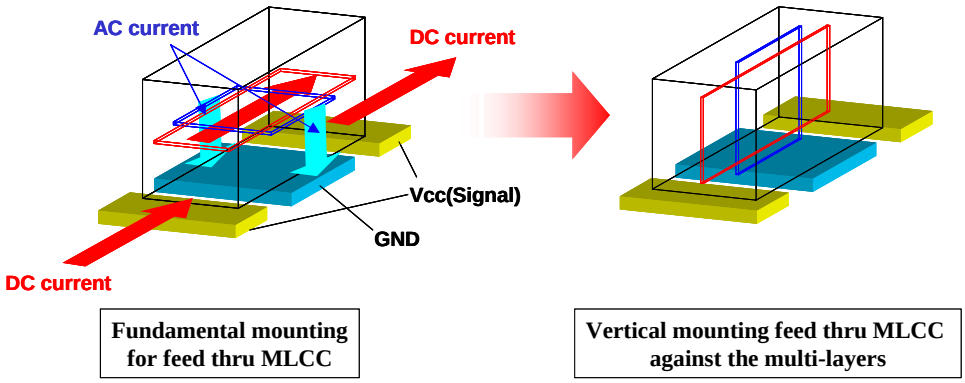
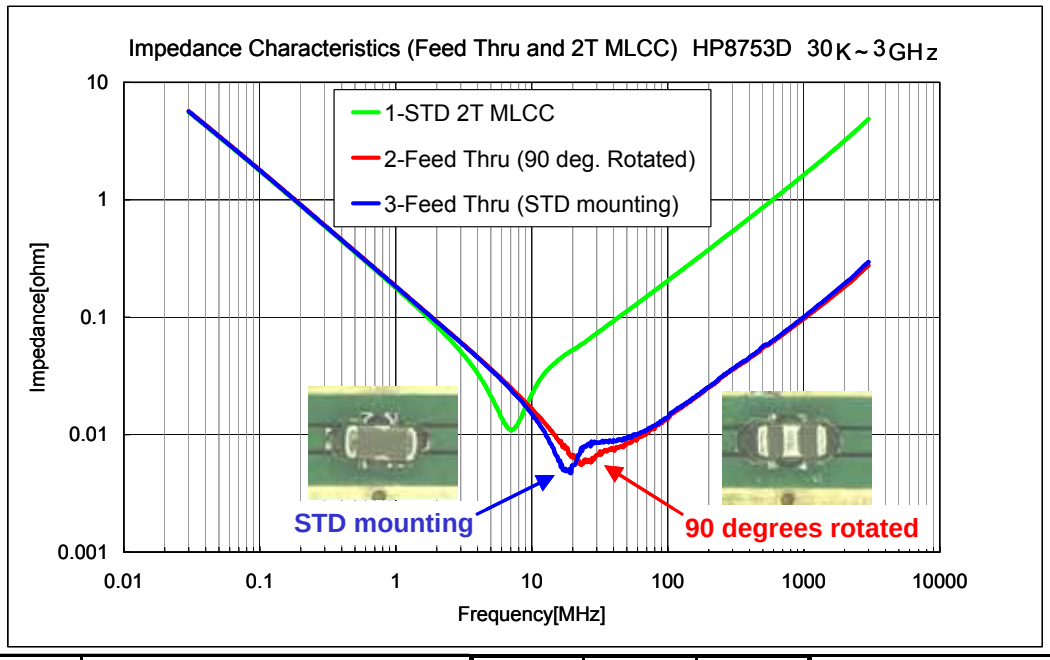


Figure6.90 degrees rotated mounting for the fixture



No.	DUT Condition	L[pH]	C[uF]	R[mohm]	remarks
1	Feed Thru MLCC sample1	79.80	0.856	4.78	
2	Feed Thru MLCC sample2	87.80	0.859	4.99	
3	Feed Thru MLCC sample1	54.90	0.857	6.13	90 degrees rotation
4	Feed Thru MLCC sample2	46.70	0.861	5.34	90 degrees rotation
5	STD 2-terminal MLCC(0603)	560.00	0.894	10.90	

Figure7.Impedance characteristics changing mounting direction

From these results, it turns out that ESL carried out about 33 pH changes on the average by changing only the mounting direction. This is involving about the internal structure of the component. MLCC has alternate stacked layers, which consist of a dielectric and conductive material. The current loop length between signal layers and ground layers will change in case that the stacked layers are horizontal or vertical for the PCB [6]. In case of Figure8-A, the loop length becomes longer and longer with the layer position. In case of Figure8-B, the loop length stays constant. Therefore the ESL was changed.
It is necessary to comprehend preliminarily the mounting direction against the PCB for measuring capacitor's ESL.

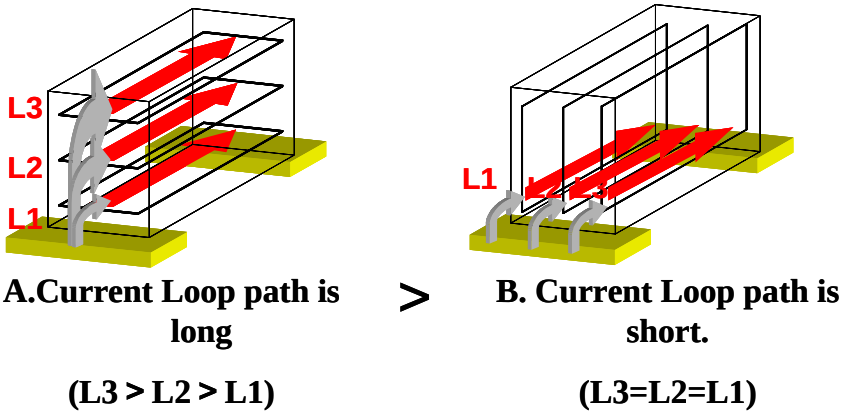


Figure8.Current loop length

2-port test fixture for the 8T MLCC

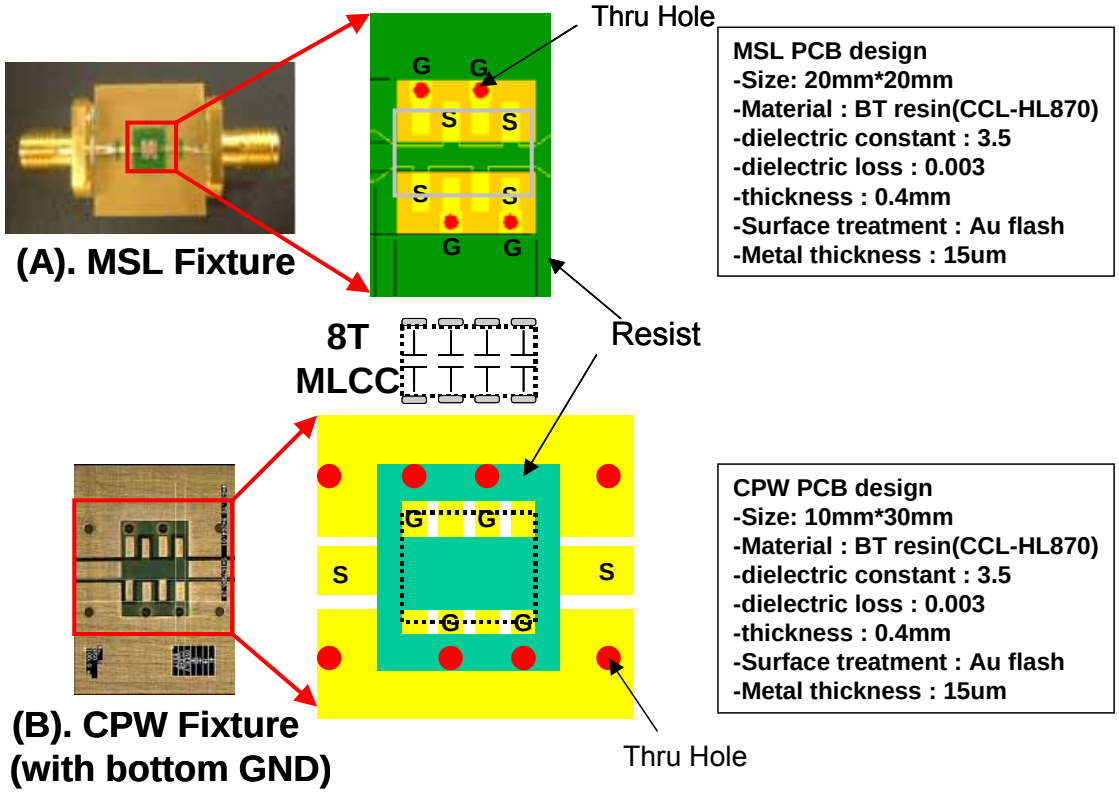


Figure9. Redesigned PCB for 8-terminal MLCC

Furthermore, in order to make the ESL decrease, more multi-terminal MLCC[1] has been developed such as Figure 9. To measure like this MLCC by using the generic method, we redesigned the measuring fixture PCB of Figure5 to Figure9 PCBs. Figure9-(A) shows a micro-strip-line PCB like EIA-Std [3] with SMA connectors for measuring 8 terminals MLCC, Figure9- (B) shows a co-planer PCB with bottom GND with probe-system. Both of two PCB is designed 50 ohm impedance characteristics.

Those two PCB have alternated signal and GND pad to mount the DUT to decrease the residual PCB and DUT inductance. But it's necessary to cancel a residual PCB inductance, that the thru-hole inductance stays in like a MSL fixture which has bottom GND. [5][7]

Structure simulation of the MSL Fixture

Before the measurement, the MSL fixture was simulated by Ansoft HFSS (High Frequency Structure Simulator) in order to seek the thru-hole inductance of the fixture connected between capacitor's GND and PCB's GND.Figure10 shows a structure of the simulation using a short-bar with a perfect conductor in exchange for using a capacitor. After getting 2 port S-parameter of the fixture by the simulation, the inductance was calculated to become equivalent to the S-parameter by the circuit simulator.

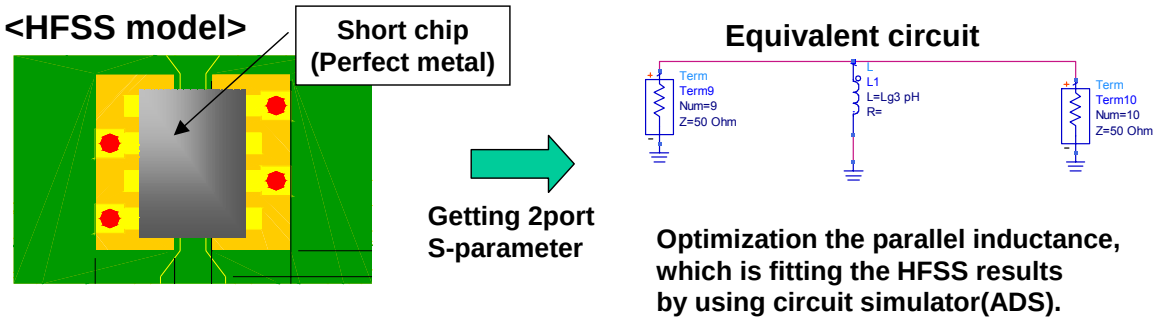


Figure10. Modeling procedure for the fixture inductance

In addition, Figure11 shows 4 models to simulate the MSL fixture about how much inductance will be decreased by the number of the thru-hole connection.

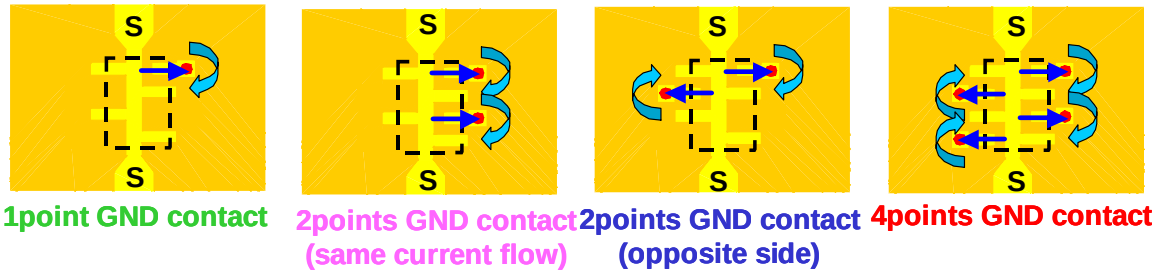


Figure11.Different current flow on the MSL fixture

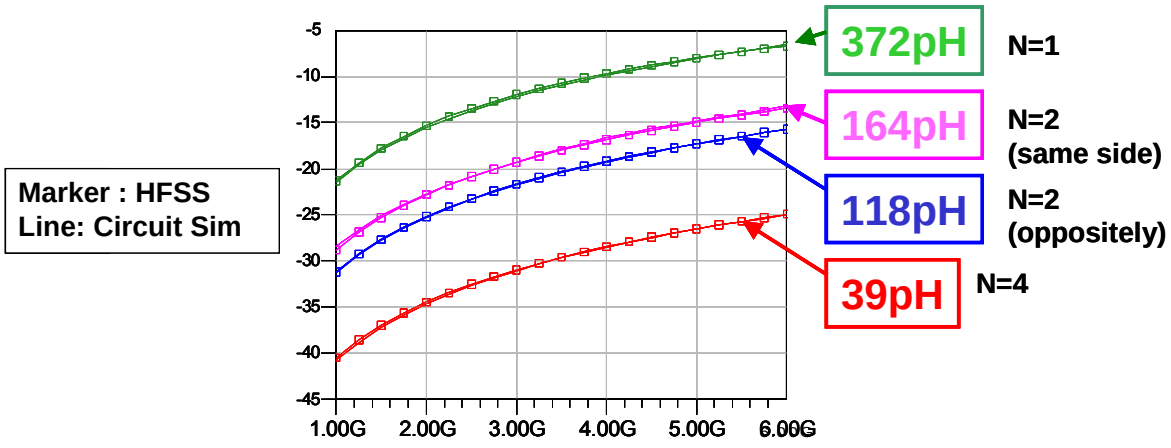


Figure12.Fitting results (S21) between measured and simulated inductance

Figure12 shows a result of the structure simulation and the equivalent inductance calculation. The equivalent inductance in Figure12 shows a reduction in the proportion as the number of the connection increases. The inductance value of 4 connections was 39pH. But if the current flows in the same direction at N=2, the inductance serves as the half approximately at the time of N=1. Also if current flows in the opposite direction at N=2, its inductance reduced by about 1/4 of N=1 by canceling magnetic field.

Therefore, it is predicted that it is set to ESL of a capacitor simple substance from the measurement data of the DUT that used this fixture by deducting 39pH. However this value doesn't contain other frequency dependence effect such as a skin effect.

Calibration and measurement condition

Measuring instrument was HP8753D (with Option1D5) VNA.

The frequency range was set to 0.03MHz to 3GHz. Bandwidth was set to 100Hz. Measuring temperature was room temperature.

In case of using MSL fixture, the coaxial cable and system was calibrated in full two port calibration with HP85033D calibration kit and with using Adaptor-removal method [3].

In case of using CPW fixture, cables and semi-rigid probes were first calibrated in full two port calibration in the 0.3MHz-3GHz frequency range with 801 points. The capacitors were soldered onto the CPW fixture, which was placed on a Cascade Micro-tech probe station. The connections to the DUT were made with two 500um GSG-probes.

Compensation procedure

The 2 port S-parameter data can be represented as Eq. 2 and Eq. 3 with Zp (parallel impedance) and Z0 (characteristic impedance), if there is the impedance, which becomes Zp is connected in parallel between signal and GND like Figure13. An attenuation property of 2 port S-parameter data can be converted to the impedance in parallel from Eq4.

Then if it divides into a real part and imaginary part like an Eq. 5,each part of the Zp can be represented as Eq. 6 and Eq. 7.

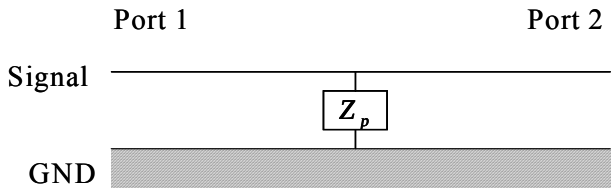


Figure13.Converting impedance from S-parameter with shunt to GND model

$$S_{11} = -\frac{Z_0}{Z_0 + 2Z_p} \quad \text{------ (Eq.2)} \qquad S_{21} = \frac{2Z_p}{Z_0 + 2Z_p} \quad \text{------ (Eq.3)}$$

$$Z_p = -\frac{1 + S_{11}}{2S_{11}} Z_0 = \frac{S_{21}}{2(1 - S_{21})} Z_0 \quad \text{------ (Eq.4)}$$

$$\left(Z_p = R_p + j X_p, \quad S_{11} = S_r + j T_r, \quad S_{21} = S_t + j T_t \right) \quad \text{------ (Eq.5)}$$

$$\begin{cases} R_p = -\dfrac{S_r(1 + S_r) + T_r^2}{2(S_r^2 + T_r^2)} Z_0 = \dfrac{S_t(1 - S_t) - T_t^2}{2\left[(1 - S_t)^2 + T_t^2\right]} Z_0 & \text{------ (Eq.6)} \\ X_p = \dfrac{T_r}{2(S_r^2 + T_r^2)} Z_0 = \dfrac{T_t}{2\left[(1 - S_t)^2 + T_t^2\right]} Z_0 & \text{------ (Eq.7)} \end{cases}$$

Zp consists of DUT impedance (Zdut) and fixture impedance (Zfixture), canceling the characteristic of fixture can express the characteristic of DUT impedance by Eq. 8.

$$Zdut = Rd + jXd = (Rp - Rf) + j(Xp - Xf) \quad \text{------ (Eq.8)}$$

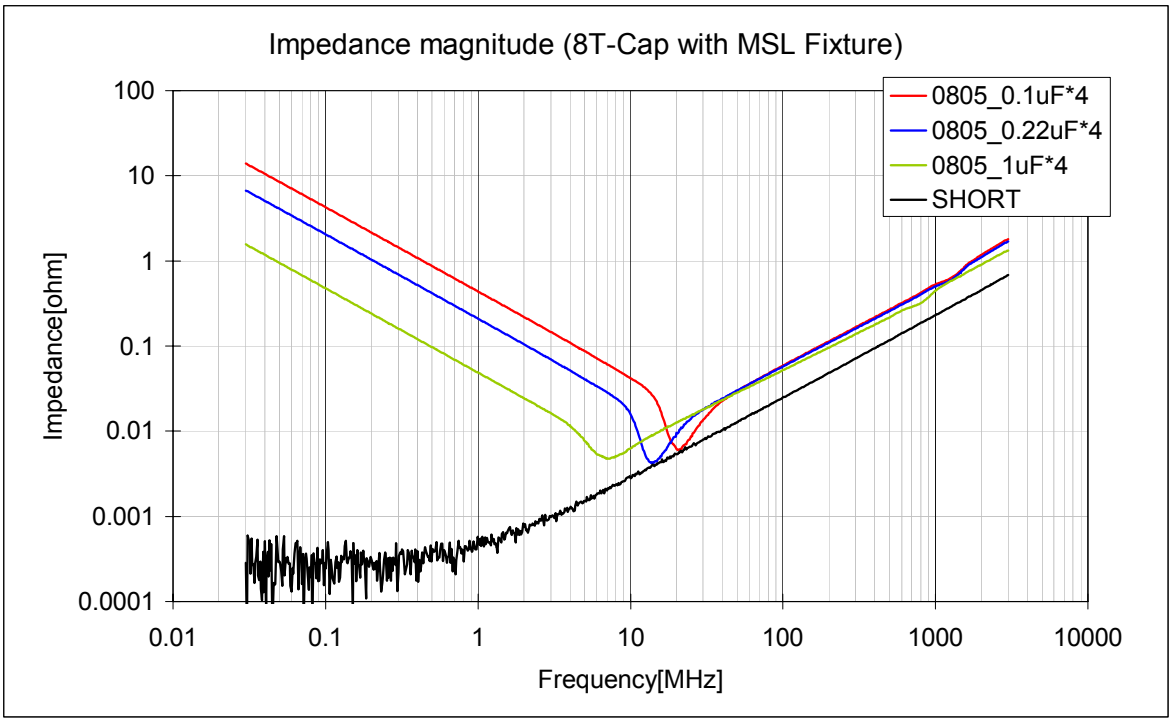
If it sets with Zdut=Rd+jXd and Zfixture=Rf+jXf, the fixture characteristic can be subtracted by the following formula Eq. 9 from Eq. 6 and 7.

$$Zp = Zdut + Zfixture$$

$$Zdut = Zp - Zfixture \quad \text{------ (Eq.9)}$$

Measurement results

Figure14 shows measured impedance of the 8T-MLCC (0.1uFx4, 0.22uFx4, and 1uFx4 with MSL and CPW fixture).



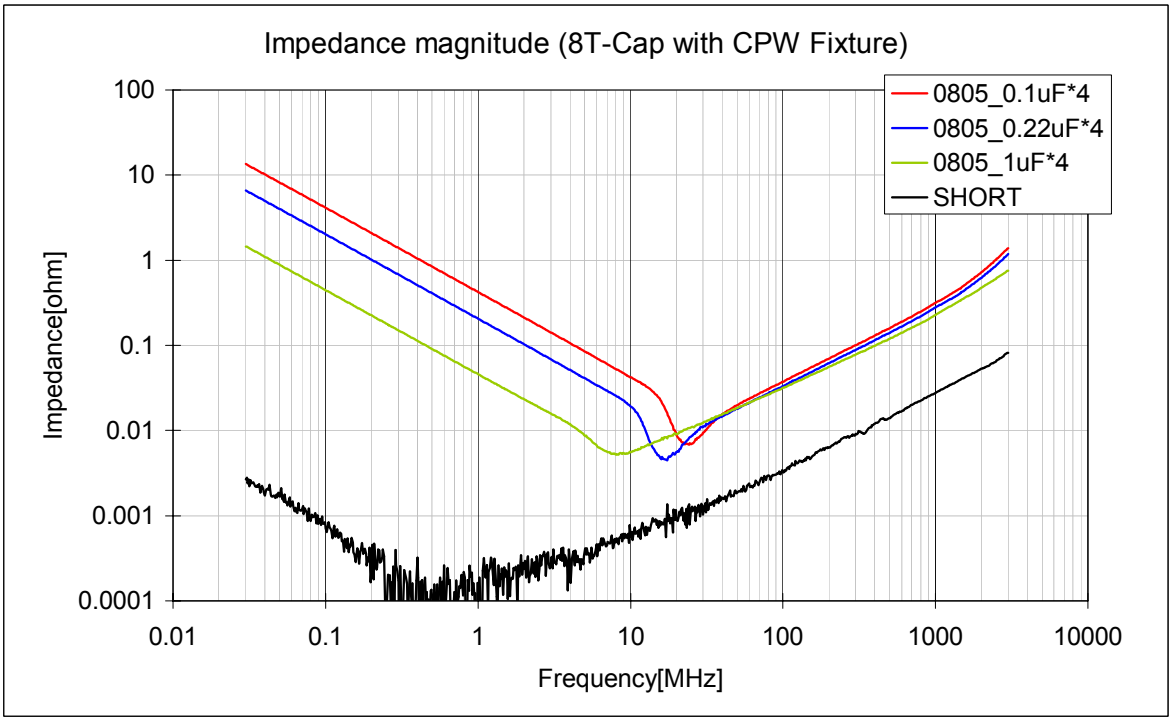
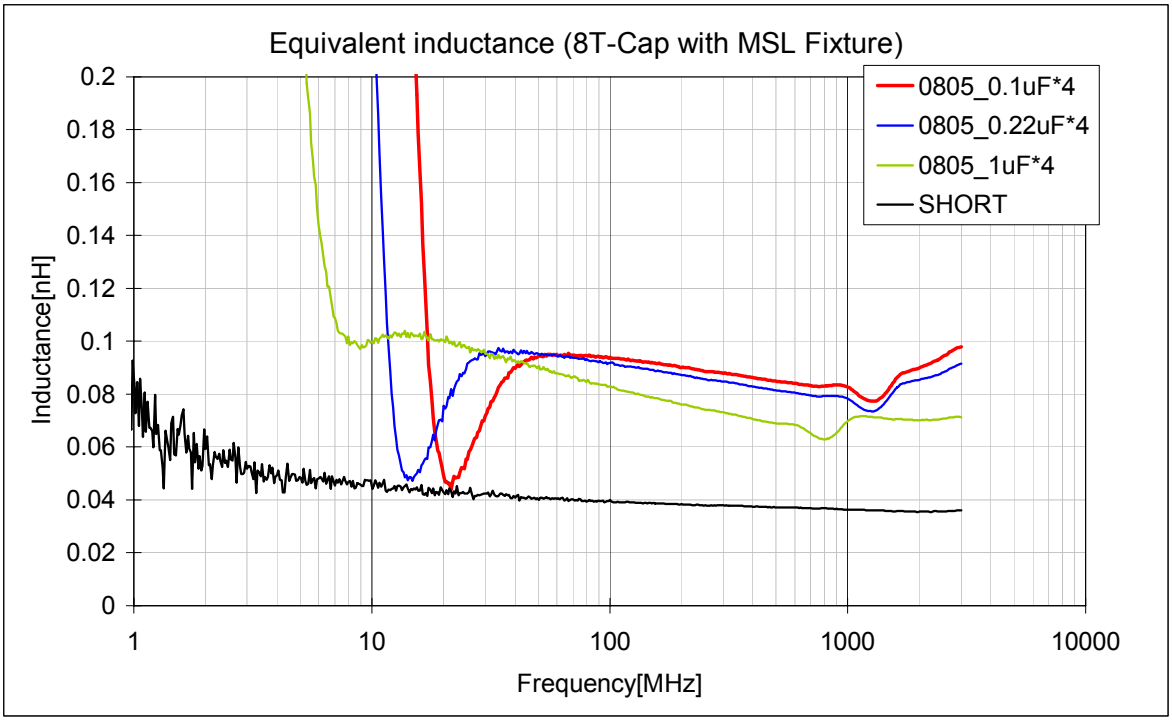


Figure14.Measuring impedance with two fixture and 8T MLCC

Figure15 shows measured equivalent inductance of the 8T-MLCC (0.1uFx4, 0.22uFx4, and 1uFx4 with MSL and CPW fixture).



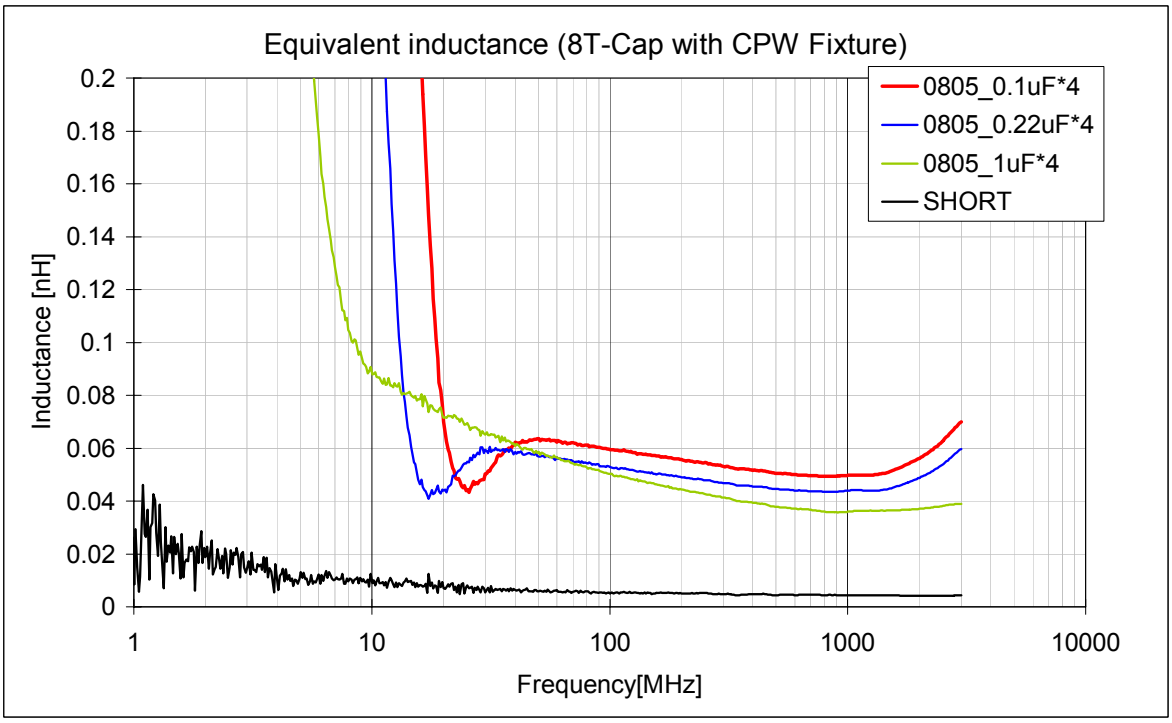


Figure15.Measuring equivalent inductance with the two fixtures and 8T MLCC

Figure16 shows the compensated short-bar data from Figure14, which contains the fixture property.

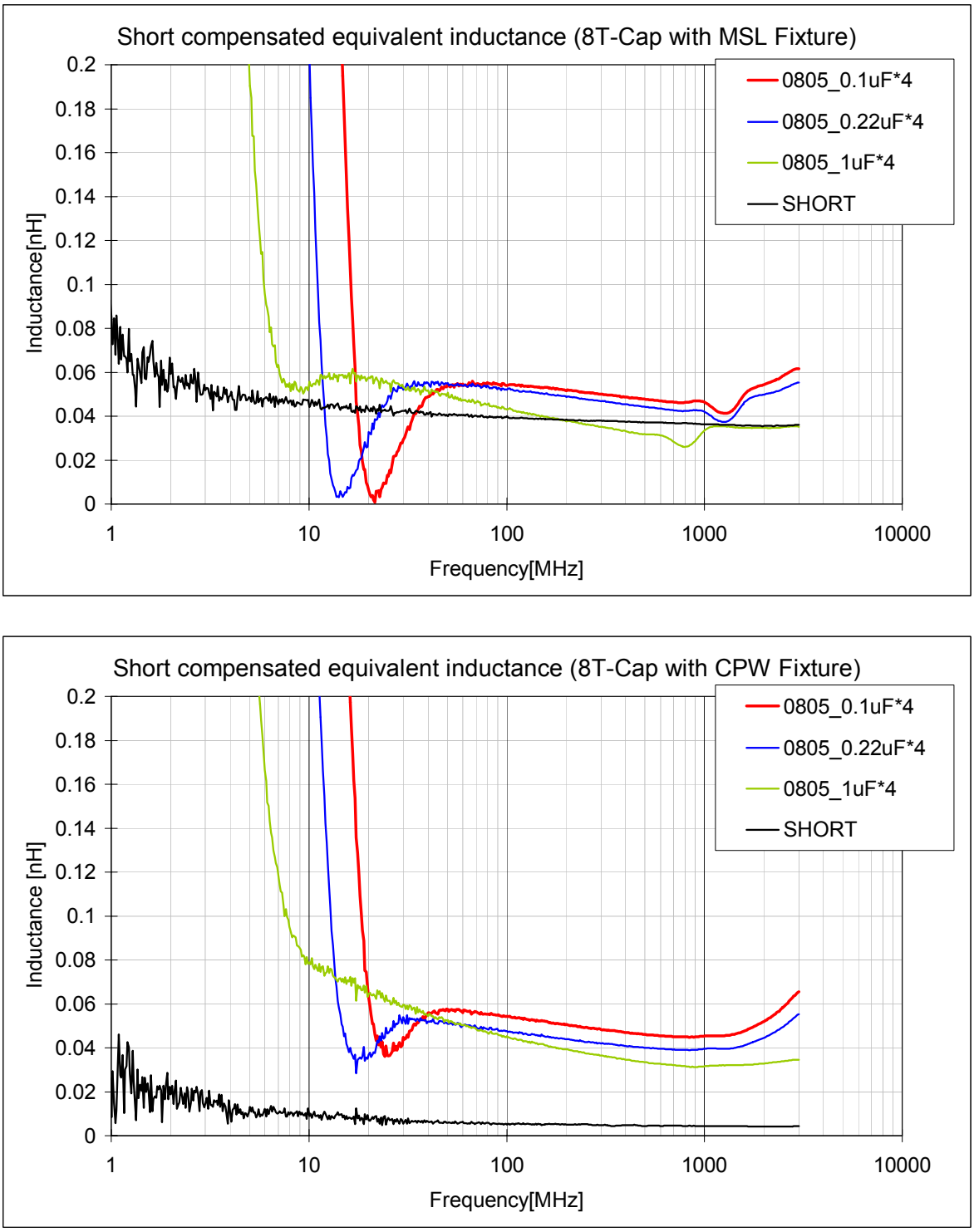


Figure16.Short compensated equivalent inductance with the two fixtures and 8T MLCC

Table1 shows the results, which were averaged three samples of the 8T-MLCC.

Compared with the impedance curves of the shorted MSL fixture and shorted CPW fixture, obviously CPW fixture's impedance was lower than MSL's. This is because the GND pads of the CPW fixture is very close to calibration line that GSG type probes are used to calibrate.

MSL Fixture

Sample	Cap[μF]	ESR[mΩ]	ESL[pH]	SRF[MHz]
8T Cap 0.1uF*4	0.37	5.1	134.7	21.2
8T Cap 0.22uF*4	0.74	3.6	136.5	14.2
8T Cap 1uF*4	3.25	4.5	116.1	7.2

CPW Fixture

Sample	Cap[μF]	ESR[mΩ]	ESL[pH]	SRF[MHz]
8T Cap 0.1uF*4	0.37	6.4	95.0	24.2
8T Cap 0.22uF*4	0.76	4.4	90.4	17.4
8T Cap 1uF*4	3.41	5.1	75.9	8.2

Table1.8T-MLCC measurement results (with fixture property)

And then the ESL values from Table1 that calculated from the capacitance and SRF were about 40pH lower than the values from CPW fixture.

Figure15 shows the MSL fixture has about 40pH inductance at 100MHz,and the CPW fixture has about 5pH inductance.

Figure16 shows the ESL data which was subtracted the fixture characteristics (shorted) from raw data (Figure15). Compared with the compensated ESL value(Table2) at 100MHz, it is mostly in agreement within 5 pH. It can be getting the data which is close to a single piece of the capacitor and independent of the fixture by performing short compensation.

Fixture Compensation

	MSL Fixture	CPW Fixture
Sample	ESL[pH] at 100MHz	ESL[pH] at 100MHz
8T Cap 0.1uF*4	54.0	54.4
8T Cap 0.22uF*4	51.9	47.7
8T Cap 1uF*4	43.1	45.2

Table2. Correlation of short compensated ESL data between MSL and CPW fixture

Conclusion

For the VNA 2-port measurement with a soldered capacitor on a PCB, the residual inductance is changed depended on the used substrates. However, it is possible to extract the DUT characteristics by subtracting a fixture data mounted a short-bar that is the same size as the DUT. By using this method, ESL values at 100MHz was matched within 5 pH between MSL PCB and CPW PCB.

MLCC has stacked layers alternately that consist of a dielectric and conductive material. The current loop length between signal layers and ground layers will be changed in the case that the stacked layers are horizontal or vertical for the PCB. It is necessary to comprehend preliminarily the mounting direction against the PCB for measuring capacitor's ESL.

References

[1] Istvan Novak, Leesa Noujeim, Valerie St. Cyr, Nick Biunno, Atul Patel, George Korony, Andy Ritter "Distributed Matched Bypasssing for Board-Level Power Distribution Networks" Manuscript for IEEE CPMT, August 2002

[2] Agilent "8 Hints for Successful Impedance Measurements" Application Note 346-4

[3] International Standard IEC 62024-1 "High frequency inductive components electrical characteristics and measuring methods"

[4] EIA Standard "Test procedure for high frequency characterization of low inductance multi-layer ceramic chip capacitors" PN-4563

[5] Agilent "How To Accurately Evaluate Low ESR, High Q RF Chip Devices" Application Note 1369-6

[6] C.R. Sullivan and Yuqin Sun, "Using Distributed Models of Inductive Effects in Multilayer Ceramic Capacitors to Design for Fast Response." Intel Technology Symposium, August 2002.

[7] Istvan Novak, Jason R. Miller "Frequency-Dependent Characterization of Bulk and Ceramic Bypass Capacitors" Manuscript for the 12th Topical Meeting on Electrical Performance of Electronic Packaging October 2003, Princeton, NJ