# DesignCon 2008

# Impact of PCB Laminate Parameters on Suppressing Modal Resonances

Jason R. Miller
Gustavo Blando
K. Barry A. Williams
Istvan Novak

Sun Microsystems, Inc.
Tel: (781) 442-2274, e-mail: Jason.R.Miller@Sun.com

## Abstract

Power planes are capacitive at low frequencies, then develop resonances according to their cavity dimensions. By reducing the plane thickness, the downward impedance slope is pushed to lower values and at the same time the modal resonances get gradually suppressed. The *Q* of these resonances is related to the effective loss of the composite material of dielectric and metallization. In this paper, we show how the total area and aspect ratio, together with laminate thickness, impact the high frequency impedance profile. Simulated results will be correlated to test structure measurements.

## Authors Biography

Jason Miller is a senior staff engineer at Sun Microsystems where he works on ASIC development, ASIC packaging, interconnect modeling and characterization, and system simulation. He received his Ph.D. in electrical engineering from Columbia University. He has authored or coauthored over 30 technical articles on the topics such as high-speed modeling and simulation.

Gustavo Blando is a staff engineer with over 10 years of experience in the industry. Currently at Sun Microsystems, he is responsible for the development of new processes and methodologies in the areas of broadband measurement, high speed modeling and system simulations. He received his M.S. from Northeastern University.

Barry Williams is a staff engineer at Sun Microsystems. He holds a bachelor's degree from Northeastern University and has worked at Sun Microsystems since 2005. Before Sun Microsystems, he worked for 16 years as a principal engineer at Digital Equipment Corp, Compaq Computer Corp, and Hewlett Packard Corp (Digital Equipment Corp. merged with Compaq Computer Corp. and Compaq Computer Corp. merged with Hewlett Packard Corp.). He worked within the midrange VAX servers groups until 1998 and later with the Alpha based high performance computing groups before retiring from Hewlett Packard Corp. in 2003.

Istvan Novak is a principle engineer at Sun Microsystems. Besides signal integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is a Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies.

# 1 Introduction

A common approach for reducing simultaneous switching noise (SSN) and electromagnetic interference (EMI) in printed circuit boards (PCBs) is to decrease the thickness of the laminate material. Thinner laminates provide three primary benefits for SSN reduction when compared to thicker plane pairs. First, the static capacitance is increased, which decreases the plane impedance. Second, the plane inductance is lowered by the same factor that the capacitance is increased. Although this inductance does offer energy storage (magnetic), the overriding concern is that inductance reduces the effectiveness of the delivery network by increasing the impedance between the device and supply network. Thinner laminates have lower inductance, which results in lower high-frequency impedance. Finally, thin laminates can help to suppress modal resonances in the impedance profile. Resonances are an inevitable consequence of the open (or closed) plane boundaries, producing standing waves and resonances. Resonances are not only important to suppress because a flat impedance profile yields a smooth step response and the low voltage noise [1] but also because a flat impedance profile helps to minimize EMI and radiation. The mechanisms responsible for this suppression are the conductive and dielectric loss of the planes and dielectric material, respectively. Although the series resistance of planes itself does not increase, thinner dielectrics can cause a redistribution of fields which increases the effective loss. The first two benefits of thin laminates can be accomplished by using multiple plane pairs in parallel, the third benefit, i.e. the additional loss, can only be achieved using thin plane pairs.

Industry trends, such as increased functionality and decreased form factor, are pushing PCB designs to be smaller and more densely packed. These trends coupled with the differing device voltage and power requirements lead to splits in the power (or ground) planes, creating multiple plane puddles or islands. Previously published studies on thin laminate have focused on the impact of laminate thickness on suppressing resonances (e.g., [2]) on average-size computer boards without plane splits. Overall area, aspect ratio and surface roughness of the structure were not individually considered in the resonance suppression. In this paper, we show how secondary laminate dimensions, primarily the total area and aspect ratio, together with laminate thickness, impact the high frequency impedance profile.

# 2 Theory

Open-edge rectangular plane pairs, like transmission lines, resonate at multiples of half wavelengths (e.g., 1, 3/2, 2, 5/2, …). At these frequencies the self-impedance profile exhibits peaks. These peaks are often called *parallel resonances* due to the fact that the impedance of a lossless tank circuit tends towards infinity at resonance. Also like transmission lines, there are dips in the impedance profile between the peaks, but not necessarily at multiples of quarter wavelengths (e.g., 3/4, 5/4, 7/4, 9/4, …). The first of these resonances, i.e., the fundamental, is often referred to as the *series resonance*, due to the fact that the impedance of a series circuit at resonance, approaches its series

resistance loss. The overall impedance profile is spatially dependent. The parallel resonances, for example, may be suppressed where there is modal cancellation. As the frequency increases, the magnitude ratio of subsequent peaks and dips diminishes due to two reasons: higher-order modes follow each other with lower relative frequency spacing and also due to frequency dependent losses.

The amplitude of these resonances can be reduced by decreasing either the metal or dielectric thickness. The impact of metal and dielectric thickness on losses can be understood by again referencing transmission line theory. In transmission line theory, the propagation constant, $\alpha$, tells us the rate of exponential attenuation whereas the phase constant, $\beta$, tells us the amount of phase shift [3]. If we assume the transmission line is low loss[1] and model this loss using a frequency-dependent series resistance, *R(f)*, and frequency-dependent distributed shunt conductance, *G(f)*, the following approximations can be obtained for the propagation constant (which is our primary concern here):

$$\alpha \approx \frac{R(f)}{2Z_0} + \frac{G(f)Z_0}{2} \tag{1}$$

The first and second terms in (1) capture the losses due to the conductor and dielectric, respectively. $Z_0$, in this case, is defined as follows [4]

$$Z_0 = \frac{532}{\sqrt{\varepsilon_r}} \frac{t}{P} \tag{2}$$

where $t$ is the thickness of the dielectric and $P$ is the perimeter of the rectangular plane. This is a similar expression to that of a parallel plate waveguide [5]. (2) shows that as the dielectric thickness, $t$, decreases, the characteristic impedance, $Z_0$, decreases. Although the conductive losses remain constant as the thickness is decreased in the first term of (1), the attenuation from conductor increases due to the reduced $Z_0$. $G$ is inversely proportional to dielectric thickness and $Z_0$ is proportional to the dielectric thickness. This makes the second term of (2) constant with dielectric thickness. Thus, the attenuation introduced by decreasing dielectric thickness is due to conductive losses.

# 3 Simulation Methodology

The self- and transfer impedance of laminates can be simulated using mathematics based models (analytical expressions), circuit models, and electromagnetic field models. There are a number of different mathematical models which can be employed for the first simulation method, including both lossless and lossy expressions. In this paper, the transmission plane model (TPM) [6] was used because it removes several of the limitations and deficiencies observed in other models including low-frequency inaccuracy and causality violations [7]. In this formulation, the complex, relative

[1] Power planes can be considered low loss because $R << \omega L$ and $G << \omega C$.

dielectric constant $\varepsilon_r(\omega)$, is defined over a broadband frequency range using the Debye model. Compared to the other two simulation methods, it also has the advantage of solving relatively rapidly. In this approach, partial differential equations are derived in the frequency domain for a parallel plane structure. This yields expressions for the distributed admittance and impedance of the plane pair. These results are then substituted in the lossless analytical model to obtain the final expression which includes the effects of both conductive and dielectric losses. This expression has been previously correlated to measurement results, circuit models and electromagnetic solver results [7].

# 4 Modal Suppression as a Function of Laminate Parameters

As (1) and (2) show, there are multiple parameters which influence the high-frequency attenuation of laminates. In the following sections we examine the impact of these parameters on the plane impedance and modal suppression.

## 4.1 Impact of Dielectric Thickness

Figure 1 shows the impact of reducing the dielectric thickness on a rectangular plane that is 10 x 10 inch using the TPM. This size can be representative of a computer board with unsplit planes. The simulation used a fixed copper thickness of 1 oz while stepping the dielectric thickness in the following steps: 0.01 mil, 0.1 mil, 1 mil, and 10 mil. Notice that using thin dielectric (< 8 μ) results in an almost complete suppression of plane resonances. We also observe that the thinner laminates lower the overall impedance, as expected. As a side note, notice that the series resonances moves to lower values as the additional losses detune the resonance. Although not as pronounced on this plot, the parallel resonance also detunes due to the additional losses.

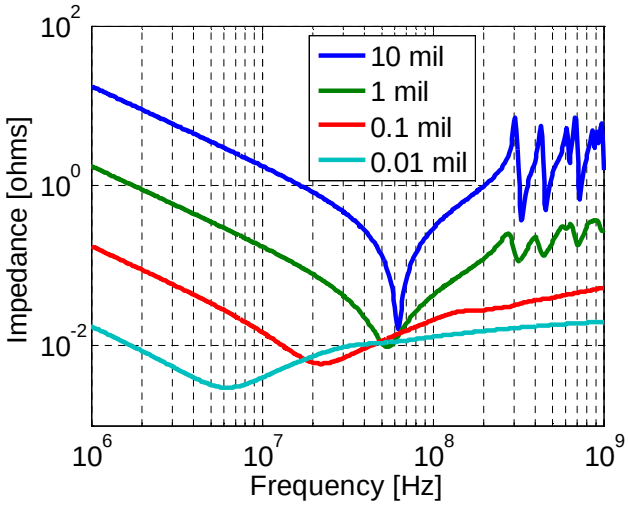



**Figure 1** Effect of dielectric thickness on self impedance of a 10 x 10 inch plane pair. The impedance for self impedance was probed at the corner. The dielectric had Dk=4 and Df=2%.

## 4.2 Impact of Conductor Thickness

Thinner metals also increase the attenuation. Conductor losses consist of both AC and DC components. Ideally, high-frequency AC losses don't increase with thinner metals, the losses simply increase with increasing frequency. The DC component, however, is inversely proportional to the plane thickness. Figure 2 shows the impact of conductor thickness on the same 10 x 10 inch laminate with (a) 1 mil and (b) 10 mil thick dielectric simulated using the TPM. Overall, reducing the copper thickness is much less effective at suppressing resonances compared to thin dielectrics.

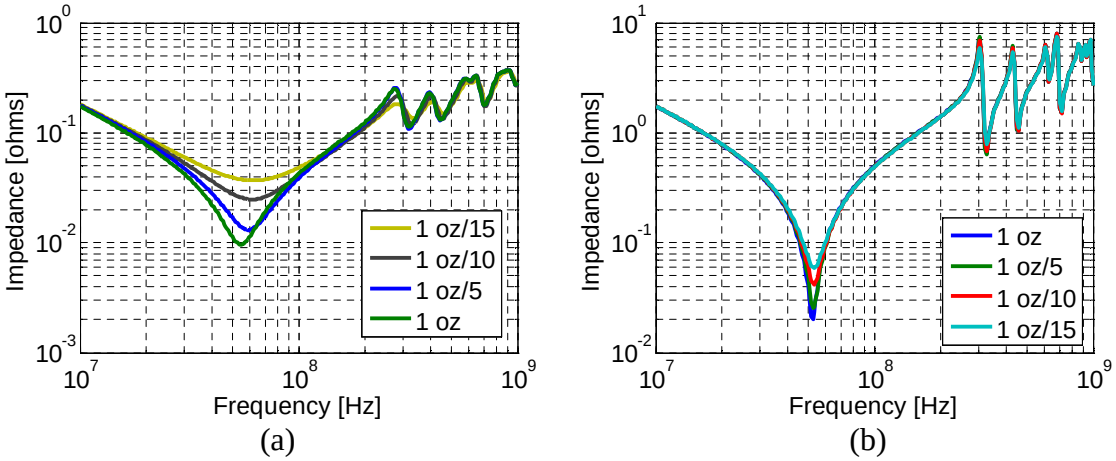



**Figure 2** Effect of copper thickness on the self impedance of a 10 x 10 inch plane pair with (a) 1 mil and (b) 10 mil laminate. The impedance was probed at the corner of the plane. The dielectric had Dk=4 and Df=2%.

## 4.3 Impact of Plane Size

Plane area per rail tends to shrink as boards get denser and more complex; there is less overall area available plus there are different rails to accommodate. The impact of plane size on resonance attenuation can be understood by examining (1)-(2). Keeping all other parameters constant, reducing the plane area will reduce the overall attenuation by increasing the characteristic impedance. In this section we examine the impact of plane size on resonance suppression using a 3-mil thick 18 x 12 inch laminate cut into progressively smaller pieces in the following steps: 9 x 6", 4.5" x 3", 2.25" x 1.5" and 1.125" x 0.75". The range of dimensions represents large boards, add-in cards, plane puddles, and packages. Figure 3 shows that the same laminate thickness (3 mil in this case) results in a significant resonance suppression on large plane, but still resonates badly in package size shapes. (b) is a zoom of (a), showing the differences in peak resonance excursions.

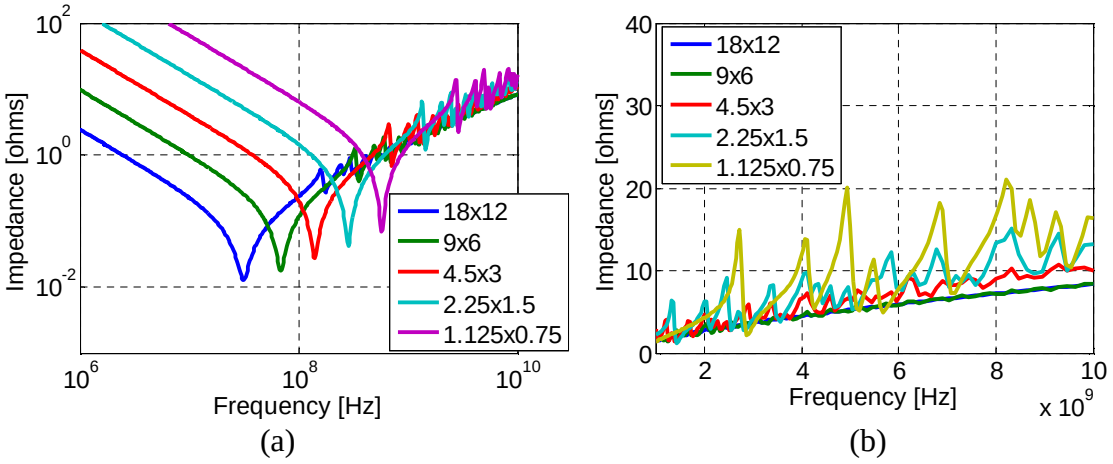



**Figure 3** Effect of plane area on the self impedance of a 18" x 12" plane pair with a 3 mil laminate cut into the following smaller pieces: 9" x 6", 4.5" x 3", 2.25" x 1.5" and 1.125" x 0.75". The impedance was probed at the corner of the plane. The dielectric had Dk=4 and Df=2%. (b) is a zoom of (a), showing the differences in peak resonance excursions.

## 4.4 Impact of Plane Aspect Ratio

In densely populated boards with many split planes we find that planes are often forced to take on irregular shapes (non-rectangular). One prevalent example of this is dedicated power and grounds for sensitive PLL circuits; these planes are often narrow and long due to the routing constraints that they connect to the device pins in a dense pin field and then connect to external filtering components, outside of the pin field. The additional inductance of the narrow plane isn't a problem in and of itself because these rails are often low-power but the reduced plane area can have a significant impact on resonance suppression. Figure 4 shows the impact of parameterizing the width of a small 240 x 240 mil plane, while maintaining the length at 240 mil. The plane width was progressively cut

in the following steps: 120, 60, 30 and 15 mil. Since the length is constant, the location of the first parallel resonance remains the same (although the higher order modes don't). As the width of the plane shrinks, we see that the same laminate thickness begins to resonate strongly. One way to quantify the degree of modal suppression is using the ratio of first peak impedance magnitude and second minimum impedance magnitude (after the first peak). Figure 4(c) plots this ratio for the same 240 mil plane but with the width stepped in increments of 30 from 10 mils to 240 mils.

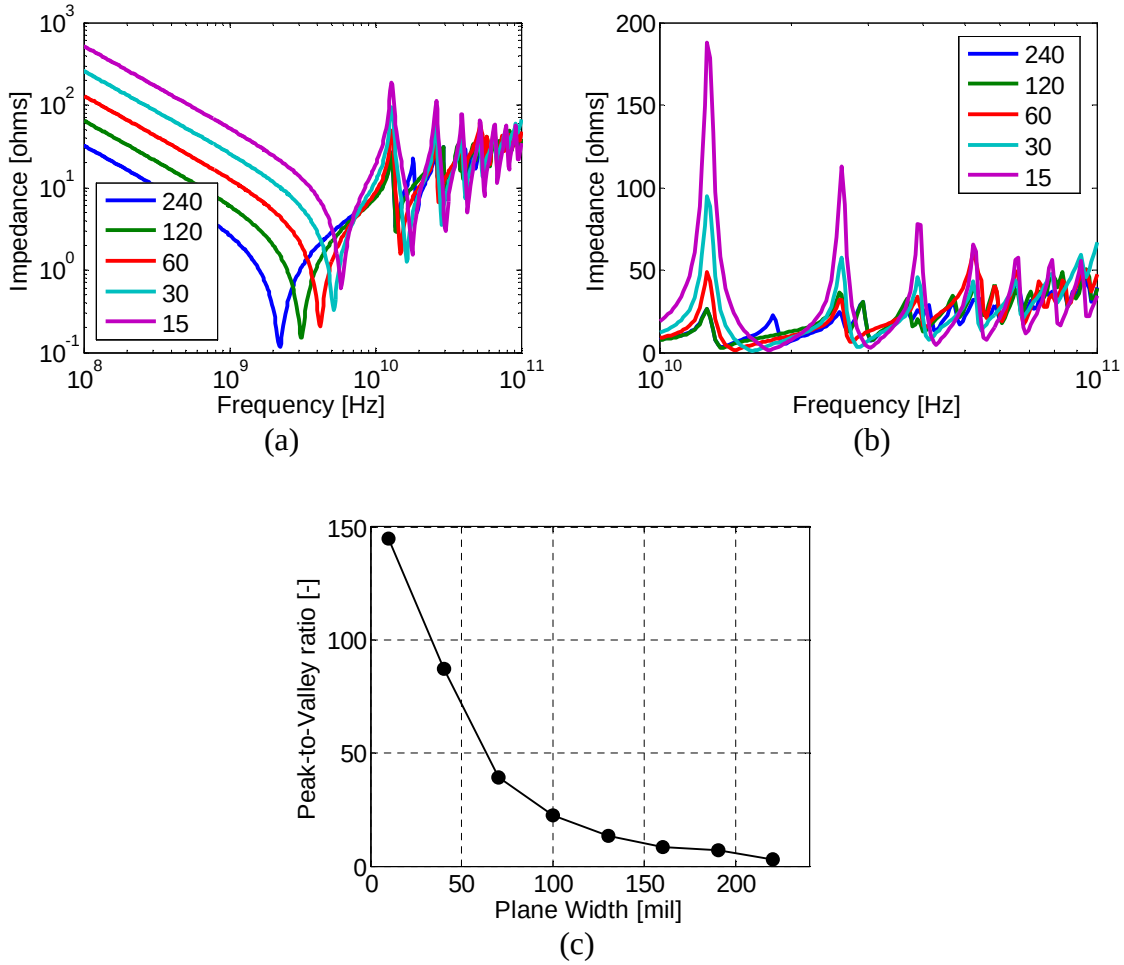



**Figure 4** Simulation of a 240 mil long plane with the following widths: 240, 120, 60, 30, and 15 mil. (b) is a zoom of (a) showing the higher-order modes. Df was 2%, the plane was probed at the corner, and the dielectric thickness was 1 mil. (c) plots the ratio of first peak impedance magnitude and second minimum impedance magnitude as a function of the plane width.

## 4.5 Impact of Dielectric Constant

(2) indicates that we can trade plane width or plane area for dielectric constant to achieve the same resonance suppression. For example, if we increase the dielectric constant

proportional to the decrease the plane area, we can maintain the impedance. Consider a plane that is 240 x 240 mil with Dk = 4: the same impedance can be achieved on a plane that is 120 x 120 mil by increasing Dk by a factor of four. This scaling procedure also maintains the static capacitance and the location of the modal resonances, making for a straightforward comparison of the two curves. Figure 5 has these two curves as overlapping demonstrating that modifying the dielectric constant or changing the plane area can achieve nearly identical resonance suppression.

Increasing the dielectric constant also pushes the resonances to lower frequencies, just like increasing plane area. Figure 5 (red) shows the simulation results for a 120 x 120 mil plane but without scaling Dk. We can observe that the larger plane or higher Dk laminate will have not only have a lower baseline impedance but the resonances are suppressed compared to the smaller plane.

However, there are practical limits to raising the dielectric constant to compensate for small plane area; first, increasing Dk requires more ceramic filling, but by doing so, the laminate becomes brittle and harder to process. Second, there are limits on the extent to which the dielectric constant can be increased; none so far have managed to get beyond 30. High dielectric constants are more practical to achieve in thin-film construction.

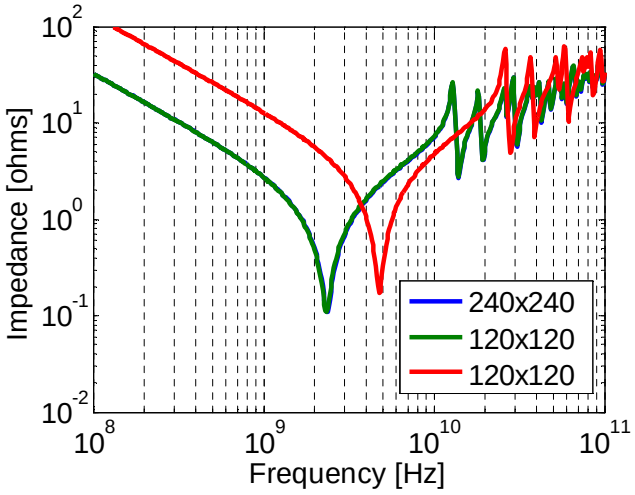



**Figure 5** Simulation of a 240 x 240 mil plane with Dk=4, a 120 x 120 mil plane with Dk=16 (4*4), and a 120 x 120 mil plane with Dk=4. The plot shows that plane area can be traded for dielectric constant to maintain the same impedance and modal suppression. Df was 2%, the plane was probed at the corner, and the dielectric thickness was 1 mil.

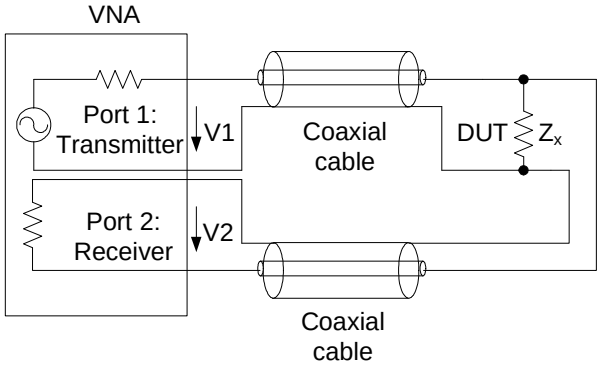
## 4.6 Impact of Dielectric Loss Tangent

There are other possible approaches to suppressing resonances as well. One possibility is to increase the loss tangent of the dielectric. Unfortunately, not only is there a lack of available materials but causality requirements would reduce the dielectric constant, decreasing the buried capacitance and increasing the impedance. Also, since typical PCB

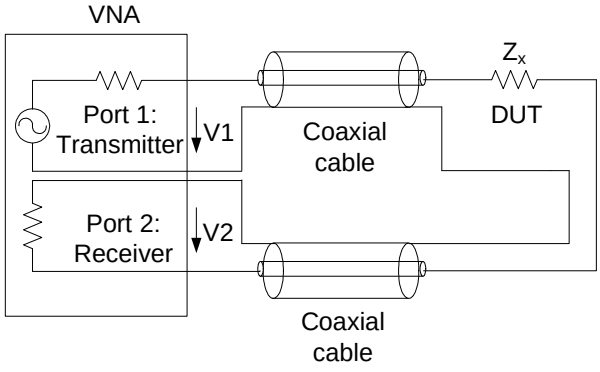
materials have been optimized for low-loss signal transmission, a high Df material would need to be utilized only on power and ground layers. This leads to another challenge: assessing the impact of these differing dielectric materials on via transitions handling high-speed signals.

# 5 Measurement Methodology

Power-ground plane pairs, especially the ones which exhibit modal-resonance suppression, have low impedance at high frequencies, thus making it challenging to measure the impedance with reasonable accuracy. The challenge at high frequencies is multi-fold. The two biggest items are: 1) we need to reduce the impact of connection uncertainties and discontinuities, and 2) we need a connection scheme to overcome the increasing error when trying to measure low impedances based on one-port reflection coefficient data. As it was shown previously [8], the Two-port Shunt-through (see also [9]) connection is a viable alternative to address this challenge. Figure 6 shows the Two-port Shunt-through and Two-port Series-through connection schemes when used with a Vector Network Analyzer (VNA).




Two-port Shunt-through connection




Two-port Series-through connection

**Figure 6** Two-port Shunt-through connection scheme for measuring low impedances (top) and Two-port Series-through connection scheme to measure high impedances (bottom). Both schemes reduce the impact of discontinuities in the connections to the DUT.

A further practical question about connectivity is how we create the connection ports on the laminate. We can put the laminate into a fabricated printed-circuit board and bring out the connections with vias. Similarly, we can do the measurement on a finished production board with connections through vias. In either case, we need to pay attention how the via connections are arranged [10]. The possible connection options are shown in Figure 7.

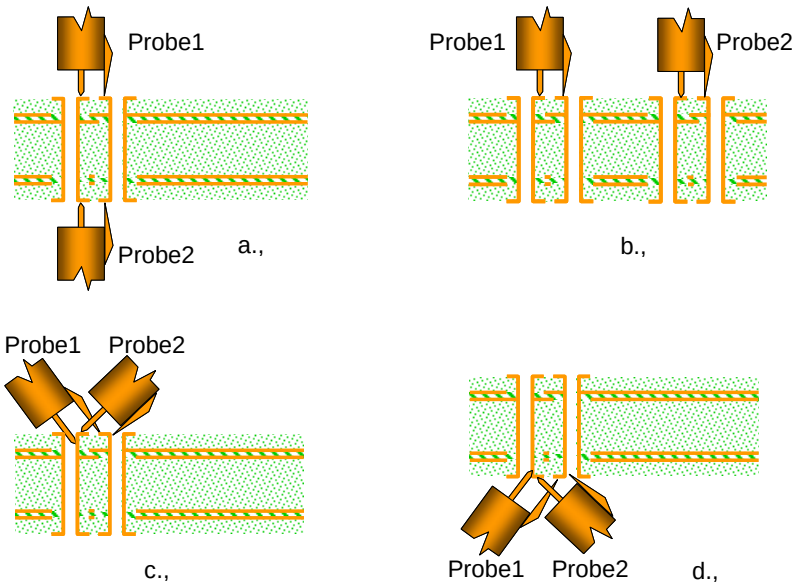



**Figure 7** Four possible connection schemes with Two-port Shunt-through method to a laminate through vias.

Only options (a) and (b) will yield the actual impedance of the laminate itself. Connection schemes (c) and (d) will result in the sum of the laminate impedance in series to the impedance of the vias. Especially for thin laminates, the via inductance can be order of magnitude higher than the plane impedance, masking out completely the plane impedance we want to measure.

Measuring the plane pair in a fabricated board carries the benefits of having a well-defined geometry (through etching) and being able to measure the plane impedance anywhere we put vias. But even if we use schemes (a) or (b) from Figure 7, there is still a small error associated with the via connections. The Two-port Shunt-through connection scheme removes the vertical via impedance from the measured data, but there is still a local disturbance of current flow at the antipads associated with the vias. The antipads reduce the static capacitance of the plane pair and slightly increases the measured inductance. Overlapping antipads can introduce significant additional inductance and should be avoided.

If we have a trusted simulation methodology to obtain the plane impedance at arbitrary points, it is then enough to do correlations at a few selected locations. This can be done on bare two-sided laminates, without etching and without the aforementioned complications associated with vias. We can connect wafer probes to the edge of the laminates as shown in Figure 8. This technique was used for all of the sample measurements and correlation examples in the following section.

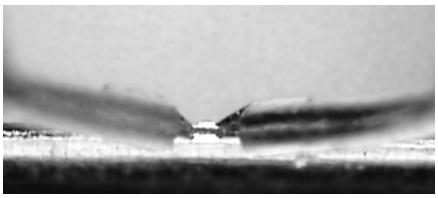


**Figure 8** Measuring bare laminates with wafer probes. Bare two-sided laminate measured along its edge.

A further possibility is to measure the laminate from the top on a fabricated laminate with edge shorting ring [11]. This, however, requires etching, drilling and plating of the laminate.

# 6 Correlations

Correlation between the TPM and measurement data was performed. The sample was a bare sheet of two-sided, 3-mil, composite laminate (DuPont Pyralux LF911R), which was probed at the edges (as shown in Figure 8) with 100 μ wafer probes. The nominal plane dimension of the samples were 0.75 x 1.125 inch, 1.5 x 2.25 inch, 3 x 4.5 inch, 6 x 9 inch, and 12 x 18 inch. Although all plane samples were measured, simulations were only performed on the smaller plane sizes in order to achieve a good accuracy in a reasonable solve time. The simulated plane stackup and dielectric material properties were identical to those shown in reference [12].

The self-impedance was measured at the middle of the shorter side using two different VNA's: the 1-1800 MHz frequencies were covered with a 4396A VNA and the 1 - 10 GHz frequencies were covered by a Agilent N5230. For both VNAs, calibration was done to the tips of the probes with a GGB Industries CS-14 calibration substrate.

Figure 9 shows two separate VNA measurements plotted on the same figure for the smallest plane. The independent datasets run on top of each other, indicating that the measured data is of good quality. At each plane size, the two plots were overlaid to examine the quality of the measured datasets.

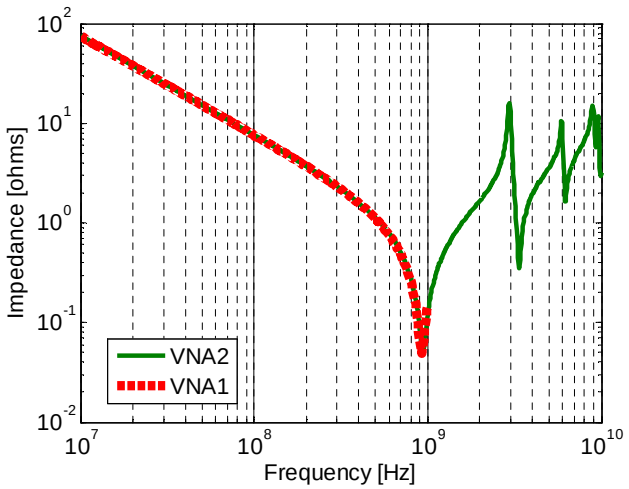



**Figure 9** Self impedance magnitude measured on the 0.75 x 1.125 inch sample.

The TPM for the plane impedance has a double infinite series, which for practical calculations must be truncated. Convergence can be examined in various ways, for instance by plotting the location of the series resonance and the peak of the parallel resonances (see Figure 10, shown for the smallest plane sample). The plot shows a rapid change in the series resonance frequency and impedance maxima for less than approximately m,n=100, after which the series resonance frequency and impedance maxima asymptotically converge. A similar plot to (b) can be generated for the higher-order parallel resonances.

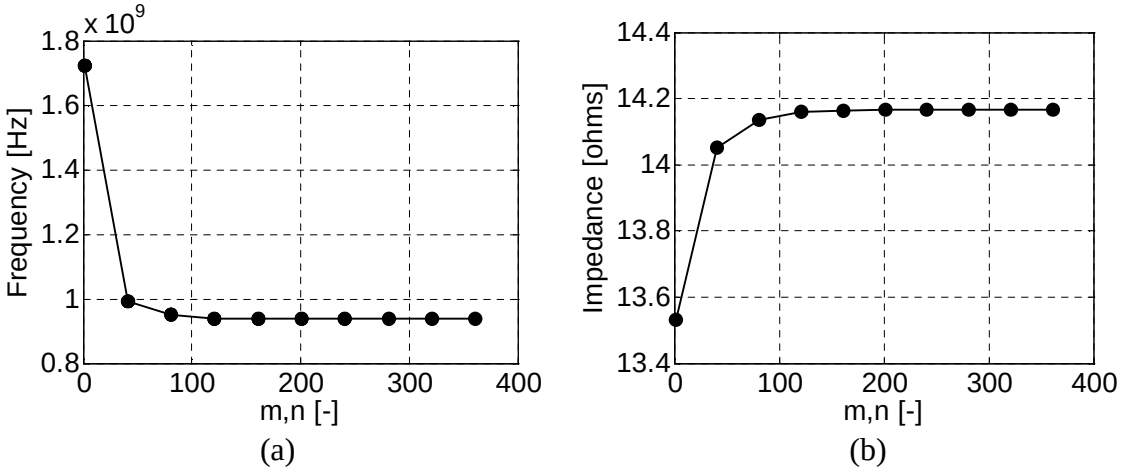



**Figure 10** Plot of the (a) series resonance frequency minima and (b) peak impedance values of the first parallel resonance as a function of m,n summation limits for the 0.75 x 1.125 inch plane pair.

Figure 11(a) shows the correlation for the 0.75 x 1.125 inch sample using m,n = 400 (well above the knee observed in Figure 10) and a port size 10 x 10 mil, which approximates the footprint of each probe after landing on the copper edges. Good correlation is observed between measured and simulated data. Figure 11(b) shows the correlation for the 1.5 x 2.25 inch plane using the same simulation conditions and m,n, limits.

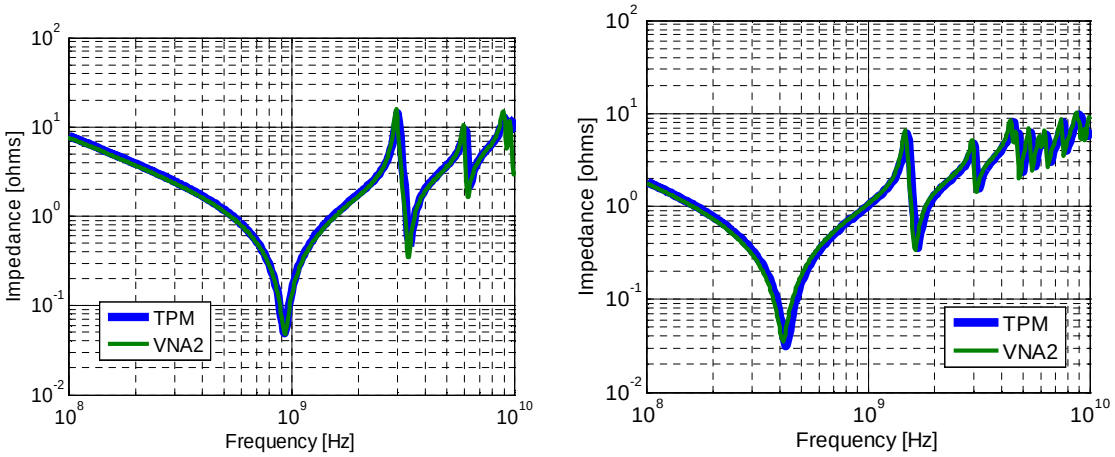



**Figure 11** Self-impedance magnitude simulated and measure on the (a) 0.75 x 1.125 inch sample and (b) 1.5 x 2.25 inch sample. "VNA2" was measured using the Agilent N5230 VNA.

As we move on to simulating and correlating the larger plane sizes, the solve time increases due to the required number of modes. Figure 12 plots the same quantities shown in Figure 10 but for the 3 x 4.5 inch sample. The point where the series resonance frequency and first impedance maximum asymptotically converge has been pushed further to the right due to the larger plane size. Eyeballing the curves, we find an m,n limit of greater than 400 is required. A more rigorous approach to quantifying convergence error can be undertaken by plotting the percentage change in both frequency and impedance as a function of summation limits.

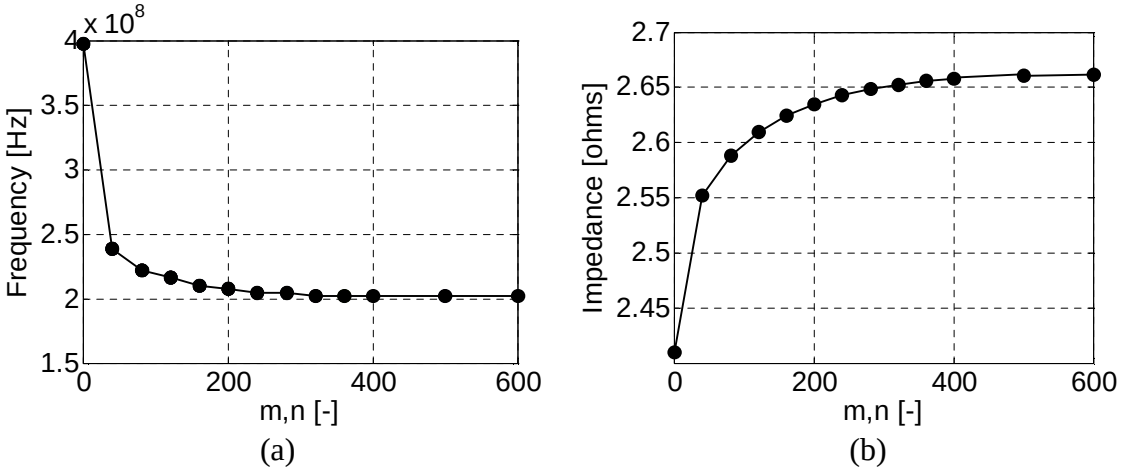



**Figure 12** Plot of the (a) series resonance frequency minima and (b) peak impedance values of the first parallel resonance as a function of m,n summation limits for the 3 x 4.5 inch plane pair.

Figure 13 shows the correlation for (a) 3 x 4.5 inch sample using m,n = 600 (well above the knee observed in Figure 12) and (b) 6 x 9 inch sample using m,n = 1300. Identical simulation conditions were used for Figure 13 as in the previous two cases. Good correlation is observed between measured and simulated data.

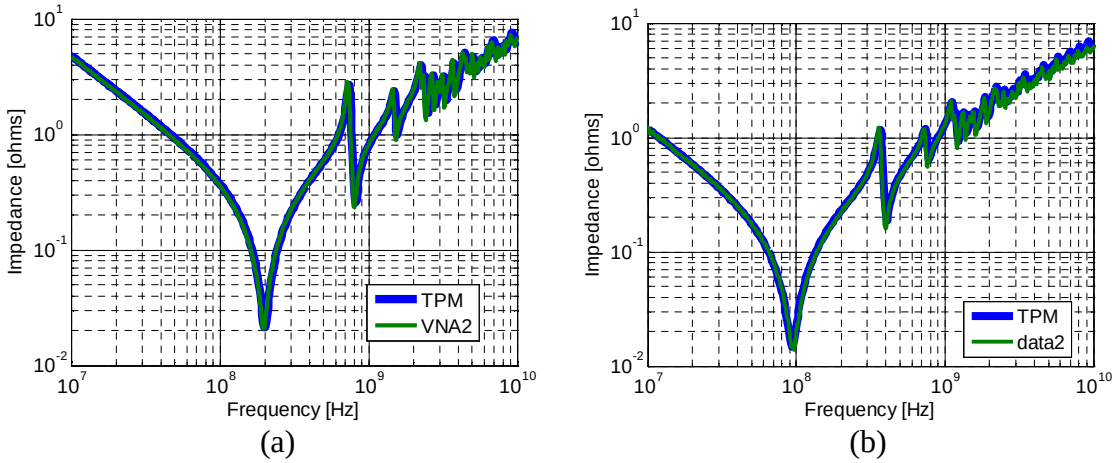



**Figure 13** Self-impedance magnitude simulated and measured of the (a) 3 x 4.5 inch and (b) 6 x 9 inch sample.

Figure 14 shows a 3D plot of the convergence of the higher order modes up to 10 GHz (but above the series resonance) as a function of the summation limit for the 6 x 9 inch sample.

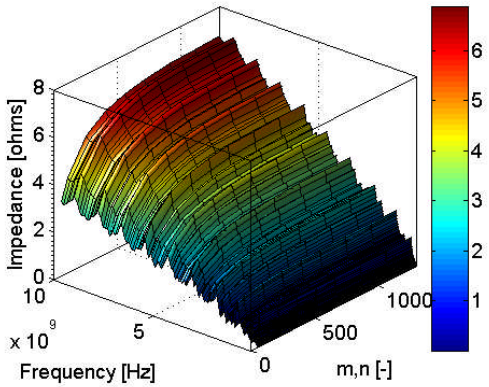



**Figure 14** Convergence of higher order modes as a function of the summation limit on the 6 x 9 inch sample.

# 7 Conclusions

Modal suppression is important not only to achieve a flat impedance profile but also because a flat impedance profile helps to minimize EMI and radiation. In this paper we've examined how several plane parameters impact modal suppression, including dielectric thickness, copper thickness, plane area, plane aspect ratio, dielectric constant and dielectric loss. Of particular relevance and importance is the plane area, which due to increased design functionality and decreased form factor, is shrinking. These plane shapes, compared to large boards with the same laminate thickness, can exhibit high Q's due to their higher impedance. Packages, puddles, and dedicated small supplies are examples of planes which may exhibit this behavior.

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