Impact of PCB Laminate Parameters on Suppressing Modal Resonances

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Agenda

- **Introduction**
- **Simulation methodology**
- **Impact of**
  - > Dielectric thickness
  - > Conductor thickness
  - > Dielectric constant
  - > Dielectric loss tangent
  - > Plane size
  - > Plane aspect ratio
- **Measurement methodology**
- **Correlation studies**
- **Conclusions**

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Intro

- Flat impedance profiles yield a smooth step response, low voltage noise [1] and help to minimize EMI and radiation
- Bare PCBs have modal resonances due to plane boundaries
- Open-edge rectangular plane pairs, like transmission lines, have peaks at multiples of half wavelengths (e.g., 1, 3/2, 2, 5/2, …). These are called parallel resonances.
- The amplitude of these resonances can be reduced by decreasing either the metal or dielectric thickness
- This can be understood by treating a PCB as a low-loss transmission line:

$$\alpha \approx \frac{R(f)}{2Z_0} + \frac{G(f)Z_0}{2} \qquad Z_0 = \frac{532}{\sqrt{\varepsilon_r}}\frac{t}{P}$$

1. Novak, I., "Comparison of Power Distribution Network Methods: Bypass Capacitor Selection Based on Time Domain and Frequency Domain Performances," Proceedings of DesignCon 2006, Santa Clara, CA, February 6-9, 2006.

Intro

- Increased functionality and decreased form factor, push PCB designs to be smaller and more densely packed
- This coupled with the differing device voltage and power requirements lead to splits in P/G planes, creating multiple plane puddles or islands
- Lowest parallel resonance frequency is determined by Dk and length of longest side

$$f_{res} = \frac{1}{2a\sqrt{\varepsilon_0 \varepsilon_r \mu_0}}$$

- Long narrow planes can have a low parallel resonance with little damping due to high impedance

Intro

- Previously studies on thin laminate have focused on the impact of laminate thickness on suppressing resonances on average-size computer boards without plane splits
- Here we consider how area and aspect ratio, together with laminate thickness, conductor thickness, Dk and Df, impact the high frequency impedance profile

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Simulation Methodology

- Self and transfer impedance of laminates can be simulated using
  > Mathematics based models (analytical expressions)
  > Circuit models
  > Electromagnetic field models
- Mathematic based models approximate plane pair as 2D waveguide (i.e. assume that plane separation is negligible compared to plane dimensions)
- For this study we use a mathematics based model using Transmission Plane Model (TPM) [1]. Benefits:
  > Speed/accuracy when compared to circuit models or electromagnetic solvers
- Compared to other analytic expressions:
  > No low-frequency inaccuracy
  > No causality violations

1. Shlepnev, Y., "Transmission Plane Models for Parallel-Plane Power Distribution System and Signal Integrity Analysis," 22nd Annual Review of Progress in Applied Computational Electromagnetics, March 12-16, 2006, Miami, FL pp. 382-389

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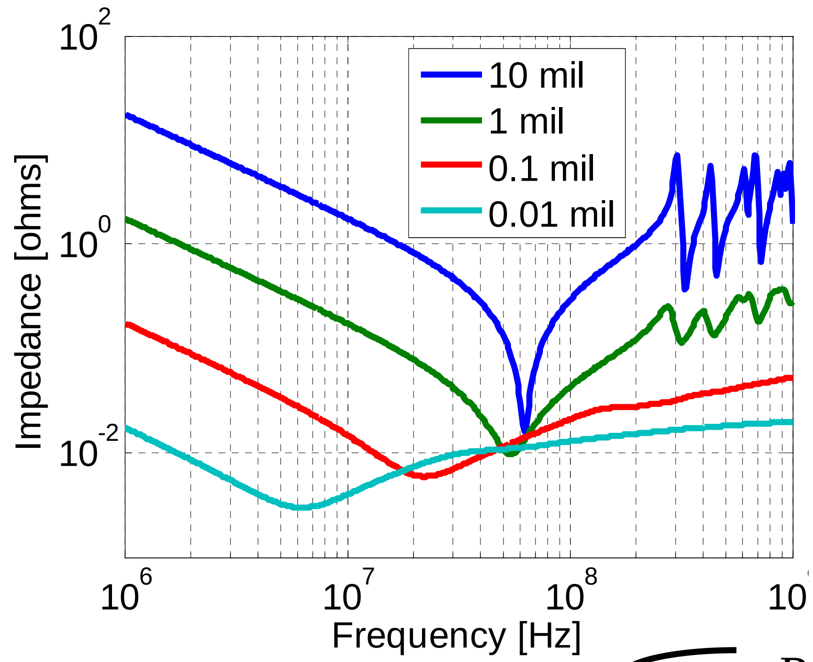
Dielectric Thickness



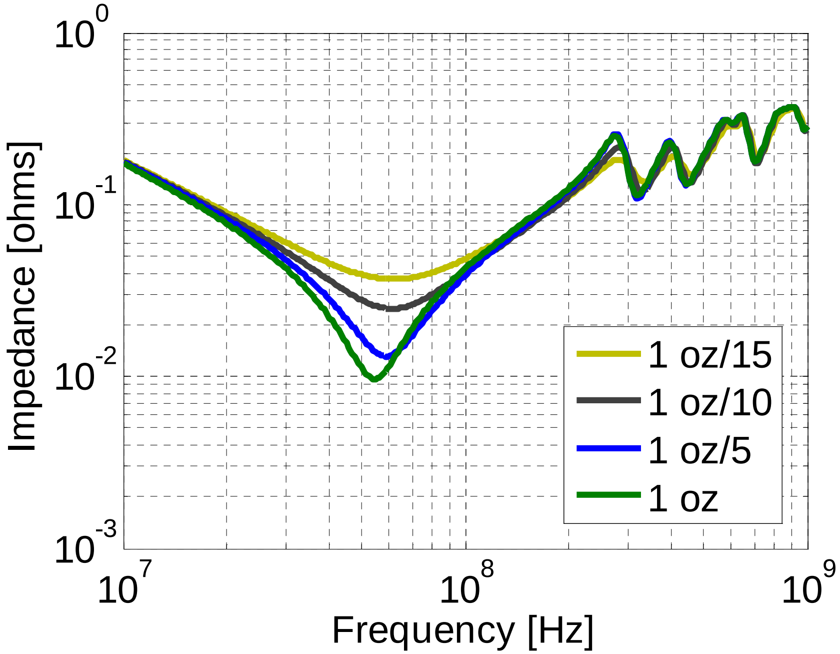
- Reducing the dielectric thickness
  1. Decreases the impedance
  2. Reduces the inductance
  3. Suppresses resonances

$$\alpha \approx \frac{R(f)}{2Z_0} + \frac{G(f)Z_0}{2}$$

$$Z_0 = \frac{532}{\sqrt{\varepsilon_r}}\frac{t}{P}$$

- Multiple plane pairs can achieve the first two benefits but not the third
- Conventional approach to achieving low impedance and suppress resonances, e.g. 10 x 10 inch plane pair

Conductor Thickness

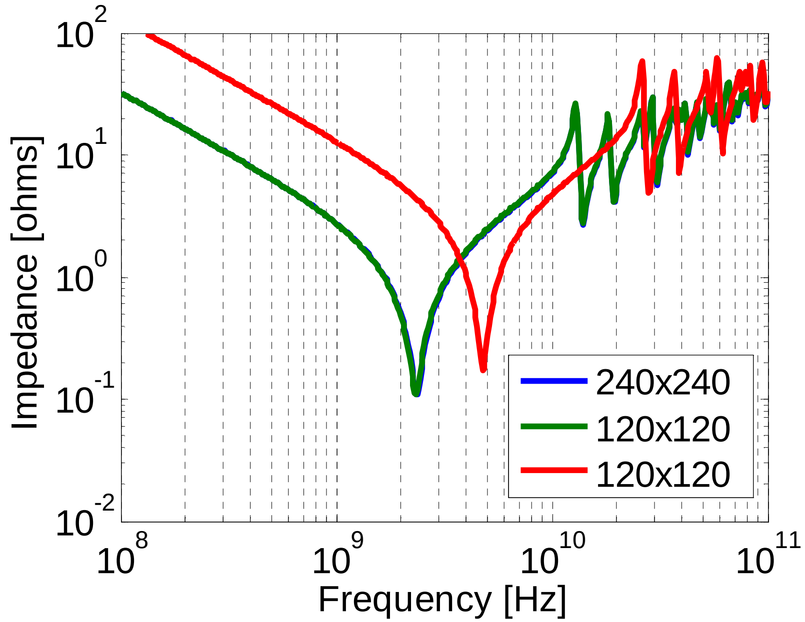


- Conductor losses consist of both AC and DC components

$$\alpha \approx \frac{R(f)}{2Z_0} + \frac{G(f)Z_0}{2}$$

- Ideally, high-frequency AC losses don't increase with thinner metals, the losses simply increase with increasing frequency
- Overall, not as effective or practical as reducing the dielectric thickness
- E.g., 10 x 10 inch plane pair w/ 1 mil laminate

Dielectric Constant



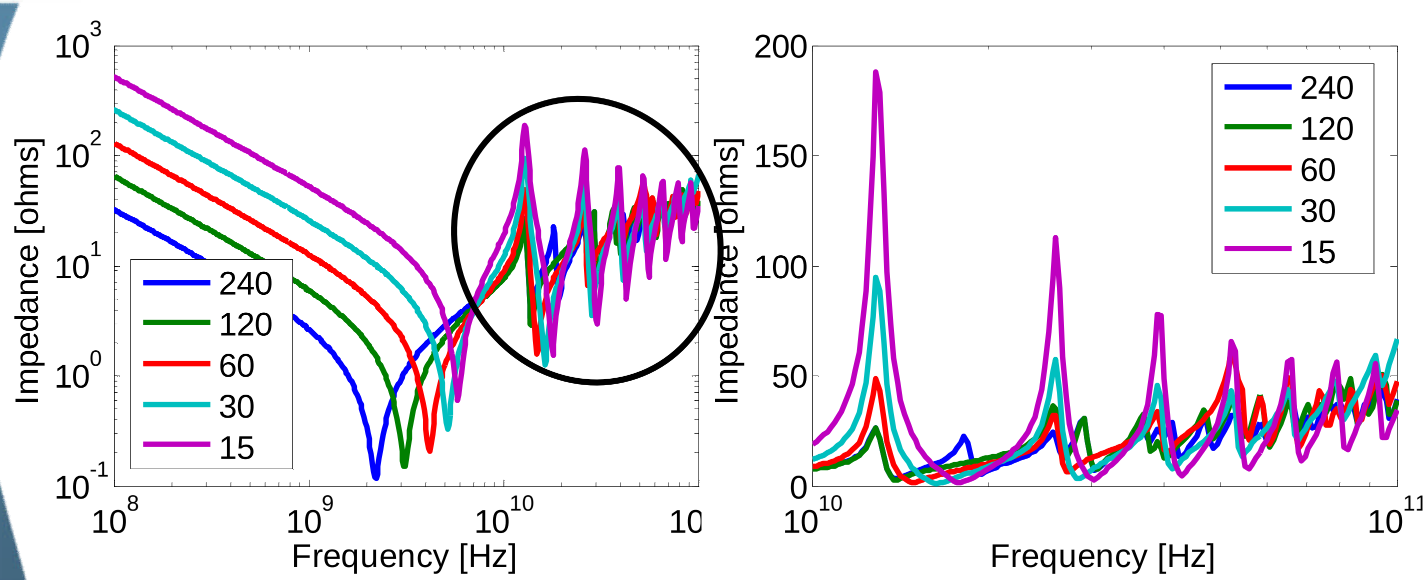
- Can trade plane width or plane area for dielectric constant to achieve the same resonance suppression

$$f_{res} = \frac{1}{2a\sqrt{\varepsilon_0 \varepsilon_r \mu_0}} \qquad Z_0 = \frac{532}{\sqrt{\varepsilon_r}} \frac{t}{P}$$

- There are practical limits to raising the dielectric constant to compensate for small plane area:
  - > Increasing Dk requires more ceramic filling - becomes brittle, harder to process
  - > Limits on the extent to which the dielectric constant can be increased; none so far have managed to get beyond 30

Dielectric Loss

- Another possibility is to increase the loss tangent of the dielectric. Several problems exist:
  - There is a lack of available materials
  - Causality requirements would reduce the dielectric constant, decreasing the buried capacitance and increasing the impedance
  - Typical PCB materials have been optimized for low-loss signal transmission, a high Df material would need to be utilized only on power and ground layers… would need to assess the impact of differing dielectric materials on via transitions handling high-speed signals



Plane Aspect Ratio

- Simulation of 240 mil long plane with the followings widths: 120, 60, 30 and 15 mil
  - > Location of the first parallel resonance remains the same (although the higher order modes don't)

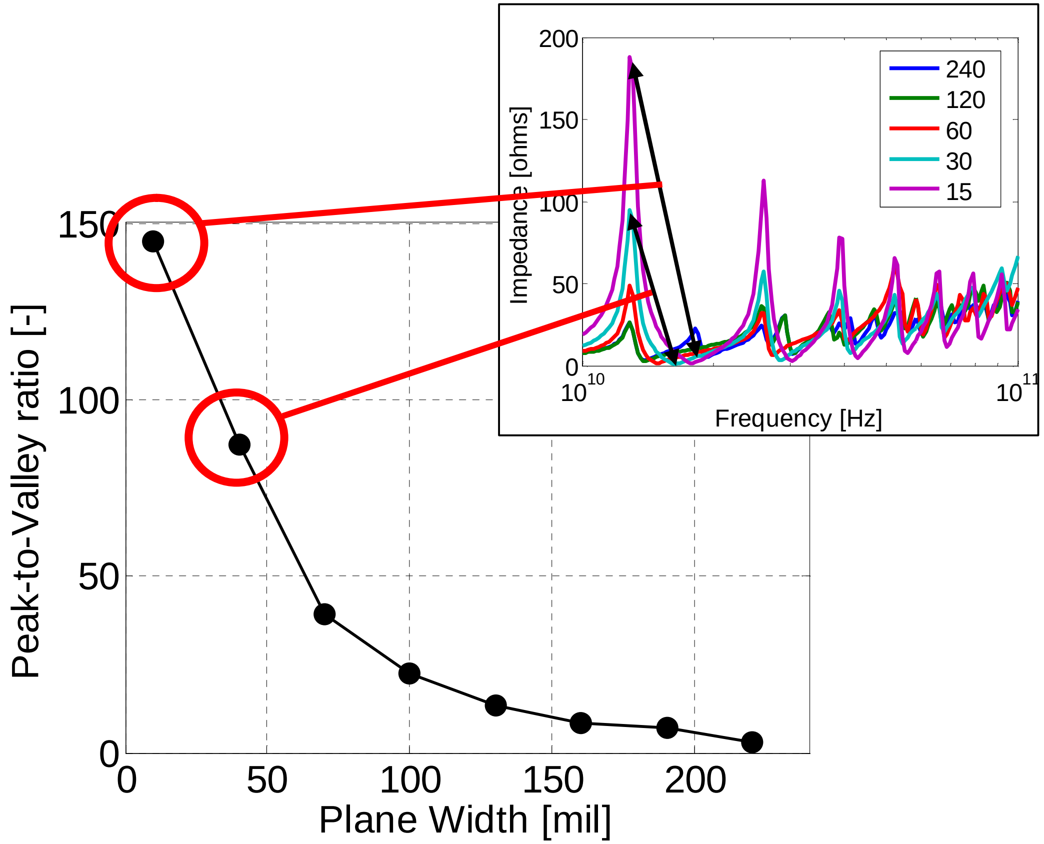
$$f_{res} = \frac{1}{2a\sqrt{\varepsilon_0 \varepsilon_r \mu_0}}$$

  - > As the width of the plane shrinks, the same laminate thickness begins to resonate strongly

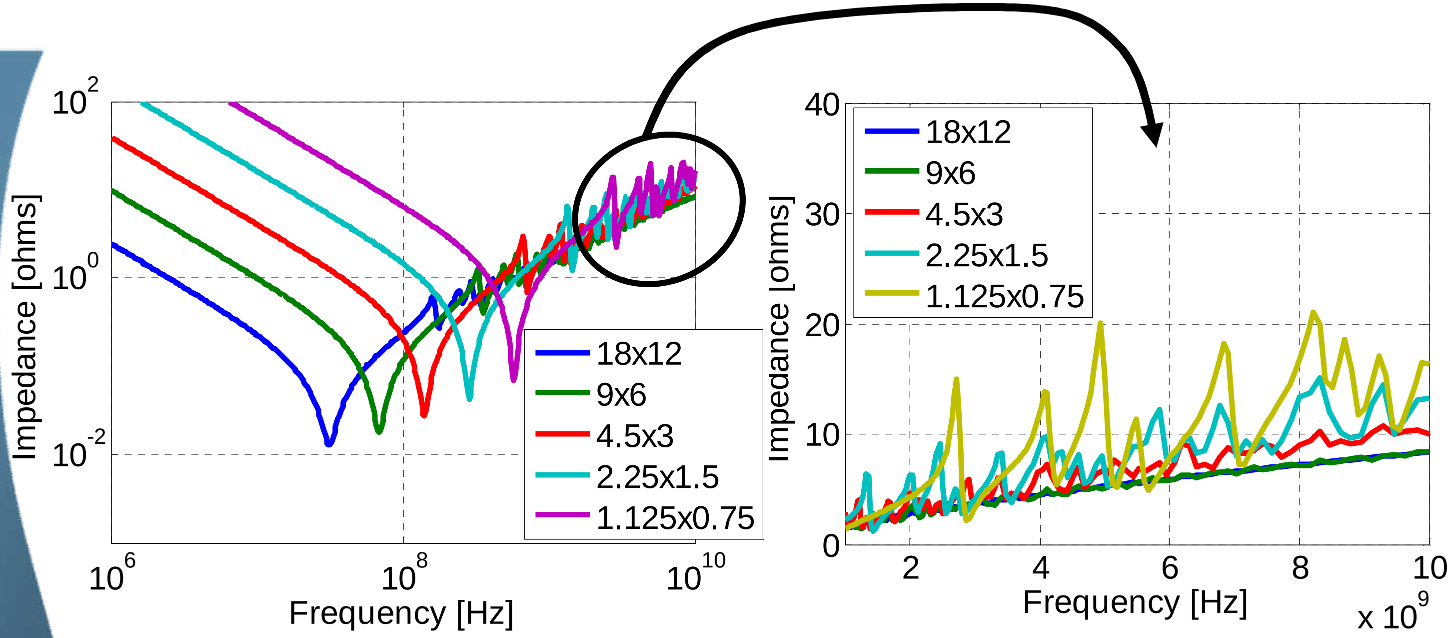
$$\alpha \approx \frac{R(f)}{2Z_0} + \frac{G(f)Z_0}{2} \qquad Z_0 = \frac{532}{\sqrt{\varepsilon_r}} \frac{t}{P}$$

Plane Aspect Ratio

- One way to quantify modal suppression is using the ratio of first peak impedance magnitude and second minimum impedance magnitude



Plane Size



- 3-mil thick 18 x 12 inch laminate was progressively halved into smaller pieces in the following steps: 9 x 6", 4.5" x 3", 2.25" x 1.5" and 1.125" x 0.75"
- Spans typical sizes for: large boards, add-in cards, plane puddles, and packages
- Shows that the same laminate thickness results in a significant resonance suppression on large plane, but still resonates badly in package size shapes

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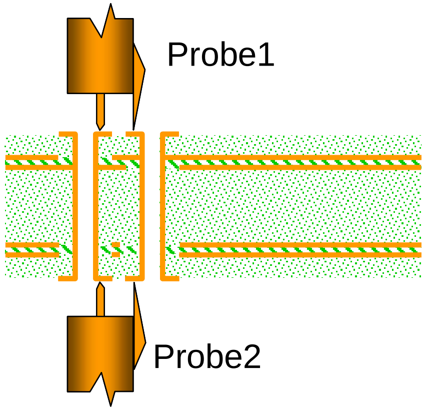
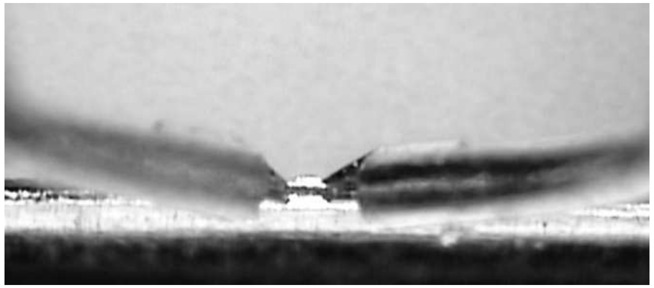
Measurement Methodology

- Plane shapes typically have low impedance (milliohms)
- Measurement challenges for low impedances:
  1. Remove/minimize uncertainties and discontinuities
  2. Need to avoid error with reflection measurements

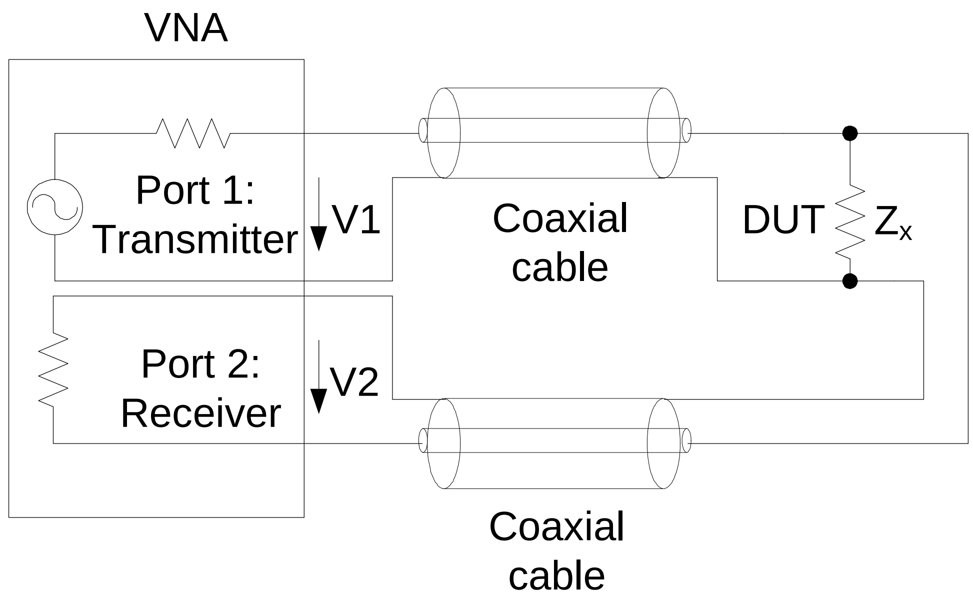


- Even if measured as illustrated above there is still an error due to vias and antipads
- Cleanest is to use wafer probes on bare two sided laminate



Measurement Methodology

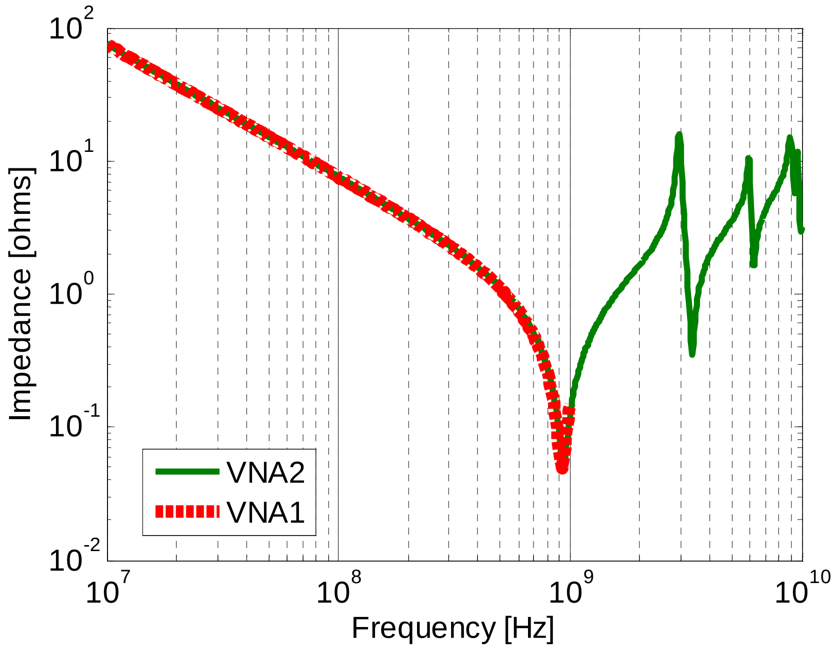
- Second challenge can be addressed using two-port shunt through connection arrangement



Two-port Shunt-through connection

Measurement Methodology

- Probed at the edges with 100 μ wafer probes using two VNAs:
  - > HP 4396 1-1800 MHz
  - > Agilent N5230 1-10 GHz
- Calibration was done to the tips of the probes with a GGB Industries CS-14 calibration substrate
- Frequency overlap provides a quality check point



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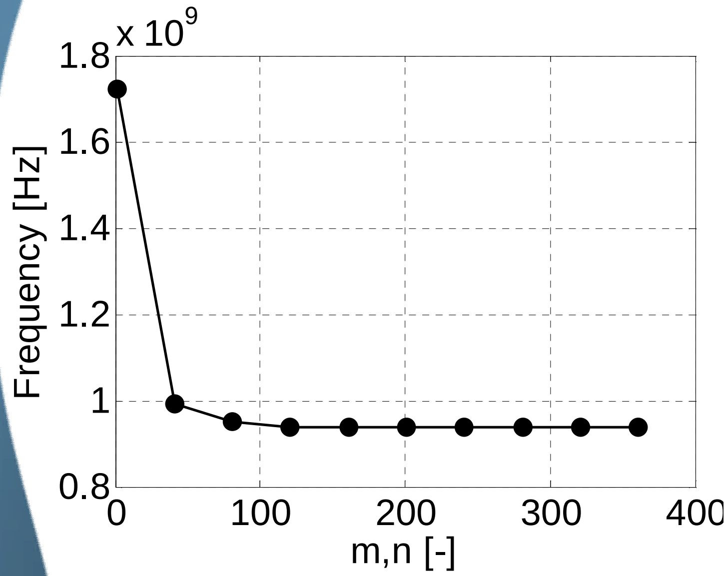
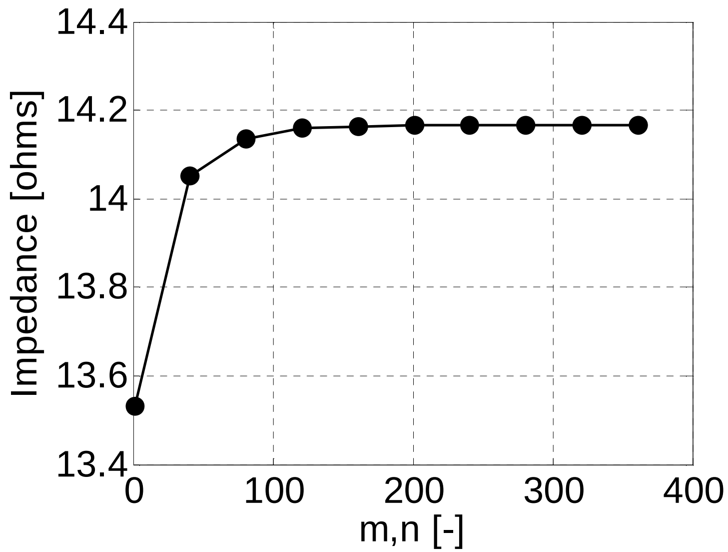
Correlation Studies

- Sample suite were bare sheets of two-sided, 3-mil, composite laminate (DuPont Pyralux LF911R) of varying dimensions
- Nominal plane dimension of the samples were 0.75 x 1.125 inch, 1.5 x 2.25 inch, 3 x 4.5 inch, 6 x 9 inch, and 12 x 18 inch

Correlation Studies

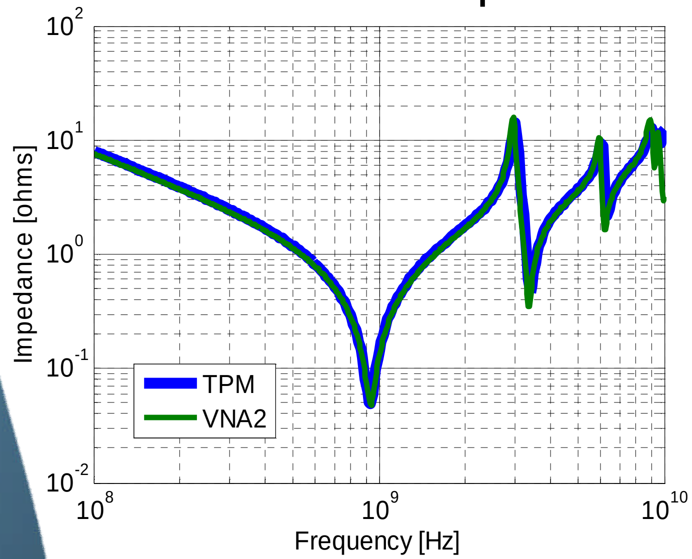




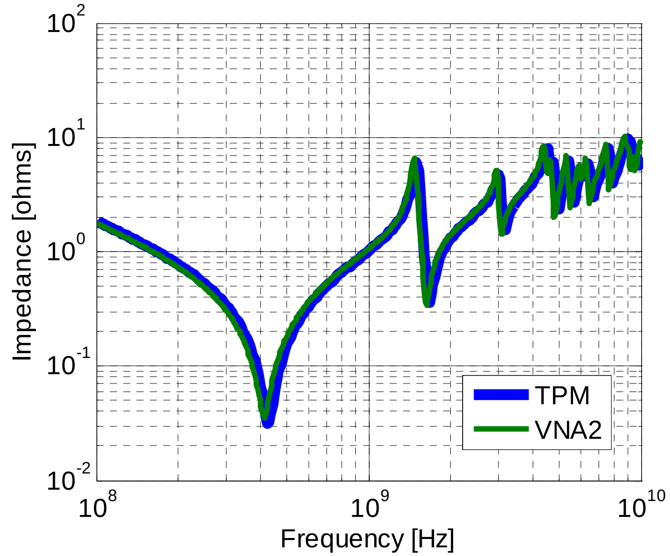
- Planes simulated using TPM
- TPM has a double infinite series, which for practical calculations must be truncated
  - Convergence can be examined by plotting the location of the series resonance and the peak of the parallel resonances
- Simulation time increases as plane size increases and as max frequency increases (to achieve the same level of accuracy)

Correlation studies

0.75 x 1.125 inch plane



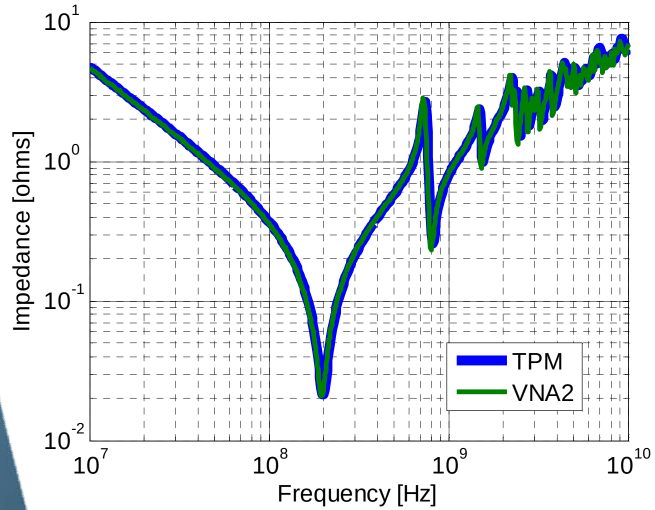
1.5 x 2.25 inch pla



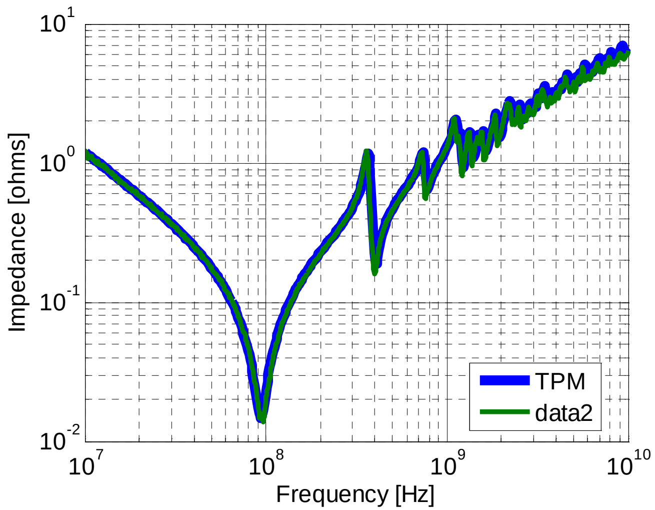
- m,n = 400
- port size = 10 x 10 mil approximating probe footprint

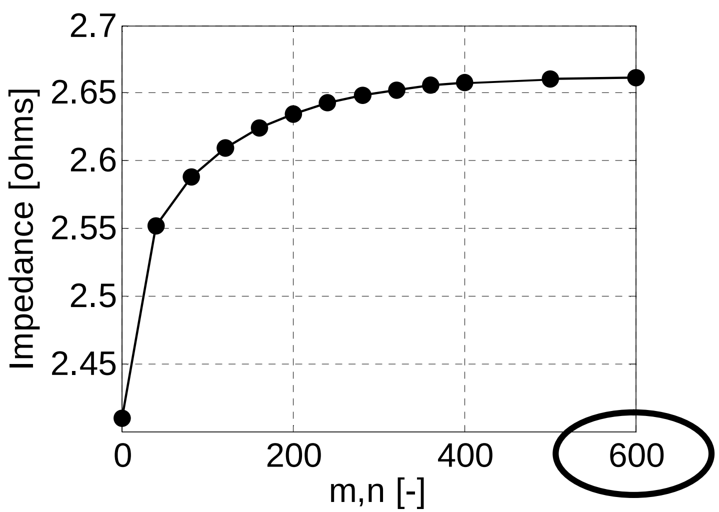
Correlation Studies

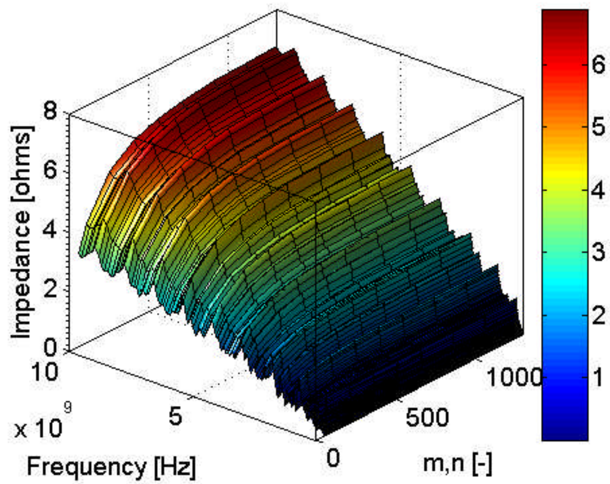
3 x 4.5 inch plane



6 x 9 i







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Conclusions

- Modal resonance suppression is important
  - > to achieve a flat impedance profile
  - > to minimize EMI and radiation
- Previous studies examined how laminate thickness suppresses resonances on average-size computer boards without plane splits
- Plane area is important to consider because due to increased design functionality and decreased form factor, it is shrinking
- Small plane shapes, compared to large boards with the same laminate thickness, can exhibit high Q's due to higher impedance
- Packages, puddles, and dedicated narrow feed rails are examples of planes which may exhibit this behavior

Conclusions

- Here we examined how plane parameters impact modal suppression including:
  > dielectric thickness
  > copper thickness
  > plane area
  > plane aspect ratio
  > Dk and Df
- Mitigating the loss of damping on small planes:
  > Use proportionally thinner laminates to keep pace with the increasing impedance
  > Using thinner metals isn't very effective
  > Higher Dk and Df materials can help but there are practical limitations
  > Avoid shapes that are long and narrow (where the PRF is low and the impedance is high)

Backup Slides

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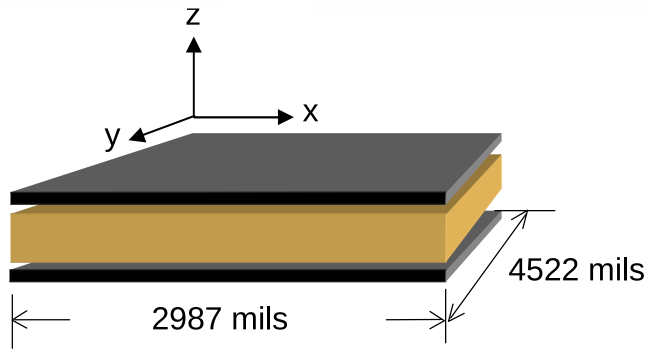
Simulation Accuracy Issues

- Double infinite summations must be truncated

$$Z_{ij}(\omega) = j\omega\mu h \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} \frac{\chi_{mn}^{2}}{w_x w_y \left(k_{xm}^{2} + k_{yn}^{2} - k^2\right)} f(x_i, y_i, x_j, y_j)$$

- What is the impact on accuracy?
- Longest plane dimension requires the most modes
- The relationship is

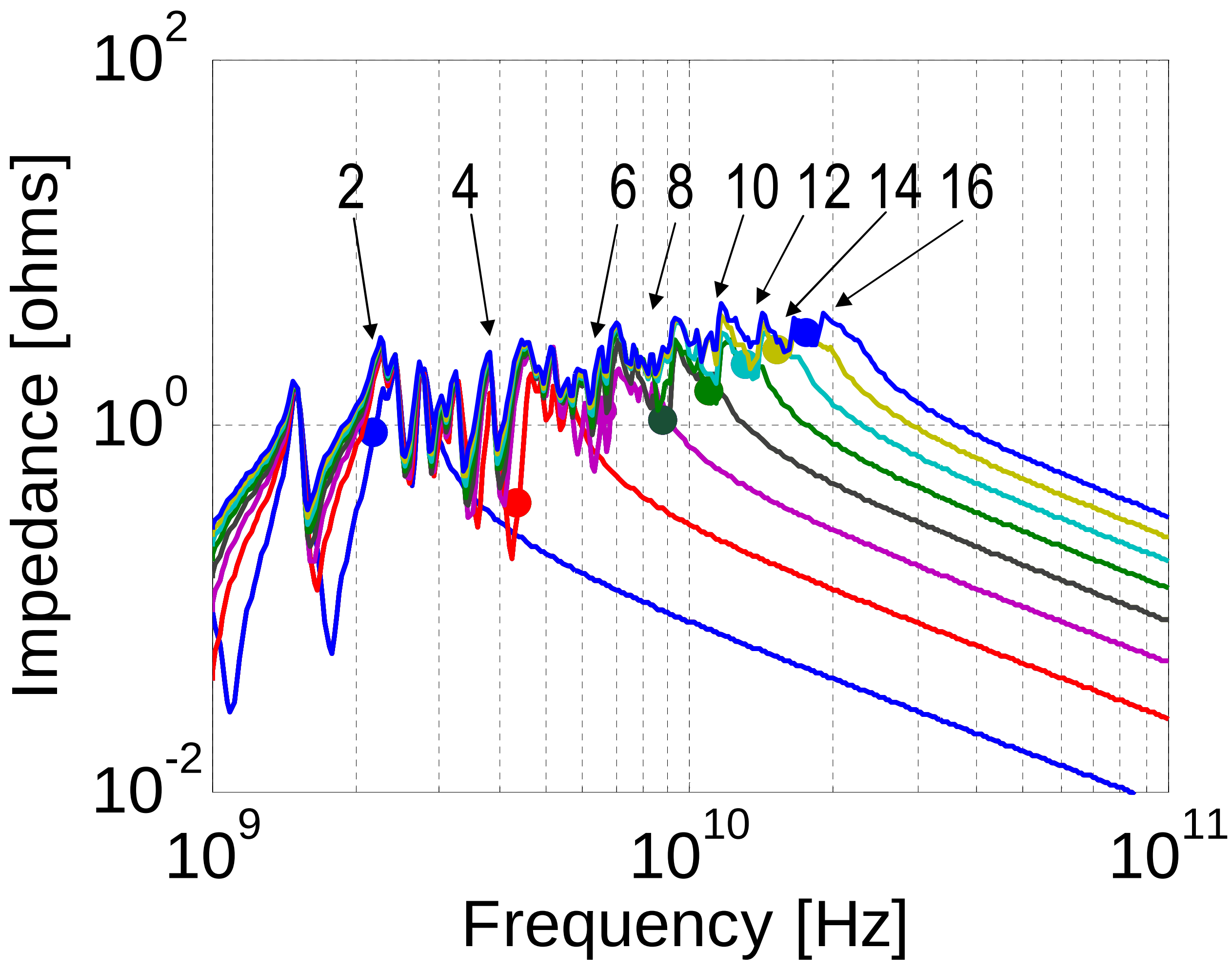
$$f_{\max\_N} = \frac{N}{2a}\frac{c}{\sqrt{\varepsilon_r}}, \qquad f_{\max\_M} = \frac{M}{2b}\frac{c}{\sqrt{\varepsilon_r}}$$



- Test case has Dk=3.27 and Df=2.2% @ 1 MHz, t=2.91
- By this rule, 10 GHz would dictate **m >= 10** for x and **n >= 14** for y

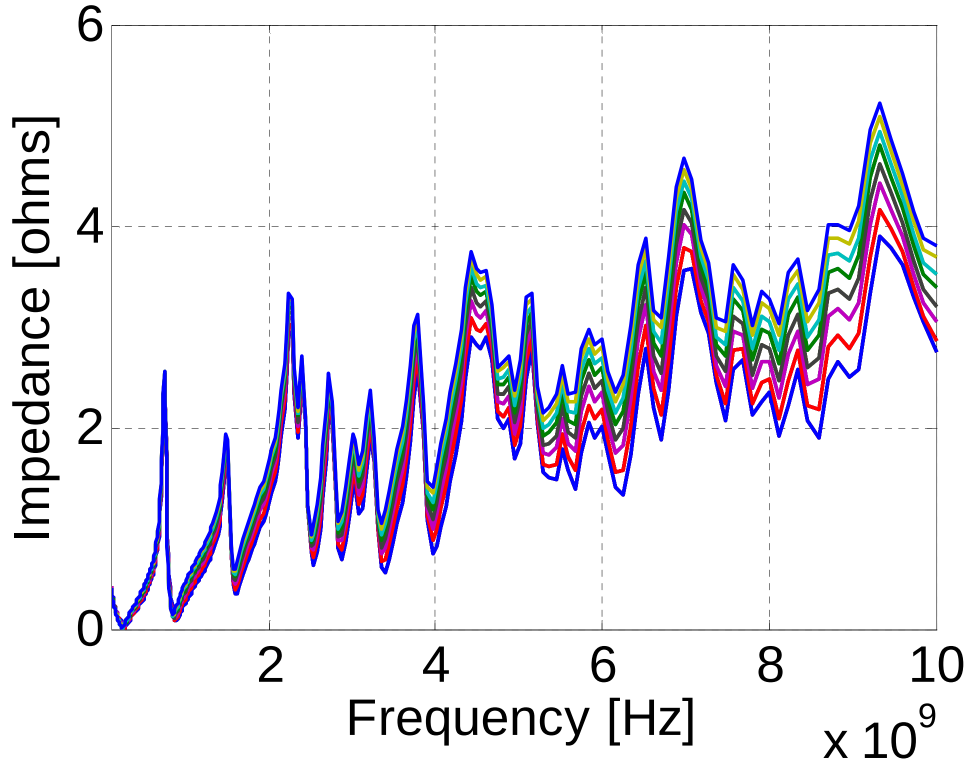
Simulation Accuracy Issues

- Parametric sweep with m,n = 2, 4, 6, 8, 10, 12, 14, 16



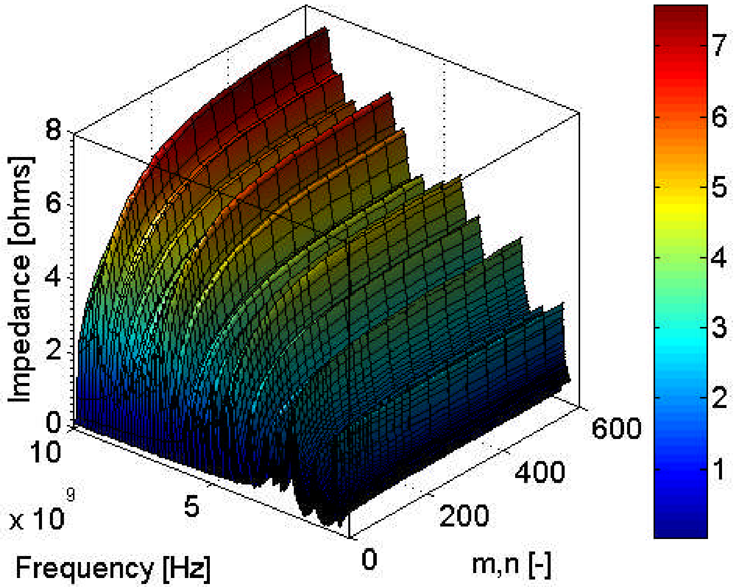
Simulation Accuracy Issues

- Aside from the truncation at high frequencies we observe slow convergence of the frequency minima and the peak impedance values
- Figure below started with the minimum number of modes to avoid truncation (m,n = 15) and increased in steps of 5. Which is correct?
- Notice that there is more spread as the frequency increases



Simulation Accuracy Issues

- Now we increase the number of modes in the following steps: 2, 4, 6, 8, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100, 120, 140, 160, 180, 200, 250, 300, 350, 400, 450, 500, 550, 600
- This plot shows convergence of the resonance peaks as a function of m, n
- There is rapid convergence of the max impedance value at lower frequencies



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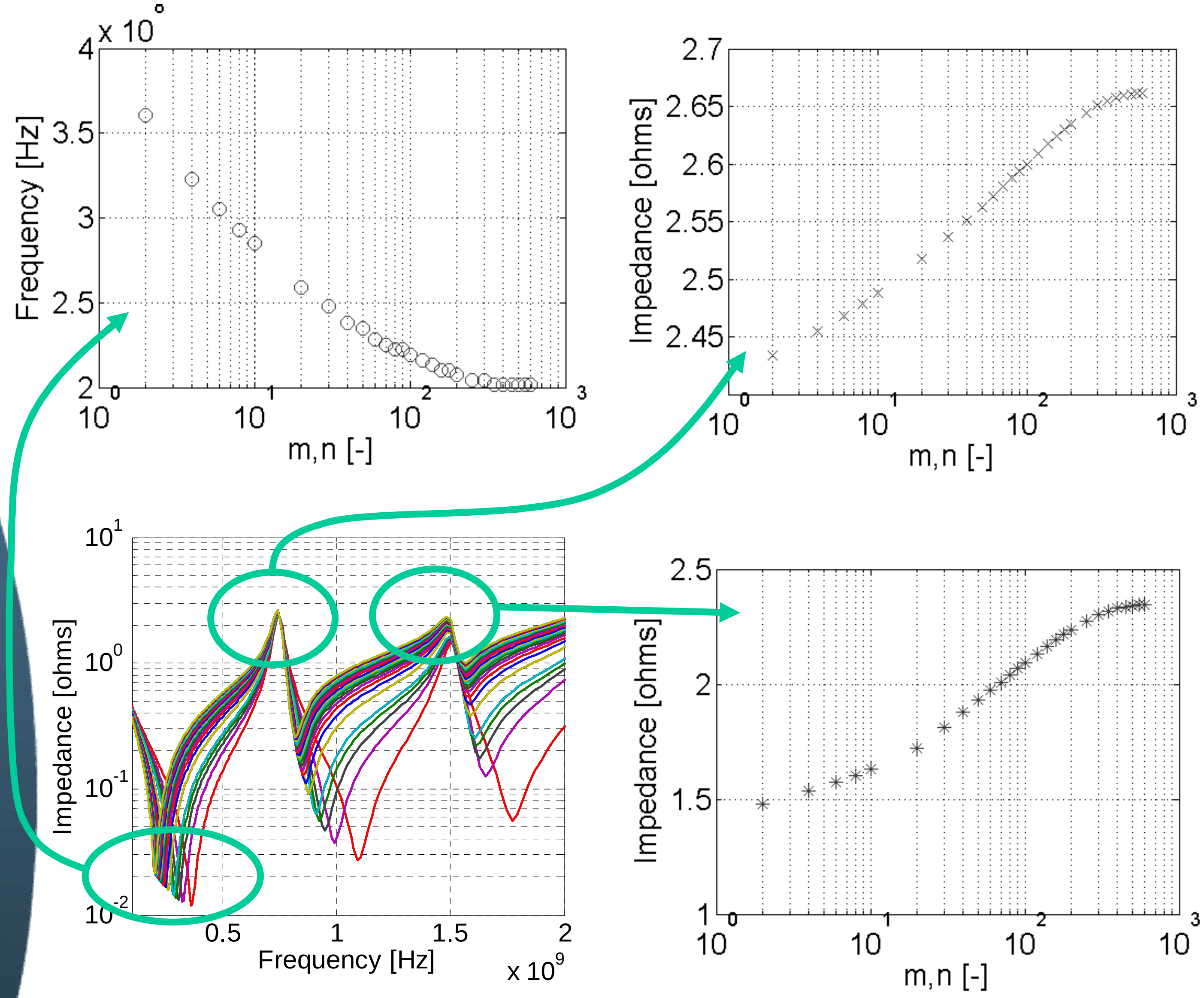
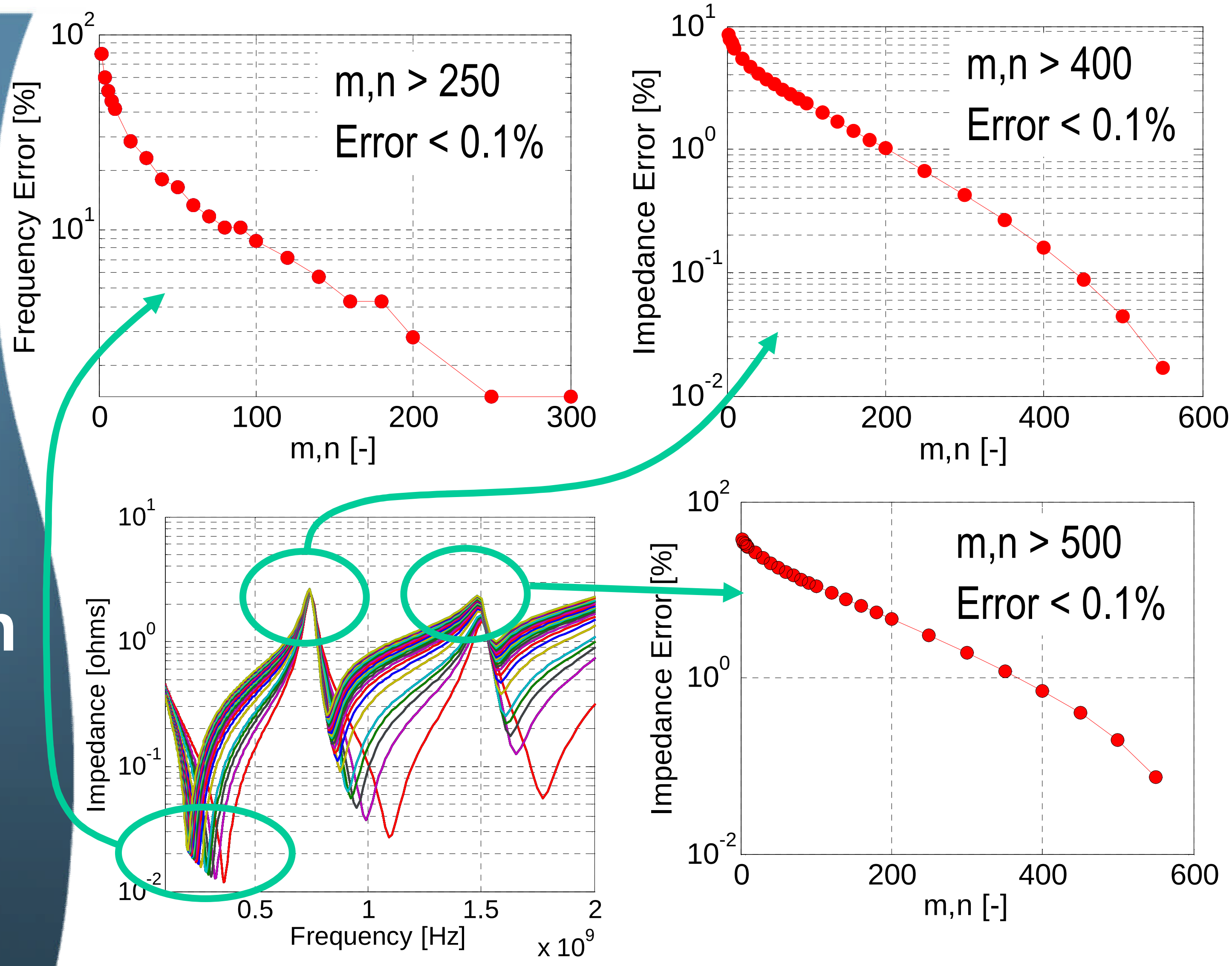


Simulation Accuracy Issues



Summary Points

- Double infinite summations must be truncated which results in some inaccuracy in location of resonances and magnitude
- Must be aware of the following:
  1. Need to have sufficient number of modes to not “truncate” the series. This is determined by the electrical length of longest side.
  2. Need to set m,n based on required accuracy at highest frequency
- General trends with the second issue:
  > More modes are required at higher frequencies to achieve the same accuracy target at lower frequencies

  > More modes are required on larger planes to achieve the same accuracy target of a smaller plane