

DesignCon 2009

Technical panel:

Power Distribution Planes: To Split or Not to Split?

Panelists:

Bruce Archambeault

Eric Bogatin

Michael Steinberger

Madhavan Swaminathan

Istvan Novak*

IBM

Bogatin Enterprises

SiSoft

Georgia Tech

SUN Microsystems

* panel organizer

Abstract

Though the title might suggest that designers have a choice, in today's increasingly dense electronic packaging, we many times do not have the freedom to avoid splitting power distribution planes. Many years ago, splits in planes were rare and were employed primarily to implement some intentional isolation between subcircuits. Such typical scenarios were the splits between analog and digital grounds or isolation between chassis and logic ground. Today the density of trace interconnects drives up layer count in PCBs and packages alike, and the power optimization creates more and more separate power domains. These two factors dictate that we have to reuse power distribution planes by splitting the planes in certain layers to serve multiple circuits. This, however, creates severe routing restrictions if we don't want to cross the splits with signal traces or need to carefully weigh the possible negative consequences in signal distortion, increased crosstalk, mode conversion, and increased radiation and susceptibility. This panel brings together experts from the industry and academia to discuss the various tradeoffs to be considered by package and board designers.

Panelist biographies

Bruce Archambeault, Distinguished Engineer, IBM

Dr. Archambeault leads EMC tool development and use on a variety of products. He has authored or co-authored a number of publications on computational electromagnetics applied to real-world EMC problems and authored the book PCB Design for Real-World EMI Control. Dr. Archambeault is a member of the board of directors of the IEEE EMC Society and past board member of the ACES.

Eric Bogatin, President, Bogatin Enterprises

Dr. Bogatin received his BS in physics from MIT and MS and PhD in physics from the University of Arizona in Tucson. He has held senior engineering and management positions at Bell Labs, Raychem, Sun Microsystems, Ansoft and Interconnect Devices. Dr. Bogatin has written four books on signal integrity and interconnect design and more than 200 papers. His latest book, Signal Integrity-Simplified, was published in 2004 by Prentice Hall. He has taught more than 4,000 engineers in the last 20 years. Many of his papers and columns are posted on the www.BeTheSignal.com web site.

Michael Steinberger, Ph.D., Distinguished Member, Technical Staff, SiSoft

Michael Steinberger, Ph.D., has over 29 years experience designing very high speed electronic circuits. Dr. Steinberger holds a Ph.D. from the of and has been awarded 7 patents. Before joining SiSoft, Dr. Steinberger led a group at Cray, Inc. performing SerDes design, high speed channel analysis, PCB design and custom RAM design. He drove development of methodologies and software at Cray used to successfully design and validate 6+ Gbps serial links.

Dr. Madhavan Swaminathan, Professor, Georgia Tech University

Dr. Swaminathan is the Joseph M. Pettit Professor in Electronics in the School of Electrical and Computer Engineering. He was the deputy director of the Microsystems Packaging Research Center, Georgia Tech from 2004 - 2008. Dr. Swaminathan is the co-founder of Jacket Micro Devices, a leader in integrated RF modules and substrates for wireless applications. Prior to joining Georgia Tech, he was with IBM working on the packaging for supercomputers. He is the author of more than 300 journal and conference publications, holds 15 patents, and is the author of two books entitled "Power Integrity Modeling and Design for Semiconductors and Systems."

Istvan Novak, Distinguished Engineer, SPARC Volume Servers, Sun Microsystems

Dr. Novak is engaged in the design and characterization of power distribution networks and packages for Sun servers. He creates simulation models and develops measurement techniques for power distribution. Dr. Novak has more than 20 years of experience with high-speed digital, RF and analog circuits, and system design. He is a fellow of IEEE for his contributions to the fields of signal integrity, RF measurements, and simulation methodologies.

PCB EMI Effects from Trace Crossing Split Planes

Bruce Archambeault, Ph.D.
IBM Distinguished Engineer
barch@us.ibm.com

Trace Crossing Split Reference Plane

- Known to be 'bad'!
- Often done anyway due to PCB stackup limitations
- Causes SI impact at high frequencies
- Causes EMI impact
 - Additional emissions above board
 - Additional noise between planes
 - Additional noise coupled onto other traces

Quantify EMI Impact

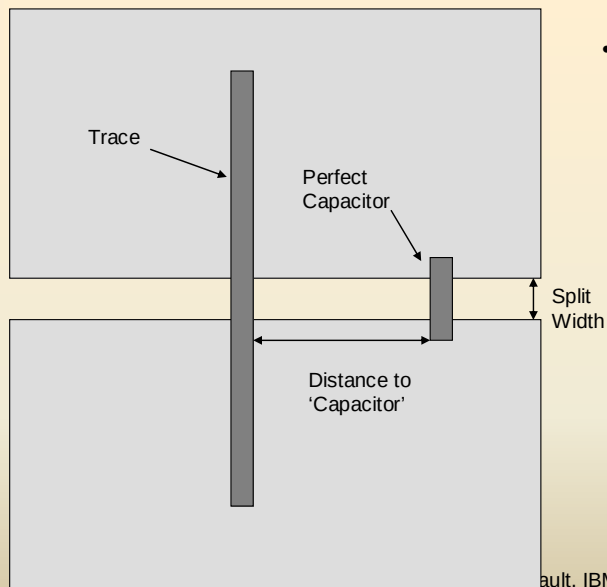
- Use full wave simulations and laboratory measurements
- Find maximum noise across split relative to trace current
 - Use perfect stitching 'capacitor' at varying distance from crossing point
 - Convert to 'transfer inductance' to allow estimation

Feb 2009

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Microstrip Configuration

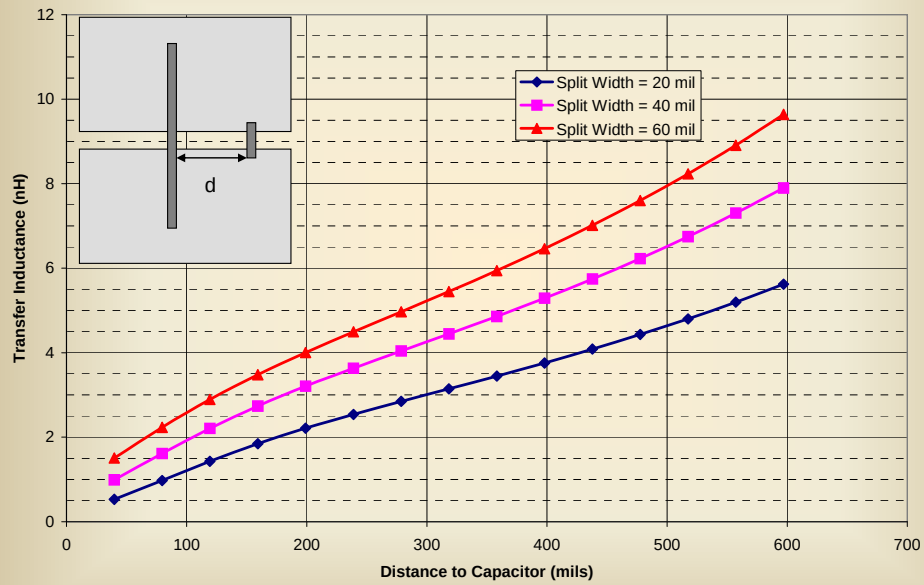


- Also
 - Microstrip with solid plane below split plane
 - Strip line
 - Symmetrical and Asymmetrical
 - Strip line with solid plane below split plane
 - Symmetrical and Asymmetrical

Dr. Bruce Archambeault, IBM

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Estimated Transfer Inductance for Trace Crossing Split Plane
Microstrip Configuration (Valid to 2 GHz)

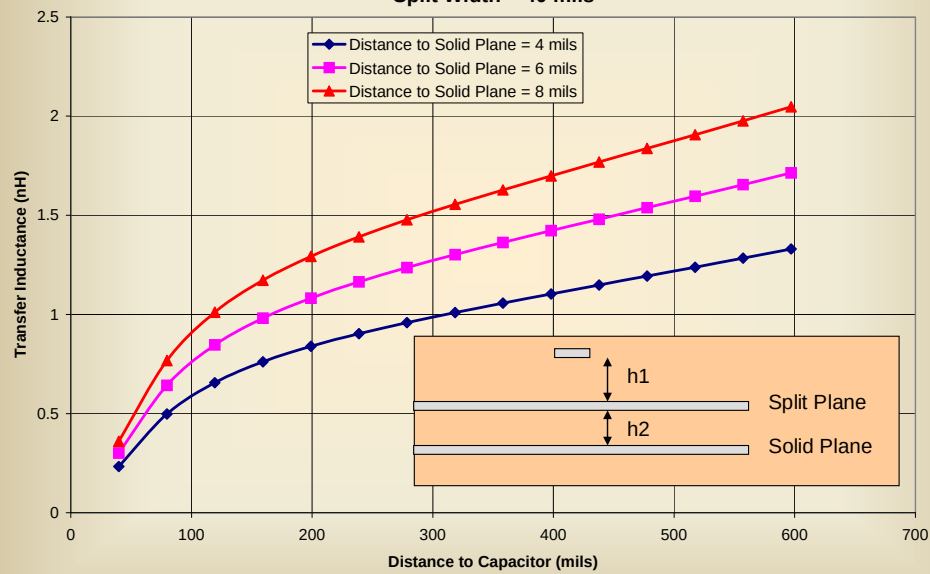


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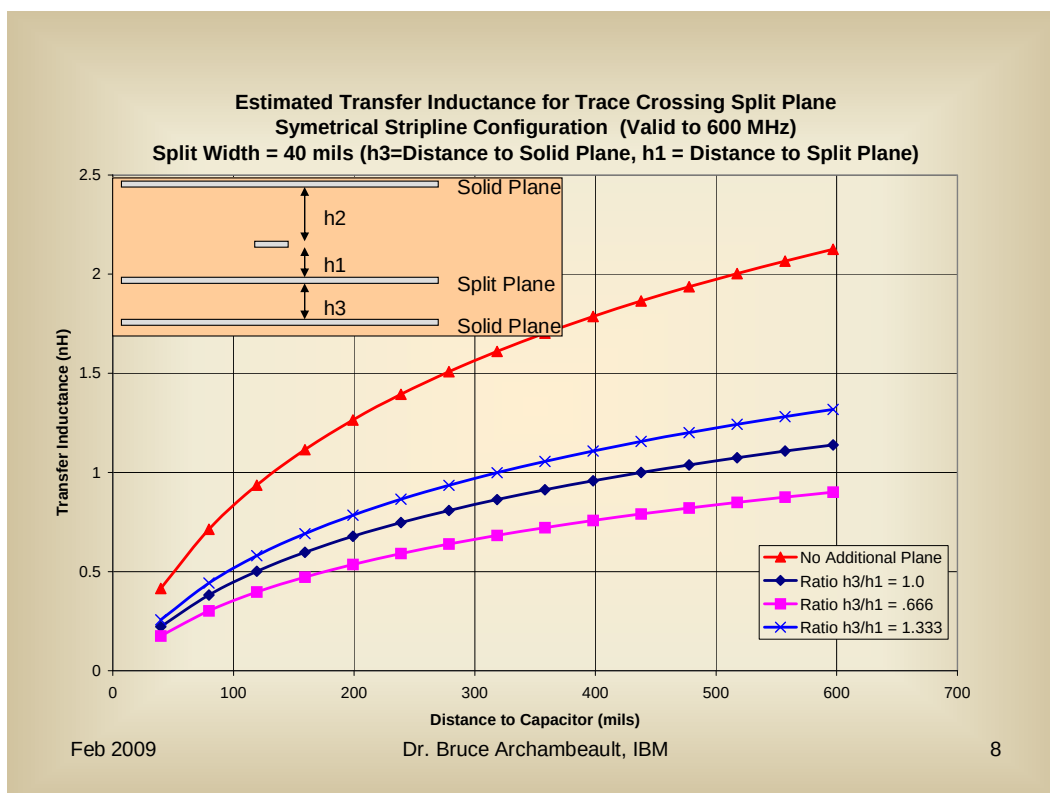
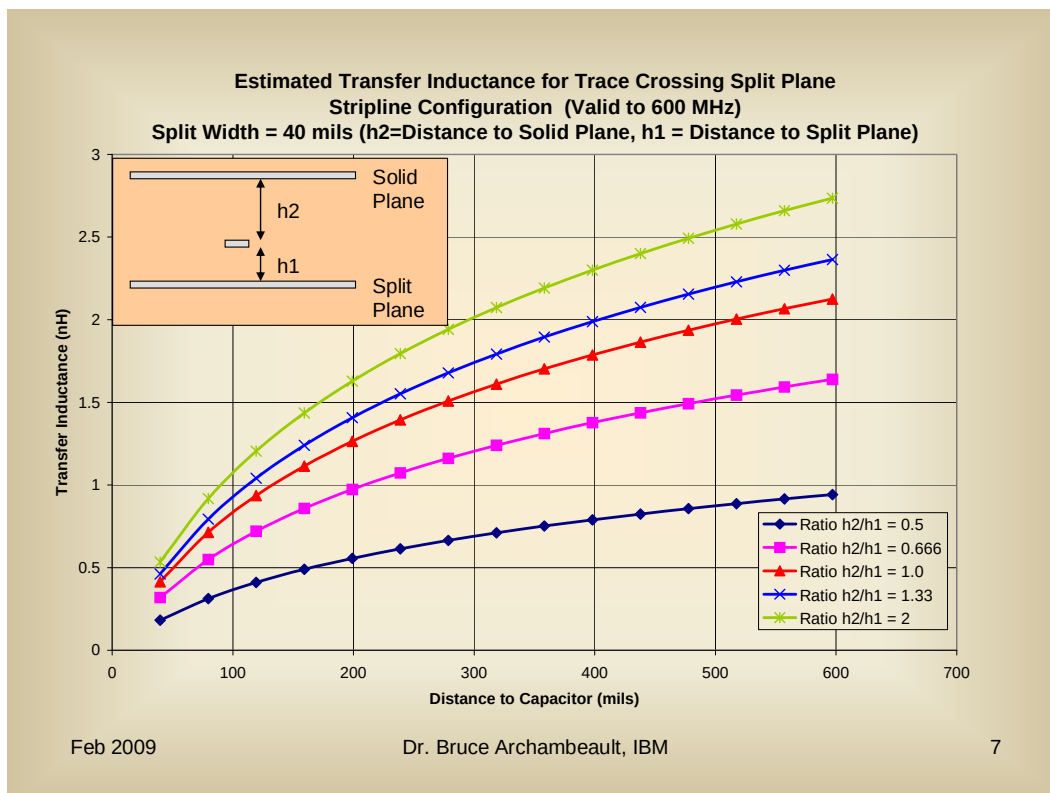
Estimated Transfer Inductance for Trace Crossing Split Plane
Microstrip Configuration with Solid Plane Below (Valid to 400 MHz)
Split Width = 40 mils



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Dr. Bruce Archambeault, IBM

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Summary

- Estimate noise in split for various configurations
 - Additional solid planes below split plane can help a little
- REMEMBER to add inductance of capacitor connection!
- Applies to differential traces as well as single ended traces



Signal Integrity in Kansas

- An important design process:
 - ✓ “be the signal”
- An equally important design process:
 - ✓ “be the return current”
- Engineering the return current to control switching noise and cross talk
 - ✓ Routing the signal path
 - ✓ Adjusting the relative signal to plane spacing



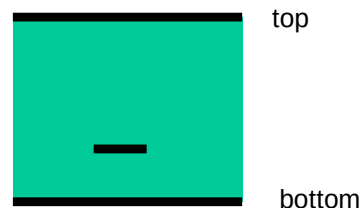
Controlling Return Current in the Adjacent Planes

Symmetrical Stripline



Which plane has more return current?

Asymmetrical Stripline



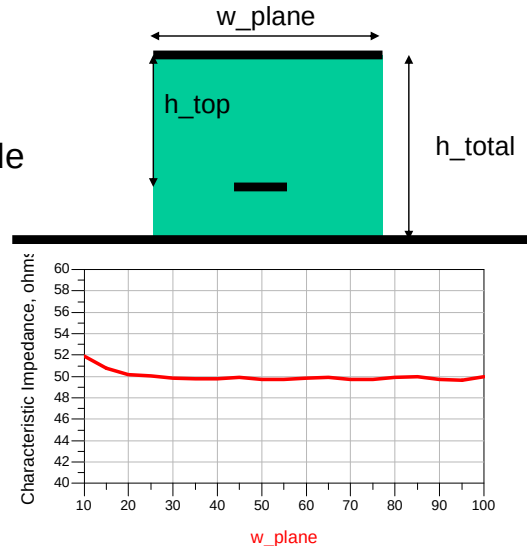
But, how much current is in the top plane?

“it depends”



Using a 2D field solver with integrated circuit simulator

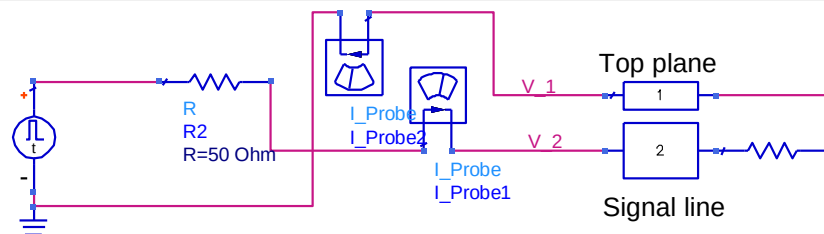
- 3 layer stack up
- Bottom layer is infinite
- Signal line is 10 mils wide
- Top layer is “wide”
 - ✓ How wide is wide enough?



Top plane width should be $> h_{\text{total}}$



Measuring the current in the top plane (using ADS)

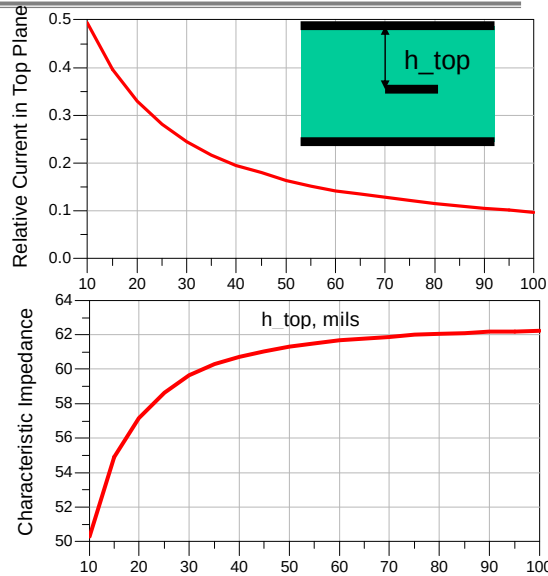


- Drive signal into signal line
 - ✓ Measure the signal current
- Ground top plane
 - ✓ Measure the top plane current
- Current into top plane = $I_{\text{plane}}/I_{\text{signal}}$



Current in Top Plane as Top Plane is Moved Away

- $h_{\text{bottom}} = 10$ mils
- When $h_{\text{top}} > 4 \times h_{\text{bottom}}$, current in top plane is $< 20\%$
- But, what else happens when h_{top} increases?
- What happens to the current in top plane if bottom thickness is adjusted to keep $Z_0 = 50$ ohms?

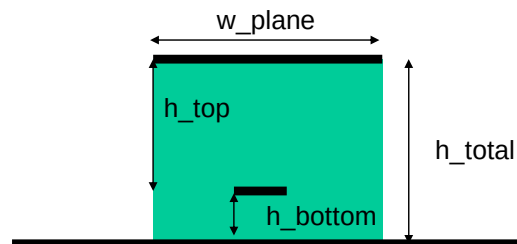


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Adjusting bottom thickness for 50 ohms

"Never do a simulation without first anticipating the result"



To keep $Z_0 = 50$ ohms
As h_{top} increases,

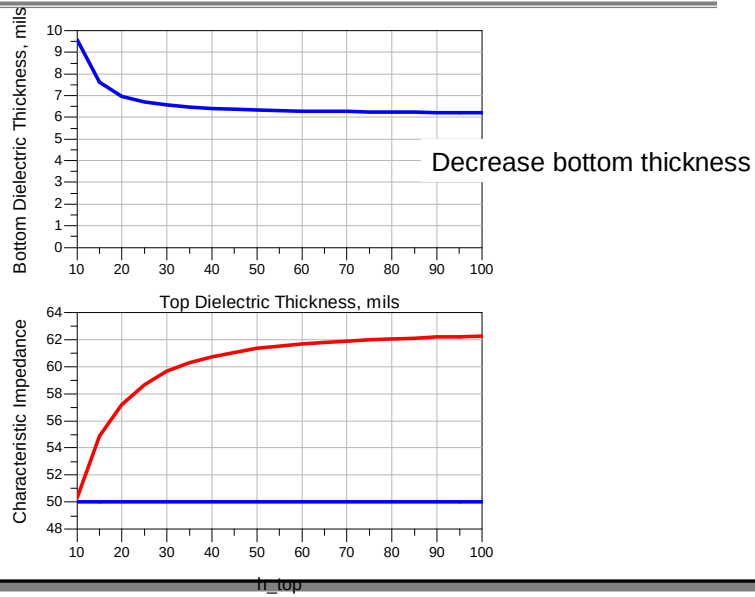
1. What happens to h_{bottom} ?
2. What happens to the current in the top plane?

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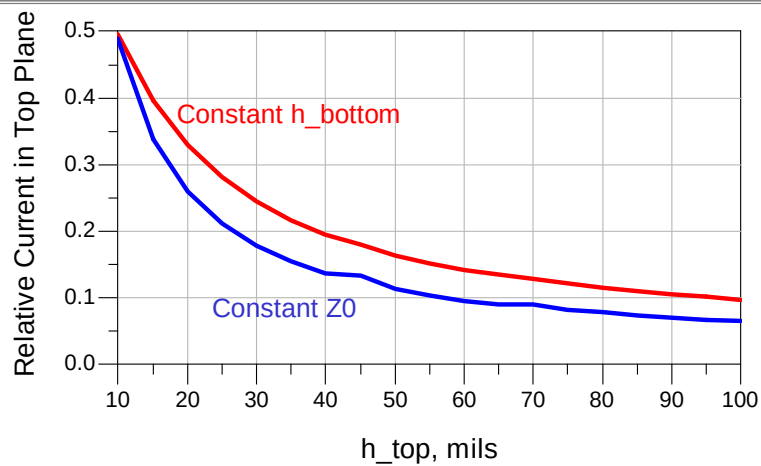
To Keep Constant Impedance



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Current in Top Plane: constant Z_0 , adjusted bottom thickness



Rough rule of thumb: keep $h_{top} > 4 \times w$, for less than 15% current in the top plane

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Summary

- Return current crossing a split plane creates
 - ✓ Impedance discontinuity
 - ✓ Switching noise (ground bounce cross talk)
 - ✓ EMI
- Engineer return current from crossing splits by
 - ✓ Routing signal paths around split return planes
 - ✓ Keeping spacing to split plane $> 4 \times$ line width
- Is it enough?
 - ✓ It depends on each design
 - ✓ Evaluate with simulation

Split Planes: Do You Know Where Your Ground Currents Are?

Mike Steinberger

1.0 General Remarks

This narrative is written in response to the question as to whether or not one should use split planes in PC board designs. On the one hand, PC boards tend to have many separate power domains, either because different devices on the board use different supply voltages, or because sensitive devices such as clock distribution devices should be isolated from the rest of the board by three terminal power regulators. On the other hand, modern PC boards tend to have a lot of high speed serial channels on them, and splits in the power planes can disrupt the propagation of these signals, or cause EMI problems.

The short answer to this question is: “If the design can meet performance requirements with split planes, and split planes will reduce product cost, then by all means, use them. Otherwise, don’t.”

The cost part of this statement is easy enough to evaluate, but the performance part is a bit harder. The impact of split planes on performance is not necessarily well understood, and so it can be hard to decide whether or not that impact is acceptable. The underlying difficulty is that the split affects the ground currents, and it’s not always clear where the ground currents are going.

The purpose of this narrative, therefore, is to describe where the ground currents are actually going, to suggest analytic approaches which can evaluate the ground currents correctly and accurately, and to suggest what types of performance impacts should therefore be considered.

2.0 Decaps? F’get about ‘em.

Years ago, the conventional wisdom was that the ground currents around split planes somehow made their way back to the decoupling capacitors. I confidently and authoritatively said such a thing as little as five years ago. Trouble is, this statement is only valid at tens of MegaHertz. At higher frequencies, the ground currents can find other paths that are lower impedance.

Experimental evidence for this assertion can be found in Dr. James Weaver’s Ph. D. dissertation [1]. Using very small loop probes, Jim measured the power supply currents on individual vias in the power/ground via field of a complex IC. What he found was that the power/ground planes distributed the DC currents among the vias fairly well, they had only a very small effect on current sharing between even closely spaced adjacent vias at frequencies as low as 10 MHz. What he observed was that the

current going to a de-coupling capacitor attached on the back side of the board to a given pair of vias was almost exactly equal to the current on those vias, and was unrelated to the current on adjacent vias.

While it is true that the impedances in a power distribution system are quite low compared to the impedances in a high speed serial channel, it is also true that the via spacing in Jim's measurements was much smaller than would be practical for decoupling capacitors trying to stitch across a split in a power/ground plane. We're presenting a paper [2] at this conference which demonstrates with measured data that the effect of a ground via is approximately inversely proportional to the number of wavelengths of distance between the signal via and the ground via, and that at more than a quarter wavelength distance, the ground via has essentially no effect at all.

The net result is that by the time you take the parasitics associated with mounting the de-cap into account, decaps are only important at relatively low frequencies.

3.0 Other Ground Paths

3.1 Split plane with microstrip: a slot antenna

Suppose that a microstrip crosses a split in a ground plane as shown in Figure 1.

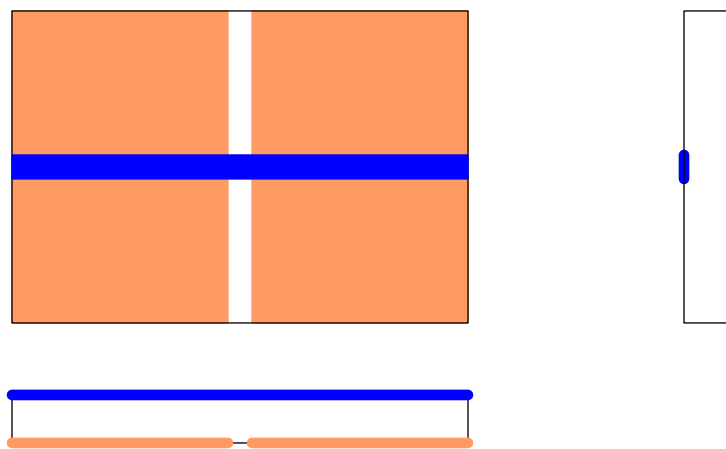


Figure 1: Mechanical drawing of microstrip crossing split plane

One would suppose that in this case, the split in the ground plane would result in a completely open circuit, with all of the ground current reflected back toward the signal source. At DC that's clearly the case; however, at higher frequencies, other things can happen.

The fact of the matter is that some RF engineers call the structure in Figure 1 a slot antenna, and they build them on purpose to efficiently couple the energy on the microstrip at some frequency into the atmosphere. So, at some frequency the ground impedance across the split plane could very likely be

comparable to the impedance of the transmission line and some appreciable signal energy could flow across the split. I expect to have measured data on such a structure in time for DesignCon2009. The ground ground currents might look something like Figure 2.

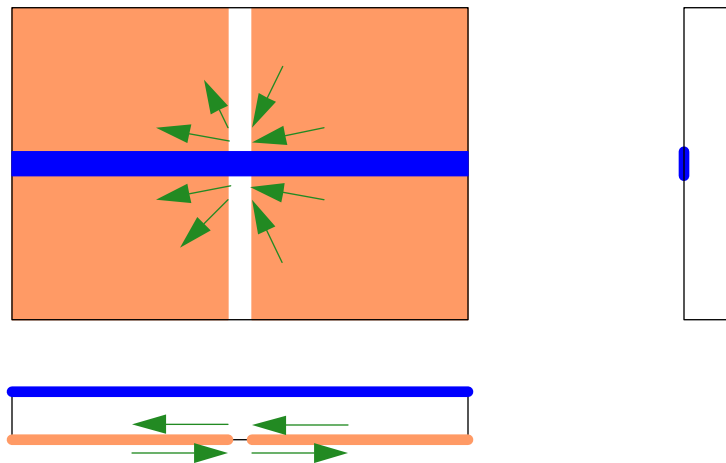


Figure 2: Mechanical drawing of microstrip ground currents crossing split plane

Note that in general ground currents will flow on both the top and bottom of the ground plane, and that they will be anti-symmetric with respect to the split.

3.2 Split plane on top of continuous plane: radial TEM modes

Suppose that the structure in Figure 1 is augmented with another ground plane underneath the split, as shown in Figure 3.

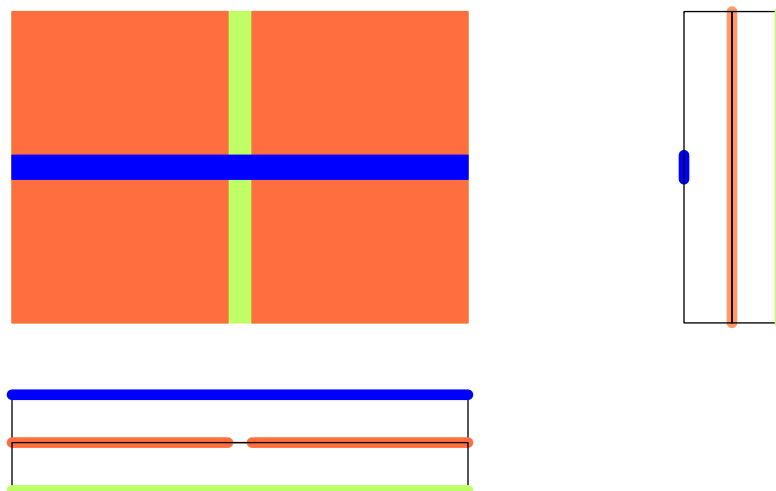


Figure 3: Mechanical drawing of microstrip crossing split plane over continuous plane

The adjacent plane alters the physics of the structure quite substantially. Note, for example, that there will be a considerable capacitance between each side of the split plane and the ground plane underneath it. At low frequencies, the capacitance on each side will behave as a lumped capacitance, and the two capacitances are connected in series by the adjacent ground plane. Especially if the adjacent plane is close to the split plane, and if there is a lot of overlap area on each side of the split, the ground impedance will be quite low, and most of the ground current will follow that path. This situation is illustrated in Figure 4.

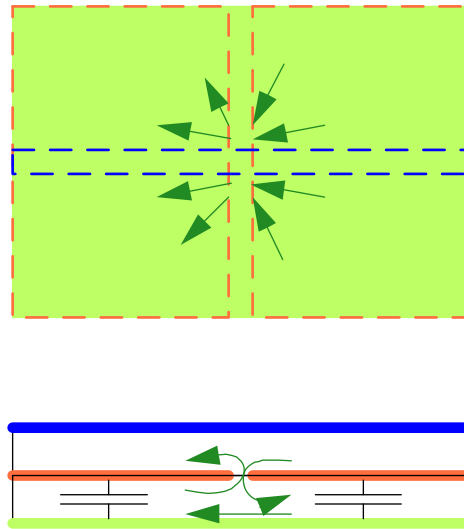


Figure 4: *Ground current path for microstrip crossing split plane over continuous plane*

At higher frequencies, the ground plane capacitances will cease to behave as lumped circuit elements, and there will be frequencies at which they resonate as open circuits. These resonances and the coupling to them can be analyzed very effectively on the basis of radial TEM waves. [2] describes both circumferentially symmetric TEM waves associated with a single ended via and circumferentially varying radial TEM waves associated with differential vias. The radial TEM waves associated with the structure in Figure 3 will be antisymmetric with respect to the split, and will therefore be of the circumferentially varying type.

3.3 Split plane with stripline: radial TEM modes, but weaker

If another ground plane is added to the structure in Figure 3 on the other side of the transmission line, as shown in Figure 5, then the transmission line becomes stripline rather than microstrip.

One clear advantage of this structure is that only half the ground current needs to cross the split plane, thus cutting the effect of the split in half. The half of the ground current that still has to cross the split will follow the path shown in Figure 4.

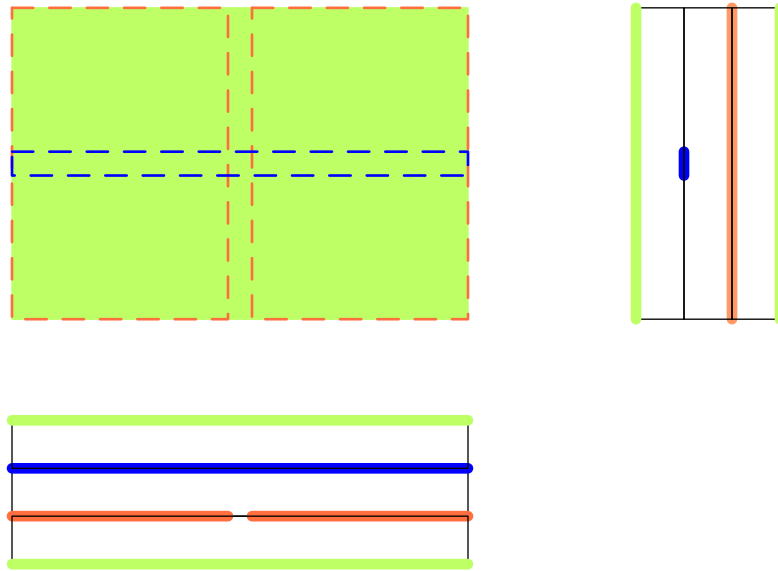


Figure 5: Mechanical drawing of stripline crossing split plane over continuous plane

One remaining detail is that the fields at the split will not be completely symmetrical, resulting in a small voltage between the split plane and the upper ground plane. This will generate antisymmetrical radial TEM waves similar to those depicted in Figure 4, only with much smaller amplitude. These waves should still be accounted for in the PC board's EMI solution.

3.4 Split plane with differential pair

Any of the above structures could be used with a differential pair rather than a single ended transmission line. For the sake of clarity, we will show a differential version of the structure in Figure 6.

When the differential pair is driven in differential mode, the ground currents nearly cancel each other out, with the degree of cancellation dependent on the number of wave-lengths by which the two traces are separated. For separations up to a tenth of a wave-length, the cancellation of ground currents is quite good, and there is still some useful cancellation at a quarter wavelength. Most differential pairs have a much smaller spacing than that. Figure 7 depicts this cancellation.

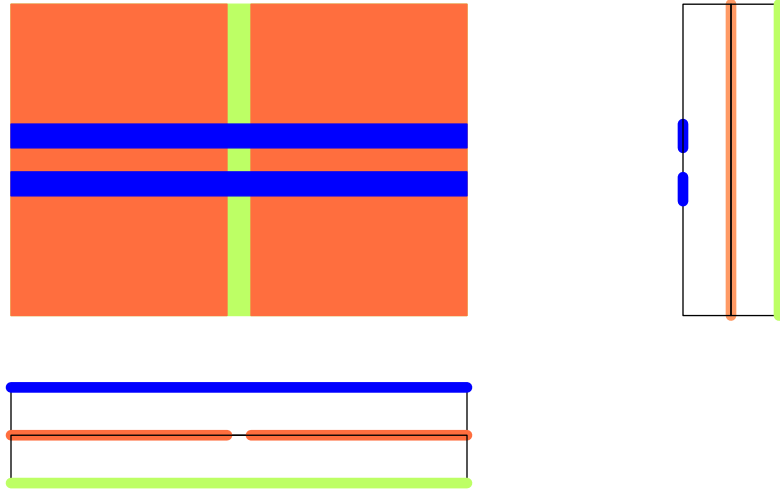


Figure 6: Mechanical drawing of differential pair crossing split plane over continuous plane

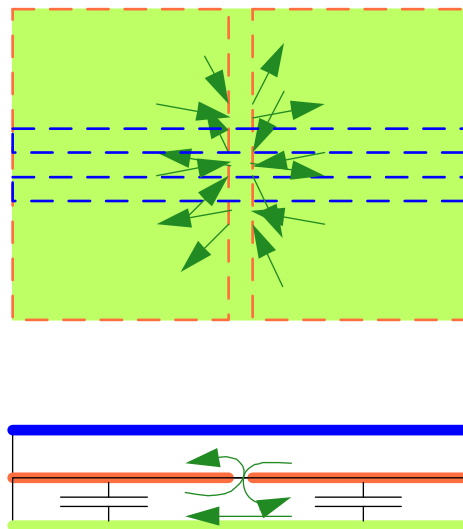


Figure 7: Ground current cancellation for differential pair crossing split plane over continuous plane

In short, a split plane will have very little effect on a different pair.

4.0 Crosstalk Considerations

For single ended signals, split planes can be a significant source of crosstalk due to the common ground impedance they introduce into adjacent traces. Figure 8 shows the crosstalk measured between the two sides of a differential via, as reported in [2].

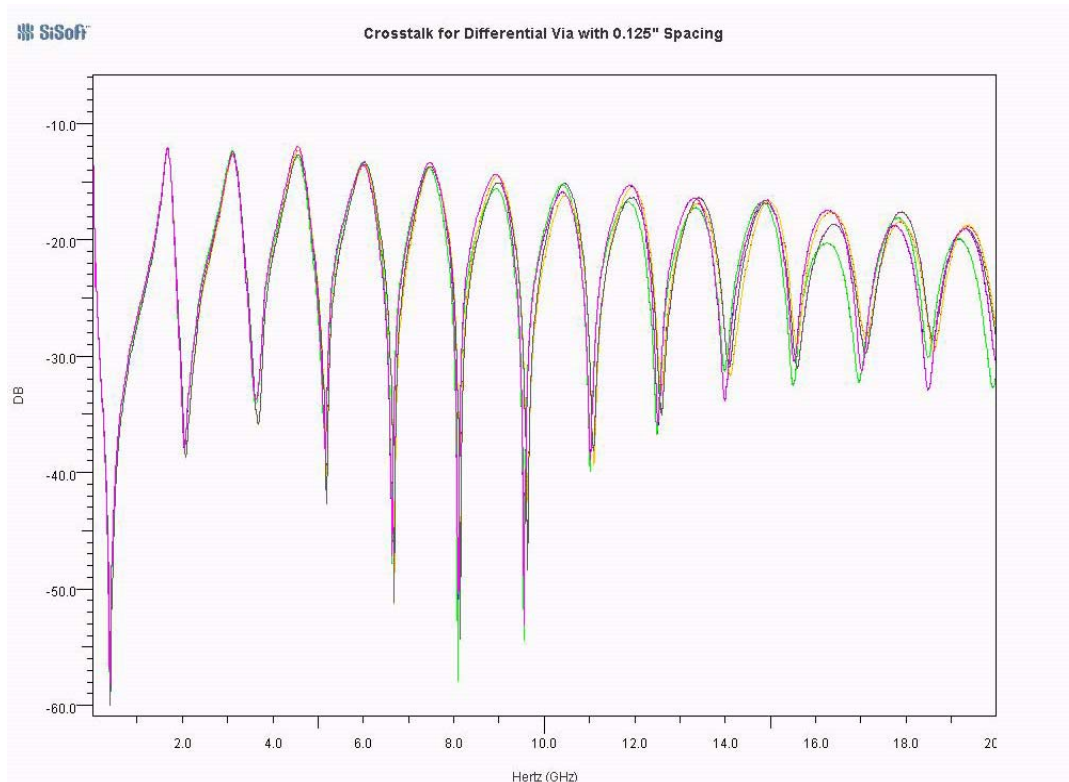


Figure 8: Measured crosstalk between adjacent vias

The vias in this measurement were separated by twice the dielectric thickness.

This measurement was made for a structure which is different from a split plane, and so the actual crosstalk for the split plane will be different in detail; however, this measurement does serve to illustrate the amount of crosstalk that can be generated by the common ground impedance introduced by radial TEM waves propagating between parallel planes. In point of fact, the structure measured for Figure 8 produces circumferentially symmetric TEM waves, which introduce a lower impedance than the circumferentially asymmetric waves produced by a split plane. Thus, the crosstalk for adjacent traces crossing a split in a plane will most likely be greater than that shown in Figure 8.

One of the steps that can be taken to reduce the crosstalk between adjacent single ended traces is to make them not quite so adjacent; that is, increase their separation. For distances which are small compared to a wavelength, the radial TEM waves fall off as the inverse of the distance, and so the crosstalk should fall off at about the same rate. Thus, increasing the separation by a factor of four should reduce the crosstalk by about 12dB. Given that the data in Figure 8 more or less represents a trace spacing of twice the dielectric thickness, it is reasonable to expect that a trace spacing of eight to ten

times the dielectric thickness would be required to get an isolation significantly greater than 24dB, which is the minimum isolation digital signals require in a practical system.

5.0 EMI Considerations

Let's start by disposing of the case of a microstrip with a split plane and no other planes in sight. This is simply a bad idea. Microstrip radiates anyway, and adding a slot antenna created by the split in the ground plane will make the radiation a great deal worse. Regardless whether or not the board is OK when tested on top of the bench, what you've done is to make the entire equipment enclosure part of your electrical design, which means that the behavior will change whenever a door or cover is opened, or PC board spacing changes, or different PC boards get placed next to each other, or Mother Nature simply decided to get creative. DON'T DO IT.

For single ended paths for which the ground return path is completed by radial TEM waves, there will be some signal distortion created by the split plane, but it will be a relatively small impairment. I still recommend against microstrip because the equipment enclosure still becomes part of your electrical design, but if you use stripline, the total signal impairment should be quite tolerable.

There remains, however, the question of EMI compliance. If there is no shielding at the edge of the board, then the radial TEM waves will generate some radiation there, and that radiation could very well exceed requirements. As described in H. W. Ott's classic book [3], however, shorting out the fields at regular intervals using ground vias will be effective in suppressing the radiation. The way this works is actually a little more complex than is described in Ott's book. What happens is that in response to the radial TEM waves, the ground vias reflect a wave which cancels out the electric field near that via. That cancellation will remain effective up to about an eighth of a wavelength from the ground via. Therefore, if ground vias are placed about a quarter wavelength apart around the periphery of the board, the electric field at the edge of the board should be fairly well suppressed.

Within the board, one might also wonder whether the split plane will generate unacceptable crosstalk. The answer is the same as for vias related to decoupling capacitors. The coupling between signals at a split plane goes as the inverse square of the number of wavelengths between signals. Thus, except for very sensitive nets such as clocks, crosstalk should only be a consideration for nearest neighbor nets.

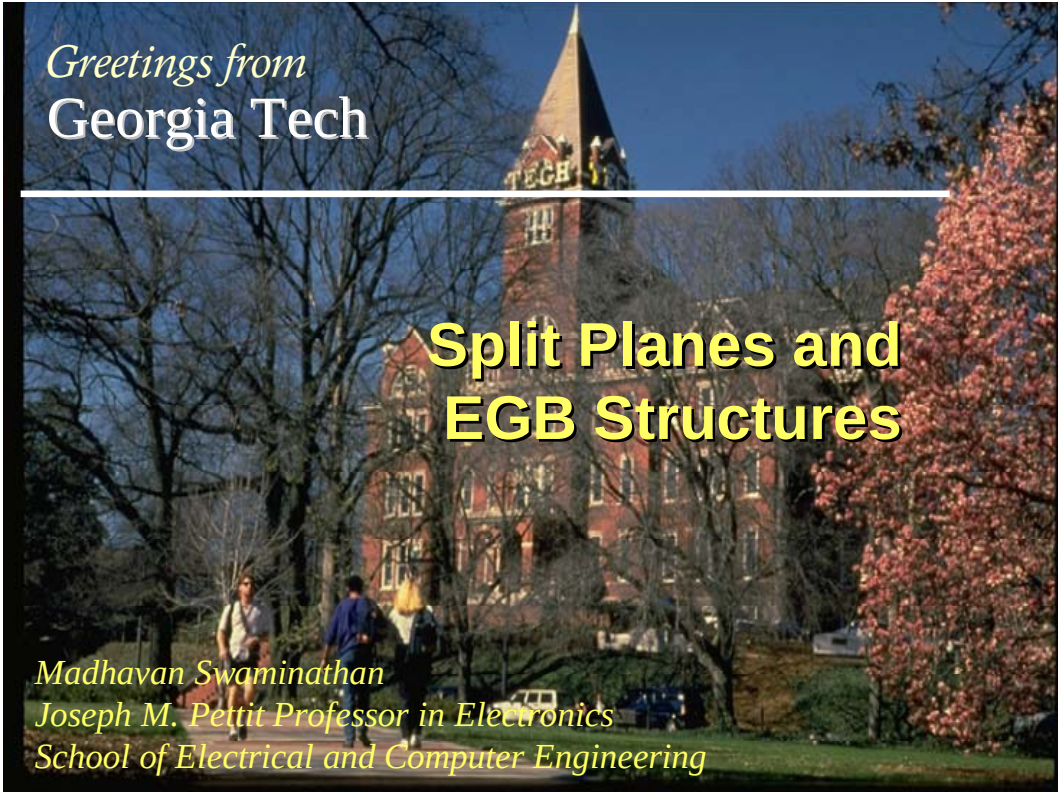
If the design uses differential pairs, the situation becomes very much better. In this case, the suppression of radial TEM waves goes as the inverse of the number of wavelengths between the true and complement side, and is therefore effective until the two sides are more than a quarter wavelength apart. For most designs, this will provide ample suppression of crosstalk and EMI for all frequencies of interest. It's still a good idea to stitch the edge of the board with ground vias, but this is more a matter of cheap insurance rather than a critical design requirement.

6.0 Recommendations

1. Don't use microstrip for any high frequency signal, ever. Power supplies and control signals are OK.
2. For each split, provide a complete overlap with as much area as possible on adjacent ground planes.
3. Stitch the edges of the board with ground vias less than a quarter wavelength apart at the maximum frequency of interest.
4. If single ended traces cross a split in the ground plane, try to minimize crosstalk by spacing them as far apart as possible where they cross the split. A spacing of at least ten times the ground plane spacing is strongly recommended.
5. Whenever possible, use differential traces to cross a split plane.

7.0 References

- [1] James Weaver, Measuring Supply Currents in Printed Circuit Boards, Doctoral Dissertation, Department of Electrical Engineering, Stanford University, November 2007.
- [2] C. Ding, D. Gopinath, D. Searce, M. Steinberger, D. White, "A Simple Via Experiment", DesignCon2009.
- [3] H. W. Ott, Noise Reduction Techniques in Electronic Systems, second edition, John Wiley and Sons, copyright 1988.



*Greetings from
Georgia Tech*

Split Planes and EGB Structures

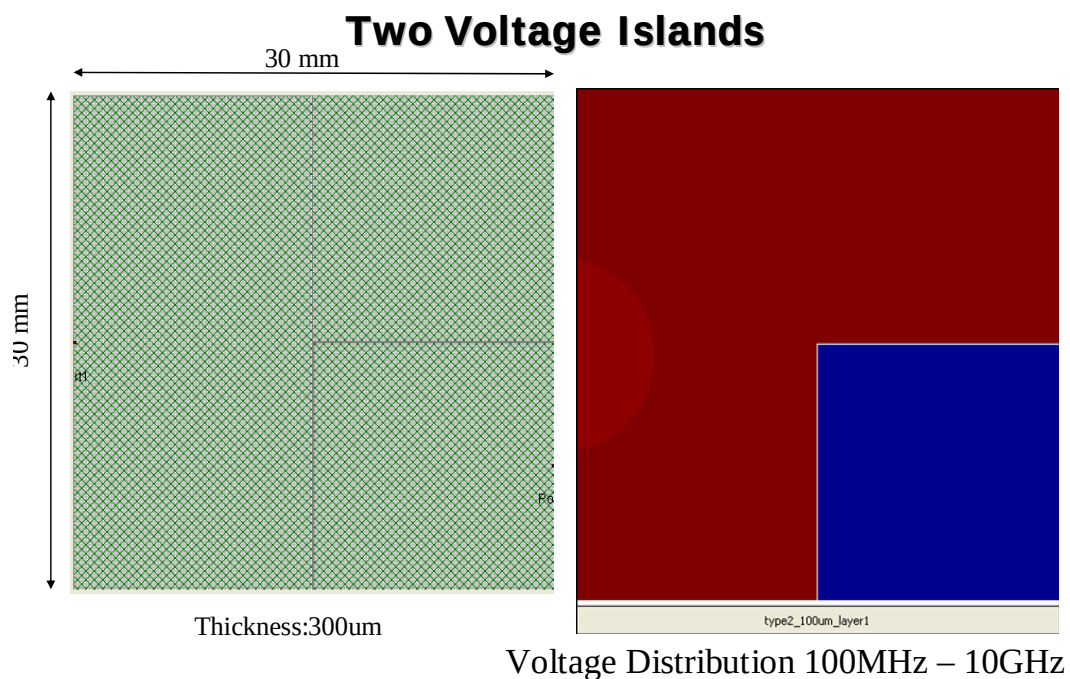
*Madhavan Swaminathan
Joseph M. Pettit Professor in Electronics
School of Electrical and Computer Engineering*

Questions to be answered

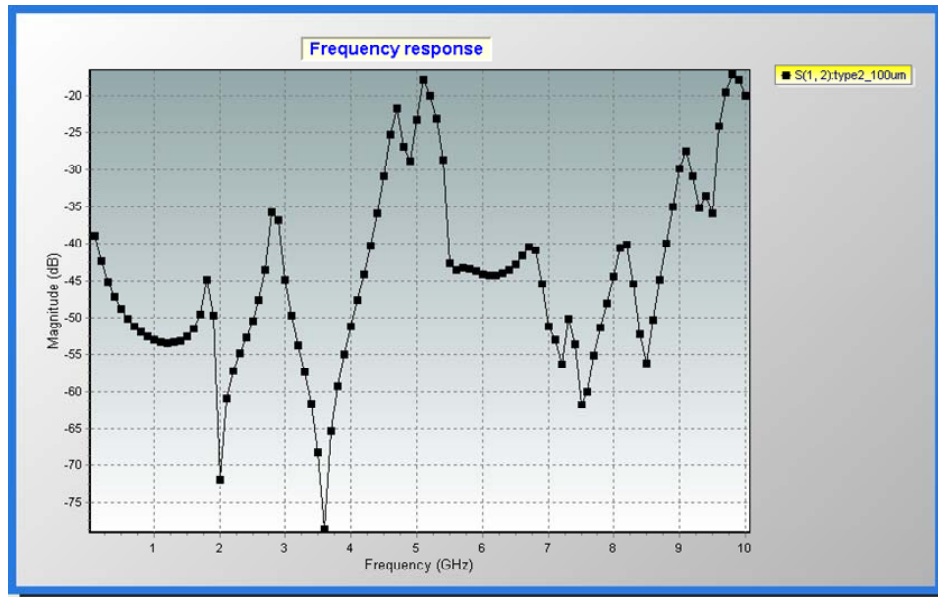
- ☐ Can planes be decoupled by splitting them ?
- ☐ What is the source of coupling between split planes ?
- ☐ Can structures be developed that help decouple split planes ?

Coupling between Voltage Islands

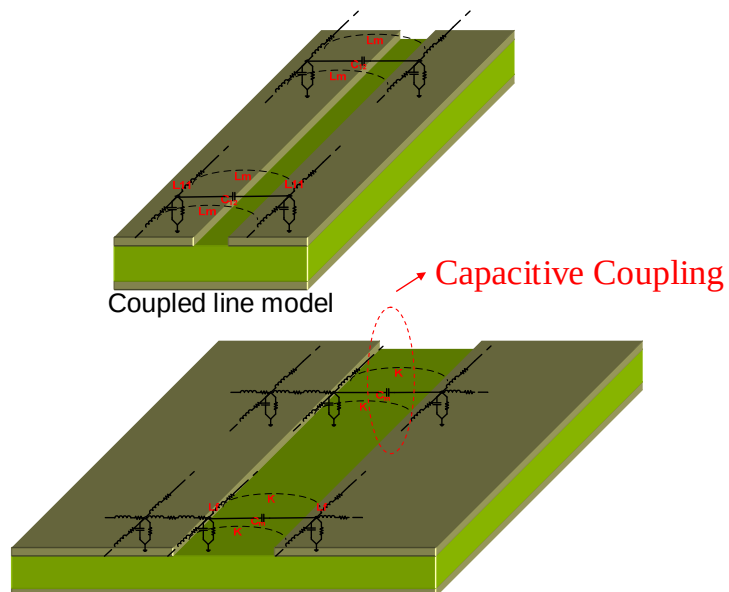
An Example



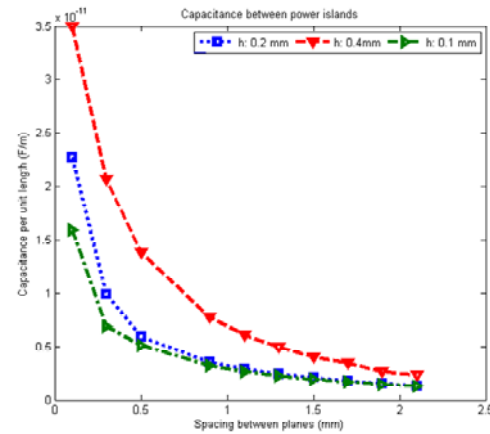
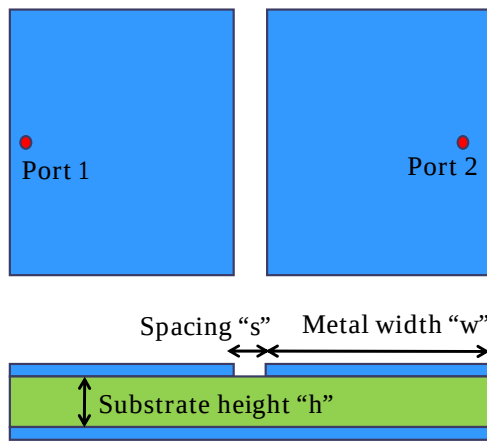
Coupling between Voltage Islands (S12)



What Causes Coupling Across Slots ?



Design Parameters Affecting Coupling

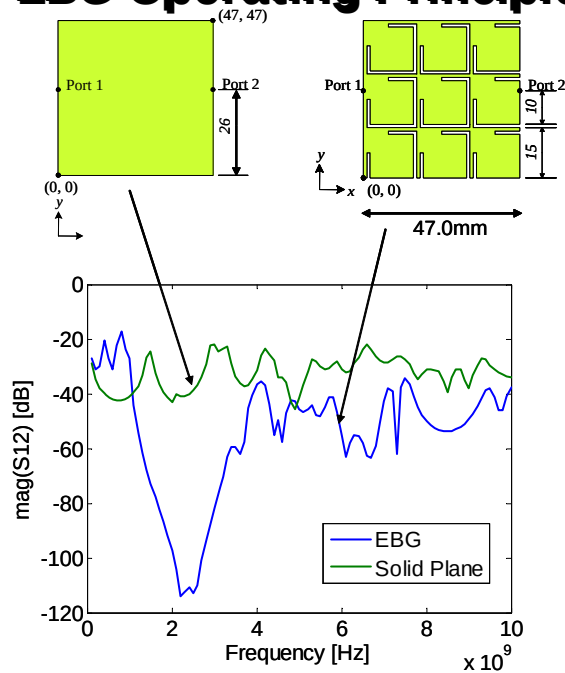


Coupling Capacitance strongly related to the ratio s/h

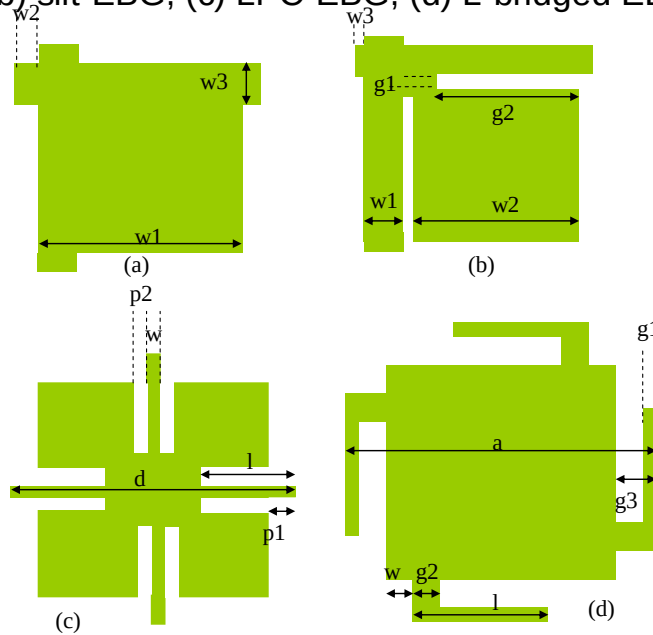
EBG Structures for Shielding in Split Island Designs

Case Study: Load Board for Testing ADC ICs

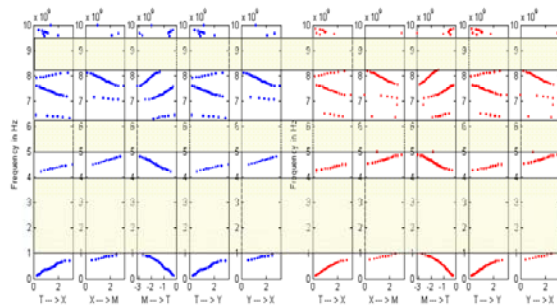
EBG Operating Principle



Examples of two-layered EBG unit cells: (a) AI-EBG, (b) slit-EBG, (c) LPC-EBG, (d) L-bridged EBG

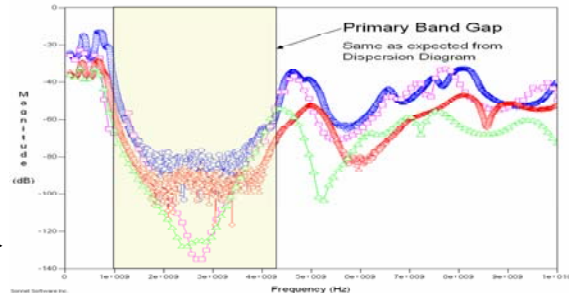


Design of EBG Structures



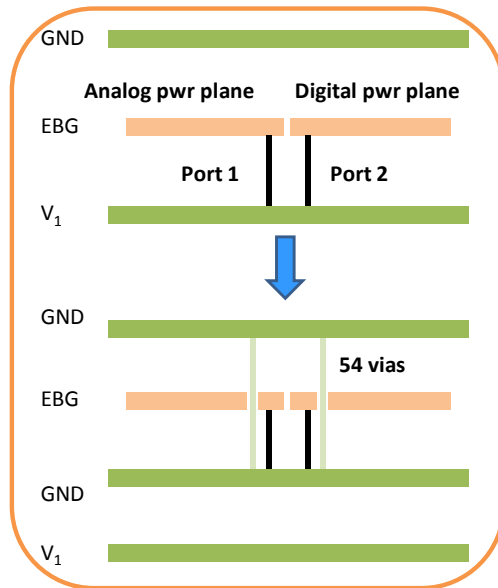
o Dispersion Diagram to determine shape of unit cell

o S-Parameters to determine number of unit cells



Dispersion Diagram – FR4 and Scaled BC16T

Layer Modification



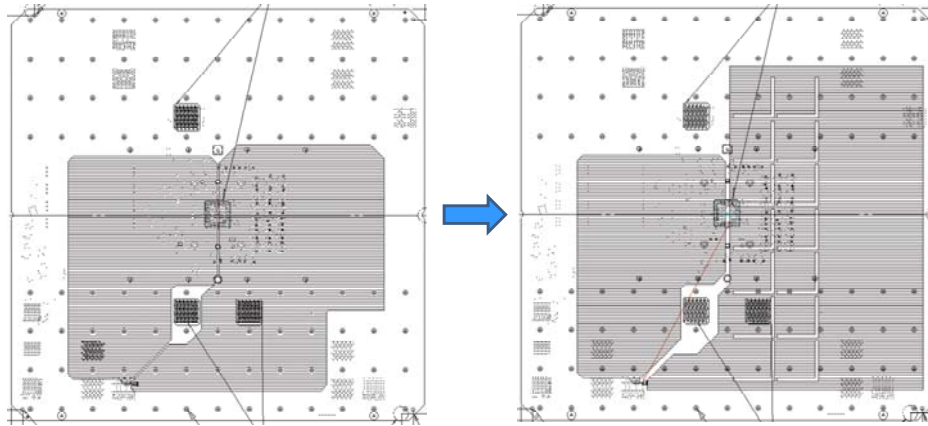
CIRCUIT SIDE(TOP)

LAYER 1	TOP(50 OHMS/8 MII
LAYER 2	PLANE GND
LAYER 3	HSD1-OUTPUTS
LAYER 4	PLANE GND
LAYER 5	HSD2-TAC-OUT
LAYER 6	PLANE GND
LAYER 7	HSD3-OUTPUTS
LAYER 8	PLANE GND
LAYER 9	PLANE GND
LAYER 10	VA-VDP
LAYER 11	PLANE +12-RELAY
LAYER 12	UDB
LAYER 13	PLANE GND
LAYER 14	0.004 VAC-VAT-VENC
LAYER 15	PLANE GND
LAYER 16	dc30
LAYER 17	PLANE GND
LAYER 18	SB6G 1 50 OHMS/8 M
LAYER 19	PLANE GND
LAYER 20	BOTTOM 1 50 OHMS/8

COMPONENTSIDE(BOT)

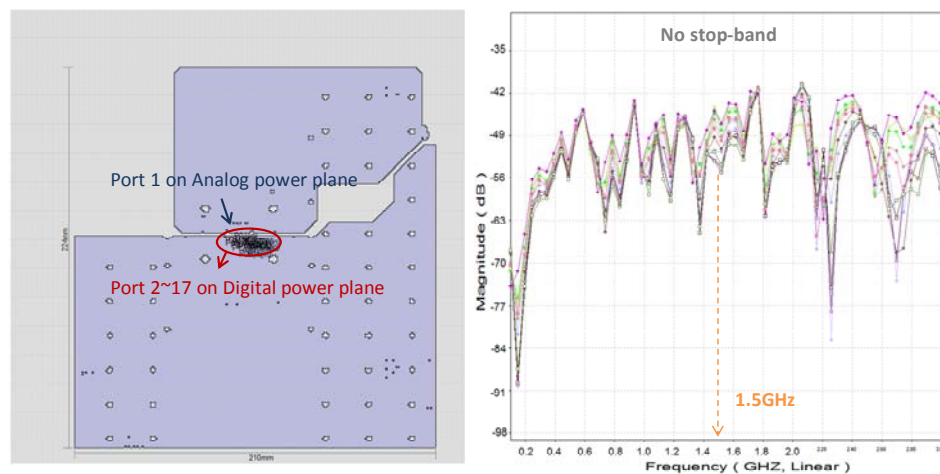
Layer order reversed (+12-RELAY ↔ GND)

Plane Modification

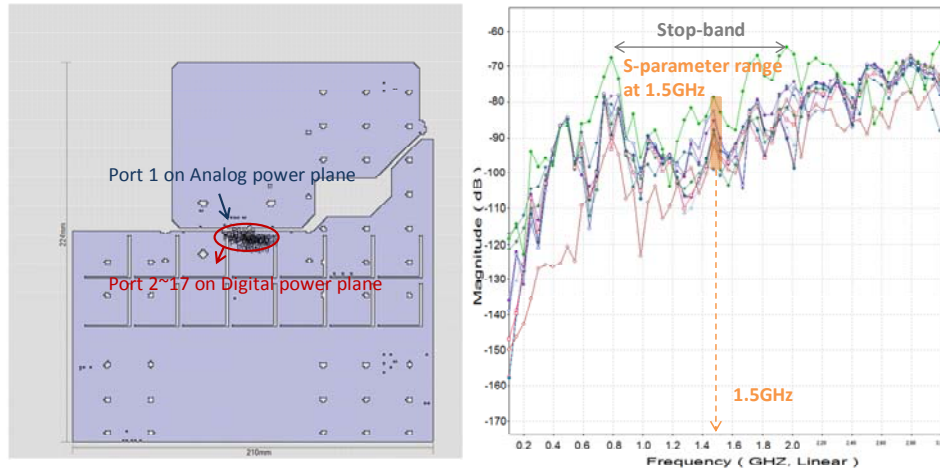


EBG implemented on the digital power plane
(EBG size aimed for 1.5GHz)

S-parameter before Modification



S-parameter after Modification



Summary

- ❑ If power planes need to be split – do not blindly split them but instead use design rules !
- ❑ Structures (EBG) are now available that help decouple parts of planes from each other – so why bother splitting planes if a common power supply needs to be used.



Ref: M. Swaminathan and E. Engin, “Power Integrity Modeling and Design for Semiconductors and Systems”, Prentice Hall, Nov ’07
Free Software Download: www.powerintegrity.net

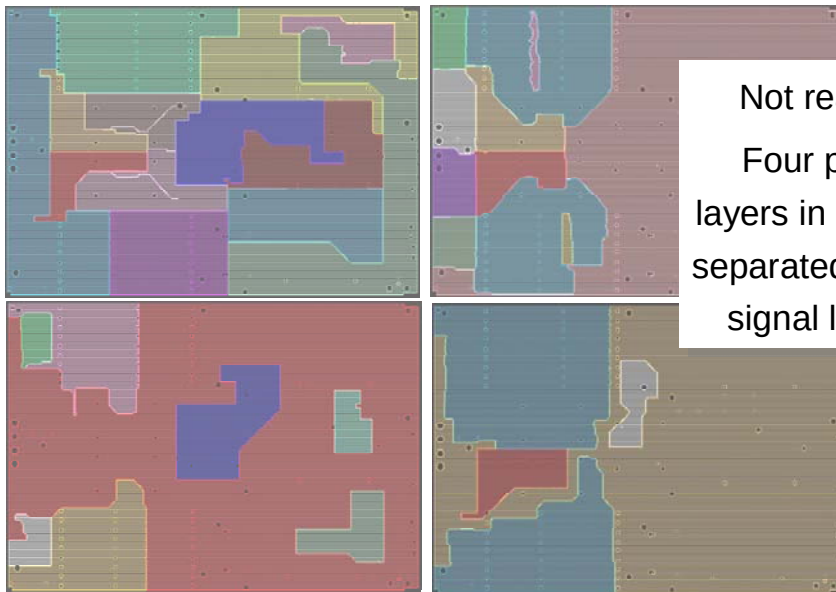
Any questions, please send email to madhavan@ece.gatech.edu

URL: epsilonlab.ece.gatech.edu

Challenges with Split Power Planes

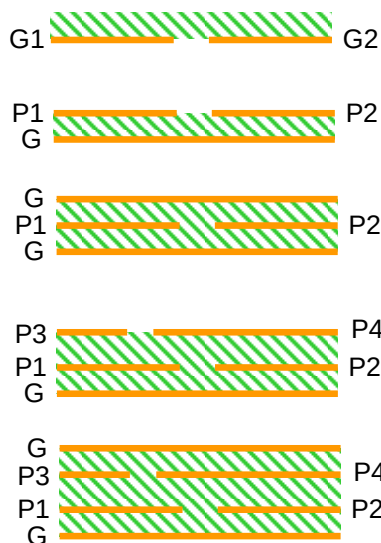
Istvan Novak, Sun Microsystems
DesignCon 2009, TP_M3

Do We Have a Choice to Split or Not?



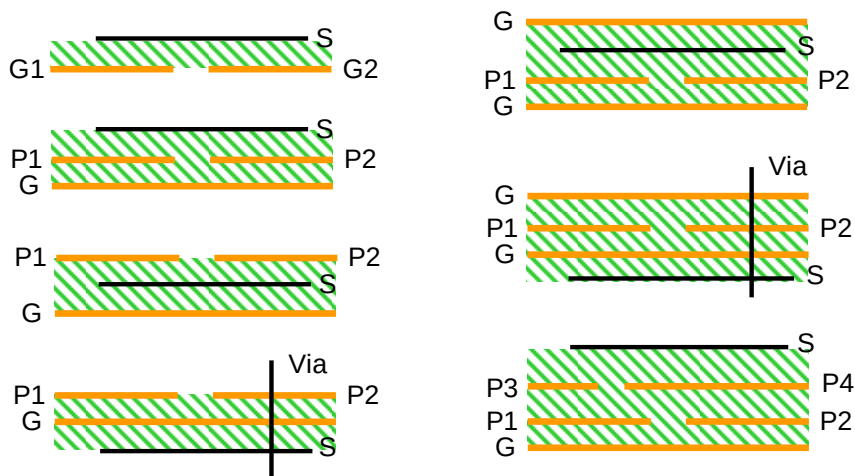
Not really...
Four power
layers in a board,
separated only by
signal layers!

Some Split Plane Types



Only power-ground building blocks shown here, no signal layer/trace yet.

Lets Add Signal Traces



The number of possible permutations explodes.
Just a few combinations are shown here.

Some of the Potential Issues

What could be the problem with plane splits?

- Power distribution
 - > Noise coupling from one domain to others
- Signal integrity
 - > Discontinuity
 - > Increased crosstalk
- EMI
 - > Increased radiation and/or susceptibility, legal limit
 - > Increased radiation or susceptibility, in-system interference
- And any combination of the above

Nature of Potential Issues

Dimensional space of potential problems

- Power distribution
 - > Mostly a **2D** phenomenon
- Signal integrity
 - > On a macro level mostly a **1D** problem
- EMI
 - > Almost always a **3D** problem
- Add time to all of the above as the fourth dimension
 - > Noise is generated by SW/FW-driven state machines

The Result...

- Phenomena and contributors to issues can be easily simulated one by one
- **BUT** except for obvious extremes, it is very hard to prove/disprove risks or solutions on live systems with split planes

For More Details...

For more details, listen to:

- 10-WA3; Examining the Impact of Split Planes on Signal and Power Integrity
- 6-TA1; Analysis of Crosstalk between Signals Routed over Discontinuous Reference Plane