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## Introduction and Comparison of an Alternate Methodology for Measuring Loss Tangent of PCB Laminates

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# Abstract

Recent advances in PCB density and increased interconnect speeds have raised the mainstream need for low-loss dielectric materials. Although the availability of mid- and low-loss laminates is exploding, it comes with a confusing array of possible test methods for dielectric loss (Df) measurement. One of the primary challenges is measuring Df at high frequencies independent of other contributors, such as copper losses, radiation and potential non-homogeneities and non-isotropy of materials. This paper introduces the model-based Capacitance Gradient Method (CGM), which is largely independent of conductive and radiation losses. The paper will also discuss the results of a laminate study conducted to provide a comparative overview of CGM with a few IPC accepted methodologies, such as Split-Cylinder Resonance and Parallel-Plate methods. Their strengths and potential pitfalls will be compared including surprising results that contradicted a commonly accepted understanding of wide band frequency dependent dielectric loss behavior

## Author Biographies

Kevin Hinckley is a Signal Integrity Engineer at Sun Microsystems with more than 15 years in the industry. Current responsibilities include all aspects of signal integrity modeling, analysis and validation within Sun's x64 server division. Prior to his time at Sun, Kevin worked in the Defense Industry with a focus on semiconductor device modeling, simulation and measurement. He received a BSEE from Rensselaer Polytechnic Institute.

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Michael Ballou is a Graduate of Southern New Hampshire University B.S. with over 20 years experience in Material Measurement with Agilent Technologies and the Aerospace and Defense Industry

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Jason R. Miller is a Senior Staff Engineer at Sun Microsystems where he works on ASIC development, ASIC packaging, interconnect modeling and characterization, and system simulation. He has published over 30 technical articles on the topics such as high-speed modeling and simulation and co-authored the book "Frequency-Domain Characterization

of Power Distribution Networks” published by Artech House in 2007. He received his Ph.D. in electrical engineering from Columbia University.

Roger Dame is a Member of Technical Staff Engineer at Sun Microsystems where he works on mid-ranged servers, SI work in general, simulation, and lab work. He has 34 years of experience on analog, digital design and SI work with DEC, Compaq, and HP. He received his BS in electrical engineering from CNEC.

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Gregory Truhlar is a Signal Integrity Engineer at Sun Microsystems with 3 years of experience in the design, simulation, and validation of high speed serial interconnects on Sun's SPARC server platforms. He received his B.S. and M.S. degrees in Electrical Engineering from Tufts University.

Shelley Begley is an Application Development Engineer with 25 years experience in the HP/Agilent network analyzer business, working in production engineering electrical metrology, and product marketing. She currently leads a small team of both R&D and marketing, focused on advancing dielectric measurement techniques. She has given countless papers and seminars around the world on the topic.

Istvan Novak is a Distinguished Engineer at Sun Microsystems. Besides signal integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is a Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies.

# 1 Introduction

Recent advances in printed-circuit board density and increase of interconnect speed have raised the mainstream need for lower-loss dielectric materials. Even though the choice of available laminates with medium and low loss is exploding, it comes with a confusing array of possible test and measurement methods for dielectric loss measurement. One of the primary challenges is that dielectric loss mostly matters at high frequencies, where the dielectric loss cannot be measured independent of other loss contributors and no method, instrument or fixture appears to cover the entire frequency range of interest.

Alternatively, we can measure various signatures of overall loss, which is the result of not only dielectric loss, but also copper resistivity, copper volume, copper surface roughness, radiation and potential non-homogeneities and non-isotropic nature of the structure and materials.

There are three broad categories of measurement techniques for dielectric loss:

- direct impedance measurements
- resonance-based methods
- wide-band model-based signature tests

Several of these measurement techniques are now IPC standards.

The methods based on direct impedance measurements use the real and imaginary part of the impedance of a laminate sample to obtain loss tangent. Bare dielectric laminates can be measured between parallel plate electrodes [1], which is one of the inherent limitations of this test method: trapped air due to surface roughness and/or non-planarity between the electrodes and specimen will artificially lower both dielectric constant and loss tangent readings. The effect of the fringing field can be reduced by appropriately patterned test fixture and/or calibration software [2]. This test method uses electric fields perpendicular to the laminate surfaces, which is the actual orientation of regular use in typical PCBs and therefore potential anisotropy due to glass reinforcement is not a source of additional error. Parallel-plate methods can be carried out anywhere sufficiently below the modal resonance frequencies of the sample and/or fixture, usually in the kHz and MHz range. Careful calibrations and compensations can extend the useful frequency range up to about 1GHz. Copper-clad samples can be measured in a similar way. Just the fixture or probe has to change accordingly. Options and limitations will be further detailed at the description of the Capacitance Gradient Method.

At GHz frequencies the direct impedance-based measurements fail due to structural resonances of the samples and/or fixtures. Dielectric loss can no longer be measured separately from other sources of loss. Resonance-based methods measure the sample at one or more of the natural modal resonance frequencies of the sample or the fixture, and the loss tangent is back-calculated from the Q around the resonance with and without the sample. Resonating traces either in microstrip or stripline form can be used [3], resonant cavities can be formed around the sample by the test fixture [4], or the resonances of a copper-clad sample sheet can be measured [5]. These options measure dielectric loss tangent indirectly, since the Q of resonance is dependent on the conductive losses as well. Additionally, the radiation and fringing effects may be higher at resonance so that it can

not be ignored any more, something that we can often do at low-frequency direct-impedance measurements. Microstrip and stripline test structures and Full-Sheet Resonance Methods use the same orientation of fields that are used during normal operation, but many resonant cavity fixtures use an electric field parallel to the laminate surface. Due to the anisotropy of glass-reinforced laminates, this gives rise to potentially different test results of the same sample with different resonant methods [6].

Wide-band model-based test methods use the measured signature of laminated samples over a wide frequency band and the signature is fitted to trusted models. Three such methods are now recommended by IPC. Some methods recover all important electrical parameters of the dielectric laminate and copper [7], some give an overall ranking of laminate behavior [8], [9]. While these methods offer a wide-band characterization, their accuracy heavily depends on the various details of measurements to be performed, such as DC resistance, surface-roughness and time-domain response [7]. Simpler-to-perform methods may provide GO/NO-GO results for fabricated boards, but do not give numerical loss tangent results [8], [9]. On the other hand, wide-band model-based test methods use finished fabricated boards, so the measurement result will refer closely to the actual usage. This is a huge benefit, but a complication as well at the same time: strictly speaking each stackup of the user application has to be measured and characterized separately with the unique copper and PCB lamination process

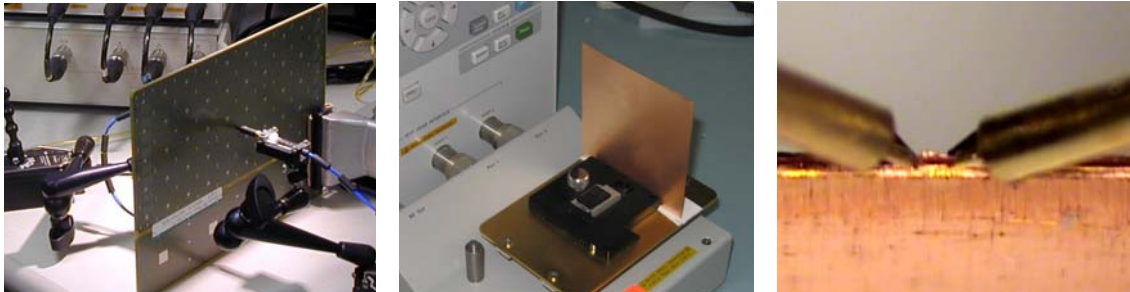
In this paper first we introduce the Capacitance Gradient Method (CGM), followed by the results of a laminate study conducted in the second half of year 2009.

## 2 The Capacitance Gradient Method

CGM derives loss tangent data from the change of capacitance with frequency. The real part of the complex permittivity of a laminate is what we commonly call dielectric constant, and it is usually denoted by  $D_k$  or  $\epsilon_r'$ . The imaginary part of the complex permittivity,  $\epsilon_r''$ , is related to dielectric loss. The ratio of the imaginary and real parts,  $\epsilon_r''/\epsilon_r'$  is called the dielectric loss tangent or Dissipation Factor (Df). When we look at these parameters over a very wide frequency range, both the real and imaginary parts vary with frequency and their values are cross-linked through causality constraints. If we know the wide-band behavior of the real part, we can reconstruct the imaginary part [10]. Capacitance usually can be measured more accurately, with less influence from noise and instrumentation errors, than the imaginary part of complex permittivity. The essence of CGM is that we measure capacitance versus frequency at a convenient frequency range and extrapolate Df(f) for a wider frequency range based on a wide-band Debye model.

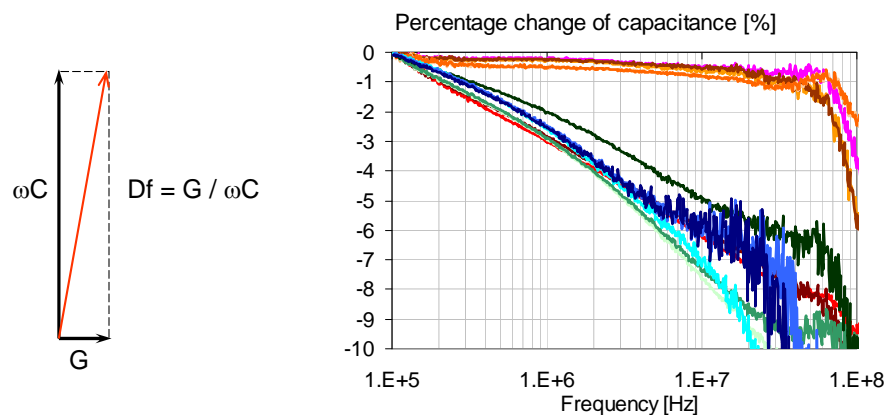
CGM gradually grew out from testing thin laminates for power-distribution characterization. At first it was a variant of IPC's Full-Sheet Resonance method. [11] describes a combination of CGM and resonance-based methods, where at low frequencies the capacitance is extracted. At high frequencies the loss tangent is calculated from the measured Q of modal resonance peaks. Measuring instrumentation was connected to the laminate by a pair of through-holes, making the connection reliable, easy and robust. However, the antipads around the through-holes inevitably modify the sample's

resonance structure and capacitance, and the impact increases as the DUT size gets smaller. This error can be reduced if we use a compensated SMD fixture or a calibrated wafer probe to connect directly to the two copper sheets at the edge of the sample [12]. *Figure 1* shows illustrations of these connection options.



**Figure 1:** Photo of semirigid probes attached to through-hole test points (on the left), SMD test fixture holding a laminate sample (in the middle) and wafer probes connecting to laminate edge (on the right).

*Figure 2* shows an admittance phasor of a parallel-plate capacitor. When we assume that the series conductor losses of the electrodes can be neglected, the absolute value of the ratio of the real and imaginary parts is the same regardless whether we calculate it from impedance or admittance. Laminate materials used today in high-speed circuits have Df values of a couple of percent or less. For a loss-less dielectric  $G = 0$  and the phase of admittance is 90 degrees. To measure a small finite Df value, we have to rely on very accurate phase measurements to resolve the difference from the 90-degree baseline. In contrast, the capacitance is carried by the magnitude of the vector, which can be measured with less noise. The graph on the right of *Figure 2* contains the capacitance versus frequency curves of a dozen different laminates. We can notice that on logarithmic frequency and linear capacitance scales the traces are almost straight lines over a wide frequency range. The greater the slope, the higher the Df of the laminate.



**Figure 2:** Admittance phasor of a lossy dielectric (on the left) and representative  $C(f)$  curves of various thin laminates.

When dielectrics are subjected to an external electric field, the electron polarization, the dipole polarization, the ion polarization and the macrodipole polarization mechanisms are

responsible for dielectric losses. Further classifications are elastic and relaxation polarizations. Inhomogeneous materials (such as the widely used glass-reinforced laminates) may exhibit an additional space-charge polarization [13].

The traditional narrow-band model for dielectric relaxation losses use a one-pole Debye term in the form of:

$$\varepsilon(\omega) = \varepsilon_0 + \frac{\Delta\varepsilon}{1 + j\omega\tau} \quad (1)$$

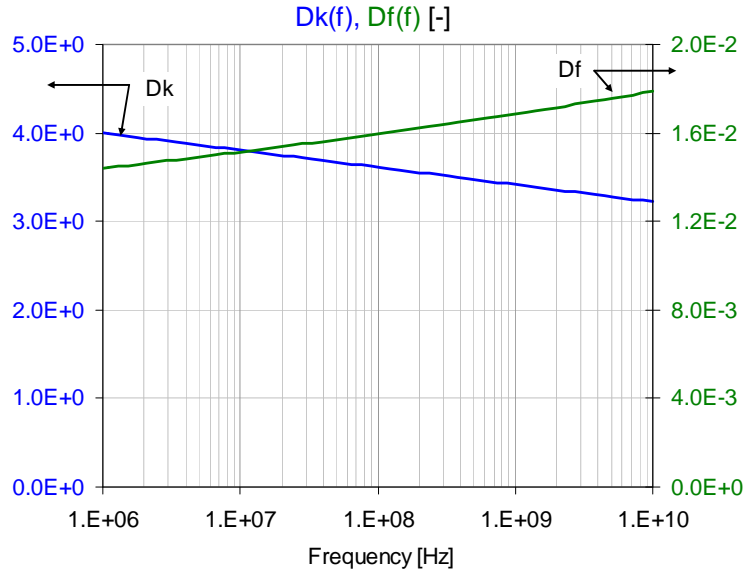
In contrast to (1), based on experimental data, it has been commonly assumed that medium- and high-loss glass-reinforced laminates exhibit an almost constant  $\varepsilon_r''$  over several decades of frequencies, resulting in an almost linear rise of Df on a logarithmic frequency scale. To obey causality rules, (1) can be used in a finite or infinite sum of terms, which can approximate the relatively constant  $\varepsilon_r''$  versus frequency curve [10], [14]. With the assumption that capacitance drops linearly on a logarithmic frequency scale, the complex permittivity can be expressed as:

$$\varepsilon_r(\omega) = \varepsilon_\infty' + \frac{\Delta\varepsilon'}{m_2 - m_1} \ln \frac{\omega_2 + j\omega}{\omega_1 + j\omega} \frac{1}{\ln(10)} \quad (2)$$

where  $m_1$  and  $m_2$  denote the  $\omega_1$  lower and  $\omega_2$  upper frequency corners for the models,  $\Delta\varepsilon'$  is the total variation of the real part between  $\omega_1$  and  $\omega_2$ . In between the upper and lower corners, far away from the corner frequencies, the imaginary part is basically constant. If the sample's aspect ratio is such that fringing can be neglected, the real part of complex permittivity is directly proportional to the sample's capacitance through a constant geometry multiplier. Further assuming that we limit ourselves to  $\omega \gg \omega_1$  and  $\omega \ll \omega_2$  frequencies, (2) can be rearranged to yield  $Df = \varepsilon_r''/\varepsilon_r'$  from the measured C(f) curve. We can do this because to calculate Df(f) we need only the relative change of the real part of complex permittivity and therefore the (unknown) geometry constant linking capacitance to the real part of permittivity drops out of the equations. By expressing the slope of capacitance by a finite difference rather than a derivative, we get:

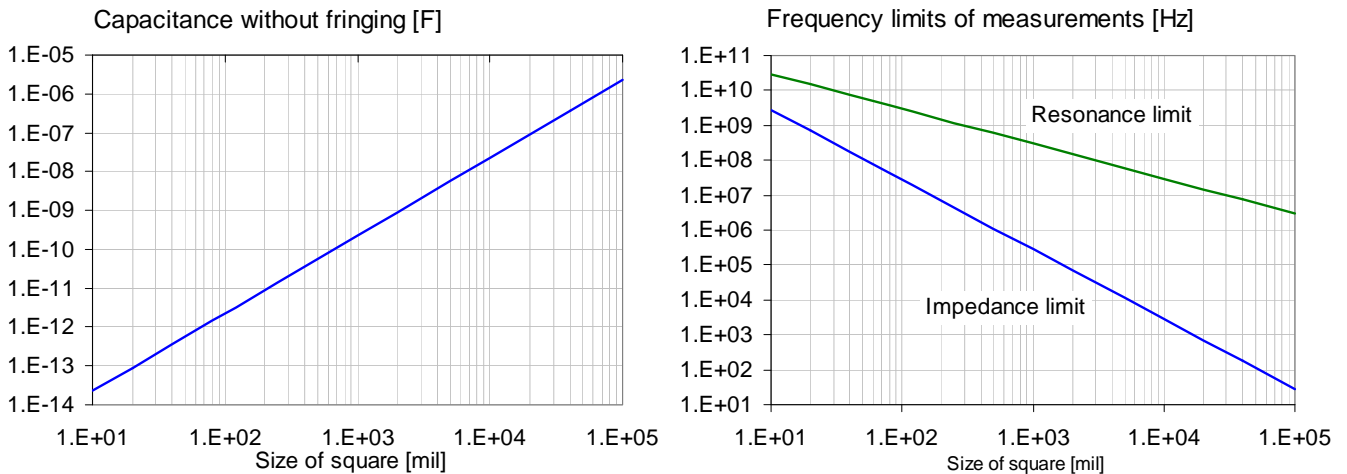
$$Df(f) = Df(f_0) \frac{C(f_0)}{C(f)}; \quad Df(f_0) = \frac{C(f_0) - C(f)}{C(f_0)} \frac{a}{\ln\left(\frac{f}{f_0}\right)}; \quad a = \frac{\pi/2}{\ln(10)} \quad (3)$$

*Figure 3* illustrates *Equation (3)*. On a logarithmic frequency scale the model assumes a constant slope for the Dk(f) and C(f). Since Df(f) is inversely proportional to C(f), Df(f) will look like a linear rise for small values, but in fact its gradient is rising with increasing frequency. *Equation (3)* tells us that within the range of validity of this model, we can measure Df(f) indirectly by measuring the slope of the capacitance versus frequency curve. And since this model assumes that the capacitance gradient is independent of frequency (in the range  $\omega_1 \ll \omega \ll \omega_2$ ), it should be enough to measure the capacitance versus frequency curve in any sub-range of  $\omega_1$  and  $\omega_2$  and from that data we can extrapolate the results for the entire frequency range. Since C(f) slowly and almost linearly varies with the logarithm of frequency, we can suppress measurement noise by fitting an appropriate low-order polynomial to C(f) before putting it into *Equation (3)*.



**Figure 3:** Illustration of  $Dk(f)$  and  $Df(f)$  based on the wide-band Debye model, using Equation (3).

Since CGM relies on extrapolation of measured data, we now have the freedom to choose the measurement range for capacitance, wherever we can minimize known side effects. For instance, radiation losses and errors due to series conductor losses will diminish as we go to lower frequencies. However, since the impedance of a capacitance increases as frequency goes down, very low frequencies will require the measurement of high impedance values, which will stress the dynamic range of the measuring instrument and high DUT impedances are more impacted by stray capacitance as well. At high frequencies the result will get distorted by the approaching modal resonances. These considerations will limit the usable frequency range as illustrated in *Figure 4*.



**Figure 4:** Capacitance of a square cavity, without fringing (on the left) and lower and upper frequency limits of a typical CGM VNA measurement (on the right).



The plot on the left of *Figure 4* shows the static capacitance of a square parallel-plate cavity assuming a dielectric thickness of 4 mils and Dk of 4. The plot uses the simple formula of:

$$C = \epsilon_0 \epsilon_r \frac{A}{s} \quad (4)$$

where  $\epsilon_0$  is the permittivity of free space,  $\epsilon_r = D_k$  is the relative dielectric constant,  $A$  is the area of the capacitor plate and  $s$  is the dielectric thickness or plate separation. The practical range for laminate measurement is a few hundred mils to a few inches square, which gives a capacitance range to measure of approximately 10 pF to 10 nF. The plot on the right of *Figure 4* gives further practical limitations: we need to stay away from modal resonances and we have to have a reasonable value of capacitive reactance to measure. A square parallel-plate structure will have its first modal resonance peak at a frequency, which equals the inverse of round-trip delay along each side:

$$F_{peak1} = \frac{c}{2a\sqrt{\epsilon_r}} \quad (5)$$

where  $a$  is the length of a side and  $c$  is speed of light. Below the modal resonance peak a minimum will occur. While the frequencies of modal resonance peaks are approximately the same regardless of where they are measured on the planes, the impedance minima between the peaks do also depend on the locations. As an illustration, *Figure 5* shows how the frequency of the first impedance minimum varies with location.

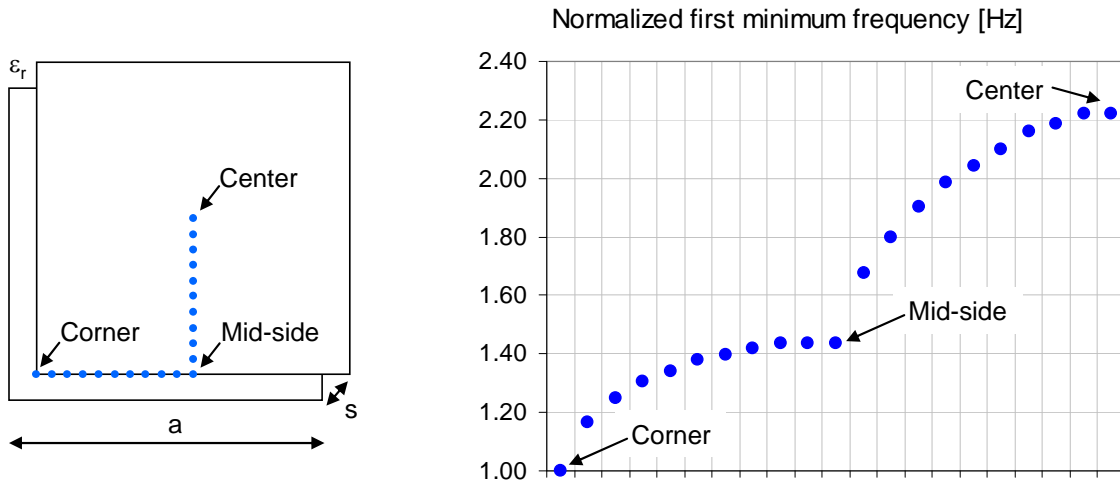


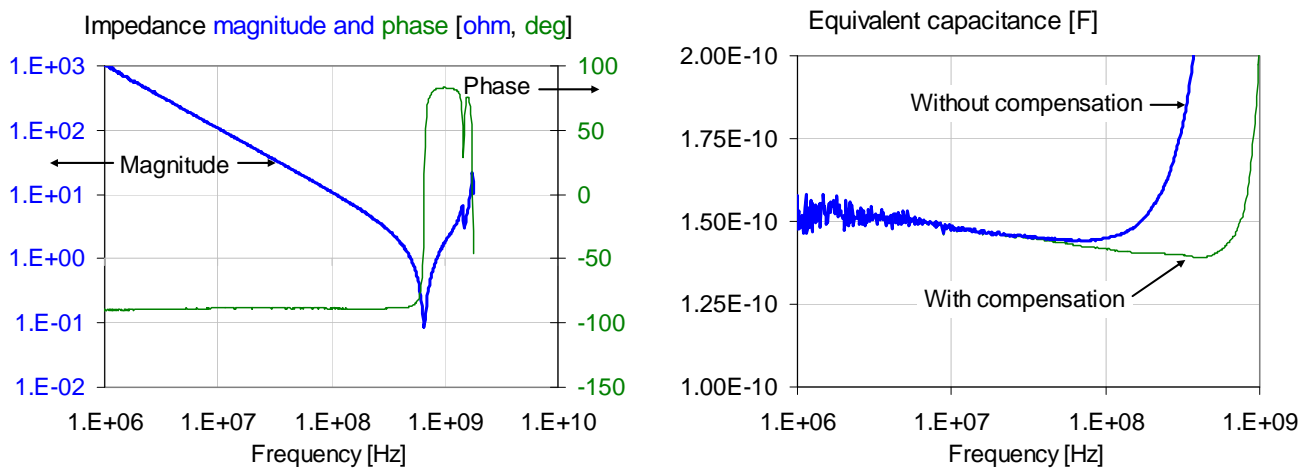
Figure 5: Parallel-plate capacitor with the simulation locations marked (on the left) and frequency of first impedance minimum normalized to the corner value.

Note that the size of square in *Figure 5* is arbitrary, since the resonance frequency scales with the dimensions. The figure tells us that the lowest first resonance-minimum frequency occurs at the corners and the highest in the center. Assuming no through holes on the planes, we are limited to the edges and therefore we can increase our measurable frequency range by 44% if we measure  $C(f)$  in the middle of a side.

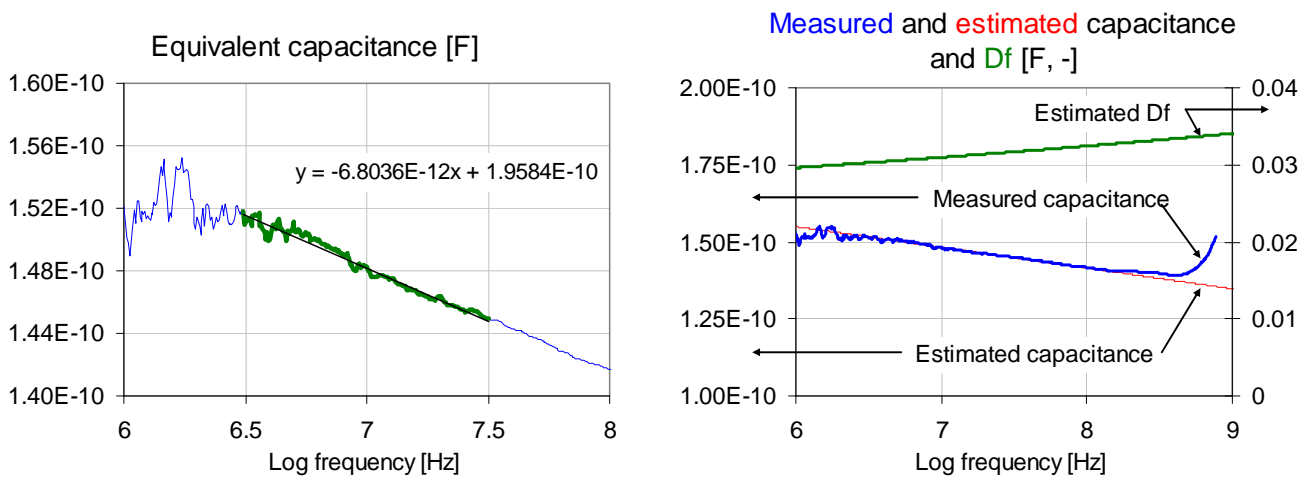
Figure 6 shows a typical impedance plot of a small cut section from a multi-layer PCB, measured at the edges with wafer probes. The plot on the right shows the equivalent capacitance extracted from the imaginary part of the impedance. The impedance plot exhibits a series resonance at 670 MHz. Note that the extracted capacitance trace on the right curves up after 100MHz. This is because of the approaching series resonance. We can make a correction of the measured  $\text{Im}\{Z\}$  imaginary part of the impedance based on the estimated  $L_{\text{plane}}$  inductance of the planes, which yields the capacitance estimate:

$$C(f) = \frac{-1}{2\pi f (\text{Im}\{Z\} - 2\pi f L_{\text{plane}})} \quad (6)$$

By this compensation the capacitance curve remains a straight line up to about one third of the series resonance frequency.



**Figure 6:** Impedance magnitude and phase (on the left) and extracted capacitance with and without plane-inductance compensation.



**Figure 7:** Curve fitting of measured capacitance (on the left) and measured and estimated capacitance as well as estimated Df on the right.

The linear portion of the capacitance trace is curve fitted. This eliminates the noise and allows us to use *Equation (3)* by plugging in the expression of the capacitance estimate. The left graph of *Figure 7* shows the curve fitting on the highlighted section of the measured capacitance trace. The graph on the right overlays measured (blue) and estimated (red) capacitance curves. Note that the horizontal scales are the logarithm of frequency.

## 3 Laminate Study

While communicating with laminate vendors and board fabricators, it became clear that although the number of available options is growing by the day, there was no single methodology emerging as a single favorite or mostly adopted solution to measure dielectric loss tangent for high-speed digital applications. This prompted our study, to enhance our understanding and to see which laminate testing methodology would be a good fit for our needs.

### 3.1 Subject, Purpose and Scope

The chosen subject of the study was to understand some of the key measurement methodologies for Df. Why only Df and not Dk as well? Simply because we experienced less confusion, less miscommunication and misinterpretation of data around Dk. We also understand that Df is only one of the important design parameters for high-speed laminates. Copper losses, including the additional loss due to surface roughness, as well as copper treatment processes are equally important, especially for narrow traces. We understood as well that wide-band model-based methods might come closest to providing an accurate representation of the built-up board's performance. However, the key challenge starts with the design phase, when the high-speed interconnect performance has to be simulated and laminates have to be selected for the board. Even if later a board is built and characterized for overall performance, simulators need numbers for Df to be plugged in, and manufacturing would prefer a laminate requirement (meaning Df specification for dielectric loss), rather than calling out specific laminates. For all these reasons, and also considering the available time and resources, the subject was limited to studying only Df.

The primary purpose of the study was to see which Df test method would fit the needs of the types of laminates we use currently and in the near future. This way we left out very low loss and special high-cost laminates.

An equally important goal was to see how data obtained by CGM compares to other methods. In general, our initial assumption was to just do a validation of CGM against other methods. Little did we know at the beginning of the study that our understanding would completely change and we would have to reset our assumptions.

After having decided to focus on Df only, there were still a tantalizing number of parameters (thickness, glass style, glass-resin ratio, copper style) and laminate choices and therefore the scope had to be further limited. We selected four primary laminates to

be tested. All four are glass reinforced, with a typical thickness in the range of 3-5 mils. All four laminates were tested copper clad, copper removed and B stage. There were at least a dozen other laminates, from different sources, tested partially as well. Many of them served the purpose to look at and test for certain signatures of laminate behavior. The chosen thickness values and glass styles limited the glass-resin ratio to 45 – 55%. All copper clad laminates shown here had one ounce copper. *Table 1* summarizes the main features of the four primary laminates.

Material	Thickness (mil)	Glass Style	Resin Content (%)	Vendor Df	Freq (GHz)	Method (IPC)
Laminate A FR408HR	5.0	#2116	55	0.0072	0.1	2.5.5.3
				0.0086	1.0	2.5.5.9
				0.0093	10.0	2.5.5.5
Laminate B R1566V	5.0	#2116	55	0.012	0.001	2.5.5.9
				0.012	1.0	2.5.5.9
				0.018	10.0	2.5.5.5
Laminate C LGC-451HR	4.0	#2116	44	0.0118	0.001	2.5.5.9
				0.0124	1.0	2.5.5.9
				0.159	10.0	2.5.5.13
Laminate D 370HR	4.0	#2116	46	0.0150	0.1	2.5.5.3
				0.0161	1.0	2.5.5.9
				0.0250	10.0	2.5.5.5

**Table 1:** Characteristics of the four primary laminates in the study.

It is also understood that environmental parameters, such as temperature and humidity, change laminate performance. In this study we focused on relative comparisons and applicability of test methods and therefore all measurements were done at room temperature. Humidity content of the laminates was not measured, but to get a qualitative answer of how moisture would impact our Df results, several of the laminates went through soaking and baking cycles with data taken after soaking and after baking.

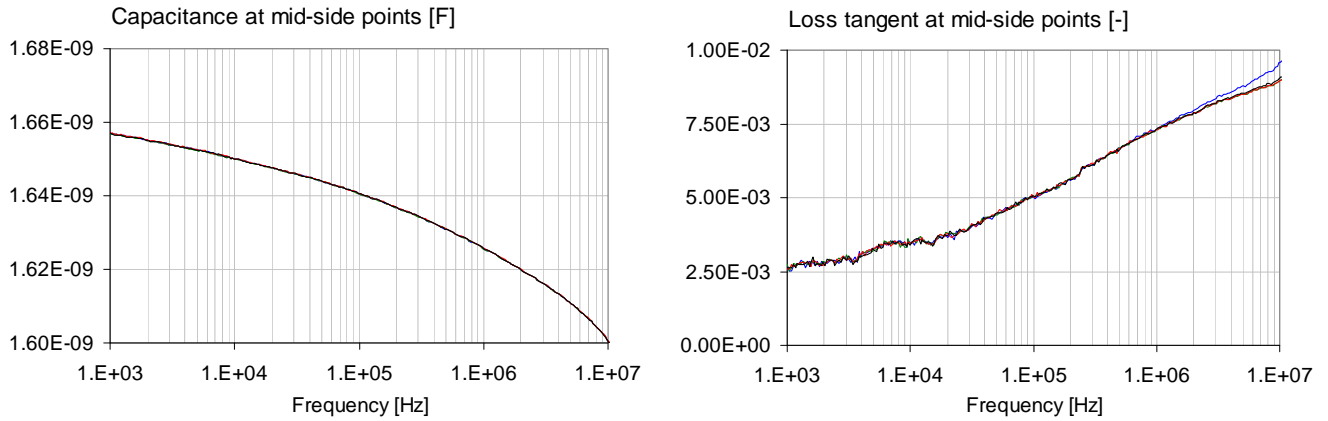
### 3.2 Low-frequency copper-clad laminate results

Three inch by three inch square copper-clad samples were measured with an E4294A Impedance Analyzer and 16192A SMD fixture. C(f) and D(f) were measured at the four corners and at the four mid-points of the sides. Data was recorded in the full 40 Hz – 100 MHz frequency range of the instrument, but the approaching modal resonance minimum associated with the sample size renders the data above 10 MHz unusable without further post processing. *Figures 8* and *9* show the results for Laminates A and D, respectively. The trends of C(f) and D(f) curves agree with the integral Debye model in *Equations (2)* and *(3)*, but not the details. Though C(f) and D(f) are monotonic, they show considerable curvature. We can test the directly measured Df(f) curve against the prediction from *Equations (2)* and *(3)*, and we find a significant difference in the slopes. The bottom left graph of *Figure 9* plots the integral Debye estimates fitted to the values at 10 kHz, 100 kHz and 1 MHz. However, if we apply the wide-band Debye model in a differential way, calculating Df(f) at each frequency point from the local slope of the C(f) curve, we get a

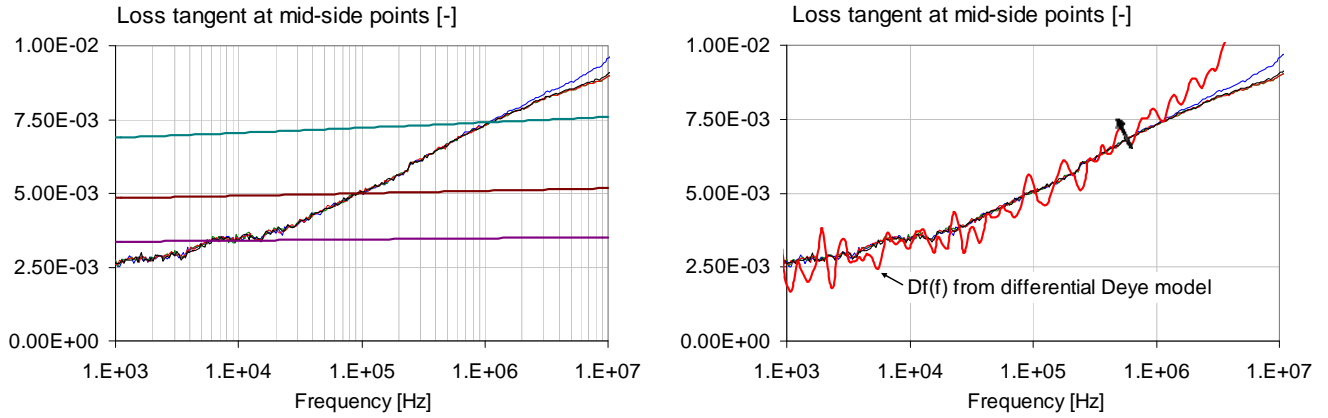
reasonably good agreement, as shown by the red trace on the bottom right graph of *Figure 9*. *Figure 10* plots the Df curves for all four base laminates.

The differential Debye form can be written from *Equation (3)* as:

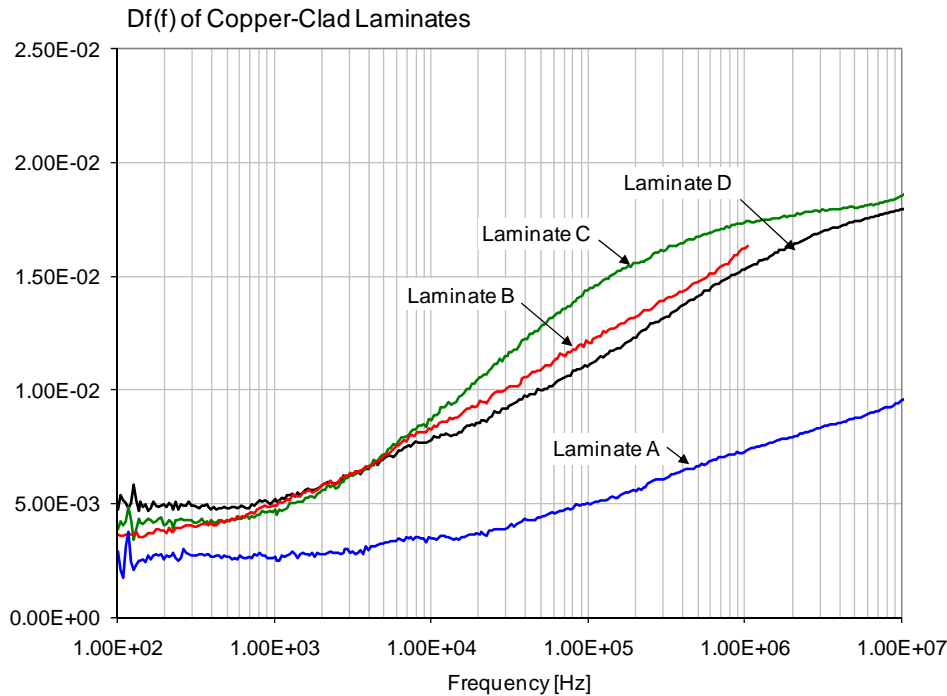
$$Df(f) = \frac{C(f) - C(f + \Delta f)}{C(f)} \frac{a}{\ln\left(\frac{f + \Delta f}{f}\right)}; \quad a = \frac{\pi/2}{\ln(10)} \quad (7)$$



**Figure 8:** Capacitance versus frequency and dielectric loss tangent versus frequency of Laminate A at the four mid-side points.



**Figure 9:** Laminate A measured  $Df(f)$  with integral Debye estimates at three frequencies (left) and measured  $Df(f)$  with differential Debye estimate (right).

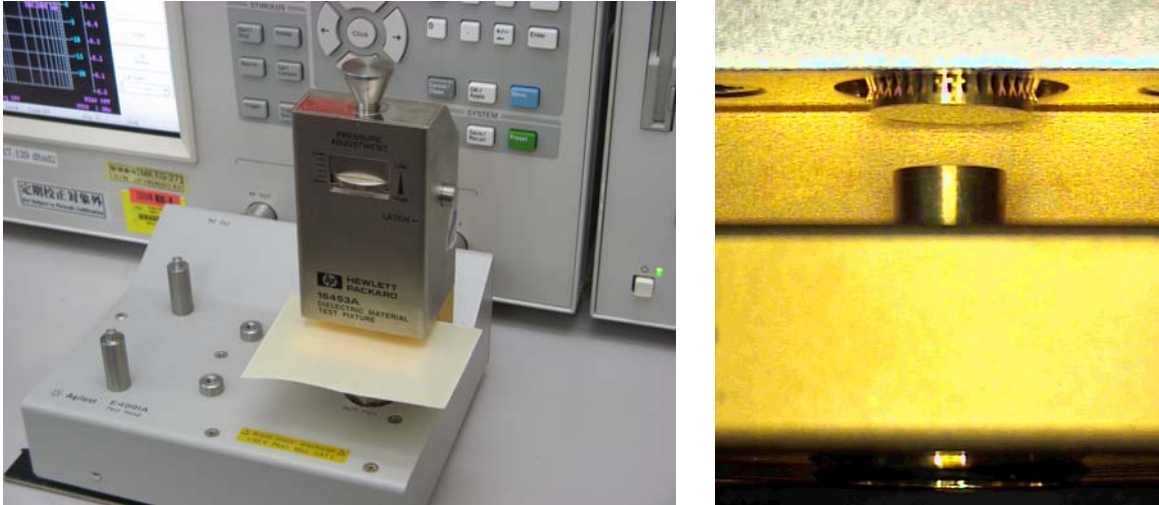


**Figure 10:** Comparison of measured  $Df(f)$  curves of the four copper-clad base laminates in the 100 Hz – 10 MHz frequency range.

### 3.3 High-frequency test results on bare laminates

#### Instrumentation

Bare laminate samples were measured in the 1 MHz – 1 GHz frequency range with an Agilent E4991A Impedance Analyzer with Option 002 and 16453A Parallel-Plate fixture. The setup is shown in *Figure 11*. The Parallel-Plate fixture interfaces with the Impedance Analyzer with the E4991A Test Head, but with Option 002 in Permittivity setup, there is no need to do a 7-mm calibration at the Test Head connector, only an Open, Load and Short calibration at the fixture electrodes. The bottom-side hot electrode of the fixture is 7 mm in diameter, whereas the top-side ground electrode has a diameter of 10 mm. With this geometry, the majority of laminate samples will create resonances somewhere above 1 GHz and therefore even though the Impedance Analyzer works up to 3 GHz, data at and above the resonance was not used. The resonance frequency depends on the laminate thickness and dielectric constant. Thin laminates and/or high-Dk laminates will resonate at a few hundred MHz, further limiting the usable frequency range. The small size of the electrode is helpful to push the lowest modal resonance into the GHz range, but it also reduces the capacitance to be measured. At lower frequencies, especially below 10 MHz, the equivalent bandwidth has to be reduced by point averaging. Data presented here was collected with 32 to 100 point average and User Frequency settings during calibration.



*Figure 11: Bare laminate sample in the Parallel-Plate fixture, attached to the Impedance Analyzer (on the left) and open fixture electrodes (on the right).*

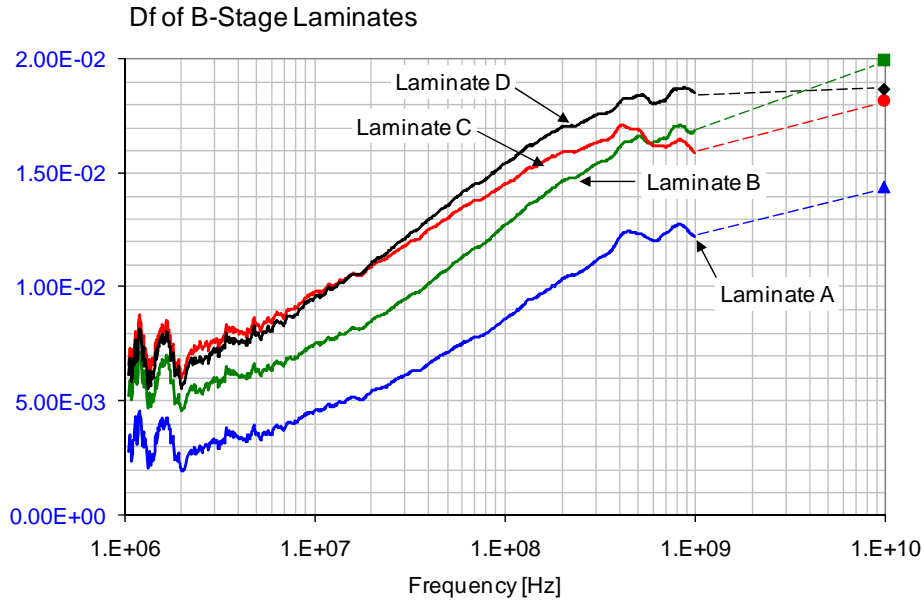
Similar to the copper-clad measurements, the Parallel-Plate fixture measures the bare laminate with an electrical field perpendicular to the laminate surface, which is the same orientation that is used in PCBs. To cover higher frequencies, instead of swept-frequency impedance measurements, a variety of resonant cavities are available. For this study, an Agilent 85072A Split-Cylinder Resonator (SCR) was used with an E8363A PNA Network Analyzer. The SCR's primary measurement frequency is around 10 GHz, with several higher order modes optionally available. *Figure 12* shows the SCR.



*Figure 12: Split-Cylinder Resonator.*

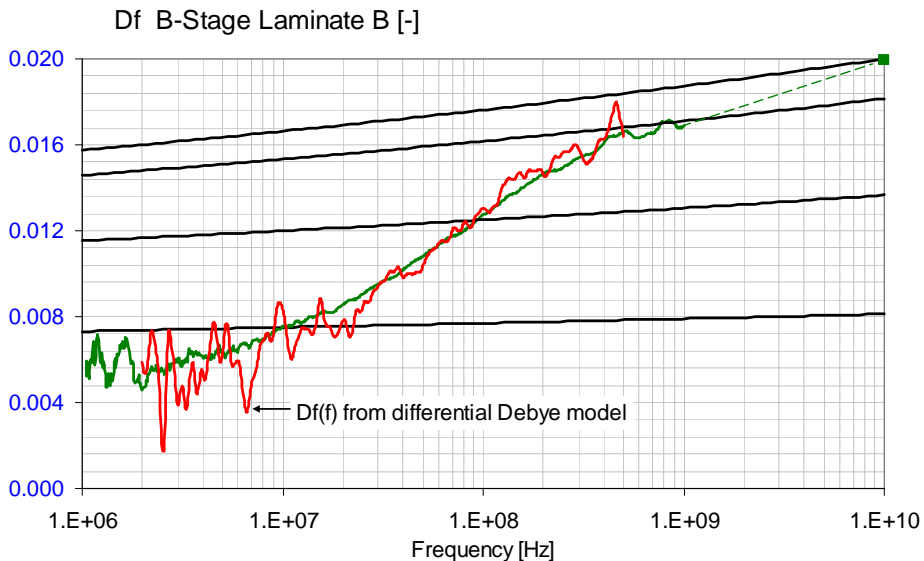
### **Prepreg results**

Multiple B-stage bare prepreg laminate samples were measured with the Agilent E4991A Impedance Analyzer and 16453A fixture in permittivity setup in the 1 MHz to 1 GHz frequency range and with the 85072A Split-Cylinder Resonator at 10 GHz. *Figure 13* shows the measured data on unconditioned B-stage samples 'as is'.



**Figure 13:** Dielectric loss tangent measurement data for B-stage samples of the four base laminates.

All four laminates start out with values below 1% at 1 MHz and ramp up with approximately the same slope and shape (except Laminate C, which has a lower gradient) until 1 GHz. There was no measurement point between 1 and 10 GHz; the dashed lines of matching colors just help to connect the continuous traces to the single 10-GHz data point.



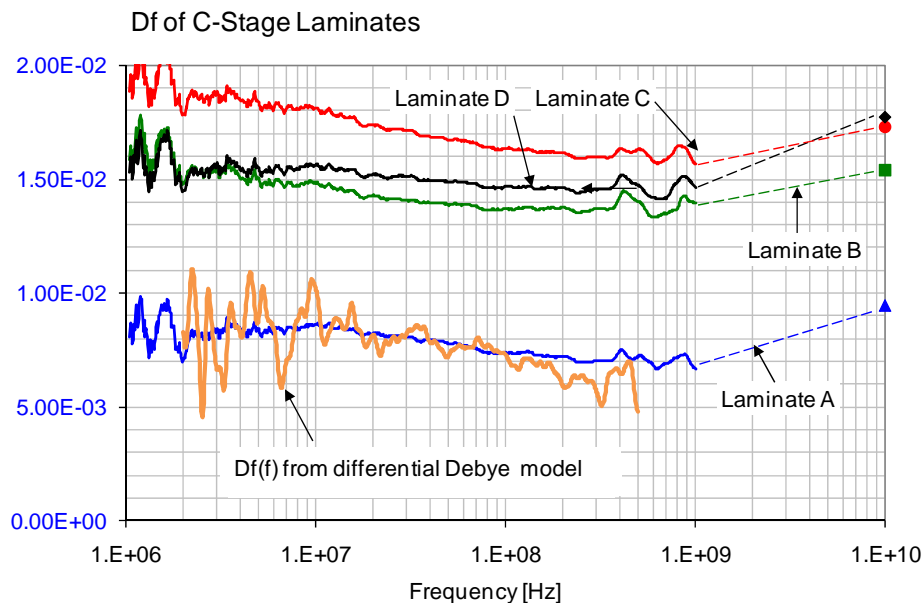
**Figure 14:** Measured  $D_f$  data on B-stage Laminate B sample (green trace), together with wide-band Debye model estimates matching the measured values at four different frequencies as well as the differential Debye estimate from Equation (7) (red trace).



The slopes of all four traces change considerably; they start out with a lower gradient; the slope appears to reach its peak somewhere around 100 MHz, and at higher frequencies the slope is somewhat reduced. Laminate D may even exhibit negative slope somewhere in the 1 to 10 GHz range or above. As shown in *Figure 14*, this measured signature clearly does not match the predicted trend of *Equation (3)*. The figure takes Laminate B data from *Figure 13* and plots it together with the estimated Df trend lines calculated with *Equation (3)* from the 10 MHz, 100 MHz, 1 GHz and 10 GHz measured Df values. The wide-band Debye model predicts a lower slope at all frequencies. Here, too, if we were to apply the wide-band Debye model in differential form from *Equation (7)*, we get a much better agreement between Df(f) curves directly measured and estimated from C(f).

### C-stage results

With the same instrumentation and setup, C-stage samples of the four base laminates were also measured. The cumulative result is shown in *Figure 15*. The trend on all four laminates is now significantly different. Though the 1 – 10 MHz frequency range is noisy, because we measure bare laminate samples with a small 7-mm electrode size, the data appear to suggest positive slope, but at higher frequencies the slope turns negative.

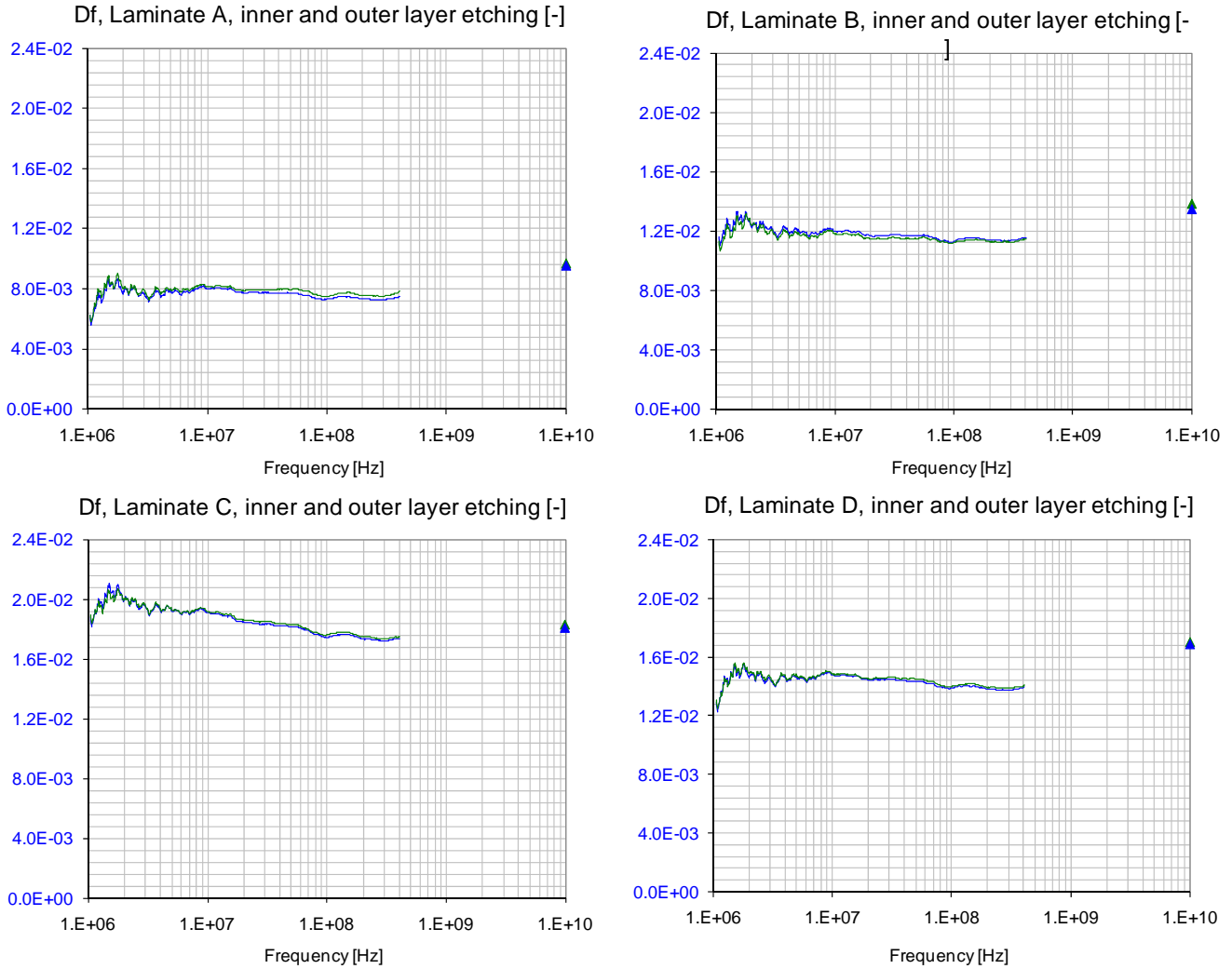


**Figure 15:** Measured Df data on C-stage samples of the four base laminates. Also shown is the differential Debye estimate for Laminate A

Also, the average loss at low frequencies increased several folds. Somewhere after 10 MHz all data traces turn to negative slope and the curves seem to hit a minimum around 1 GHz. For all four laminates the 10 GHz points represent a positive slope again, though the slope itself significantly varies with laminates.

To determine what may have created this significant change in the trends, several side exercises were performed. Since B-stage laminates never had copper on them, but the C-stage laminates measured were actually cores with the copper etched away, the question

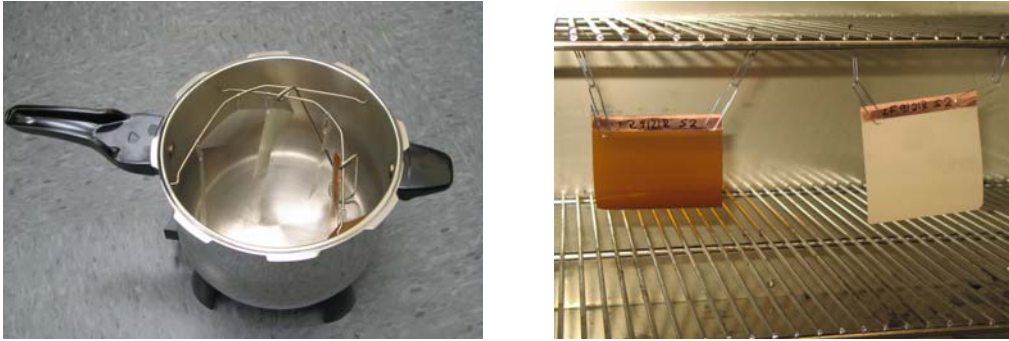
came up whether any part of the core-lamination or etching processes may be responsible for the change. After we learned that the chemistry and processing steps for inner-layer and outer-layer etching are usually different, we had a series of samples go through inner and outer layer etching in parallel. The result, however, showed that the etching process itself had only a very small influence on the dielectric loss data, and no effect on the signature itself. *Figure 16* shows the data for the four base laminates.



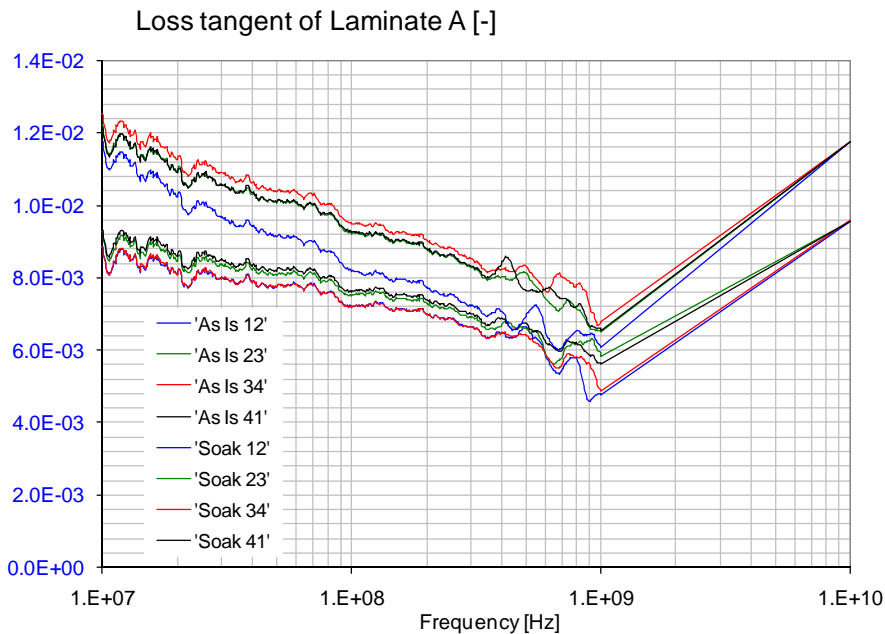
**Figure 16:** Comparison of Df signature on etched samples after inner-layer and outer-layer processes. Blue trace: outer-layer process, green trace: inner-layer process.

There were suggestions that the absorbed moisture might also be responsible for the Df signature we measured. Since we did not have any means to actually measure the moisture content, we took a simple qualitative approach. Bare laminate samples and also copper-clad laminates were repeatedly soaked and baked under different conditions to see how much difference we can observe in the measured Df values on the same samples. Baking was done in an oven at 110 Celsius and at 185 Celsius temperatures for various length of time. Soaking was done by immersing the samples into distilled water at room

temperature and also in a household pressure-cooker. The photos in *Figure 17* show the setups.



**Figure 17:** Samples in the house-hold pressure cooker and in the oven.

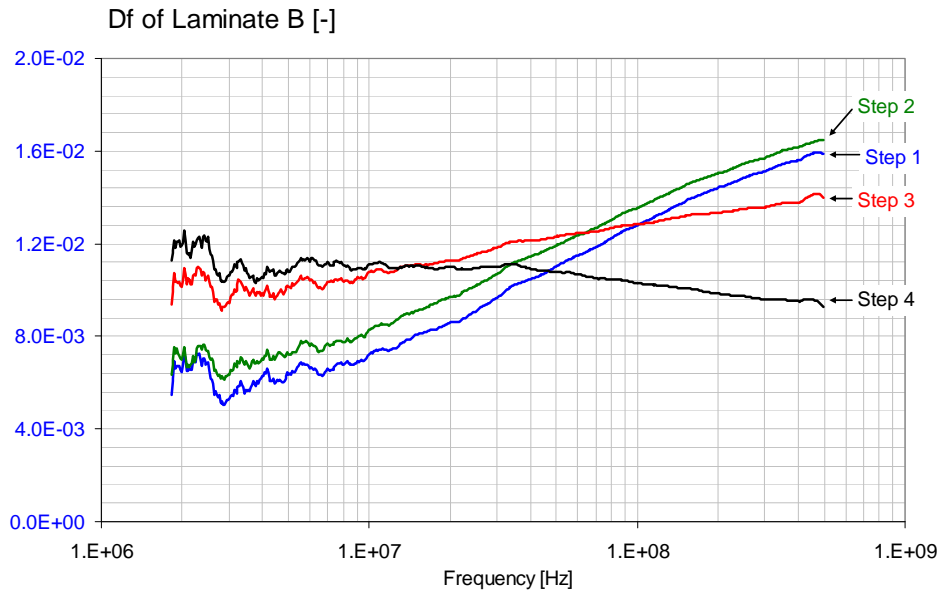


**Figure 18:** Impact of soaking.

Figure 18 shows the impact of two hours of pressure-cooker soaking on etched Laminate A samples. Df was measured on the sample using the Parallel-Plate fixture “as is” (nominal lab conditions) and after soaking. Measurement locations were at the four mid-points along each edge between the numbered corners one through four. The Split-Cylinder Resonator uses the entire sample and though the measurements were taken repeatedly, only one data point is shown for each case. It was found that moisture content did increase both Df and Dk, but it did not change the slope or other signatures of the Df(f) curve.

It was found that the largest impact of these processes on Df signature occurred during baking. *Figure 19* shows the impact of baking on a B-stage Laminate B sample. In Step

1, the sample was measured at room temperature, as is, and after 30 minutes of baking at 110 Celsius. There was no measurable difference before and after baking. In Step 2 there was an additional baking of two hours at 110 Celsius.



**Figure 19: Impact of baking.**

The Df curve shifted up slightly, but the signature did not change. In Step 3 there was an additional fourteen hours of baking at 110 Celsius. This had a noticeable impact on the signature: not only the low-frequency Df went up, but also the gradient changed. In Step 4 there was an additional 90 minutes of baking at 185 Celsius. This finally resulted in the signature that we can observe on C-stage and etched-core laminates: negative Df slope in the 10 MHz to 1 GHz range. When doing a similar exercise on C-stage laminates, the slope of Df(f) did not change further.

### 3. 4 Test results on other laminate samples

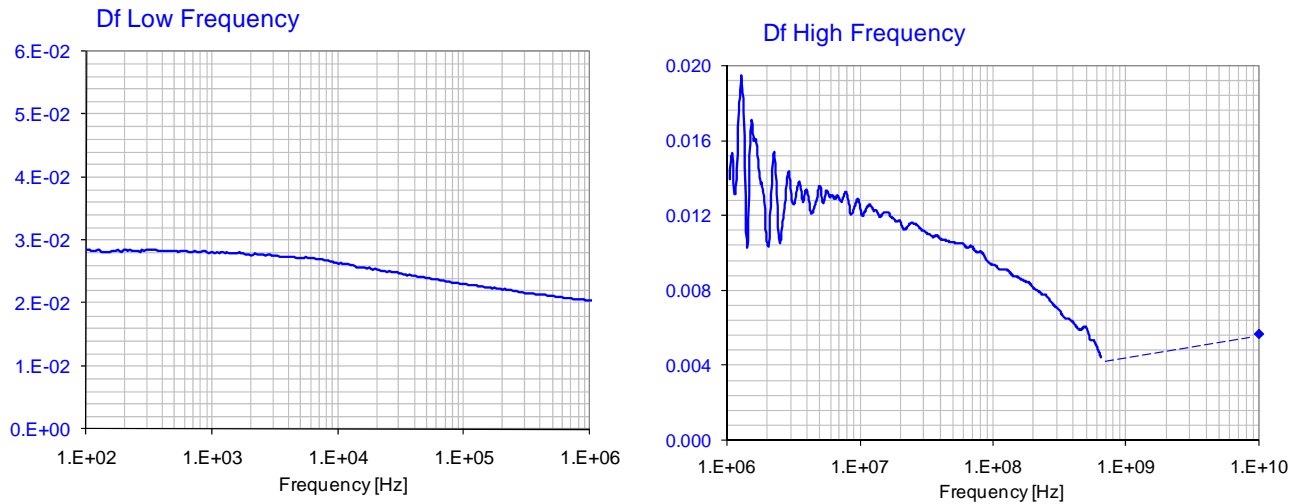
In addition to the four base laminates, several other samples in B-stage, C-stage, copper-clad and etched copper-clad form were also measured. They were used to see if there are different trends of Df(f) curves as a function of material and composition. Also, non-glass-reinforced laminates were looked at, because homogeneous laminates are not expected to have differences between their measured Df values with a field orthogonal to the sample (in a Parallel-plate test fixture) versus with fields parallel to the sample (Split-Cylinder Cavity).

#### Acrylic laminates

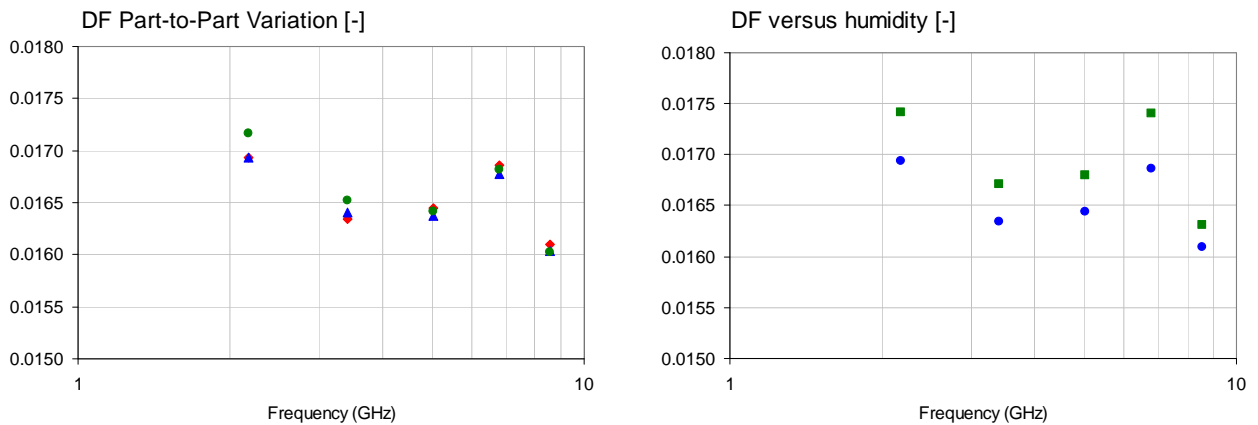
It was already found during the low-frequency measurements that acrylic materials, such as the DuPont FR0121 laminate, show a negative slope of Df(f). *Figure 20* shows the measured Df curves on two different pieces. The left-hand graph shows low-frequency data on a copper-clad sample measured with an E4294A Impedance Analyzer and 16192A SMD fixture; the right-hand graph shows mid-frequency data measured on an

etched bare laminate sample with an E4991A Impedance Analyzer and a 16453A Parallel-plate fixture as well as a 10GHz data point measured with an 85072A Split-Cylinder resonator. To rule out environmental effects impacting the relative comparison, the two different measurements were taken side-by-side within minutes. The dashed line is just a reminder that no data was obtained in the 1 GHz to 10 GHz frequency range.

Note that in the entire 10 kHz to 1 GHz frequency range the laminate exhibits a negative slope of Df. However, the data suggests that the slope may turn around somewhere between 1 GHz and 10 GHz. These samples were measured also after soaking and baking and it was found that though the Df curves shifted due to moisture content, the slope signature remained unaffected.



**Figure 20:** Measured Df of DuPont FR0121A laminate at low frequencies (left plot) and high frequencies (right plot).

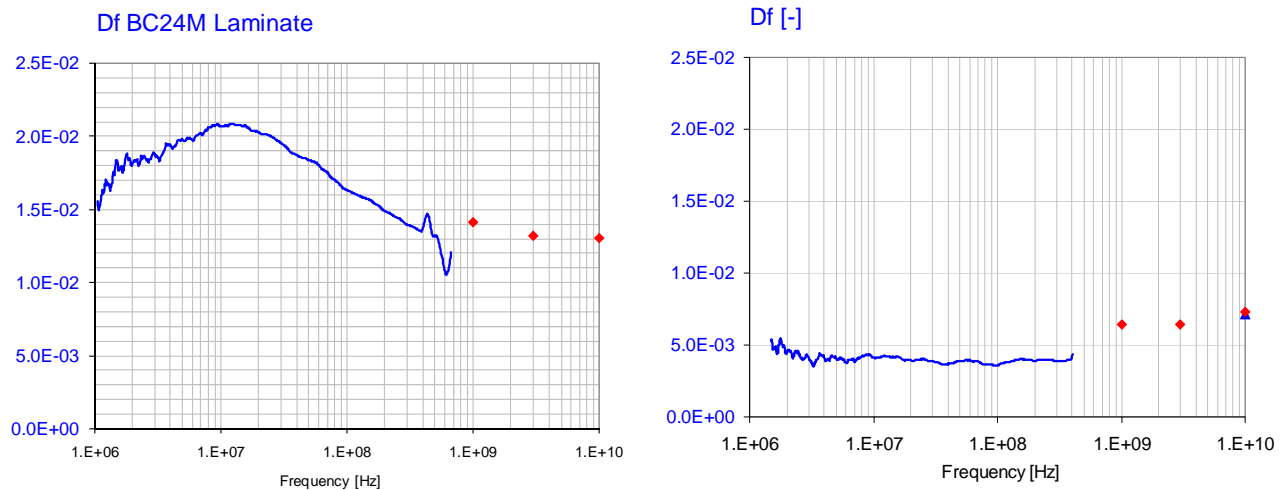


**Figure 21:** Part-to-part variation (left graph) and effect of humidity on Df of DuPont FR0121A laminate samples. Data courtesy of DuPont.

To fill the gap in the 1 GHz to 10 GHz frequency range, data was obtained from DuPont. *Figure 21* shows nominally the same material under different circumstances, measured at five frequencies between 2 GHz and 10 GHz. The graph on the left shows sample-to-sample variations across three pieces, and data points from the three samples almost completely overlap. The plot on the right shows the impact of humidity: blue dots were measured at 53% relative humidity; green squares refer to 67% relative humidity. The measurements were taken with Damaskos Inc. Model 03 Thin Sheet Tester. Note that these data points run at significantly higher numbers: 1.6-1.7% as opposed to the 0.4 – 0.6% values in *Figure 20* in this frequency range. Since the DuPont samples were measured at nominal lab conditions only, we ran a series of soaking and baking tests on samples from the same laminate family. We found that at 10GHz Df was 0.009 after a 24hour 110 Celsius bake, which increased threefold with a 2 hour soak in distilled water.

### Unreinforced resin laminates

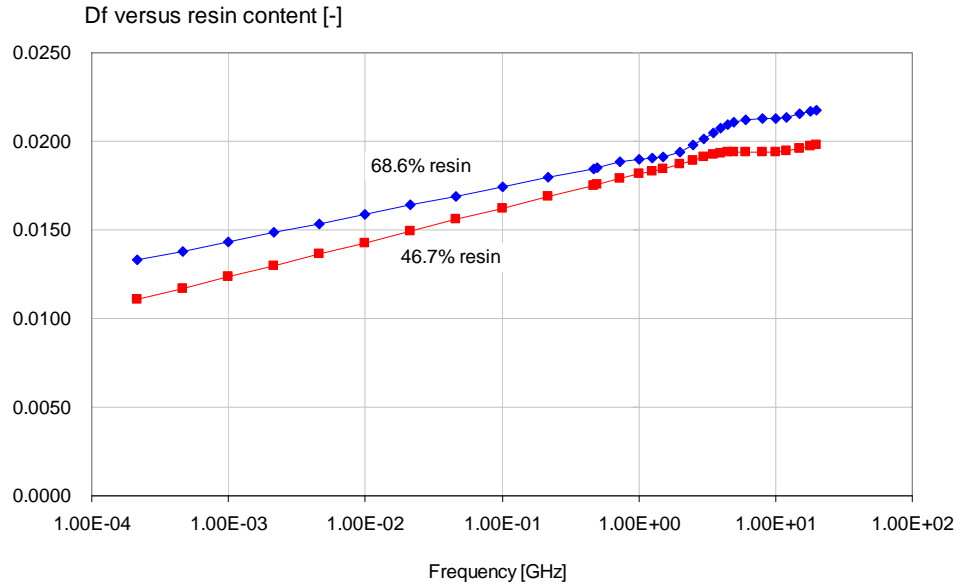
Though the DuPont FR0121A laminate is unreinforced, they are still layered vertically and therefore the question remains whether the orientation of test field when we use Parallel-plate fixture versus Split-Cylinder Resonator, may influence the result. To get some data points to answer this question, standard Oak Mitsui Technologies unreinforced BC24M and experimental laminates were also measured. The data is shown in *Figure 22*. Note that in both graphs the blue and red data points were obtained on different sample pieces with different instrumentation. The left graph clearly indicates that Df rises up to about 15 MHz and then it monotonically falls up to at least 1 GHz. This emphasizes the trend that we see in a less pronounced fashion in *Figure 15*, namely that Df rises first in the 1-10MHz range, followed by a downward slope to 1GHz or more.



**Figure 22:** Df of Oak Mitsui Technologies BC24M 1/1 (left graph) and experimental laminate (right graph). Blue data points: SUN Microsystems; red data points: courtesy of Oak Mitsui Technologies.

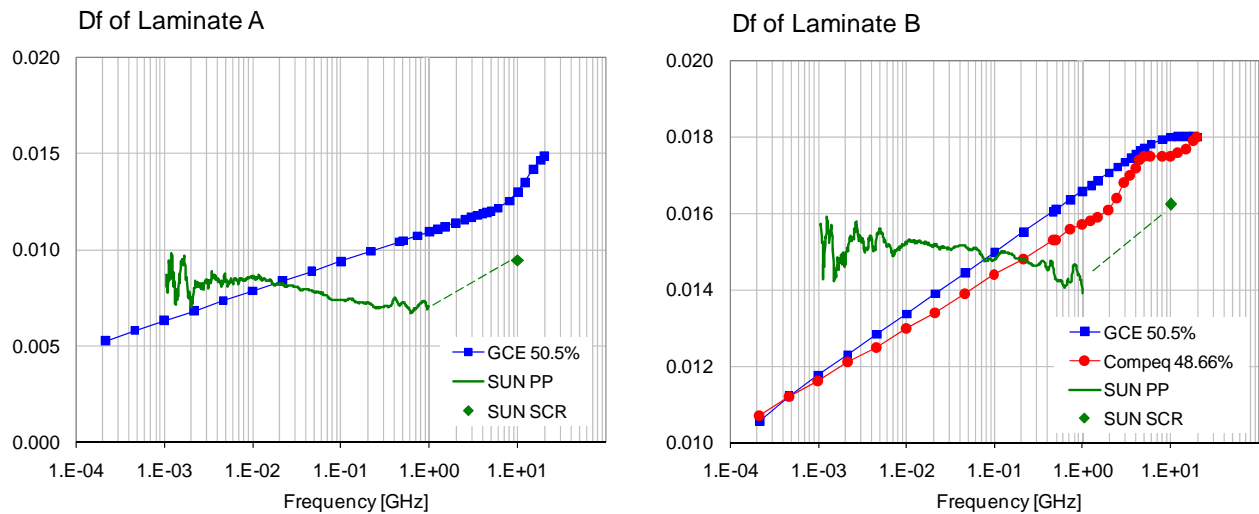
### 3. 5 Composite test results

Figure 23 shows Df data measured by Compeq on Laminate B samples by the Short Pulse Propagation (SPP) method. Note that the Df curves exhibit a monotonic positive slope in the entire 1 MHz to 10 GHz frequency range, with some wiggling above 2 GHz.



**Figure 23:** Df of Laminate B for two different resin contents, measured with SPP. Data courtesy of Compeq.

To compare data collected with different methods on nominally the same laminates, Figure 24 shows a composite graph for Laminates A and B taken on etched bare laminates with Parallel-plate fixture and Split-Cylinder Resonator measured at SUN and Short-Pulse Propagation method measured by Compeq and GCE.



**Figure 24:** Df of Laminate A (left graph) and Laminate B (right graph) with different measurement methods. SPP data courtesy of Compeq and GCE.

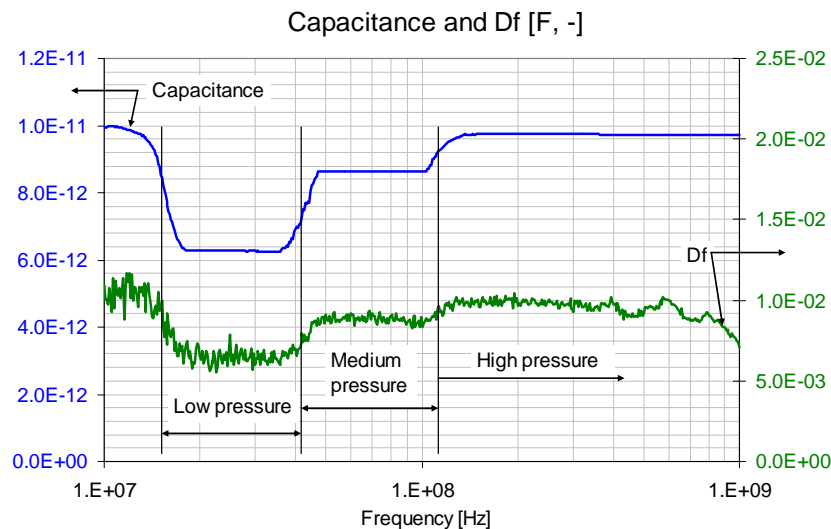
Note that the red trace of 48.66% resin content data is similar in resin content to the red trace in *Figure 23*. Note also that the SPP results shown here were taken on laminate samples with regular (rough) copper only and therefore SPP reports the effective Df of the laminate [15], which also contains the loss contributor associated with copper roughness. [15] also mentions the uncertainty of loss prediction due to the thin interface layer between the copper and laminate dielectric, which may have significantly higher resistivity than copper, thus contributing the increased effective Df reported by SPP. Microstrip and stripline methods based on wide-band de-embedding of conductor characteristics also show a positive trend in the extracted Df(f) function [16].

### 3. 6 Potential sources of errors

During our laminate-testing study we found that each measurement method we used had its own challenges, and its own potential sources of errors. This was especially important to take into account, since in several cases we had to use the equipment and fixture slightly outside of their recommended or specified range of DUT parameters. After repeating almost every kind of measurements many times over, also with different operators, we found that eventually the main signatures of the Df(f) curves were very repeatable with each setup.

#### Affect of electrode pressure with parallel-plate fixtures

It was found that especially with softer laminates, the electrode pressure did have a significant impact on both capacitance and Df data. *Figure 25* shows the result taken on a soft laminate (other than one of the four base laminates) during a single sweep, which with the particular settings, lasted for about two minutes. After the sweep started, the pressure-adjustment knob was quickly turned to the lowest pressure setting. After a stable portion of the reading, the knob was quickly turned to the mid-pressure settings, and later to the highest-pressure setting. This created the staircase function for both capacitance and loss.

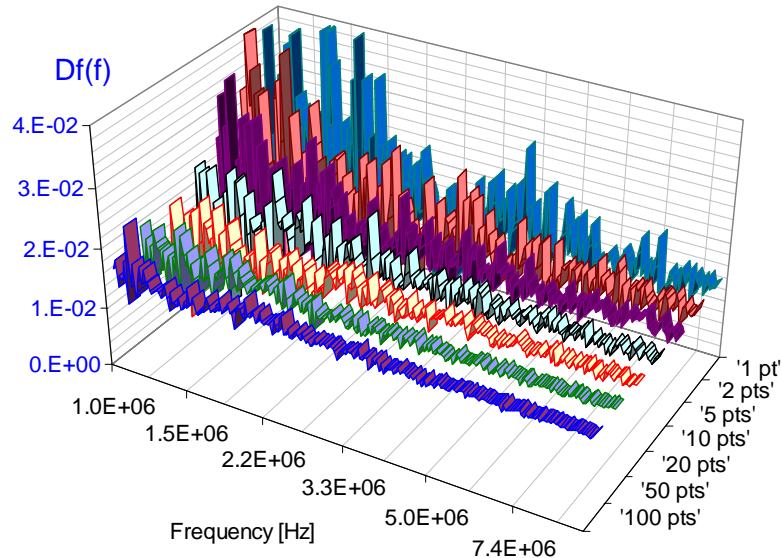


**Figure 25:** Impact of electrode pressure on the measured capacitance and Df.



### Impact of averaging

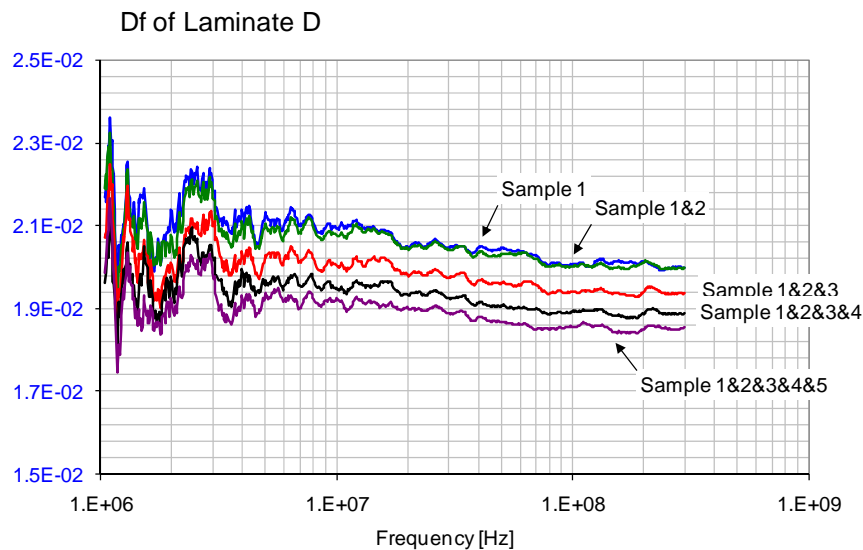
The E4991 Impedance Analyzer has a sweep average option, but strictly speaking there is no bandwidth setting. Instead, the user can select a number of point averages, so that the instrument takes the specified number of measurements and displays its average value before it steps to the next frequency point. *Figure 26* shows the impact of the point average number in the 1 – 10 MHz frequency range, where it is the most useful due to the high impedance value to be measured.



*Figure 26: Impact of point-average number on trace noise.*

### Impact of sample thickness and stacked samples

When bare laminate samples are measured with the Parallel-Plate fixture, the surface roughness of the sample creates air pockets and it reduces capacitance and loss readings. This effect can also be shown when multiple pieces of the same laminates are stacked.



*Figure 27: Impact of stacking on Df. Laminate D samples were measured in Parallel-Plate fixture.*

Five samples of Laminate D were first measured individually and found that their readings were reasonably close to each other. In the second step, the numbered samples were added to a stack, one at a time, and re-measured. *Figure 27* shows the result. Note that after adding the third sample, the  $D_f$  reading gets consistently lower. The fixture was set to its highest pressure level for all of the measurements.

## 4 Conclusions

Through our laminate study, which utilized multiple IPC methodologies, it was found that empirical data did not match the calculated wide-band Debye model, which predicts a positive  $D_f(f)$  slope over the entire frequency range of interest. In contrast we found that the majority of laminates we measured (not only low-loss laminates) had a  $D_f(f)$  slope trend which underwent multiple sign reversals. We found that the high-temperature baking turns the mostly positive slope of  $D_f$  in B-stage laminates into negative slope in C-stage laminates. It became also apparent that no one method that we looked at could accurately measure  $D_f$  alone over a sufficiently wide band of frequencies due to various limitation of the associated method. It was also evident that the different methods were better suited for different frequency ranges and purposes.

In this paper we have introduced an alternate methodology of estimating Loss Tangent ( $D_f$ ) called the Capacitance Gradient Method (CGM), which derives  $D_f$  from the change of capacitance with frequency over a measurable frequency range. When utilizing a differential form of the wide-band Debye model, we were able to obtain much better agreement between  $D_f(f)$  curves directly measured and estimated from  $C(f)$ . Because of the multiple reversals in slope trends, CGM can be used only in the frequency range where  $C(f)$  can be reliably measured. Therefore CGM's primary benefit is cross checking the results. The DUT size limited the upper frequency range due to the modal resonance of the structure but could accurately measure and predict  $D_f$  up to about 10 – 100 MHz, dependent on the sample size. At low frequencies CGM is not impacted by conductor losses and radiation effects. Additionally, capacitance can be measured more accurately than the imaginary part of complex permittivity.

Similar to CGM, the parallel plate method has an upper limit due to the test fixture resonance (around 1GHz). Additionally, the trapped air between the DUT and the fixture can skew the results to a lower  $D_f$ . The benefits of this method are that it has a wider frequency range than CGM (up to ~1GHz).

The benefits of the SCR method are the ability to measure at multi-GHz frequencies. The limitations include isolated measurement frequencies, in-plane field orientation, which is different from orientation in typical usage and potential interference of resonance modes.

$D_f(f)$  data from wide-band model-based solutions on actual interconnects don't seem to agree well with  $D_f$  data taken on laminates only. The likely cause is the presence of various additional loss sources in a real PCB interconnect. This suggests that even if we had an accurate enough procedure to obtain the true  $D_f$  profile of the laminate itself, it still would not be sufficient for design purposes without information on the additional

loss contributors, such as the metal-dielectric interface layer. SPP can capture the entire cumulative loss in an effective Df number, but by doing so it also links the dielectric properties, copper and PCB-process properties together.

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