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TecForum 11-MP2: Dynamic Characterization of DC-DC Converters

Part I: Dynamic Characterization of DC-DC Converters from a System's Perspective

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Abstract

The session starts with a brief overview of the converter block schematics and a short explanation of the basic operation of each block. Dynamic parameters are defined and their simulation and measurement options explained. It is shown how the crossover frequency and phase margin relate to the step response and output impedance characteristics. The session illustrates how compensation methods influence dynamic parameters. Simulated and measured data show that the control loop can have an effect on the output impedance even octaves above the crossover frequency. A simple test setup is used to measure transient step response, small and large signal output impedance and gain-phase plots. One simple test setup uses a dynamic load composed of a power FET with a small-valued source resistor across the converter output. The gate of the FET is driven with a step waveform or with a sinusoidal signal with a DC bias. This setup is used for both time and frequency domain testing.

Author(s) Biography

Istvan Novak is a Senior Principle Engineer at Oracle. Besides signal integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is a Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies.

Barry Williams is a principal engineer and a member of the technical staff at Oracle-Sun Microsystems since 2005. Before joining Oracle-Sun Microsystems, he worked for 17 years as principal engineer at Digital Equipment Corp - Hewlett Packard Co working in the VAX and Alpha Systems groups. Authored a book titled Power Distribution Systems for Electronic Circuits, and has co-authored several DesignCon papers that were presented. Graduate of Northeastern University.

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I. Introduction and background

The ongoing push for higher density and higher efficiency of our electronic systems makes distributed power distribution schemes with local DC-DC converters very attractive. The converters can provide isolation, if needed, and they can stabilize fluctuating raw input voltages and can convert the voltage value as well its polarity. Switching-mode DC-DC converters can achieve high efficiency and therefore their own power dissipation can be kept low, allowing the user to place them into thermally critical locations, close to the load. Another important trend in electronic design is dropping supply voltages and lower noise allowance on the supply rails. Together with the increasing speed and bandwidth of our circuits, these system trends mandate a holistic view of the performance of the DC-DC converters. The purpose of the paper is to provide an overview of the dynamic behavior of the converters, describing the inter-relationship of the transient step response, small and large signal output impedance, conventional gain-phase loop stability performance, and to show how these depend on the external system's power distribution network. The intended audience of the paper is the users and not the designers of the converters. For this reason the paper will not cover the actual selection of components, stress and loss calculations, rather it will orient the users what is reasonable to expect from the converters and how to avoid some common pitfalls associated with dynamic parameters.

DC-DC converters, or more specifically switched-mode DC-DC converters convert and many times also stabilize the input voltage to a pre-determined output value [1]. The switching action converts the incoming DC voltage to AC and it is then transformed through filters and/or transformers to produce the required output voltage. With transformer isolation the magnitude and polarity of output voltage with respect to the input voltage can be set by the output rectifier and turn ratio of the transformer, without changing the converter topology. When no isolation is needed between the primary and secondary sides, the energy storage elements can be simple inductors and/or capacitors. For inductor-capacitor storage, *Figure 1* shows the block diagrams of the three basic topologies.

One of the most widely used DC-DC converter scheme is the non-isolated buck converter. It has a pair of series-connected switches across the input rail, with the center node (also called the switch node) connected to an L-C filter. The two switches are turned ON and OFF alternating, which creates a periodical square stream of voltage pulses. The voltage pulses go through the LC filter, which passes the DC content, but sufficiently attenuates the switching waveform. An error amplifier monitors the difference between the output voltage or an attenuated version of it and a voltage reference. Through an appropriate filter circuit the error voltage controls the duty cycle (or the current) of the switches, thus keeping the output voltage constant, largely independent of the input voltage and load current. Assuming loss less components, the relationship among the input voltage (V_{in}), output voltage (V_{out}) and duty cycle of the switches (D) is described by

$$D = \frac{V_{out}}{V_{in}} \qquad (1)$$

The current in the inductor ramps up during the ON time of the upper switch and ramps down during the OFF time; with no losses in the circuits the ramps are linear and the current waveform resembles a saw-tooth. In the steady state *Continuous Mode*, the average of the inductor current equals the current supplied to the load. Note that the input current required by the switches is non-continuous: when the top switch is OFF, no current is required from the input; when the top switch is ON, the input current waveform equals the current waveform of the inductor. This also means that even

though the average input current is lower than the output current, the peak current values are the same.

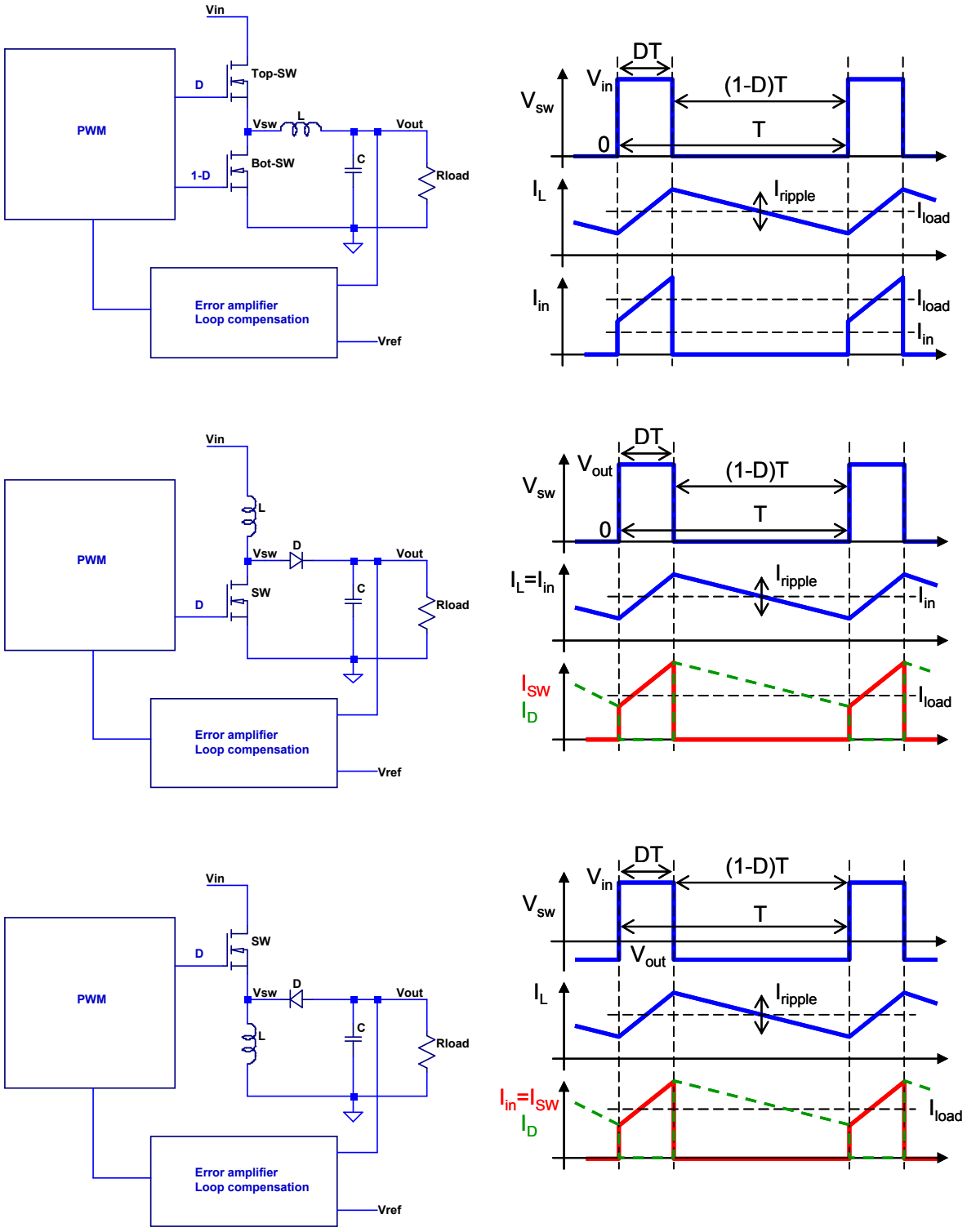


Figure 1: *Non-isolated DC-DC converters with inductor filtering for the buck (top), boost (middle) and buck-boost (bottom) topologies. Block schematics on the left, typical idealized waveforms on the right.*

When we need a non-isolated output voltage higher than the input voltage, we can use the boost converter topology. The inductor is now placed in series to the low-side switch and the switch node is connected to the output through a rectifying diode. When the switch is ON, the input voltage is connected across the inductor, and the current ramps up. When the switch turns OFF, the current cannot jump in the inductor, and the voltage at the switch node shoots up (inductive overshoot). The overshoot voltage is clamped by the diode to DC voltage of the output capacitor. In steady state *Continuous Mode* the switch node voltage swings between zero and the output voltage. For a loss-less circuit, the relationship among the input voltage (V_{in}), output voltage (V_{out}) and duty cycle of the switches (D) is described by

$$D = 1 - \frac{V_{in}}{V_{out}} \qquad (2)$$

In the boost converter the inductor is in series to the input and therefore the input current does not have jumps; this simplifies the input filter requirements. However, we now have a switch in series to the output and therefore guaranteeing low ripple on the output will require lower-impedance capacitors.

When the polarity of the input and output voltages are different, we use the buck-boost topology. The inductor now replaces the lower switch. With positive input voltage, the inductive overshoot, when the top-side switch turns OFF, creates a negative undershoot. The voltage at the switch node alternates between V_{in} and V_{out}, where the two voltages have different signs. For a loss-less circuit, the relationship among the input voltage (V_{in}), output voltage (V_{out}) and duty cycle of the switches (D) is described by

$$D = \frac{V_{out}}{V_{out} - V_{in}} \qquad (3)$$

In the buck-boost converter there is a switch in series to both the input and output and therefore the current fluctuation is large at both terminals.

Dynamic specification items

There are many possible items to specify for a DC-DC converter. They fall under several categories, among possibly others, electrical and functional requirements, mechanical, thermal and reliability specifications. In this tutorial we focus on electrical requirements, within which there are a number of sub-categories: absolute maximum voltage and current ratings, static and dynamic output voltage parameters, loop stability and periodic noise (PARD) requirements.

Dynamic specifications for a DC-DC converter can be captured in various ways. Ultimately our goal is to minimize the variation of the output voltage due to sudden changes in input voltage and load current. Traditionally the dynamic requirements were captured by the load-step response and phase margin.

Many DC-DC converters regulate the output, in the typical case the output voltage, to remain as constant as possible in spite of fluctuations in input voltage and load current, as well as environmental effects, such as temperature and aging. If it was possible to construct an ideal converter with no losses and a source with zero source impedance, the converter's output voltage would depend only on the input voltage, the other dependencies would cancel. Interestingly though

it was proven decades ago that theoretically it is impossible to achieve power transfer through a network of loss-less linear passive components [3]. In any practical circuit the source impedance is finite, converter components have losses and their parameters vary with temperature and aging. For all the above reasons the converter's output voltage will depend on those secondary parameters as well. To minimize the change in the output voltage, it is monitored by an error amplifier, and a feedback loop tries to keep it constant. For a buck converter, the feedback loop is shown in *Figure 2* [4].

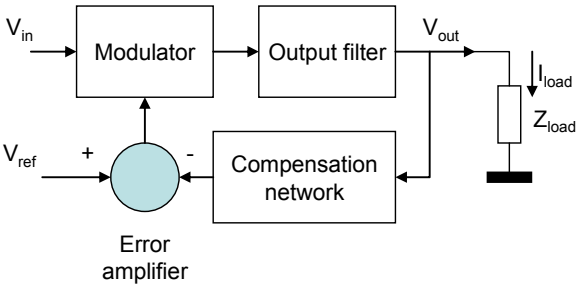


Figure 2: *Block schematics of the feedback loop of the buck converter.*

The *Modulator*, *Error amplifier* and *Compensation network* blocks in *Figure 2* can be implemented either in analog, highly time invariant and linear circuits, or in fully digital implementations, or anything in between. The *Modulator* block is always nonlinear and time variant in its heart, since it contains switches. However, the rest of the feedback loop, and primarily the *Output filter*, limit the active bandwidth of the loop so significantly that a linear, state-averaged model is very often provides suitable and accurate enough description. By applying a linearized model to each block, we can calculate the overall loop gain around the closed feedback loop and apply the conventional stability criteria during the design and analysis processes. By denoting the Modulator gain by G_M, Output filter gain by G_F, Compensation network gain by G_C and Error amplifier gain by G_{EA}, the total loop gain can be described as:

$$G_{loop} = G_M \; G_F \; G_C \; G_{EA} \tag{4}$$

Output filter

The equivalent circuit of the output filter is shown in *Figure 3*.

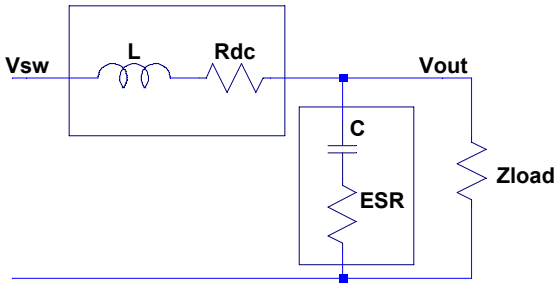


Figure 3*: Circuit schematics of the Output filter block.*

The LC output filter is simplified. We know that the inductance of the power inductor may be nonlinear and dependent on the output current, furthermore its resistance is frequency dependent. The output capacitor has frequency and voltage dependent capacitance and frequency dependent equivalent series resistance and inductance. For loop gain calculation purposes we usually ignore those second-order dependencies and use the frequency-independent parameters of *Figure 3*. One notable difference is the presence of Z_{load} in the filter circuit. It represents the cumulative impedance of external capacitors and load circuit(s). While it is not part of the original DC-DC converter circuit, we cannot leave it out, because it is directly in the feedback loop. The series impedance of the inductor is $Z_L = R_{dc} + j\omega L$. The impedance of the output capacitor is $Z_C = ESR\text{-}1/(j\omega C)$. With the above notations the voltage transfer function of the output filter is:

$$G_F = \frac{Z_{load} \parallel Z_C}{Z_L + Z_{load} \parallel Z_C} \tag{5}$$

Assuming for now that Z_{load} is infinite and using the circuit elements of *Figure 3*, G_F becomes:

$$G_F = \frac{1 + j\omega\, ESR\, C}{1 + j\omega(R_{dc} + ESR)C - \omega^2 LC} = \frac{1 + j\omega\, ESR\, C}{1 + jQ^{-1}\dfrac{\omega}{\omega_0} - \left(\dfrac{\omega}{\omega_0}\right)^2} \tag{6}$$

where $Q = \dfrac{\sqrt{L/C}}{R_{dc} + ESR}$ $\quad \omega_0 = \dfrac{1}{\sqrt{LC}}$

This is a second order transfer function and dependent on the Q, it may have substantial peaking. *Figure 4* shows the possibility of peaking as Q varies. On the right G_F is shown with nominal values for the converter circuit shown later in *Figures 16* and *17*.

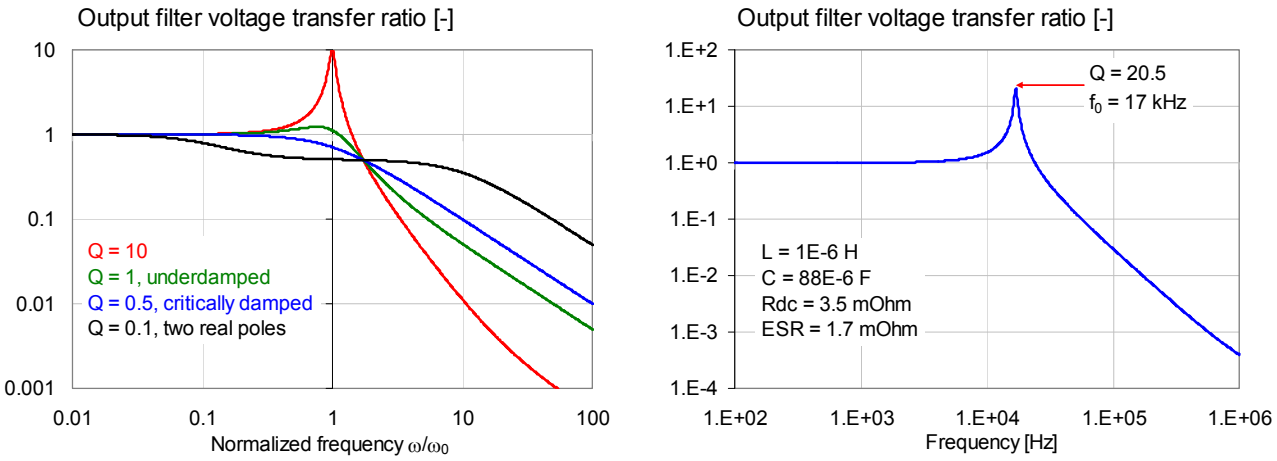


Figure 4: *Transfer function of the output filter.*

To get a reasonably high attenuation at the switching frequency, the f_0 corner frequency has to be much lower than the switching frequency. The value of the inductance is primarily determined by the switching frequency and input/output voltages and load current. To achieve high efficiency and

to keep the output ripple low, the series resistive losses in the inductor and capacitor are kept low. This leaves us with only one parameter, the *C* capacitance, to set the desired Q. To lower Q, we need to increase the capacitance, which in turn lowers the corner frequency of the filter and slows down the response of the loop. As we see on the right-side plot of *Figure 4*, in typical circuits we usually end up with a relatively high Q of the output filter and we count on the active feedback loop to provide damping.

Modulator

As shown in *Figure 5*, in voltage-mode buck regulators the Modulator compares the output of the Error amplifier against a saw-tooth waveform with a peak-to-peak value of V_{osc} and drives the output switches, which produce the switched waveform with approximately V_{in} peak-to-peak value. Assuming negligibly small delay in the comparator and output switches, the transfer function of the modulator is the ratio of the voltages:

$$G_M = \frac{V_{in}}{V_{osc}} \tag{7}$$

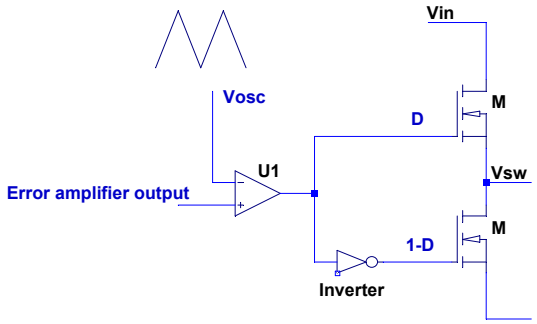


Figure 5: *Equivalent circuit of the Modulator stage.*

In current-mode control schemes a compensation ramp has to be added to the saw-tooth waveform to avoid sub-harmonic oscillation with D>0.5 duty cycles [5]. From a small-signal point of view the resulting modulator gain is the same as in voltage-mode control [6].

Error amplifier and Loop compensation

Many control systems with feedback loops use a proportional-integral-derivative controller (PID controller), which date back to the late 19th century [7]. Dependent on the nature of the loop, one or two of the features may be missing (see below). Whether it is fully analog or fully digital implementation, or anything in between, there is a certain gain or attenuation and phase shift associated in each of the modules making up the control loop. When the loop is closed, the first and utmost important goal is to make sure that the loop gain becomes less than one before the accumulated phase shift turns the negative feedback into positive, accidentally creating an oscillator. The Modulator and Output filter blocks in the feedback loop are determined by the required functionality of the converter and there is just so much we can do to adjust the complex gain in those stages. The necessary adjustment of the magnitude and phase of gain is achieved in a dedicated Loop compensation module. For sake of convenience it is easier to consider the Error amplifier and Loop compensation as one block.

There are three typical implementation options for shaping the gain-frequency curve [8]. We can use an integral-only compensation, this is called Type I (I). The proportional-integral compensation is called Type II (PI), and finally the proportional-integral-derivative compensation is called Type III (PID). The three types of basic compensations create poles and zeros to shape the gain-frequency curve. Though one might be able to create an analog circuit implementation where each pole and zero could be set independent of the others, low-cost implementations group the compensation components around the error amplifier, by placing R-C components between the output and inverting input of a voltage-mode operational amplifier, or by placing a shunt R-C network at the output of a trans-conductance amplifier. The derivative function of the Type III compensation is usually achieved by placing R-C components around the voltage divider connecting the output of the regulator to the input of the error amplifier. This solution has the limitation that the amount of available phase boost from the extra R-C element diminishes as the nominal output voltage gets lower. The interaction of poles and zeroes also creates sub-classes of compensation types [9].

Figure 6 shows possible circuit representations and their transfer functions with the compensation components around a voltage-mode operational error amplifier [4]. Type I compensation is the simplest, merely an integrator, which can always make the loop stable at a price of potentially very low bandwidth. The Type II compensation adds a pole-zero pair (ω_2 and ω_{12}), which gives a 90-degree phase boost in the frequency range between the two roots. If further phase boost is needed, another pole-zero pair can be added in the Type III compensation. In all three compensations shown in *Figure 6* we assume that the open-loop gain curve of the operational amplifier is safely above the gain curve required by the feedback network.

Once we know the contributing gain elements, the closed loop parameters can be calculated. The basis for all closed-loop parameters is the G_{loop} total loop gain around the feedback loop. *Figure 7* shows a possible $G_{loop}(f)$ function, also called Gain-Phase curves, with a Type III compensation circuit. Though for any physically realized circuit the magnitude and phase curves are inter-related by the causality constraints and therefore one cannot be set independently from the other, plotting magnitude and phase on the same chart helps gaining the necessary insight about the dynamic performance of the loop. There are three important parameters to be pointed out on the Gain-Phase curves. The *Crossover frequency* is where the declining loop gain (first) reaches unity value as frequency increases. The phase value at that point is called the *Phase margin*. A positive phase margin is necessary to create margin against parameter variations and/or to limit the tendency of peaking and ringing of the dynamic parameters (see later). The third important parameter is the *Gain margin*, the value of gain where the phase margin first drops to zero as frequency increases. The cross-over frequency and phase margin are marked and highlighted in *Figure 7*. The frequency of the Gain margin point is outside of the plotting scale with the chosen values.

Using the $G_{loop}(f)$ function, we can express the major small-signal dynamic parameters associated with the input parameters in *Figure 2*. V_{out}/I_{load} represents the closed-loop output impedance, V_{out}/V_{in} represents the transfer function from the supply voltage to the output and finally V_{out}/V_{ref} is the transfer function associated with the reference voltage. The three parameters are listed here in order of importance or significance in today's typical converters. Each of the three can be expressed either in the frequency domain as complex frequency plots or in the time domain as responses to a step stimulus.

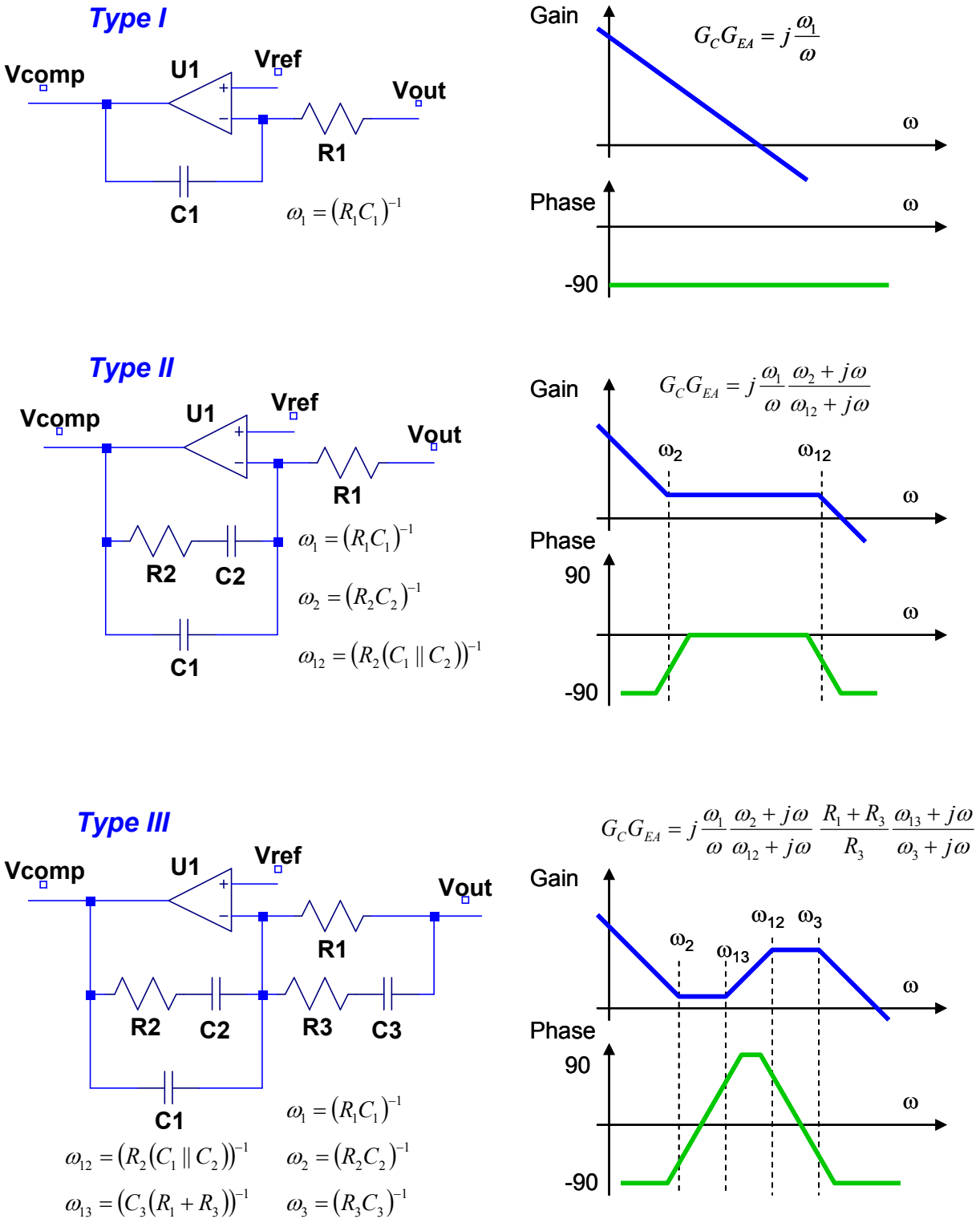


Figure 6: *Type I, Type II and Type III loop compensation circuits and their transfer functions.*

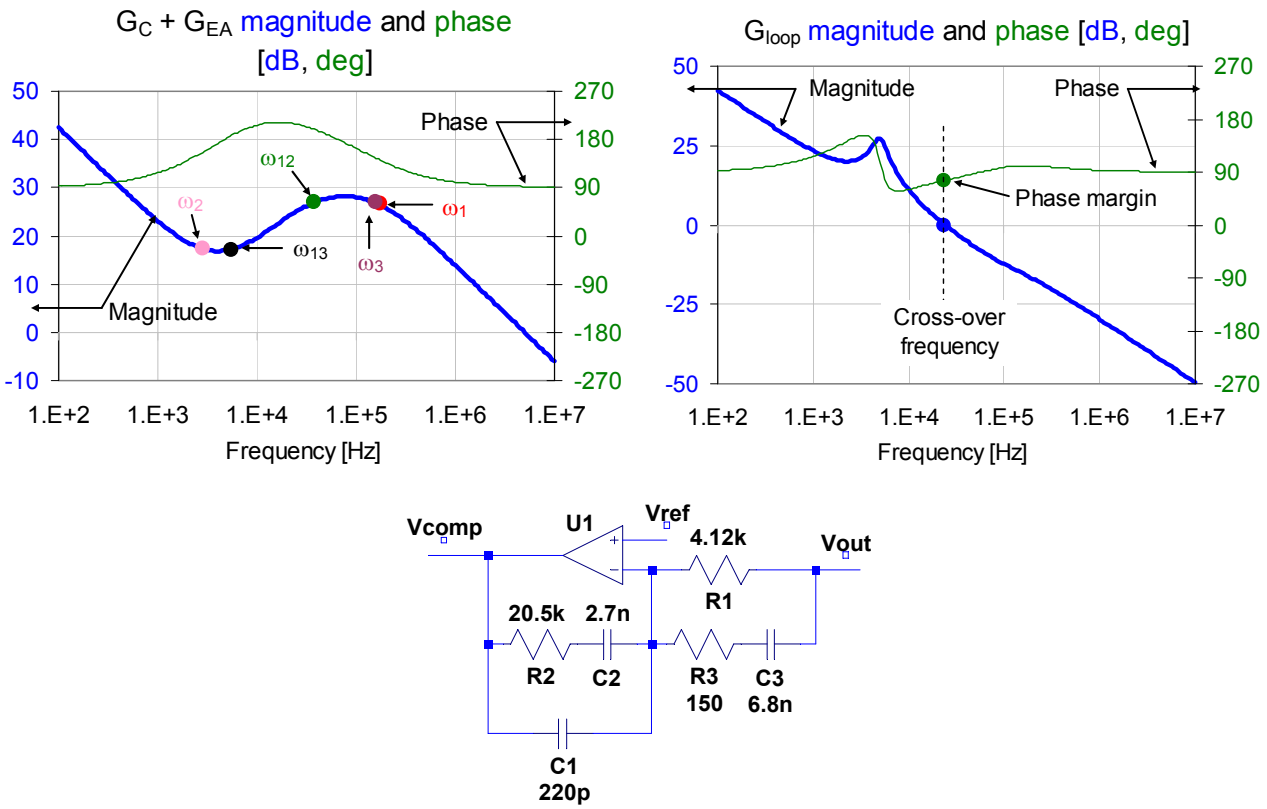


Figure 7: *Typical Gain-Phase compensation curves with Type III compensation on the top left and the resulting Loop gain with voltage-mode control on the top right. The compensation component values are shown in the schematics on the bottom [4]*

The closed-loop output impedance can be calculated by further simplifying the block diagram of *Figure 2*. We assume that the $Z_{\text{out-open-loop}}(f)$ open-loop output impedance equals the Output filter's impedance with either the low or high-side switch ON (for the voltage-mode control schemes) or both switches OFF for the current-mode control scheme [10].

$$Z_{out-closed-loop}(f) = \frac{Z_{out-open-loop}(f)}{1 + G_{loop}(f)} \tag{8}$$

The current-mode control effectively removes the switches' and the input source's finite impedance from the output impedance. With voltage-mode control, however, to account for the impedance peaking accurately, we may need to include the weighted average of the source impedance seen through the low-side and high-side switches. The open and closed loop output impedances with the equivalent circuit of open-loop output impedance are shown in *Figure 8*. As opposed to *Figure 3*, this equivalent circuit and the resulting impedance plots also account for the series inductance of the output capacitor.

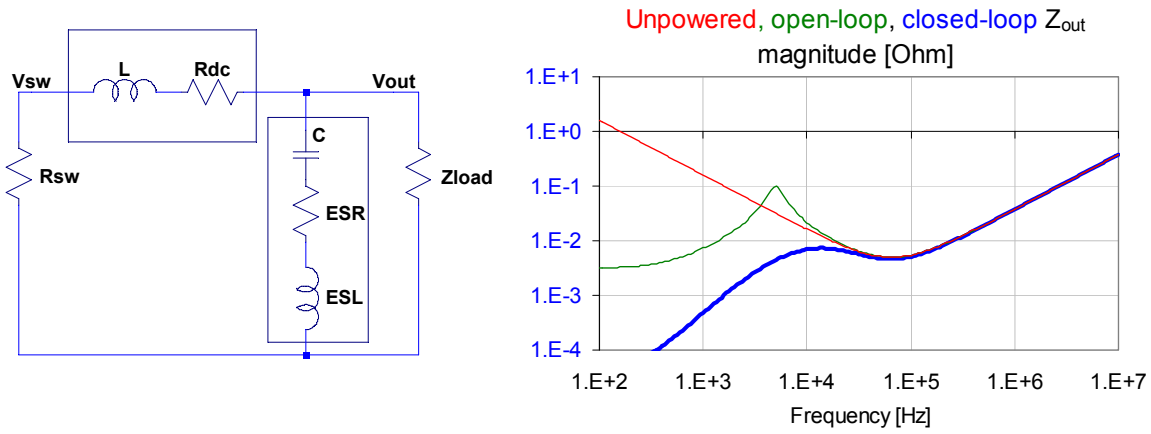


Figure 8: Simulated open-loop and closed-loop output impedance of a non-isolated buck converter with voltage-mode control on the right. The equivalent output circuit is shown on the left. The compensation circuit from Figure 7 is used.

The V_{out}/V_{in} transfer function can also be calculated from the block diagram of *Figure 2*.

$$\frac{V_{out}}{V_{in}} = \frac{G_M G_F}{1 + G_{loop}} \tag{9}$$

In certain demanding applications we may also want to place specification requirements on some dynamic parameters, which are usually not on the data sheet today. One such item could be the high-frequency burst-ringing associated with the main switching edges [11], which at the converter output can be significantly higher than the switching ripple itself [12]. The ringing is generated by second-order circuit elements, through parasitic inductances and capacitances. Since parasitic elements may be hard to control [13] and specify, as well as the high-frequency nature of the ringing makes it's testing and verifications dependent on layout and several other factors, the burst-ringing waveform is often not listed on the data sheet.

II. Dynamic parameters of DC-DC converters from a system's perspective

In today's systems the DC-DC converters are part of a larger power distribution network. The power distribution network itself has a supporting function for the electronics: among other tasks, it has to provide clean power for the active circuits. In this ecosystem the DC-DC converter has its own role within the limited frequency range where it can influence the supply rail: it is responsible for the low frequency response of the supply rail. The mid and high-frequency bypassing is left to external bypass capacitors. The wide-band transient noise excitation of the supply rail has a broad spectral content and it simultaneously exercises the various components, which target different frequency ranges. At the end we have to make sure that the various components of the supply rail play together nicely so that they minimize the noise voltage for any given transient excitation. The most important interactions are between the DC-DC converter output and the external bulk

capacitors. It was realized in the 90s that intentionally raising the low-frequency output impedance of DC-DC converters may cut the transient noise by a factor of two. The concept of *Adaptive Voltage Positioning* [14] was later extended to the mid-frequency capacitors and the *Extended Adaptive Voltage Positioning* was born [15]. At about the same time it was found that as long as the cumulative behavior of the power distribution network can be considered linear and time invariant, its worst-case noise response to any arbitrary sequence of current steps with bounded magnitude and slew rate can be obtained through a process called Reverse Pulse Technique [16].

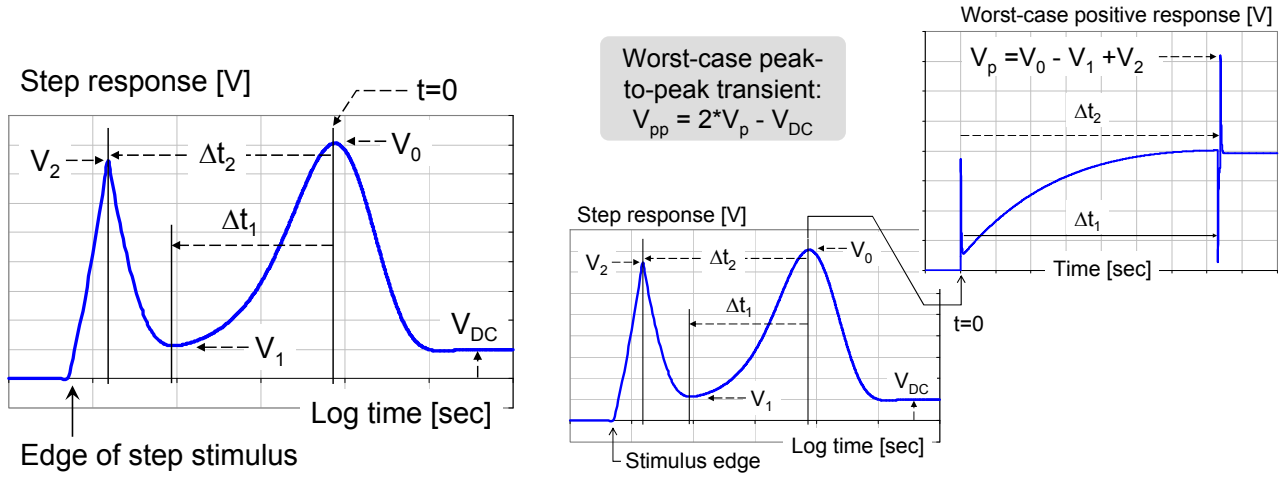


***Figure 9**: Summary of the Reverse Pulse Technique.*

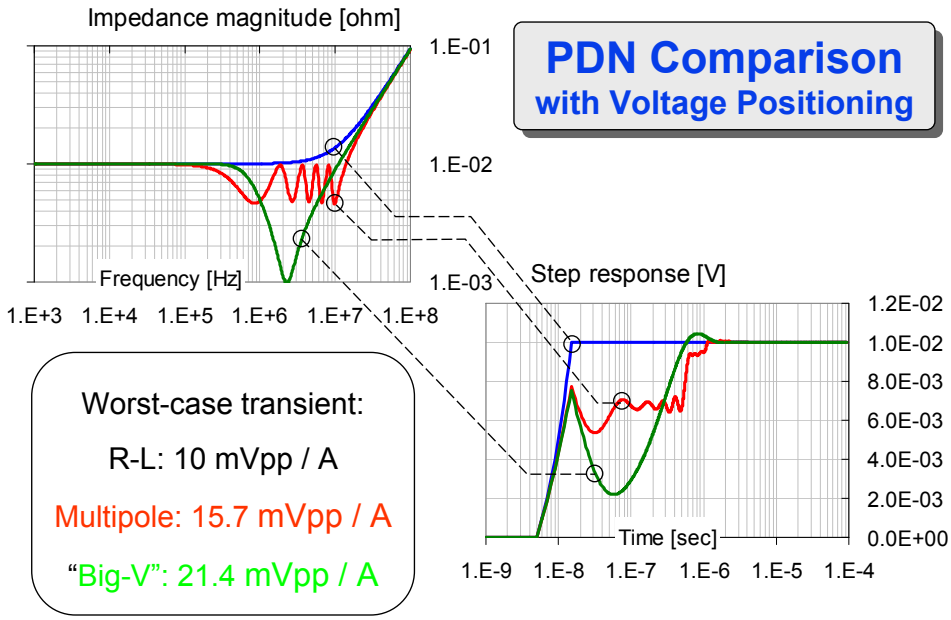


***Figure 10a**: Comparison of worst-case transient noise for three different impedance synthesis approaches with Adaptive voltage positioning.*

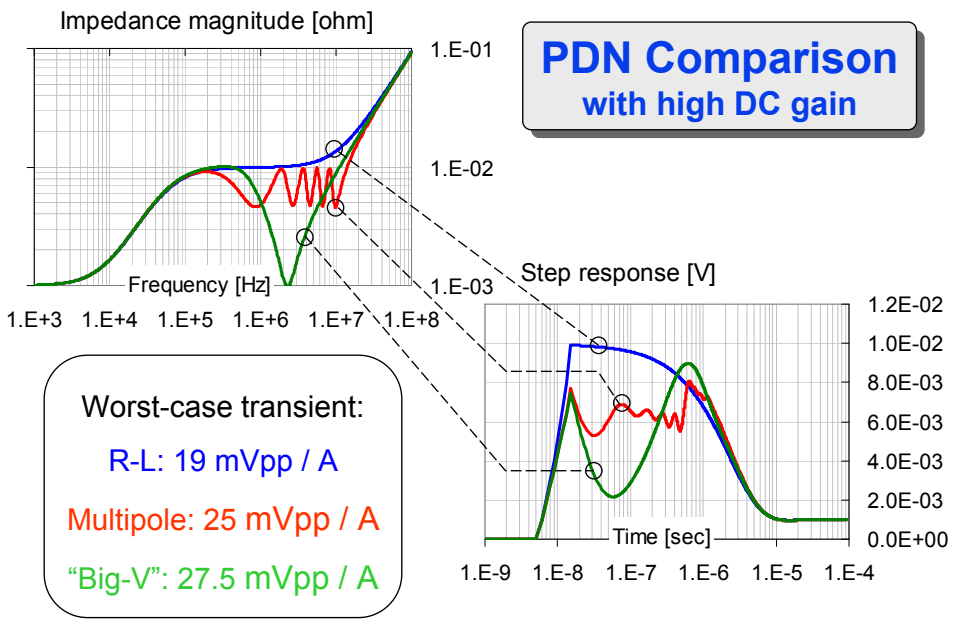


***Figure 10b**: Comparison of worst-case transient noise for three different impedance synthesis approaches without Adaptive voltage positioning.*

The Reverse Pulse Technique uses the Step Response of the power distribution network to calculate the worst-case noise. The Step Response is the time integral of the Impulse Response; furthermore the time-domain Impulse Response and frequency-domain impedance profile of the power distribution network form a Fourier pair. This gives us a very powerful and universal tool to obtain the worst-case transient noise information: we can get the Step Response either by directly measuring or simulating it in the time domain, or through a Fourier process by using simulated or measured impedance profile. Using the PDN impedance as the primary input gives us further insight how the worst-case noise can be minimized. Since the Reverse Pulse Technique sums up the peaks and valleys in the Step Response, the lowest noise is obtained when there are no peaks and valleys in the Step Response, only a monotonic change. A monotonic Step Response in the time domain is equivalent to a flat impedance response in the frequency domain. This is illustrated in *Figure 10* by comparing various PDN design options to synthesize a given target impedance.

We can see that across all examples included in *Figure 10,* the lowest worst-case transient noise comes from the PDN with the highest, but most flat impedance profile. Though we don't necessarily want to or have to create flat impedance profiles for all of our PDNs, this realization is helpful to guide us in our design decisions. Flat impedance profiles require low-Q components and systems [17], [18]. The takeaway for DC-DC converter selection or design: we may want to make sure that the output impedance of the converter provides a flat impedance continuation as it hands action over to the bulk capacitors.

When two impedances are parallel connected, at frequencies where one is inductive and the other is capacitive, an anti-resonance impedance peak develops unless the R-L and C-R impedances are matched as shown in *Figure 11* [19]. This aspect will be looked at in the next section.

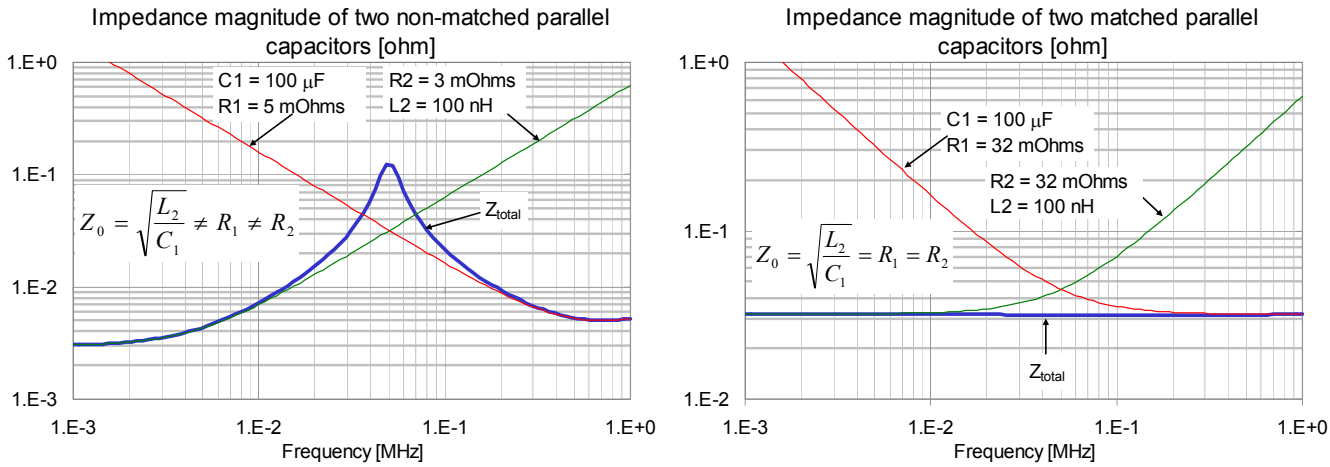


***Figure 11**: Anti-resonance peaking of un-matched (left) and matched (right) parallel-connected impedances.*

III. Output impedance of DC-DC converters

As it was shown earlier, in many applications DC-DC converters can be approximated with an averaged linearized model. We also saw that the flatness of the overall impedance profile of the power distribution network is a helpful feature to minimize worst-case transient noise. We can conclude that the output impedance profile is a useful measure for those DC-DC converters, which can be approximated properly with a linearized model. Equation (8) tells us how we can calculate the output impedance if we know the open-loop output impedance and loop gain function. We can take the component parameters from the right-hand chart of *Figure 4* and plot the open-loop output impedance assuming voltage-mode and current-mode controls. *Figure 12* shows the result. Note that for now we assume that the input-side source impedance as well as the resistance of the switches is zero. Note that the open-loop output impedance for current-mode control effectively removes the inductor from the picture and the impedance, instead of a parallel L-C circuit, becomes the impedance of the output capacitor(s). At low frequencies this introduces an extra pole in the overall transfer function.

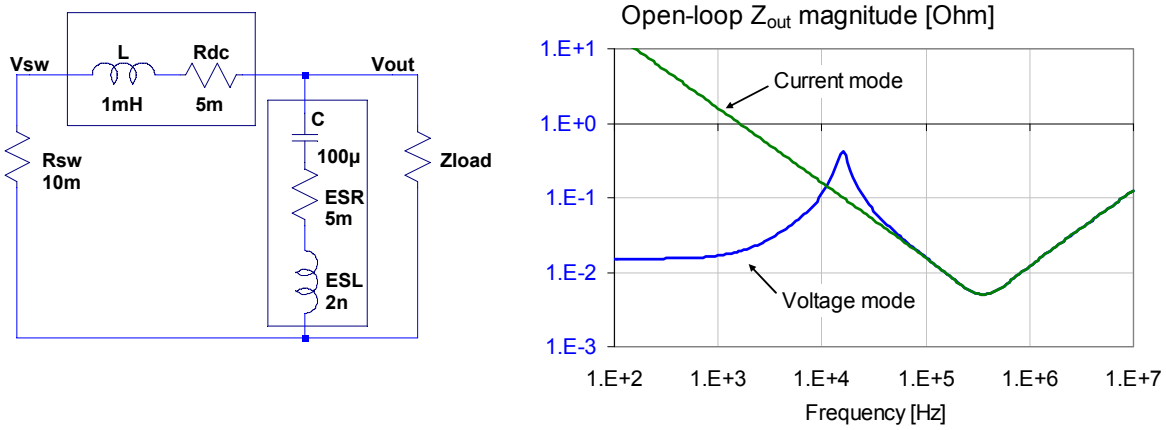
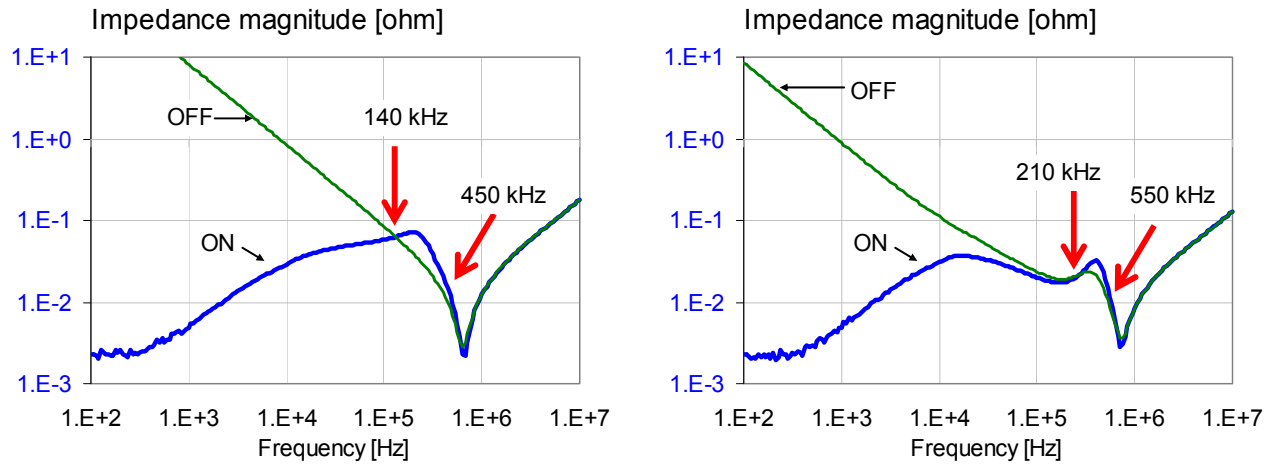


***Figure 12**: Equivalent schematic for open-loop output impedance on the left and typical impedance plots on the right.*

When we close the loop, we expect the output impedance to drop. This in fact will happen at lower frequencies, where the loop gain may be high. As the loop gain drops with increasing frequencies, the influence of the loop diminishes. Unfortunately, however, until the magnitude of the gain becomes much less than one, the complex denominator in Equation (8) may, and in fact most of the time does, increase rather than decrease the closed-loop output impedance. As a result, at the crossover frequency we almost always have some peaking, an increase of impedance magnitude with respect to the open-loop output impedance. Moreover, at higher frequencies we can still have peaking or increase of impedance, especially when Type III compensations are used, which can boost the phase margin and push out the crossover frequency, at a price of creating a wider frequency range where the loop gain may linger just slightly below unity. This phenomenon is illustrated in *Figures 13-15*.



***Figures 13-14**: Measured output impedance plots of two converters.*

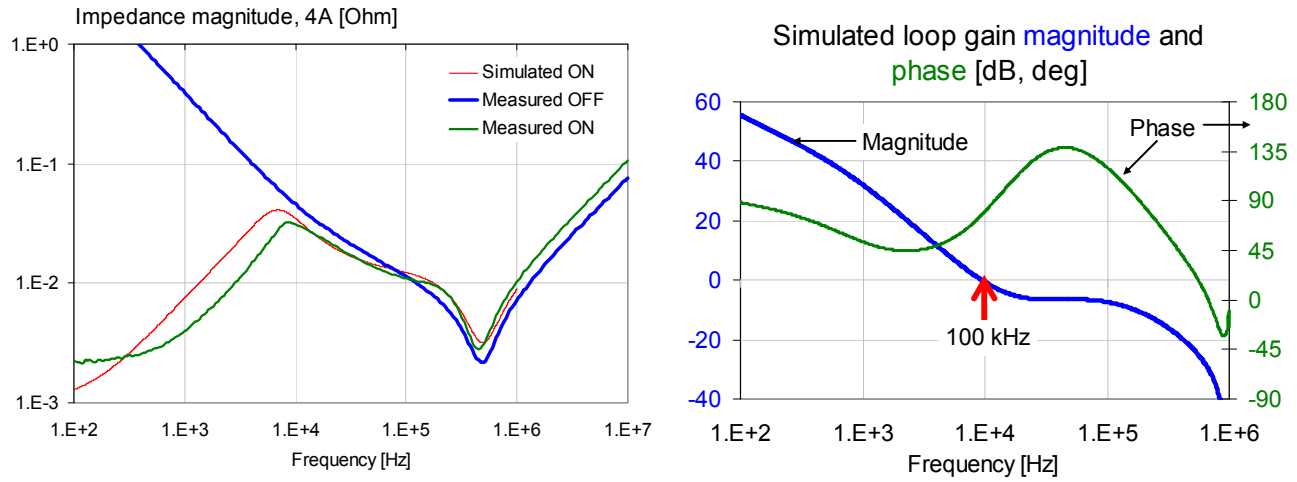


***Figure 15**: Measured and simulated output impedance of a converter (on the left) and Gain-Phase curve of the same converter on the right.*

How source impedance influences output impedance

It has been known for long that the dynamic input resistance of a DC-DC converter with closed feedback loop is negative and this can ultimately create self-oscillation in the input filtering circuit, see for instance [20]. The negative input resistance can also increase the output impedance in certain frequency ranges, where the source impedance becomes too high.

To understand this phenomenon, we need to look at the static and dynamic input resistance first. For this we assume that the control loop keeps the output voltage at a fixed V_{out} value. We also assume a constant I_{load} load current and V_{in} input voltage. With these starting parameters the converter delivers $P_{out} = V_{out} * I_{load}$ output power. If the converter had no losses, the input power would equal the power delivered to the load. With η efficiency, the power requirement on the input is 1/η times higher: $P_{in} = P_{out} / \eta$. The input current becomes: $I_{in} = P_{in} / V_{in} = (V_{out} * I_{load}) / (\eta * V_{in})$. Finally the static input resistance is:

$$R_{DC} = \frac{V_{in}}{I_{in}} = \eta \frac{V_{in}^2}{V_{out} I_{load}} \quad (10)$$

For instance, a converter providing 4A load current with 1.8V output voltage, and working with 80% efficiency (η = 0.8) out of a 3.3V input rail, will exhibit a static input resistance of 1.21 Ohms.

To get the incremental or dynamic input resistance, we need to consider what happens to the input current when the input voltage changes. If we assume that the output voltage stays the same (ideal line regulation), the output power also stays the same. If furthermore we assume that the efficiency is also constant, the input power will not change either. If the input voltage goes up and input power stays the same, the input current has to decrease. For a positive change in input voltage we get a negative change in input current; in other words the incremental input resistance is negative.

We can calculate the value of the incremental input resistance either analytically or numerically. For the analytical calculations we assume that the input voltage changes a little from V_{in} to $(V_{in} + \Delta V)$.

$$r_{in} = \frac{\Delta V}{\Delta I_{in}} = \frac{\Delta V}{\frac{V_{out} I_{load}}{\eta (V_{in} + \Delta V)} - \frac{V_{out} I_{load}}{\eta V_{in}}} = -\eta \frac{V_{in}^2}{V_{out} I_{load}} = -R_{DC} \quad (11)$$

The above equation tells us that the negative dynamic input resistance is simply the DC input resistance with a negative sign. As it was said above, this is true as long as the line regulation is very tight and the efficiency can be considered constant. In practical applications the load regulation can be (and usually is) tight, but the efficiency does change somewhat as the input voltage changes. Note also that the negative input resistance does not depend on the load regulation (as long as the line regulation is tight) and therefore the same negative input resistance expression applies to converters with a finite load line (or droop control).

To see what effect the negative input resistance may have on the output impedance, we start with a measured example. *Figure 16* shows the output impedance of a non-isolated buck converter, stepping down a 3.3V input voltage to 1.8V output voltage with a rated maximum current of 4A. The plot on the left is a full impedance magnitude plot as a function of frequency and load current. The plot on the right shows the impedance magnitude and phase as a function of frequency at 3.5A load current. There are two peaks in the impedance profile: a sharp peak at 42 kHz (marked by a red arrow) and a somewhat broader peak at 250 kHz. Note that the peak at 250 kHz does not change with load current, whereas the peak at 42 kHz does: it increases monotonically as load current increases.

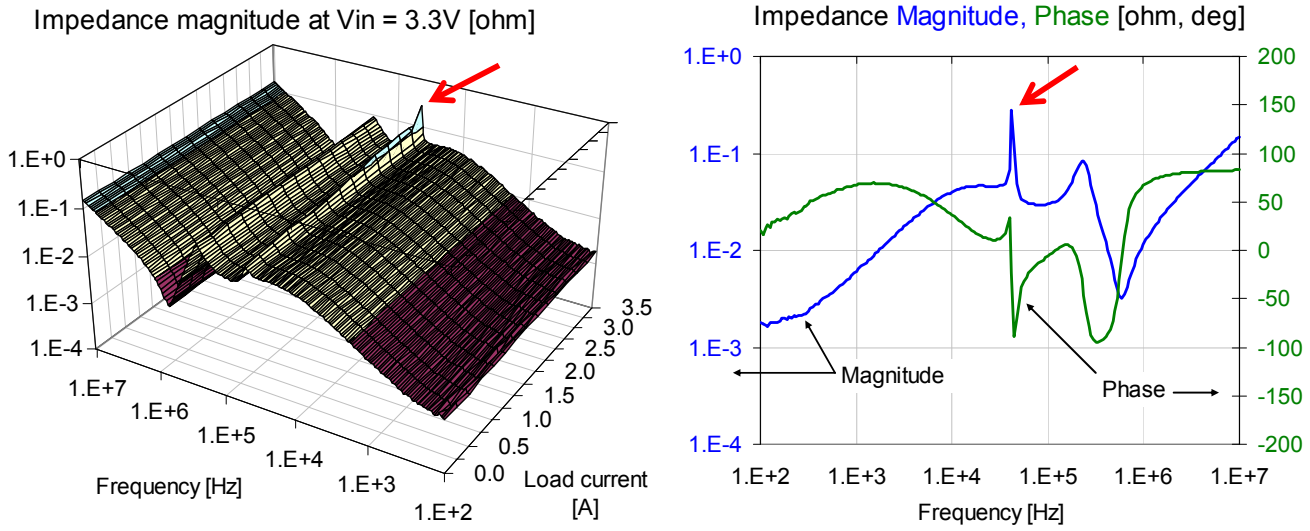


***Figure 16**: Measured output impedance profile of a DC-DC converter with 3.3V input voltage.*

It was found that the sharp ridge at 42 kHz changes with input voltage as well. *Figure 17* shows the same plots with 5V input voltage. The peak at 250 kHz did not change. However, the peak magnitude at 42 kHz decreased from 280 mOhm at 3.3V to 78 mOhm at 5V.

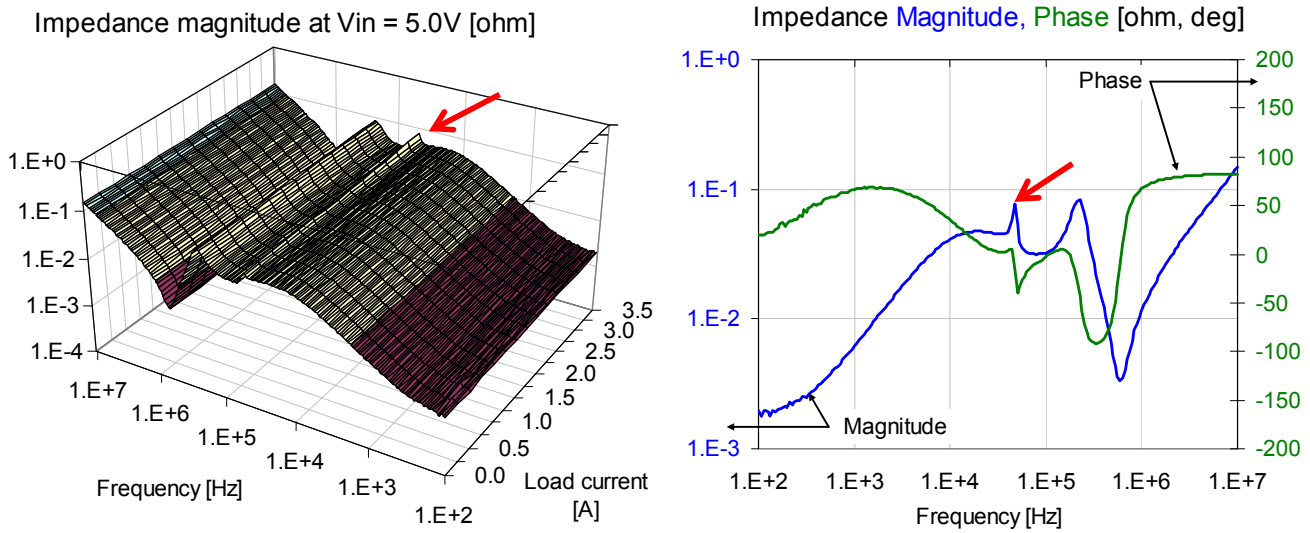


***Figure 17**: Measured output impedance profile of the same DC-DC converter with 5V input voltage.*

To rule out measurement errors or potential side-effects from the measurement setup, further tests were conducted: the output impedance was also measured with large-signal sinusoidal measurements and the Gain-Phase stability plot was obtained. Eventually all of them agreed: at 42 kHz there was a sharp resonance in all responses. *Figure 18* shows the measured small-signal output

impedance and Gain-Phase plots side-by-side for a similar converter, where the sharp peaking occurred at a slightly lower frequency.

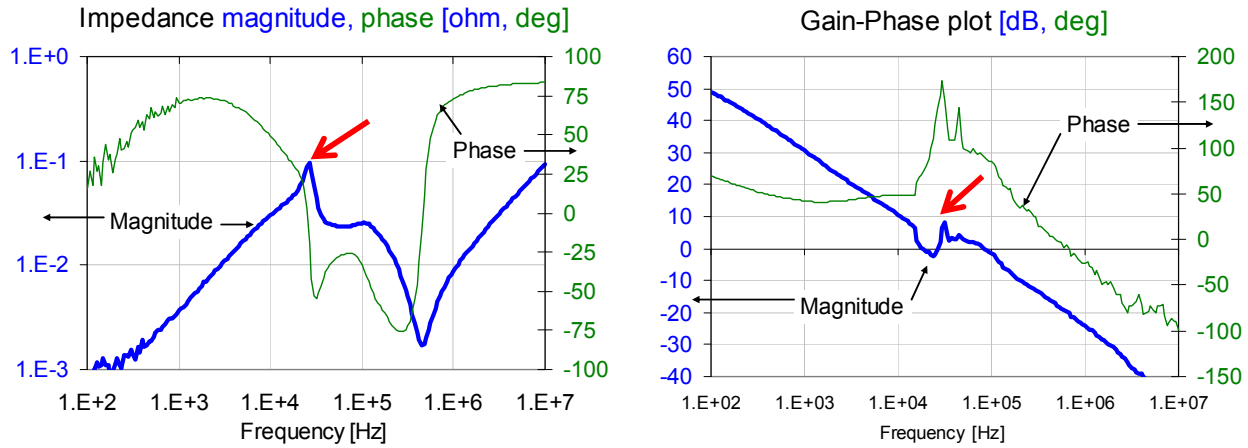


***Figure 18**: Output impedance and Gain-Phase plot for a DC-DC converter, similar to the one shown in Figures 16 and 17.*

Measuring the output response in the time domain with a large-signal sinusoidal and step excitation showed similar correlation: at the frequency where the small-signal output impedance shows the sharp peak, a corresponding time-domain noise can be measured with a large-signal excitation as well. *Figures 19* and *20* show one of these correlations on a DC-DC converter similar to the one used in the above figures. The plots in *Figure 19* show the impedance surface with the ridge and the impedance magnitude and phase plots for the selected operating point on the right. The plots in *Figure 20* show the response to large-signal time-domain excitations for the same converter.

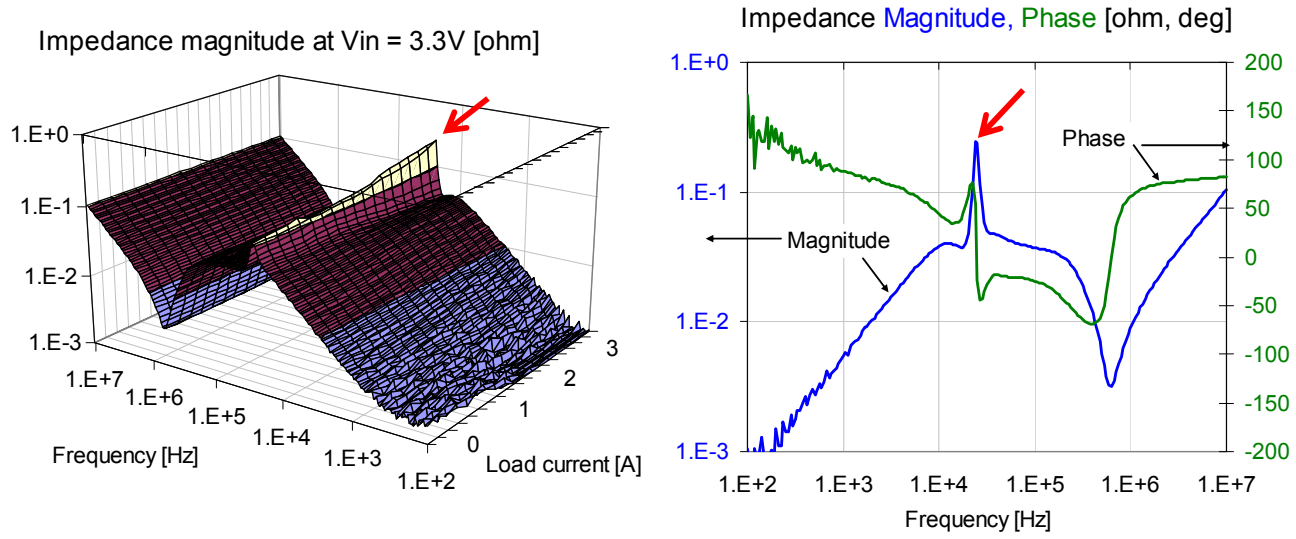


***Figure 19**: Output impedance surface (left plot) and impedance magnitude and phase at 3A load current with 3.3V input and 1.8V output voltages.*

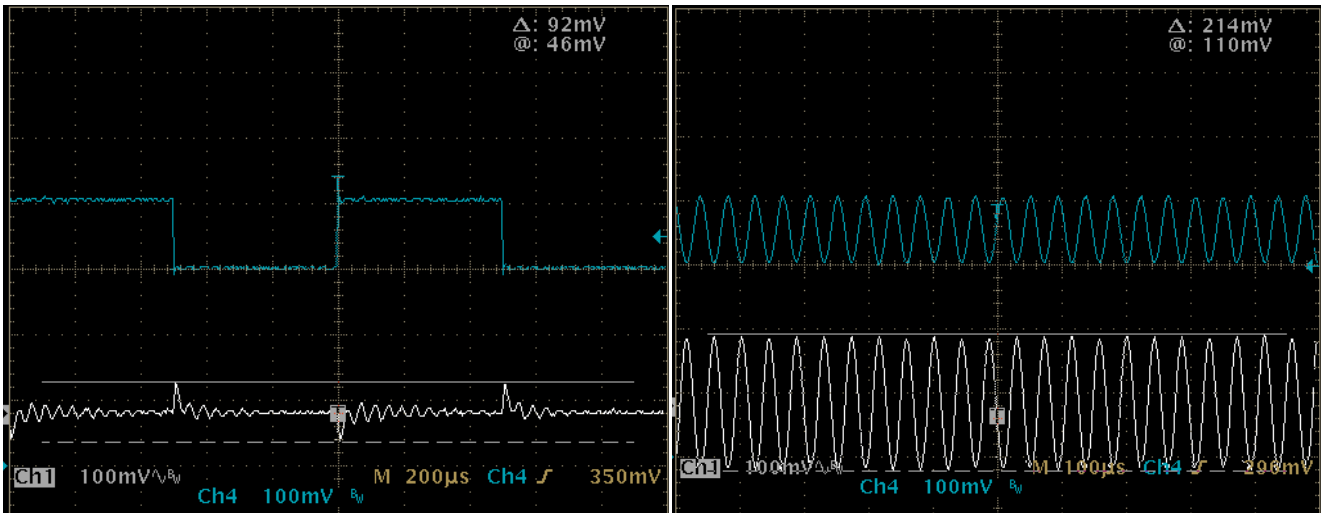


Figure 20*: Step response (on the left) and large-signal output impedance waveforms (on the right) for the converter shown in Figure 19.*

The plot on the left of *Figure 20* shows a 92 mVpp transient response (white trace) to a load current switching between 3 and 4A at 1 kHz frequency. Note that on each load transition there is a damped sinusoidal ringing. The ringing frequency is 24 kHz. When the excitation frequency hits the 24 kHz resonance frequency, the response grows into a steady sinusoidal wave. The impedance peak with small-signal measurements was 230 mOhm at 24 kHz in the operating point of 3.3V input voltage and 3.5A load current. Correspondingly the white trace on the right shows a 214 mV peak to peak response to a 24 kHz sinusoidal load current swinging between 3 and 4A (blue trace).

Next the input side of the converter was measured. Measuring the true input impedance of a running DC-DC converter is not trivial, because the input is fed by a DC source, which should have relatively low impedance and this low impedance is in parallel to the input impedance of the converter. If we measure the impedance between the input connections, we measure the parallel equivalent of the two impedances, which is then dominated by the low source impedance. When we measure the output impedance of a converter, this limitation does not exist, since the converter's output impedance is supposed to have much lower impedance than the load, or we can just use a current load with inherently high impedance. Alternately, we could measure the input impedance by separately measuring the input current and input voltage. This approach has the practical difficulty of measuring the current into a switching converter; chances are that the way how we measure the input current would have a non-negligible effect on the source impedance, which in turn changes the behavior of the converter.

In this study we did not attempt to directly measure the input impedance of the converter; rather the goal was to see how the source impedance (which is supposedly much lower than the input impedance) affects the dynamic performance, namely the output impedance profile. For this reason, measuring between the input-source terminals was a suitable approach.

The impedance on the input side was measured in different configurations for the converter shown in *Figures 19* and *20*. *Figure 21* shows the input impedance of the unpowered converter, when we

basically measure the input capacitor of the converter. The plot on the left shows the measured impedance magnitude and phase (thick lines) and a simple C-R-L model's impedance magnitude and phase (thin lines). Good match on the plot was achieved with C = 15 µF, R = 6 mOhm and L = 2 nH. The plot on the right shows the real part of the measured impedance.

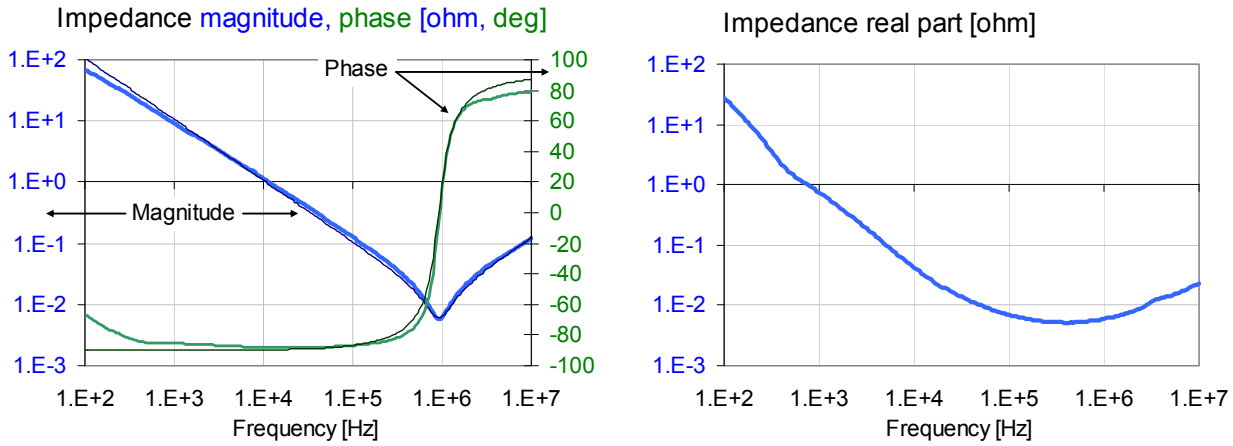


***Figure 21**: Impedance measured across the input terminals of the converter, unpowered.*

Figure 22 shows the source impedance measured at the DC-DC converter input terminals, with the converter disconnected. The source consisted of a regulated bench supply with two four-feet AWG #4 wires running in parallel to the converter. The plot on the left shows the measured impedance magnitude and phase (thick lines) and a simple R-L model's impedance magnitude and phase (thin lines). The match shown on the plot was achieved with R = 11 mOhm and L = 1 µH. The plot on the right shows the real part of the measured impedance (we will need it soon).

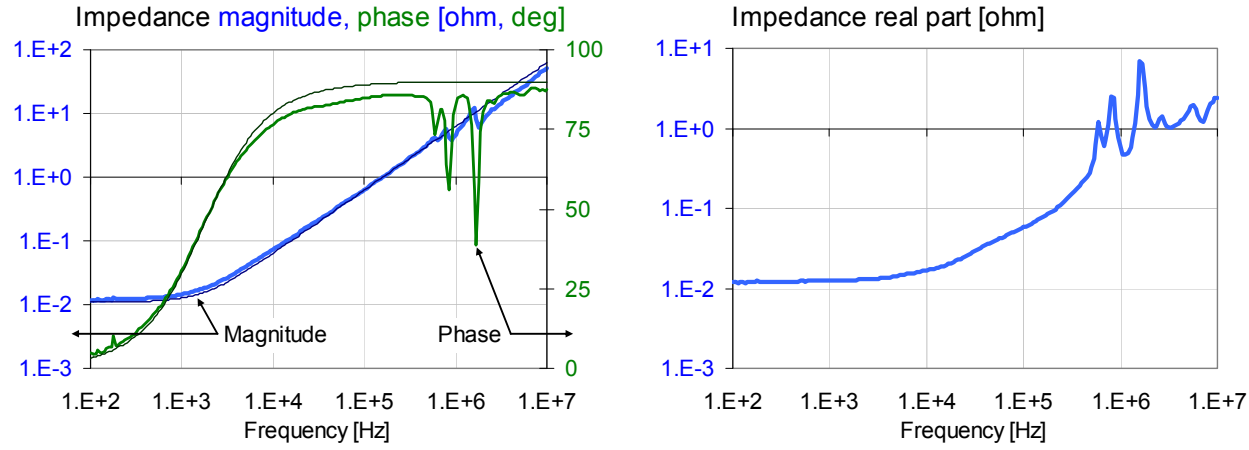


***Figure 22**: Measured and modeled impedance of the power source bench supply with connecting cables, with the DC-DC converter input disconnected.*

When the source is connected to the DC-DC converter input, the impedance across the input terminals was measured with different input voltages and load currents. *Figure 23* shows the

measured impedance magnitude and phase with the converter OFF and ON with 3.3V input voltage and 0, 2 and 4A load currents.

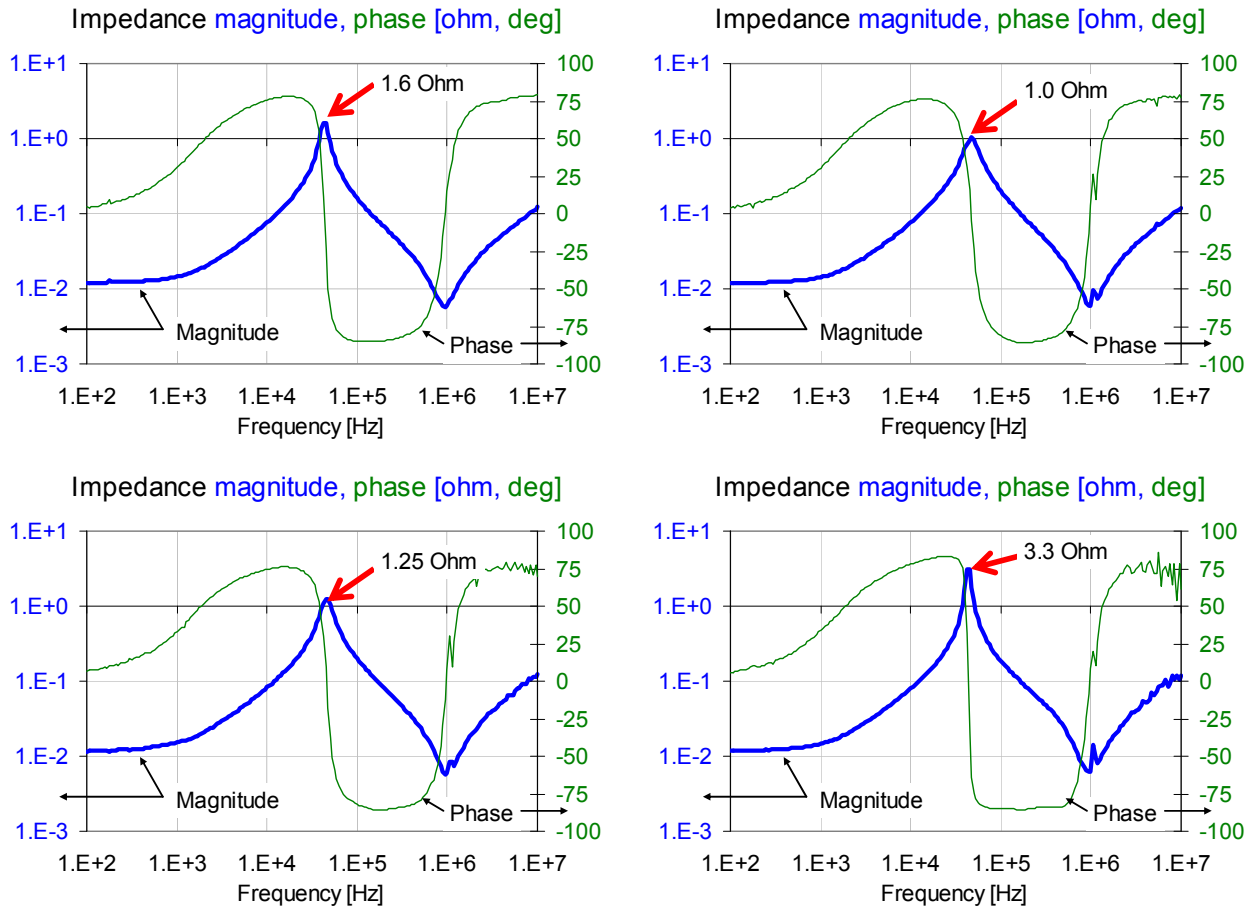


Figure 23: Impedance measured across the input terminals of the DC-DC converter. Top left: bench supply turned ON, DC-DC converter disabled. Top right: DC-DC converter ON, load current 0A. Bottom left: DC-DC converter ON, load current 2A. Bottom right: DC-DC converter ON, load current 4A.

Note the large resonance peak, which varies slightly in magnitude with the converter condition. There is a 1.6 Ohm peak when the converter is OFF. The peak magnitude drops when the converter is powered on with no load. As the load current increases, the peak magnitude increases, eventually growing to 3.3 Ohms with 4A load current.

The large peak in the source impedance occurs at a frequency, which is not far below the cross-over frequency, where the loop gain is not high. This high source impedance with the low loop gain at that frequency appears to be the reason for the peaking in the output impedance. To further test this assumption, in *Figure 24* we plot side-by-side the constituents of the source impedance and the output impedance, both OFF and ON. We see that the peaking (marked by red arrows) occurs at the same frequency in both plots and the crossover frequency is somewhere near 100 kHz. The plots on

these figures all show measured data. To check the accuracy of our models, next we compare the measured data against the model values. For now we will focus on a narrow frequency range around the peaking, and will ignore much lower and much higher frequencies.

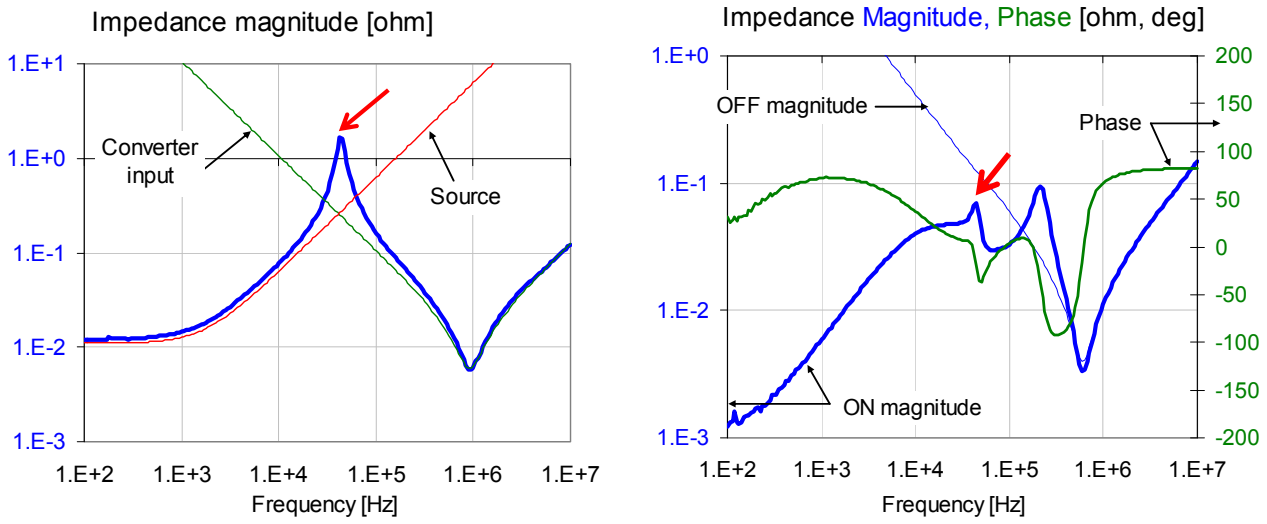


***Figure 24**: Impedance measured across the DC-DC converter input (left plot) and output (right plot) terminals. Note that the peculiar peaking in the output impedance occurs at the same frequency where there is a large peak in the source impedance (marked by red arrows).*

Figure 25 plots the measured impedance magnitude across the input terminals with no power applied (thick blue line) and its approximation from the 11 mOhm 1 µH source-impedance model and 15 µF 6 mOhm 2 nH input-impedance model. What appeared to be a good model fit separately for the source and input impedances, does not provide a good fit for the anti-resonance, created by these two impedances in parallel. The modeled peak occurs at a slightly lower frequency and with a higher magnitude. We can easily adjust the capacitance and inductance values just a little bit to get a better agreement at the resonance frequency.

The reason for the frequency shift is two-fold: with the applied DC voltage the capacitance of ceramic capacitors drop and with varied DC load current, the inductance of the ferrite-core inductor in the converter may also decline [21]. To get the peak magnitude right, we would need to increase the loss values. This makes sense after all: we adjusted the resistance for the source impedance to get a good match at 100 Hz, and we matched the resistance of the converter's input impedance to get a good match at the series resonance frequency at 1 MHz. The anti-resonance, on the other hand, happens at 42 kHz, much higher than 100 Hz, and much lower than 1 MHz. We can go back to *Figure 22* and look up the impedance real parts of the source and input impedances at 42 kHz: it is 24 mOhm. Similarly, the real part of the converter's input impedance rises to 16 mOhm as frequency goes down from 1 MHz to 42 kHz. With these revised loss values we get a better model correlation at the anti-resonance peak, as shown in *Figure 26*.

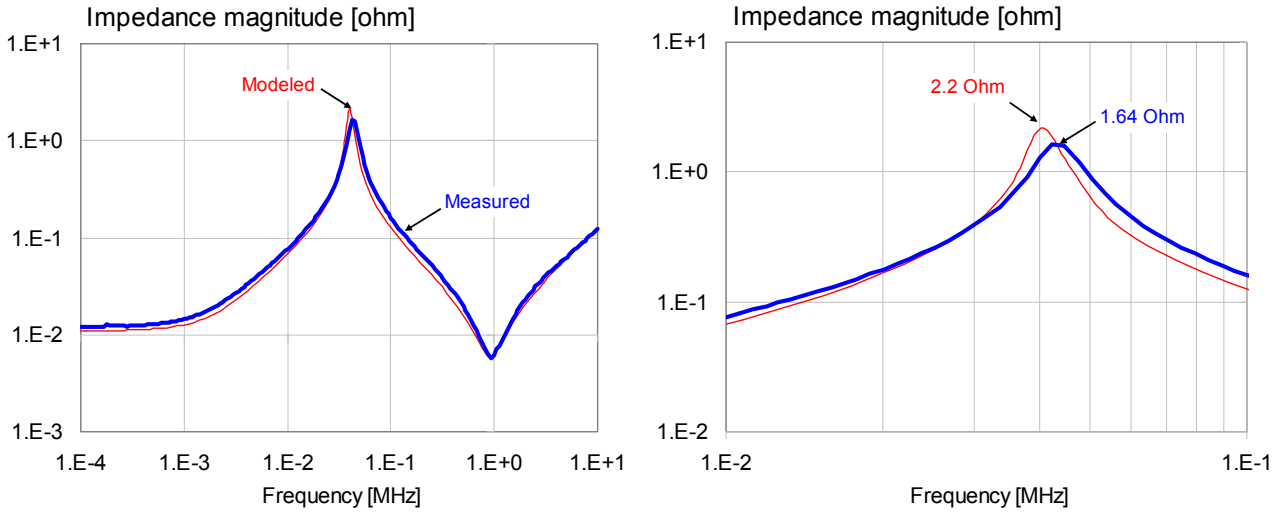


***Figure 25**: Model-to-measurement correlation of the impedance across the input terminals. Full frequency range is shown on the left, zoomed scale on the right.*

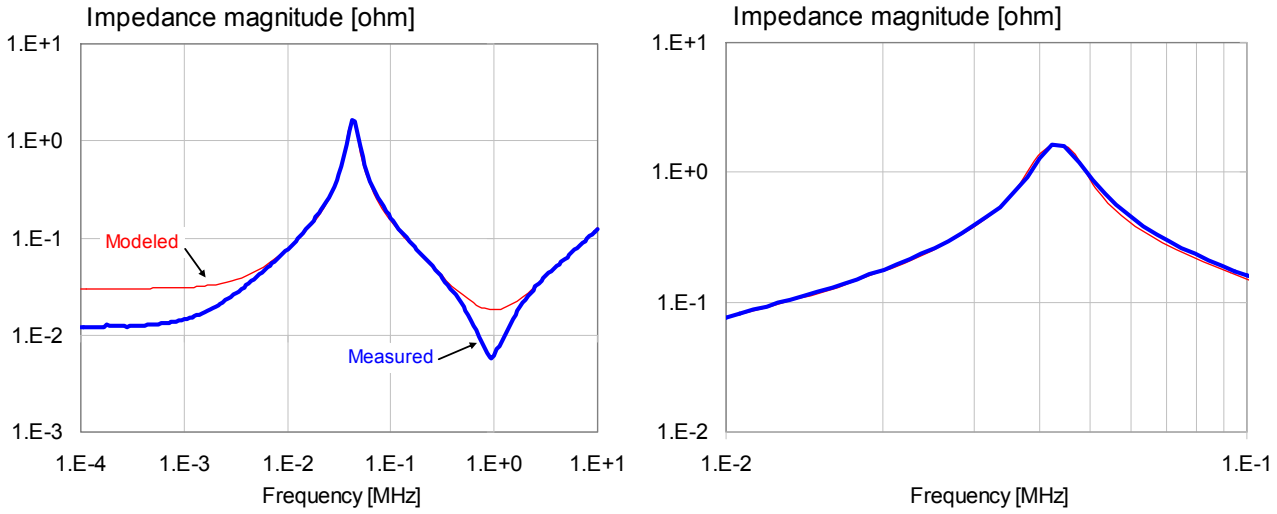


***Figure 26**: Model-to-measurement correlation of the impedance across the input terminals, converter OFF, using revised loss values. Full frequency range is shown on the left, zoomed scale on the right.*

The correlation is very poor at low and high frequencies, but we get a complete overlap around the anti-resonance frequency. We take this adjusted model and in the next step we find out what positive input resistance of the converter does it take to lower the impedance peak from 1.64 Ohms to 1.0 Ohm. *Figure 27* shows the correlation with the last model with a 2.2 Ohm resistor added in parallel. This represents the AC power loss of the converter at 42 kHz with no load.

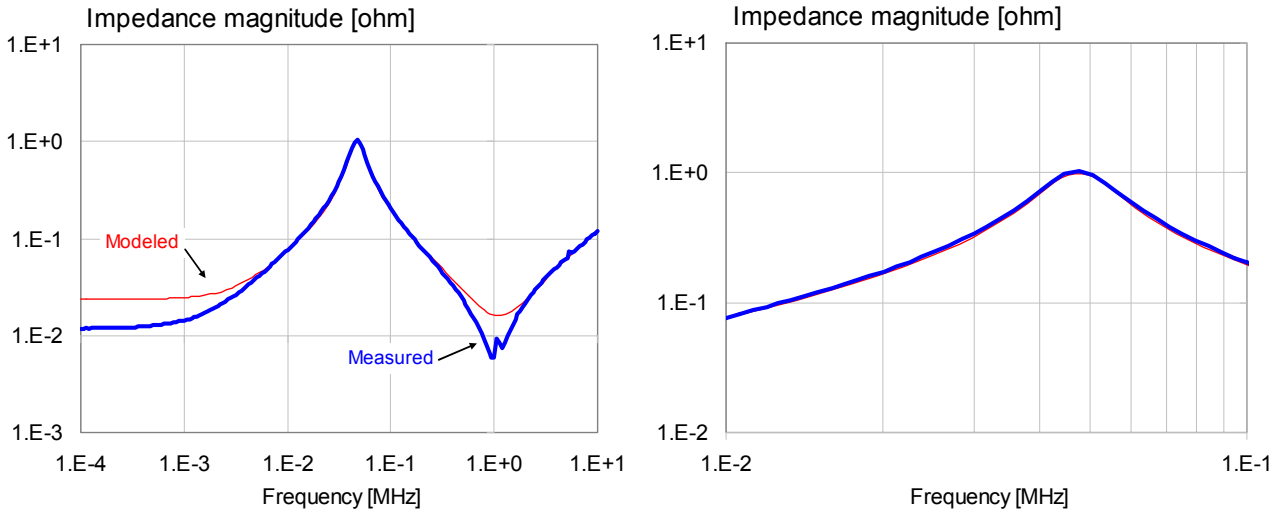


***Figure 27**: Model-to-measurement correlation of the impedance across the input terminals, converter ON with 0A load, using revised loss values and 2.2 Ohms representing the converter's input loss. Full frequency range is shown on the left, zoomed scale on the right.*

We can now calculate the incremental dynamic input resistance of the converter at 2A and 4A load currents. With 3.3V input voltage, 1.8V output voltage, 4A load current and 82% (measured) efficiency yields r_{in} = -1.24 Ohms. When we add this negative resistance in parallel to the previous model, we get the correlation shown in *Figure 28*. The frequency is a little off, but the peak magnitude is captured with reasonably good agreement.

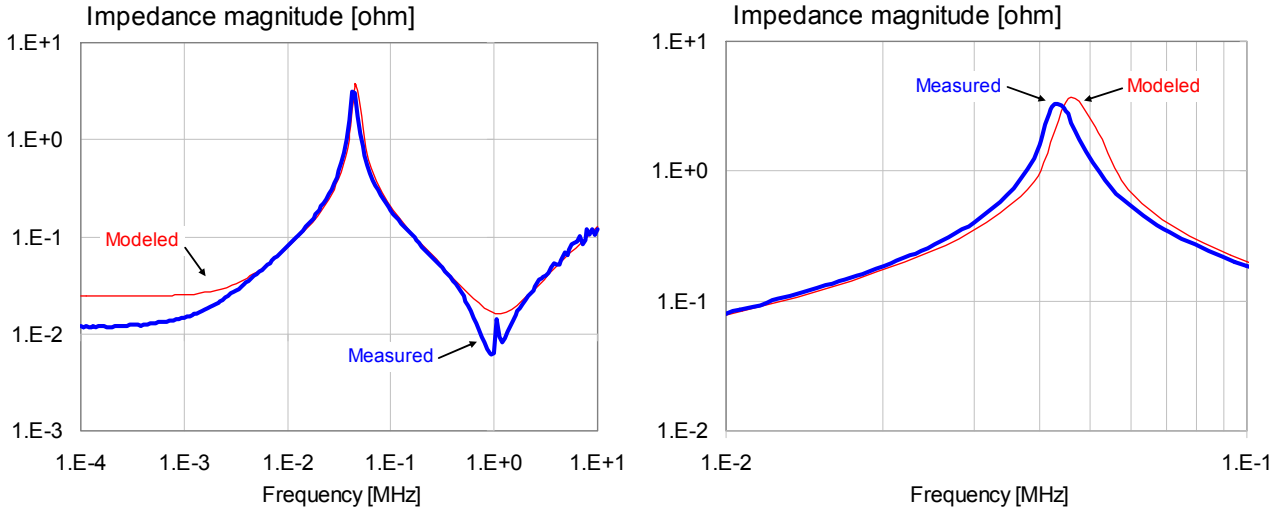


***Figure 28**: Model-to-measurement correlation of the impedance across the input terminals, converter ON with 4A load, using revised loss values and -1.24 Ohms representing the converter's input loss. Full frequency range is shown on the left, zoomed scale on the right.*

Figure 28 tells us that the negative input resistance of the converter makes the impedance peak higher in our case. Note, however, that the impedance peak magnitude is very sensitive to component values, and it can also decrease, not only increase, the peak magnitude. Ultimately the negative input resistance can cancel the effect of the two series loss resistances, leaving the input circuitry without any damping. This critical value can be found if we look at the Q of the second-order equivalent circuit formed by the source impedance and unpowered input impedance of the converter. *Figure* 29 shows the simplified equivalent circuit.

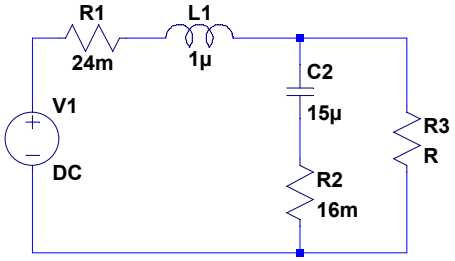


***Figure 29**: Equivalent circuit to calculate the critical value of converter's input resistance (R_3), which can leave the input-side LC circuit un-damped.*

R_1 and L_1 represent the source, C_2 and R_2 represents the input capacitor(s) of the DC-DC converter and R_3 represents the negative input resistance of the converter. With $R_1 \ll R_3$ and $R_2 \ll R_3$ the critical value of R_3 where the circuit becomes un-damped is given by Eq (1-177) of [2]:

$$R_3 = -\frac{R_1 R_2 C + L}{C(R_1 + R_2)} \tag{12}$$

With the values in the figure, the critical value becomes -2.7 Ohms. To make sure that the input L-C circuit is always sufficiently damped, we have to add positive resistance either in series or in parallel.

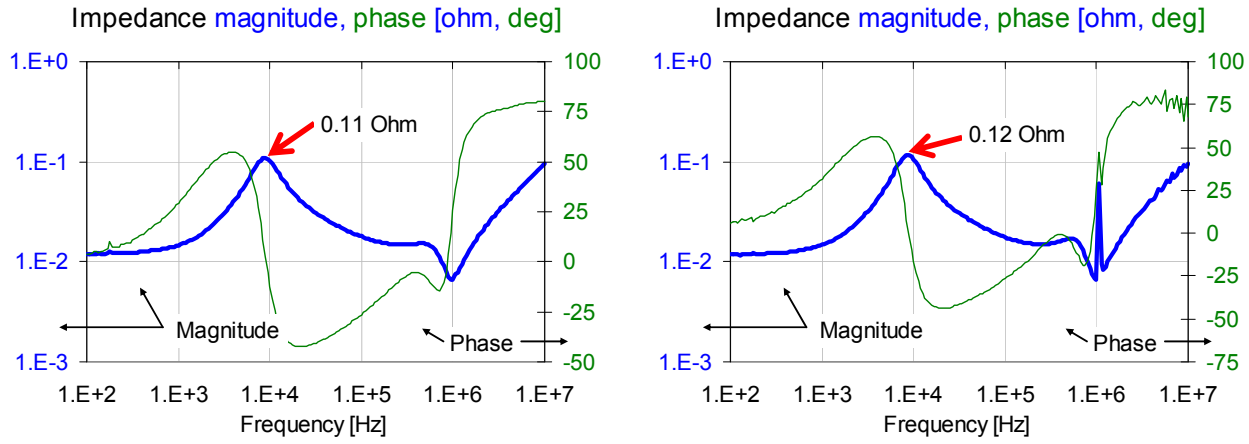


***Figure 30**: Measured impedance across the input terminals with 330uF 25 mOhm polymer capacitors added across the input and output of the converter. Left plot: converter OFF. Right plot: converter ON, load current 4A.*

Adding series resistance is not straightforward, because we don't want to increase the DC loss. We can add series AC resistance at the resonance frequency of the LC circuit by using a lossy ferrite, this, however, would also add to the series inductance. A more convenient way is to add parallel resistance in the form of a 'lossy' capacitor with sufficiently high ESR value or with an external series resistor. In addition to adding parallel resistance, we can also lower the Q of the LC circuit by either decreasing L_1 or increasing C_2. In the illustration below, we added 330µF polymer capacitors with 25 mOhm ESR to the input and output, one each. The impedance measured across the input terminals is shown in *Figure 30*. The impedance peak moved to below 10 kHz and the peak magnitude dropped to about 0.1 Ohms, hardly changing with the output load conditions. The output impedance in *Figure 31* also shows significant improvement.

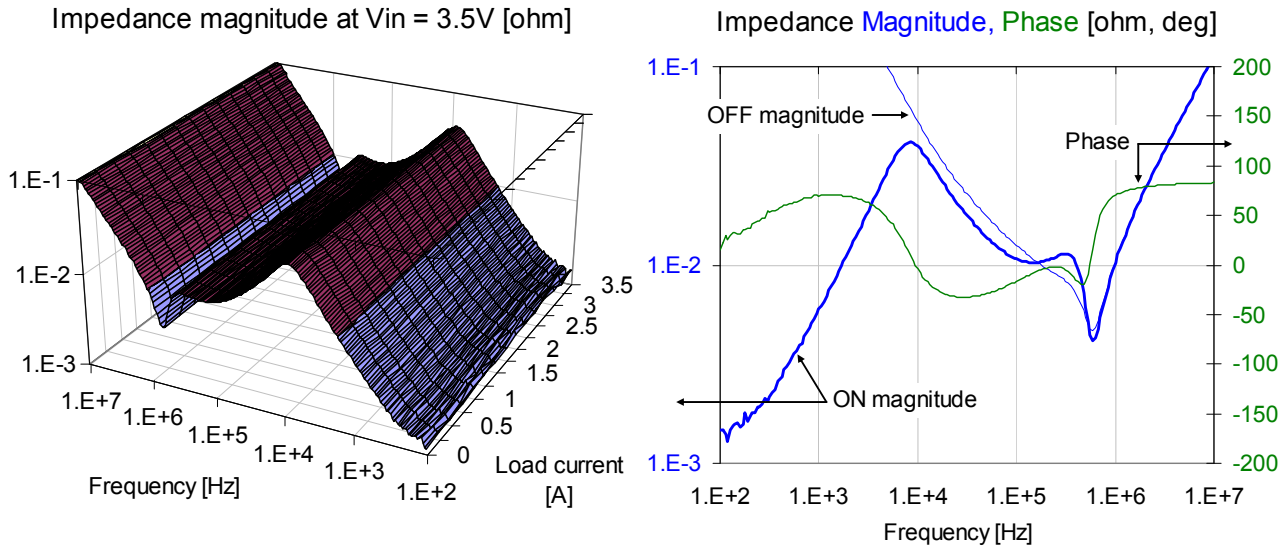


***Figure 31**: Measured output impedance with 330uF 25 mOhm polymer capacitors added across the input and output of the converter. On the left: impedance surface. On the right: impedance magnitude and phase with 4A load.*

Multiple Converters in Parallel

If the required load current is higher than what is optimal for a single converter, multiple converters may be used in parallel. Optimal current loading per phase can range from say 15 amperes to as much as 40 amperes depending on the components used. Besides providing current scalability, multiple parallel converters offer additional benefits. One benefit is the distribution of thermal loading across a larger number of components. Distributing the thermal load across a larger number of components reduces hot spot temperatures and may actually improve reliability. Another benefit is that each converter can be shifted in phase such that the output ripple and also the input ripple is reduced. If the size of the output capacitance is selected for ripple, then parallel phase shifted converters can be used to reduce the output capacitance. Many times though, the output capacitance is selected for the required transient response of the system. As described earlier, the transient response of a power supply system can be characterized in terms of the converter closed loop impedance. This raises the question of "How does the impedance scale with multiple phases?" To

answer this question, we must make a few observations and assumptions about the system and characteristics of each phase.

Observations and Assumptions:

Consider the multiphase systems illustrated in *Figure 32*.

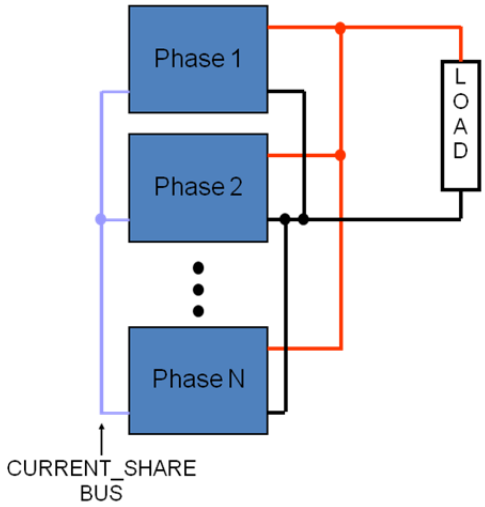


***Figure 32**: High-level block diagram of a multi-phase DC-DC converter.*

In a multi-phase system, it is important that each phase share current. If equal or near equal current sharing does not occur, one converter will source more than the average current per converter (by nature of the Mean Value Theorem) and thus must be designed to source this higher current. By sharing current, the design requirements for each phase can be minimized in terms of current source capability. The current sharing requirement is both a static and dynamic requirement. That is, not only do the converters need to share the DC current levels but, during a transient, they need to properly share the transient current as well. In this discussion, we will assume that each phase is sourced from the same input voltage source. That is, if the multi-phase power converter is a 12V to 1.2V converter, we will assume that each phase is connected to the same 12V source. This is not an overly restrictive assumption and is, in fact, the most common configuration sources each phase from the same source. This assumption allows us to make an important simplifying observation about the closed loop impedance of each phase: for current sharing, the closed loop impedance for each phase must be equal. Given that the input (e.g. 12V) and output (e.g.1.2V) for each phase is the same, if one phase has a lower closed loop impedance than another phase, it will (by Ohms law) deliver a higher current than the higher impedance phase. This violates our requirement for current sharing. Thus all closed loop impedances (each phase's impedance) must be equal. As noted above the static and dynamic current sharing requirement, this has to be true for both the static output resistance and for the dynamic output impedance as well.

An easy way to visualize, from a system perspective, the parallel combination of multiple phases is to realize that each phase can be represented by its Thevenin equivalent with an ideal voltage source and the closed loop Thevenin impedance in series with the voltage source. Now, with each phase

connected in parallel to source the load current, the system can be simplified by the parallel combination of the source impedances, Z_i. That is, the system source impedance, Z_s, can be given by:

$$\frac{1}{Z_S} = \frac{1}{Z_1} + \frac{1}{Z_2} + \cdots \frac{1}{Z_N} = \frac{N}{Z_i}$$

At very low frequencies the usually high DC loop gain sets the output impedance so low that it gets masked out by any small connection resistance, thus making the DC output resistance reading the same regardless of the number of phases. As frequency increases, the loop gain drops and gradually the impedance of the passive output network starts to dominate, which scales with the number of phases. Now we can observe that:

$$Z_S = \frac{Z_i}{N}$$

Or

$$N \cdot Z_S = Z_i$$

The conclusion then is that the dynamics of a multiphase system, under these assumptions, can be reduced to the dynamics of a single phase system with load impedance scaled by the number of phases. Since the dynamics of the system is characterized by the dynamics of a single phase, adding additional phases does not impact the dynamic response of the system except by the apparent and effective scaling of the load impedance. Another way to visualize this observation is, in the time, domain, if a single phase responds characteristically in, say, one microsecond, adding phases does not speed up the response time of the system. The bottom line is that in properly designed multi-phase systems the transient response is determined by a single phase (as described above) with the load scaled by the number of phases. This can be illustrated by looking at the closed loop impedance of multiple parallel power supplies. The unit was a voltage-mode control non-isolated buck converter, rated for 17A maximum current [22]. *Figure 33* shows the impedance of a single power supply, two power supplies in parallel, and three power supplies in parallel. Here the power supplies are turned off so that the impedance changes are simply due to the passive impedance change with the addition of each supply.

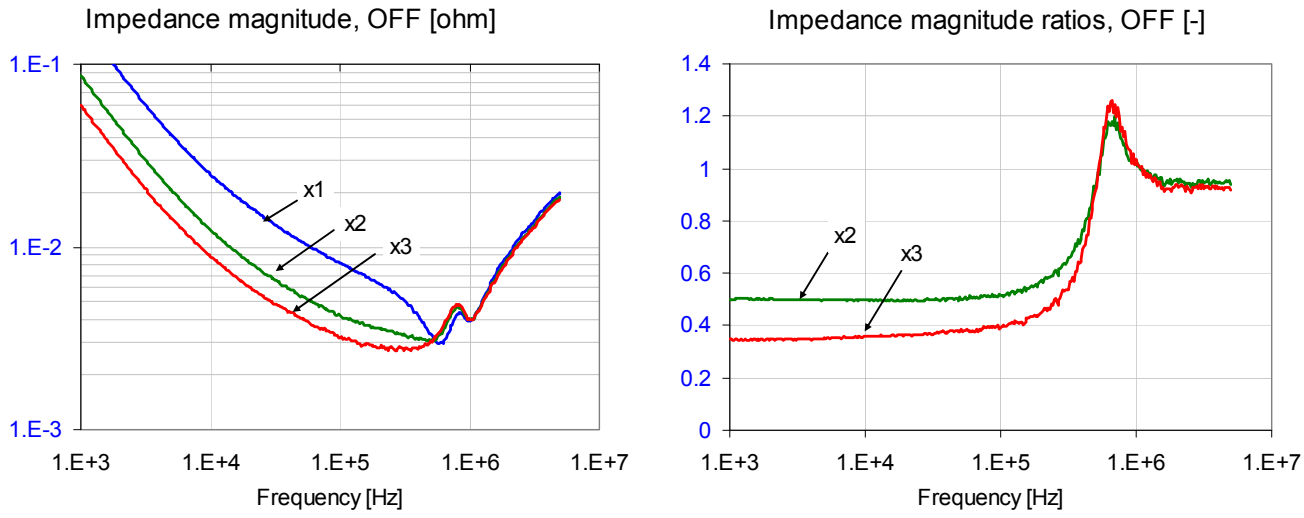


***Figure 33**: Absolute impedances and impedance ratios of a single, two, and three-phase power supply in the un-powered OFF condition.*

For low frequencies, the impedance of two supplies is one half of a single supply and the impedance of three supplies is one third of a single supply as expected. As the frequency increases, the series parasitic inductance connecting the power supplies to the common point begin to isolate the power supply impedances so that the parallel impedances of the supplies have diminishing effect.

When the power supplies are turned on and regulating, the feedback loop modifies the impedance as described above. *Figures 34* and *35* show the respective impedances for a DC load of 5A and 15A in each phase.

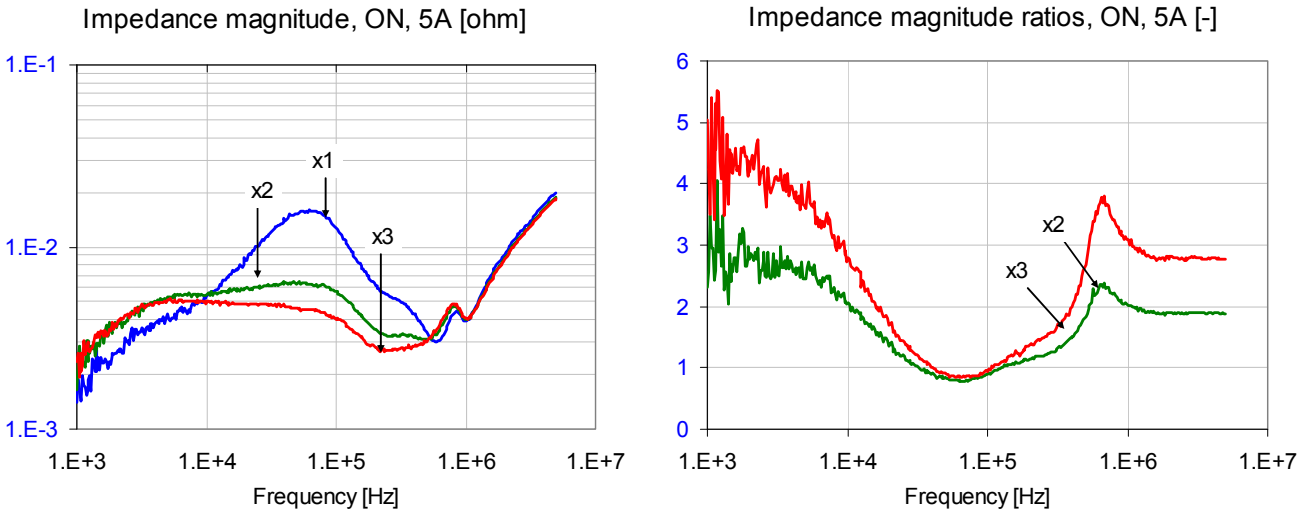


***Figure 34**: Absolute and scaled output impedances of a single, two, and three-phase power supply, each phase delivering 5A load current.*

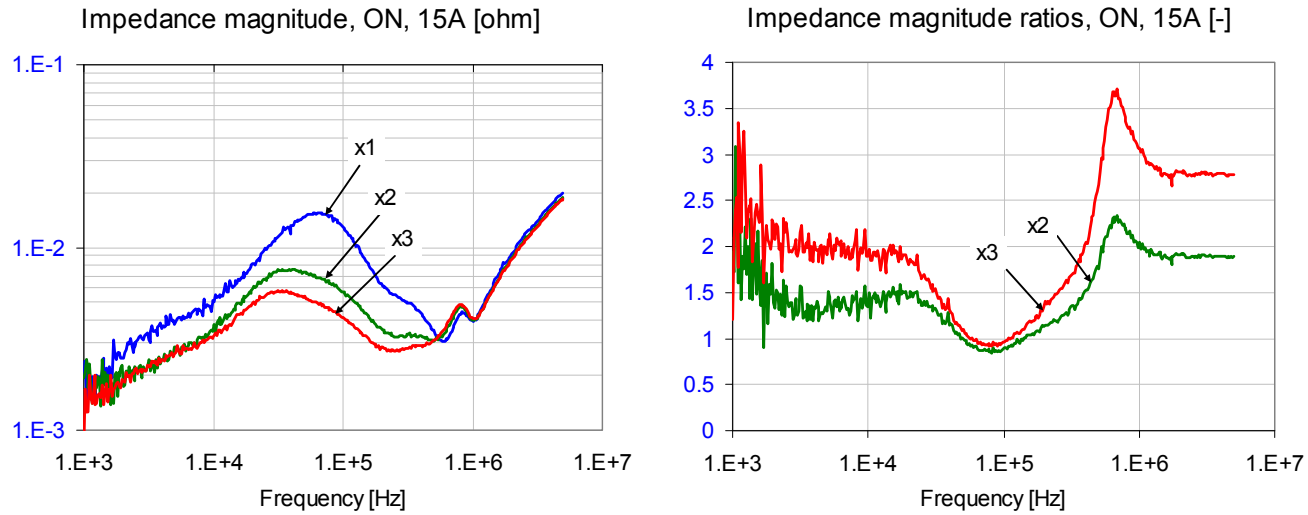


***Figure 35**: Absolute and scaled output impedances of a single, two, and three-phase power supply, each phase delivering 15A load current.*

Here we see at low frequencies, the feedback loop controls the impedance so that there is no difference between a single phase and two or three phases. As the frequency increases, the loop gain

decreases and the impedance distributes according to the passive impedances of each supply. Finally, at high frequencies, the power supply impedances become decoupled from the load and, again, there is little difference between a single phase and two or more phases.

Moving from the frequency domain to the time domain, we can see a similar scaling affect by adding supplies in parallel. *Figure 36* shows the output voltage ripple for a single supply, two parallel supplies and three parallel supplies. In each case, the output switching of each supply was phase shifted by 360˚/N, where N is the number of supplies.

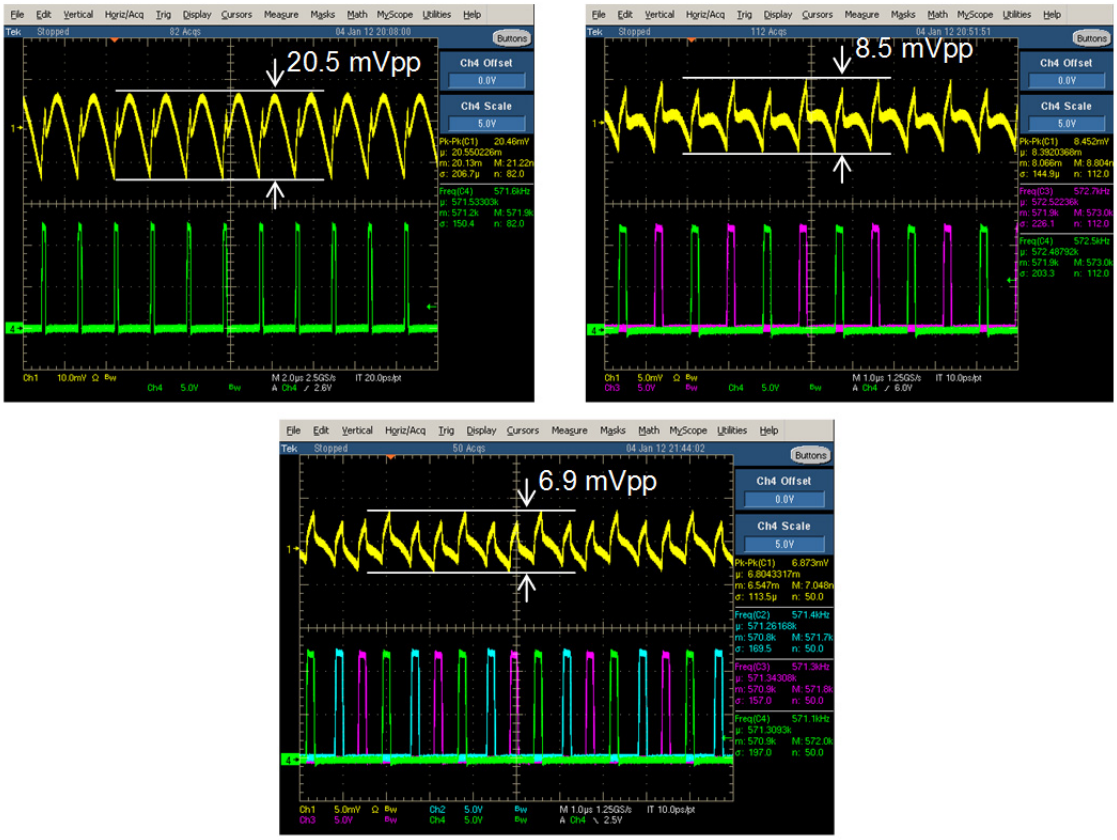


***Figure 36**: V_{out} ripple for single supply (top left), two (top right) and three (bottom) supplies in parallel.*

As the waveforms show, the output voltage ripple does in fact decrease with the addition of paralleled supplies. As was the case with the output impedance, the output voltage ripple approximately scales by 1/N, where N is the number of supplies in parallel. The output scaling is not exact - this is because there are multiple things affecting the output voltage ripple, including the scaling of the output switching frequency, the scaling of the output impedance, and the decrease LC cut-off frequency as multiple supplies (and their corresponding output cap banks) are added in parallel.

The dominant contribution to the decrease in output voltage ripple when supplies are paralleled is the apparent increase in switching frequency. Since the supplies are out of phase with each other by 360˚/N, the net effect is that a portion of inductor ripple current from each supply cancels with that of the other supply, resulting in an effective decrease in the total output inductor ripple current.

Another way to view this is the apparent switching frequency of the supply has been increase by a factor N, where N is the number of supplies in parallel. The equivalent output inductor ripple current, multiplied across the output capacitor ESR, is the main contributor to output voltage ripple.

To show the affect of the ripple current contribution to the output voltage ripple, phase shifting was turned off for the two and three supplies in parallel cases. Resulting waveforms are shown in *Figure 37*. Note that the in the scope shot, the ground reference of each switching waveform was intentionally offset to make it easier to see they were in fact over lapping. As the waveforms show, with phase shifting disabled, there was no decrease in the resulting V_{out} ripple as additional supplies were added in parallel.

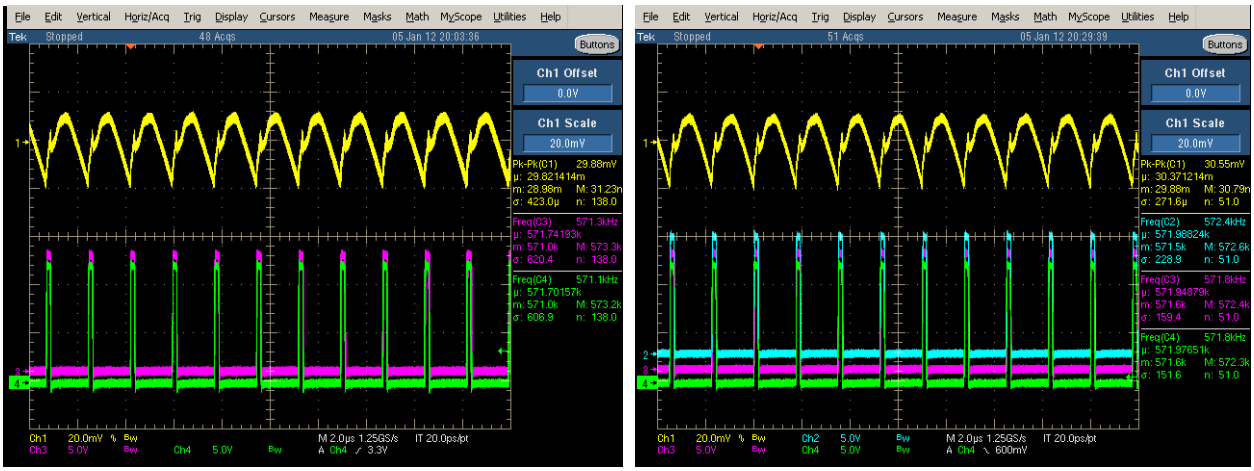


***Figure 37**: Output voltage ripple with two (on the left) and three (on the right) supplies in parallel, phase shifting disabled.*

The above results beg the question – when does it make sense to use a single supple versus multiple supplies in parallel? Due to the large number of variables associated with designing a power supply, several requirements will be fixed in this example. Namely the input voltage will be fixed at 12V, the switching frequency (per supply) at 300 kHz, the output voltage at 1.2V and the output current at 40A, with a max load step of 20A at 10 A/µs.

Starting with the above requirements, the first step would be to design an output filter so that the output voltage ripple and transient requirements are met. A typical requirement for V_{out} tolerance is +/-5%, resulting in a V_{out} tolerance of +/-60 mV for a 1.2V output. Working backwards, most controllers guarantee an output regulation tolerance of +/-1% (determined by the accuracy of the controller's internal reference), leaving +/-4% for V_{out} ripple and transients. If we assume +/-0.5% for V_{out} ripple, that leaves +/-3.5% out of the initial +/-5% V_{out} tolerance requirement for output voltage transients. To keep the output voltage within the required regulation window for a 20A load step, the output impedance of the supply must be less then:

$$Z_{out} = \frac{\text{Vout} * \text{Tolerance}}{\text{Load Step}} = \frac{(1.2\text{V} * 3.5\%)}{20\text{A}} = 2.1\text{m}\Omega$$

The output impedance of the power supply is a function of the passive output impedance of the output capacitor bank and PCB parasitics and that of the feedback loop. In equation form, this is given by Equation (8). Most controller feedback loop bandwidths are limited to 1/3rd to 1/10th the switching frequency of the supply, resulting in feedback loop bandwidths of sub-100 kHz for a 300 kHz switching frequency. In order to meet the 20A load step at10A/µs requirement, the output impedance must be flat and sub-2.1 mOhm up to about 700 kHz, meaning the output capacitor bank must be designed to have sub-2.1 mOhm impedance up to ~700 kHz. The output voltage ripple for a buck regulator can be approximated with:

$$V_{out\_ripple} = I_{L_{Pk-pk}} * ESR_{C_{out}}$$

To keep the output voltage ripple within the +/-0.5% tolerance, the peak to peak current through the output inductor must be less then:

$$I_{L_{Pk-pk}} = \frac{V_{out\_ripple}}{C_{out_{ESR}}} = \frac{1.2V * \pm 0.5\%}{2.1m\Omega} = 5.71A$$

The peak-to-peak ripple current through the inductor is given by:

$$I_{L_{Pk-pk}} = \frac{V_{in} - V_{out}}{F_{SW}\ L} \frac{V_{out}}{V_{in}}$$

Using this equation, in order to meet the output voltage ripple requirement with a single supply at a 300 kHz switching frequency, the output inductor must be greater than 630 nH. An output inductor which can support >40A of current and is greater than 630 nH is relatively large in size, and since it must support all of the load current, the losses through its equivalent DC resistance is high and concentrated in one component. A lower value inductor can be used, but the trade off is the output capacitor ESR must also be lower to meet the output voltage ripple requirement. This results in the use of a greater number of output capacitors, increasing regulator size and cost.

Alternatively, a two supply (or two phase) solution can be used. For the two supplies in parallel case with 180 deg phase shift between supplies, the total switching frequency is effectively doubled to 600 kHz. This means to meet the required output voltage ripple with an equivalent output capacitor bank, the per-supply inductor value can be cut in half to 315 nH. With effective current share, each output inductor now only needs to support one-half the load current. This results in the power loss being distributed across multiple components, improving reliability thorough reduced thermal stress. A 315 nH inductor which supports 20A of current can also be much smaller than the inductor used in the single supply case, which can actually result in a total solution size that is comparable in size to that of a single supply.

Digital Control

The majority of the discussion in this paper has been agnostic with respect to the control methodology. An emerging control technology is digital control ([23], [24]). Analog control has dominated the history of power control due to its availability and simplicity. Over the last decade, though, digital control has risen in popularity by becoming more available, more, cost effective, and simpler to use.

Digital control produces pulse width modulator control by using digital techniques, many of which, mimic analog control techniques. As an example, to stabilize the feedback loop, analog control uses analog filters to position poles and zeros to compensate the control loop. Digital power controllers use digital filters to perform the compensation role. In analog filters, the filter is realized by a circuit of resistors and capacitors. In a digital filter, the filter is realized through a digital circuit which combines current and historical gained values of samples of the signal.

While digital control offers the ability to introduce very sophisticated and complex means for compensation, this paper will assume a simple digital PID filter as illustrated in *Figure 38*.

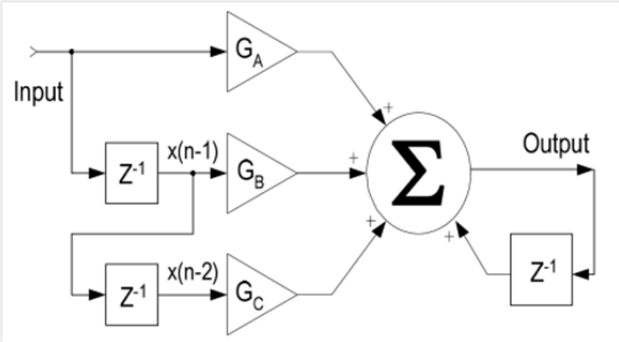


***Figure 38**: Digital PID Compensation Network.*

This digital filter takes the error signal, sums the scaled signal with scaled delayed samples of the error signal plus the integrated output to implement the compensator. Three gain coefficients are used to tune the compensator.

This filter has a transfer function given by:

$$G_d = \frac{A + Be^{-sT} + Ce^{-2sT}}{e^{-sT}\left(1 - e^{-sT}\right)}$$

Where A, B and C are the gain coefficients for the various taps, the first term in the denominator is due to the delays in the signal path, the second term in the denominator is due to the accumulator at the output of the summing stage, and T is the switching frequency of the PWM.

This compensator can be seen to have two zeros, a pole at zero, and a pole at infinity. The two zeros are available to compensate for the two poles in the output stage of the plant. These zeros arise as

solutions to the quadratic equation in the numerator. As such, depending on the values of A, B, and C, there can be two real zeros or a pair of complex conjugate zeros. The digital PID compensator therefore gives not only the same real zeros as a Type III analog compensator but also complex zeros which are more suitable for compensating complex poles. Eventually the frequency-domain transfer-function can be approximated by the PID transfer function [25].

In fact, the A, B, and C can be combined into a Gain term, Gc, a Q term, Qc, and a Frequency term, fc, to facilitate matching the corresponding characteristics of the output stage. Once the transfer function of the digital compensator is realized in terms of Gc, Qc, and fc, an observational method can be used to compensate the plant.

Another advantage of the digital filter is that the compensation values are stored in digital registers. This means that there are no external components for compensation and the values are easy to change by simply changing the value in the digital registers.

Another advantage of the digital filter is that the compensation values are stored in digital registers. This means that there are no external components for compensation and the values are easy to change by simply changing the value in the digital registers.

In addition to not requiring external components to set compensation values, Digital control loops can also add non-linear control schemes which increase the transient performance of the controller. These non-linear control blocks can be used to effectively increase the loop bandwidth of the controller, however due to their non-linear nature, they often do not show up in small signal output impedance measurements.

One way to implement a non-linear control scheme is to add a second, faster loop which by-passes the PID control loop described above. An example of a threshold based non-linear control response is shown on the left of *Figure 39*. Additional information can be found in [35].

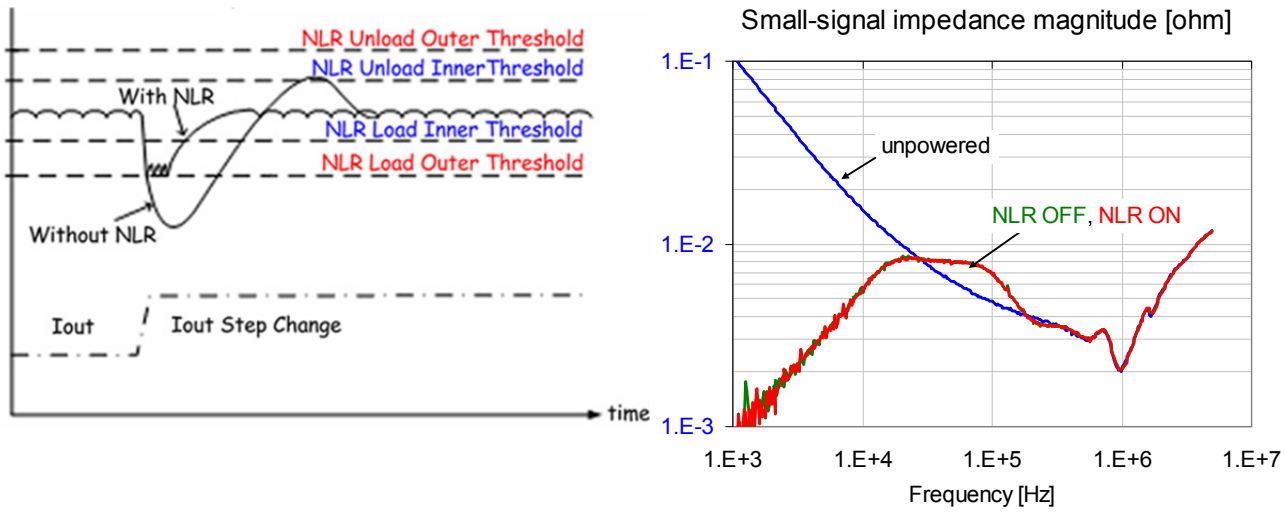


***Figure 39**: Measured small-signal output impedance of a digital controller with non-linear control (NLR) ON and OFF on the right.*

The second, faster loop, can be activated when the output voltage deviates by a prescribed amount, say +/-2%. To show how small signal measurements often do not capture the affects of non-linear control elements, the output impedance of a digital controller with a non-linear control block similar to the one described was measured. As shown in *Figure 39* on the right, the output impedance was measured with the non-linear control block both enabled and disabled. For both sets of measurements, the PID control loop parameters used were fixed.

Moving over to the time domain, an output transient was applied to the same controller, both with the non-linear block enabled and disabled. *Figure 40* shows the transient result with the non-linear block disabled. As the figure show, the total output voltage deviation to a load step and load release was 148 mV.

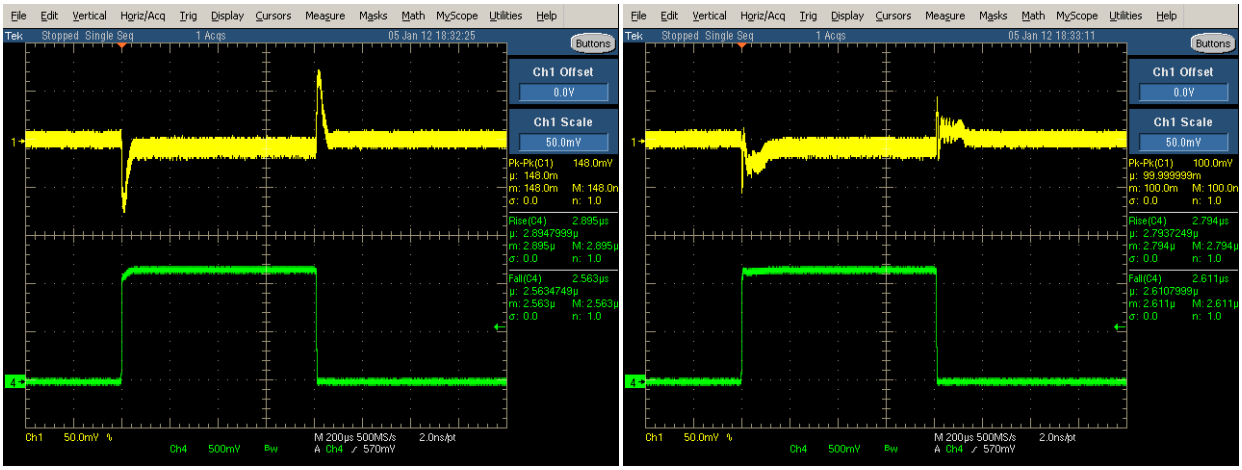


***Figure 40**: Measured transient response with NLR OFF (left plot) and ON (right plot). Yellow traces show output voltage, green traces show load current. Scales are the same on both plots.*

Figure 40 also shows the same transient with the non-linear block enabled. The affect of the non-linear control block was to reduce the total output transient to a load step and release to 100 mV, a decrease in deviation of ~50%. As the time domain results show, the non-linear control block effectively reduces the output impedance of the controller, however this affect does not show up in the small-signal output impedance measurements.

In the most recent offerings of digital controllers, automatic compensation can be performed [26]. An algorithm in the digital controller characterizes the system and adjusts the compensation parameters for stable operation. Although the exact algorithm for automatic compensation is proprietary, it works by adjusting the compensation coefficients in a systematic way while observing the response of the system [22]. While this does produce a slight perturbation on the output it is almost imperceptible and well within the allowed transient envelop. One of the nice features of this method is that it has a limited and controlled perturbation on the output unlike other methods which may have a non-deterministic or non-controlled perturbation on the output.

IV. Measurements, Modeling, Simulations

In the previous sections we included illustrations of all three kinds: among others, we had models describing the source impedance feeding the DC-DC converter (in *Figure 22*), we showed various simulated results, for instance the simulated output impedance in *Figure 8*, and finally many earlier figures showed actual measured data. During the design and later in the validation phase we need to make sure that the models and simulated results show a reasonably good agreement with measurements. Other than the switching ripple and parasitic ringing at the switch node, the important dynamic parameters can all be linked to the dynamic behavior of the closed control loop. This is true for analog and digital loop implementations, with and without non-linear control. Until intentional non-linear control kicks in, well-designed converters can be well approximated with averaged linearized models. In this session we will focus on the $G_{loop}(f)$ Gain-Phase plot and complex output impedance versus frequency. As we showed earlier, the loop gain information tells a lot not only about stability, but can also be used to predict the output impedance. For linear systems we can go between frequency and time domain parameters by the applicable Fourier transforms and can also calculate the worst-case time-domain transient response for an arbitrary sequence of step excitations with bounded magnitude and slew rate. The internal operation of a DC-DC converter is inherently non-linear and large signal. This raises the question how accurate can be any transfer response we measure or simulate with small-signal assumptions. We will show in this section that the small-signal and large-signal data show quite good agreement and the agreement breaks down only when we hit either saturation (for instance in observing the Gain-Phase curve) or intentional nonlinear control (for instance in observing output impedance).

Measurements

From early on, the loop stability measurements of DC-DC converters have been a primary goal for DC-DC converters and therefore their measurement setups and instrumentation is well established. The *Frequency Response Analyzer* instrument is a low-frequency vector network analyzer with a swept-frequency sine-wave source and two high-impedance tracking voltmeter inputs ([27], [28], [29], [30]). The usual measurement setup is shown in *Figure 41* (reproduced from *Figure 23* of [31]).

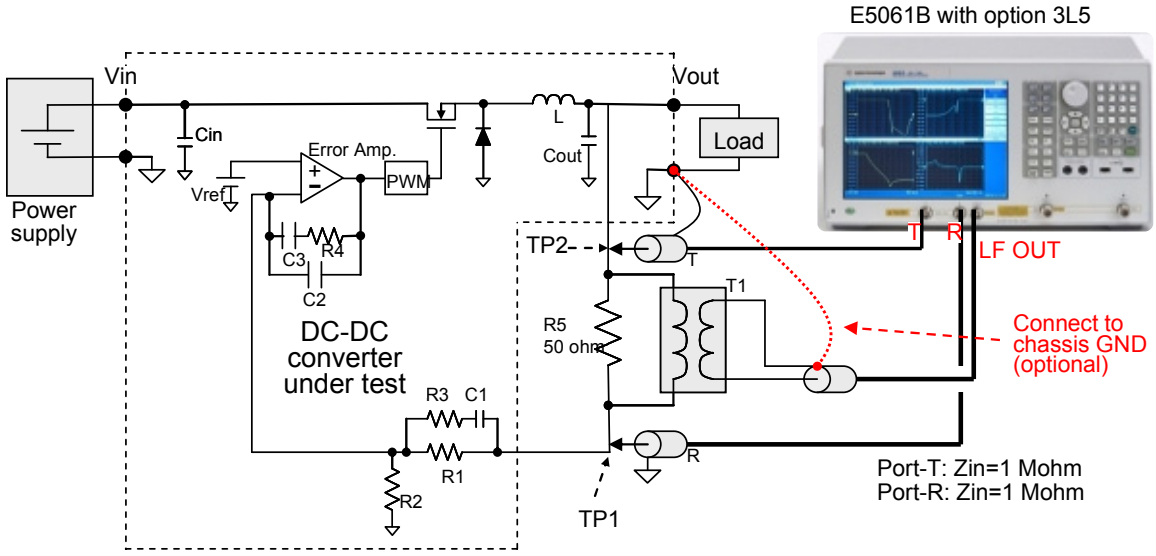


Figure 41: Instrumentation and setup to measure Gain-Phase stability of a DC-DC converter.

We inject the test signal through an isolation transformer in series to the voltage feedback path, where a low-impedance point (converter output) connects to a high-impedance point (error-amplifier input) so that the impact of the series impedance of the injecting circuit on the transfer function can be neglected. The transformer can be any small-signal low-frequency transformer suitable for the intended frequency range, which is typically 1 kHz to 1 MHz. This setup can be used for all converters, where at least the upper leg of the output voltage divider is externally accessible.

Over multiple decades of frequencies the gain magnitude can vary significantly, resulting in a stress in the dynamic range of the DUT and/or the instrument. At frequencies where the loop gain is high, the measured level at the TP1 test point could be in the noise. If we increase the output level of the analyzer, we run the risk that at frequencies, where the loop gain is low, the DUT's error amplifier goes into saturation. This was illustrated in *Figure 25* of [31], which is reproduced here as *Figure 42*. Note that as the source power is varied from -45dBm to -5dBm, different distortions show up at different frequencies: with low injected signal level the TP1 level (R level, lower left plot) becomes noisy at low frequencies, this iks where the loop gain exceeds 50dB. With high injected levels there are signs of saturations in the curves around the crossover frequency, which was verified by connecting an oscilloscope to the output of the error amplifier.

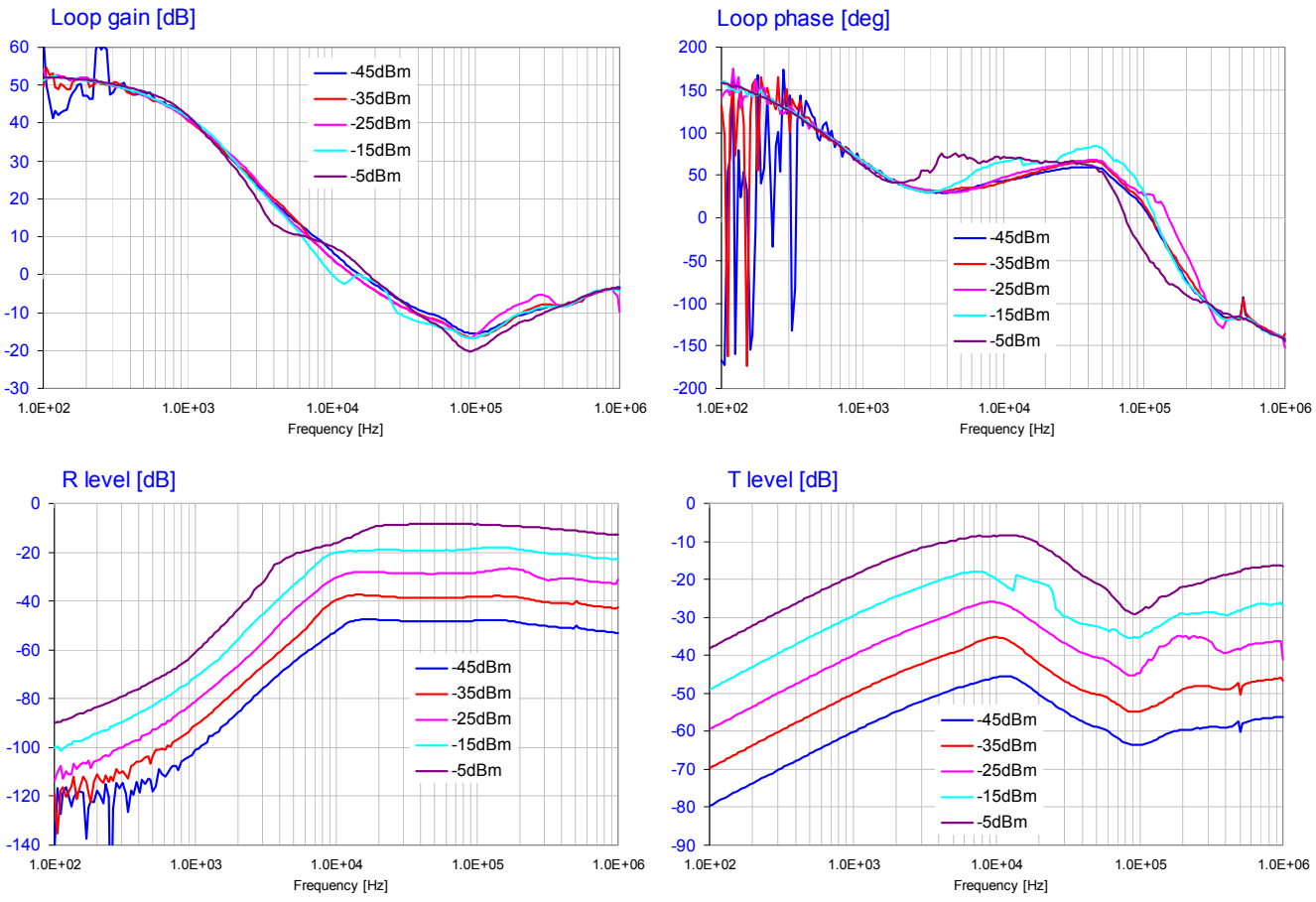


***Figure 42**: Gain-phase test measurement results with different source levels. The R and T levels refer to levels at TP1 and TP2 in Figure 41.*

Measuring the small-signal output impedance of converters required to overcome several challenges. The three major challenges are: a) the very low value of output impedance render usual impedance analyzers useless for this purpose, b) any connection discontinuity, even though the frequency involved is low, has a detrimental effect on accuracy, and c) traditional instruments have common internal grounds for their swept-frequency source and receiver inputs, creating a large error floor due to ground loops in the connecting cables. These challenges can be resolved by using a two-port shunt-through connection [32]. *Figure 43* shows side-by-side the problematic connection with one-port measurements and the two-port shunt-through measurement scheme.

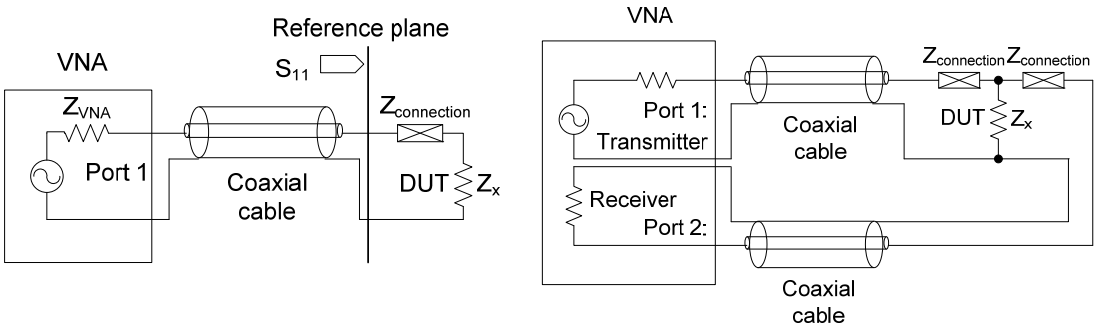


***Figure 43**: One-port impedance measurement scheme on the left, two-port shunt-through scheme on the right.*

Even with two-port shunt-through connections the selection of probe points, probe connections and calibrations have to be done carefully [33], [34]. When the instrumentation, connections, probes and calibrations are all selected properly, we can safely measure the small-signal output impedance of low-voltage DC-DC converters even in a live system board. *Figure 44* shows a setup and the corresponding results from [31].

The typical Frequency Response Analyzer or Vector Network Analyzer will allow us to measure the small-signal impedance of DC-DC converters. One may still ask: would the measured impedance be different if we did swept-frequency large-signal impedance measurements? Certainly for cases, where the large-signal excitation would drive the error amplifier, or any other part of the control loop into saturation, the result would be different, as this is the case when non-linear response is intentionally used. For most other cases though the result will be identical or very close. To test this hypothesis, we can build large-signal impedance-measuring setups by using either boost amplifiers connected in the small-signal setups, or by adding a few dedicated components to the output of the DC-DC converter we want to measure. Using an off-the-shelf boost amplifier is usually problematic because the connection from the amplifier output to the DUT needs to carry the large signal, and again we might be limited by any connection discontinuities where the amplifier's output cable is attached to the DUT. We have a much better chance to achieve the desired step-current slew rate if we use a simple FET electronic load, directly soldered to the output of the converter (note that some evaluation boards have this electronic load already built in for you). The only downside of this solution is that now we can measure only with the converter ON, since the FET requires the supply voltage to generate the load current. For small current steps we can select FETs with low gate charge, which enables us to directly use the 50-ohm VNA output to drive the gate. Note that the same setup can be used for both swept-frequency sine-wave and step-response testing.

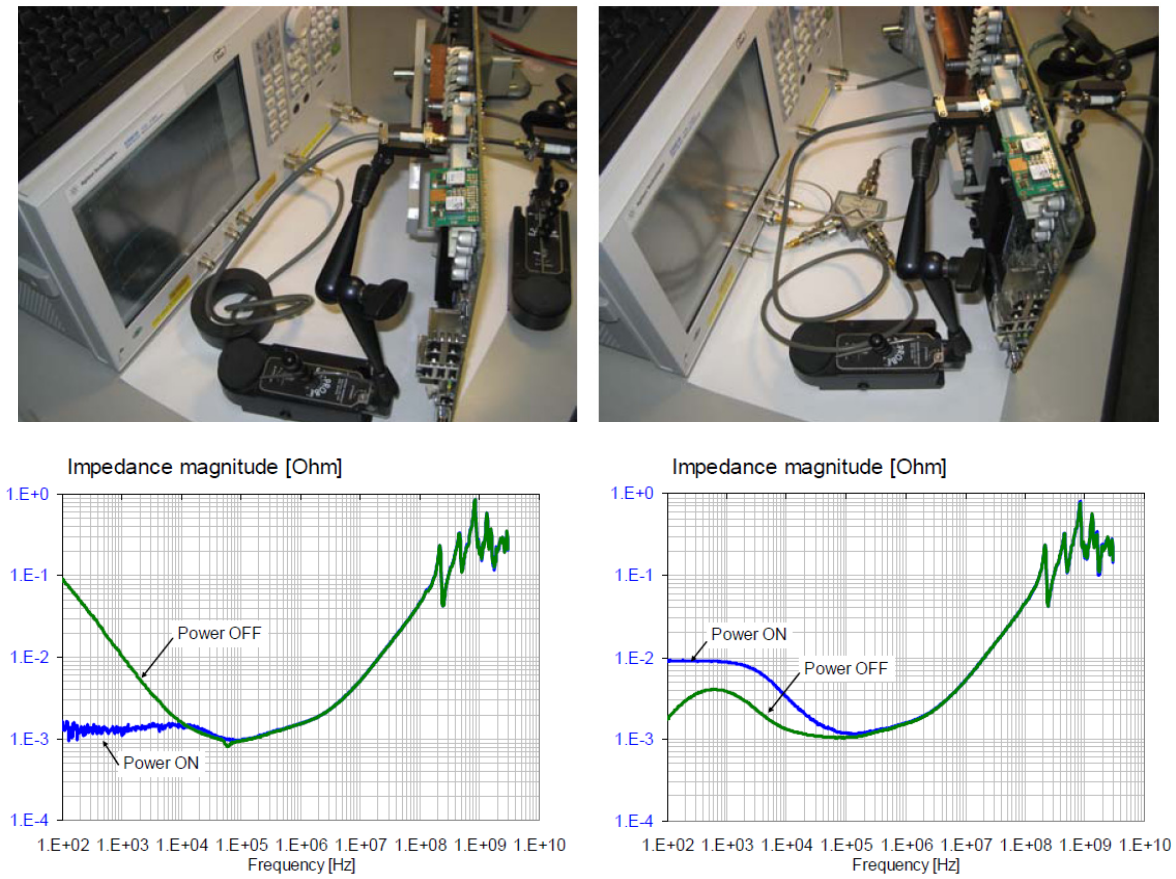


***Figure 44**: Measurement setup of a live system board with the S-parameter test port (on the top left) and Gain-Phase test port (on the top right). Bottom plots: measurement results in the 100 Hz – 3 GHz frequency range. Left graph: correct data using ferrite core on one of the cables. Right graph: incorrect low-frequency data without ferrite core.*

Figure 45 shows the schematics of two implementations, one for AC coupled VNA measurements and another scheme for DC coupled transient measurements. The FET usually requires some heat sink to deal with the dissipation because it has to operate in the Class-A mode.

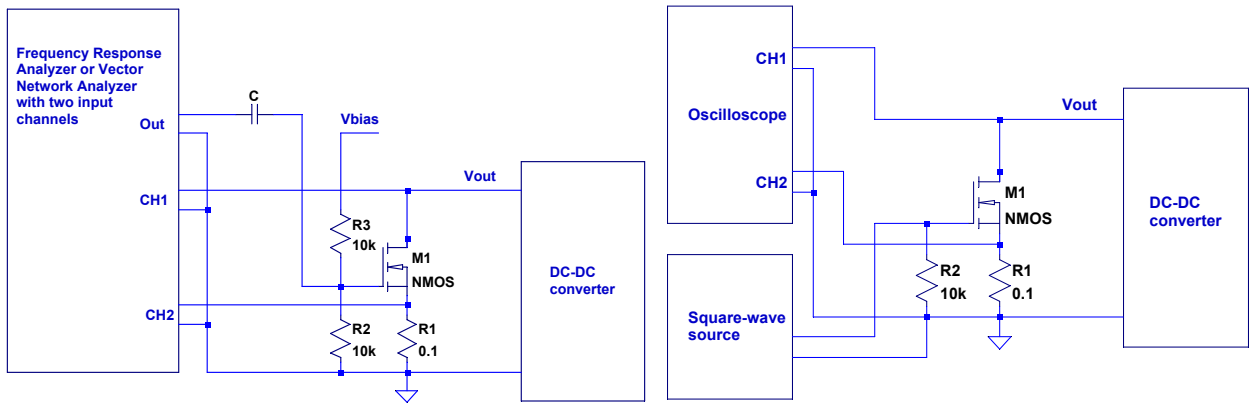


***Figure 45**: Schematics of an electronic load for large-signal swept-frequency (left) or step-response (right) measurements.*

Figure 46 shows two measurement setups. On the left there is a multi-purpose test setup with a Frequency Response Analyzer, Current injection transformer for output impedance or Gain-Phase measurement, and for transient measurement a Transient load (similar to the one shown on the right of *Figure 45*) and an oscilloscope. This setup was used to collect data for *Figures 33* through *40*. On the right a test board is shown with hand-soldered large-signal electronic load implementing the circuit on the left of *Figure 45*

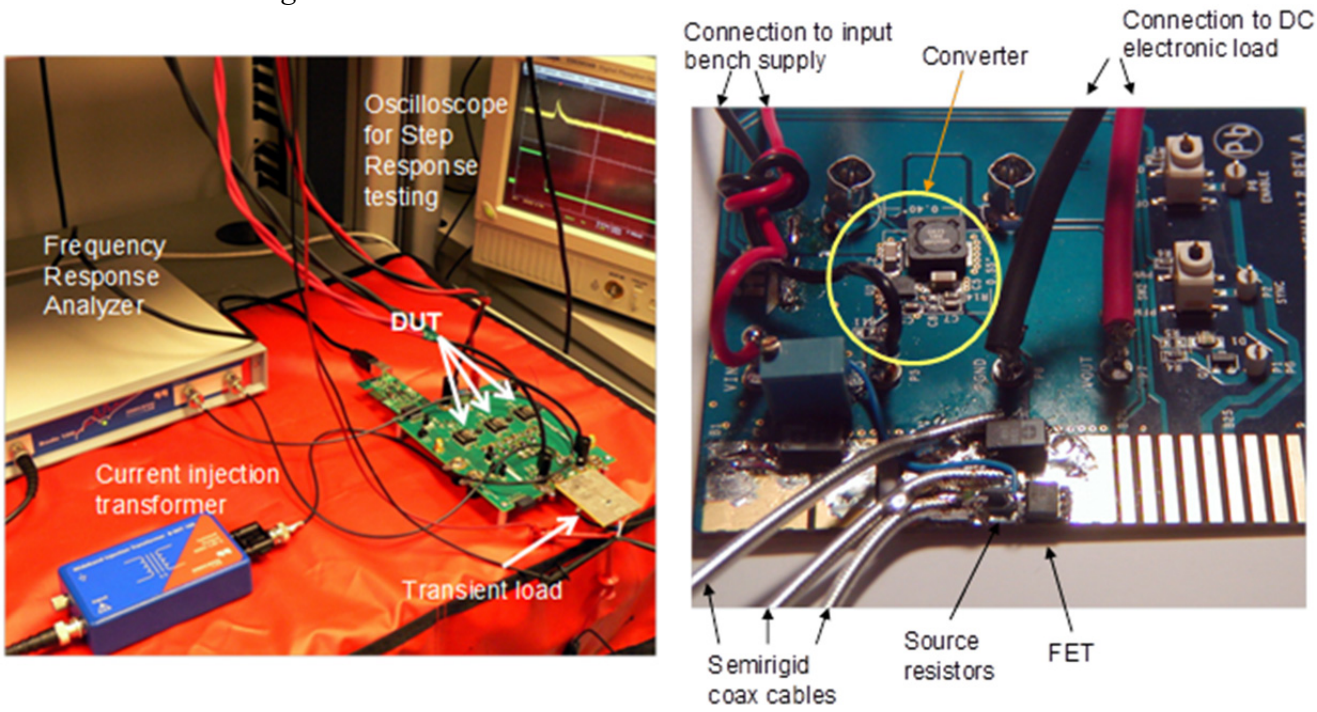


***Figure 46**: Multi-purpose test setup on the left and direct-attach electronic load for large-signal impedance measurement on the right.*

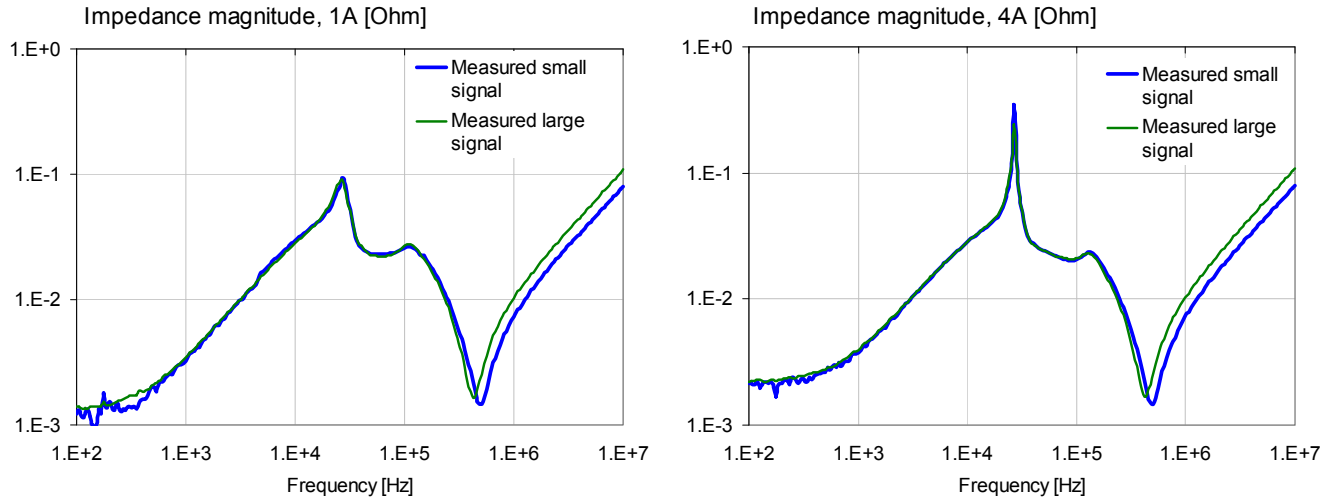


***Figure 47**: Comparison of small-signal and large-signal output impedances. The plots show results with only a pair of 22µF ceramic capacitors on the input and output, with 1A (on the left) and 4A (on the right) load current.*

To minimize inductance, the 0.1 Ohm source resistor was put together of ten pieces of 1 Ohm resistors. The FET, resistors and the connecting semirigid coaxial cables were soldered together with minimal stray loop. This setup was used to collect data for *Figure 47*. *Figure 47* shows measurement comparisons between small-signal and large-signal output impedances of a 6A current-mode buck converter, a similar one that was used for *Figures 16* through *31*.

Modeling, simulations

In addition to the various off-the-shelf simulator packages, today several of the converter vendors offer simulation models and/or tools, see for instance [36], [37]. Most of the simulations in this study were done with a SPICE-like simulator [38]. Another way to model DC-DC converters is to measure the Step Response, calculate its Fourier transform and take its frequency derivative: it yields the output impedance. *Figure 48* shows a correlation on a converter we used for *Figure 15*.

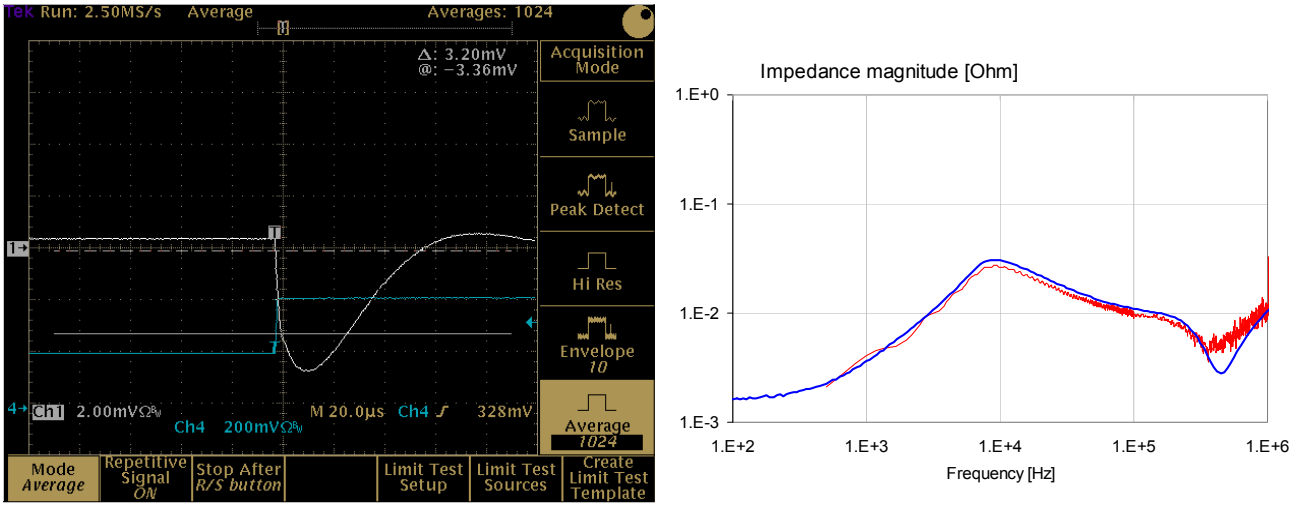


Figure 48: Time-domain excitation and step response (on the left) and output impedance calculated through the Fourier transform of Step Response on the right, red trace. Blue trace shows the output impedance obtained by large-signal swept-frequency measurement.

Conclusions

It was shown that the primary dynamic parameters in a linear-approximated converter can be linked to the Loop gain function of the closed feedback circuit. Loop stability can be obtained by maintaining sufficient phase margin. However, to avoid peaking of the output impedance with the bulk capacitors, and to avoid influencing the closed-loop output impedance high above the cross-over frequency, the phase margin and the gain-magnitude roll-off have to be appropriately selected. Type III compensations, though they help to increase the cross-over frequency, have a tendency of modifying (increasing) output impedance over a wide frequency range. Multi-phase converters do reduce the output impedance proportionally to the number of phases and they offer the advantage of lower input and output ripple. Digital control loops offer the flexibility of placing poles and zeroes in the transfer function in a convenient way, furthermore they can easily implement non-linear loop responses. Two-port shunt-through measurement setups can easily resolve the sub-milliohm low-frequency output impedance of DC-DC converters. It was shown that we can measure the output impedance with small-signal or large signal setups, alternately we can calculate it from the measured Step Response.

Part II: Power Filter Network and its Effect on DC-DC Converters

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Abstract
The usage of external filters in conjunction with DC-DC converters has been shown by demonstrated example, the effects to the stability of the DC converters when improperly implemented. Simulation of the converters characteristics and filter characteristics, clearly show how to implement subsequent filters to a DC converter and to filter the switching noise to an adequate level.

I. Introduction and Background Information

DC Converters Introduction

DC converters have evolved into several categories, the non-isolated buck converter being perhaps the most popular converter selected by circuit designers. Over the years, circuit designers were often confronted with the nagging problem of compensation of the loop within the converter to maintain stability over operating range conditions. With time to market conditions being a major issue in new product development, circuit designers also found themselves not being able to spend much time working out the problems encountered in the development of DC converters.

The increasing demands being placed on the circuit designer provided opportunities in the market for companies to specialize in the development of converter modules, thus alleviating all the design effort to create DC converters. This has been largely a very successful change and a lot of competition has resulted in lower costs of the units. With the great success of the converter modules, more modules were being used in the development of newer products. The converter modules that consisted mostly of open frame type assemblies, are now seeing more competition from those makers that provide encapsulated or closed frame modules, that include not only the switching FETs, but also the output inductor. This refinement provides yet more freedom for the circuit designer who needs higher availability in terms of FIT (Failure In Time) and smaller devices. With all the technical advances made in the development of DC converters, there has evolved the intellectual property within each company whose purpose is to provide, deliver on time, and make technical advances that prohibits others to copy and create competition. Therefore, the design of the converter whose output specifications are the same for all competitors, the internal workings is not.

Power Filter Introduction

The increasing usage of power filters comes primarily from those devices that employ PLL (Phase Lock Loop) circuits, such as memory devices and PCIe as examples. Generally, the circuit designer knows that the filtered supply rails needs to be quiet, that is a peak to peak voltage of less than 5 mV and this should occur at a frequency of about 1 MHz. This is about all that is known by the circuit designer. The implementation of the filter is done primarily based on the DCR of the inductor, that sufficient inductance is present. The mere chance of a capacitor appearing after the inductor is not likely unless the circuit designer is following some guidance provided by the chip maker that has within it a PLL.

DC Converter Specifications

The importance of the specifications of the DC converter is not confined to the specifications document provided by maker of the converter. There is a need to know for example, what is the output inductor value and DCR, the switching frequency, type of converter, and what power distribution network components that have been implemented. There are more items for the list of need-to-know.

A DC converter generally has an error amplifier which detects the output voltage, provides correction to the modulator, that keeps the converter from increasing or decreasing its voltage from the desired set point. The small signal capabilities of the error amplifier are generally required to

have its gain decrease at a rate of -20dB/decade near the cross over the "0 dB" level. There are many techniques used to provide this functionality which provides for operational stability of the regulator. It also matters whether the converter is a "Current Mode" or "Voltage Mode" converter. The actual implementation of the converter design, error amplifier, modulator, and compensation network all depend on what topology is chosen. The proper implementation for a power filter to be used in a PLL does depend on these factors mentioned here-in. We will need to estimate the cross-over frequency of the error amplifier, we will need to know what the frequency domain characteristics of the power distribution network (PDN) is, and we will need to know what the range of switching frequencies are of the converter.

Filter Specifications

The requirement of the filter usually comes from or should come from the supplier of the chip that needs to be filtered. Generally, the need for the filter is due to the fact that the chip uses a PLL to keep control over the digital logic within the chip. While the requirements should come from the chip maker, there seems in general to be a trend in what is needed in terms of attenuated noise and frequency requirements. The general terms given here is just that and should not in-of-itself, be used as a standard. The general trend seems to center on a peak to peak voltage variation of no more than 1 to 5 mV at 1 MHz, that the range of frequencies begin at 100 KHz and generally end at 100 MHz. Specifically, the attenuation begins at 100 KHz at rate of - 20 dB/decade to 1 MHz. From 10 MHz to 100 MHz, the noise is allowed to increase at a rate of + 20dB/decade. These are general in nature, it is far better to get the requirements from the chip maker.

The DC Converter Application

The DC converter application is the first element of the investigation of designing for a proper filter. The questions involved with this preliminary stage makes the assumption that the converter is an encapsulated design offering full output current without heat sinks, no additional compensation networks needed, just place the module on the board, provide a voltage divider to set the output voltage and with the recommended output capacitance, you will have a wide bandwidth functional regulator. The circuit designer has to think no more about the regulator than just these few specific items! This may be true if there was nothing more than a resistive load on the regulator.
There is more that the circuit designer must consider, the power distribution network (PDN) is a major item. The choice seems to be that of the "Big V" or a flat response. The first is generally but not always, a set of capacitors that tend to be all of the same value, mostly ceramic capacitors. The impedance over frequency when measured and plotted tends to look like a big "V". The flat response is the result of careful selection of a set of capacitors that may differ in type as well a quantity. The point being to provide a flat as possible impedance.

The amount of PDN capacitance does greatly influence the cross-over frequency of the error amplifier. The type of topology of the converter also affects the cross-over frequency. However, there is no mention in the specifications for the converter what the cross-over frequency is, nor is there any information about the type of converter it is. The information about the type, that is, is the converter a current mode or voltage mode type? If it is a voltage mode, then the value of the output inductor is important to have knowledge about. The other item for consideration is what the gain of the error amplifier over the range of its useful frequency. The gain -- bandwidth product is an important piece of information. We can assume that the product is 1E6 meaning that at 1 Hz, the

gain in dB is +120 and at 1 MHz, it is 0 and by this simplicity, the slope is a -20 dB/decade. Can we estimate what the cross-over frequency is? Yes, if the type is known.

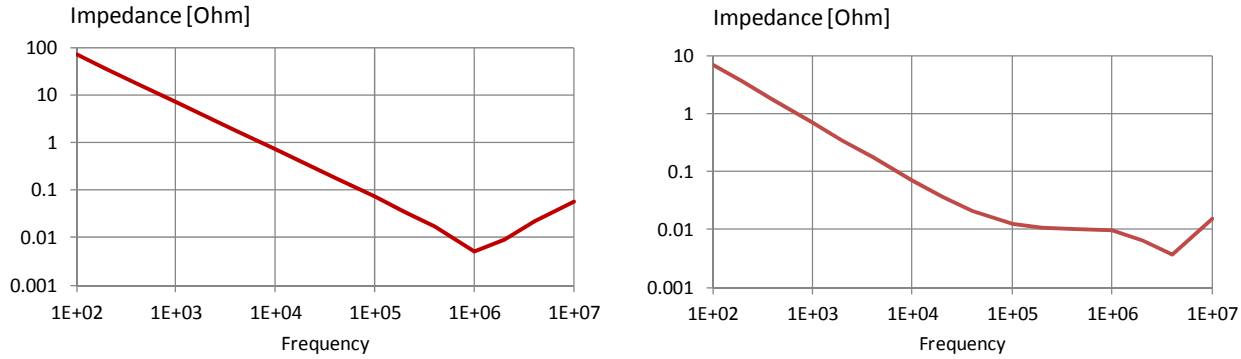

***Figure 1**: PDN Impedance for DC-DC Converters, Big V Left, Flat Impedance Right*

Cross-Over Frequency

Our example problem will be using a 4 amp device, switching at a frequency of approximately 1 MHz [1]. It is a current mode controller. The output voltage has been set to 1.800 volts, and it has a recommended minimum capacitance on the output of 22 µF. The capacitor selected is a ceramic X7R or X5R class II ceramic with a voltage rating of 10 volts or more. The voltage rating is important, these capacitors are a class II type and their capacitance values are highly influenced by the DC bias applied to them. Running the capacitors at 50% of rated voltage will reduce the capacitance to a value much less than 22 µF. The ESR value of a 22 µF capacitor, for a 0805 package is about 4 mΩ in general. We need to establish 2 corner frequencies, one based on the total bulk capacitance and the second based on the total ESR of the bulk capacitance. This is only valid for the current mode controller. The load resistance for this example is determined by the set point of the output voltage and the load current, in this case 450 mΩ. It has also been determined that the maximum ripple voltage from the regulator should not exceed 42 mV Pk. -- Pk. This sets up a rough calculation of what the gain of the error amplifier should be.

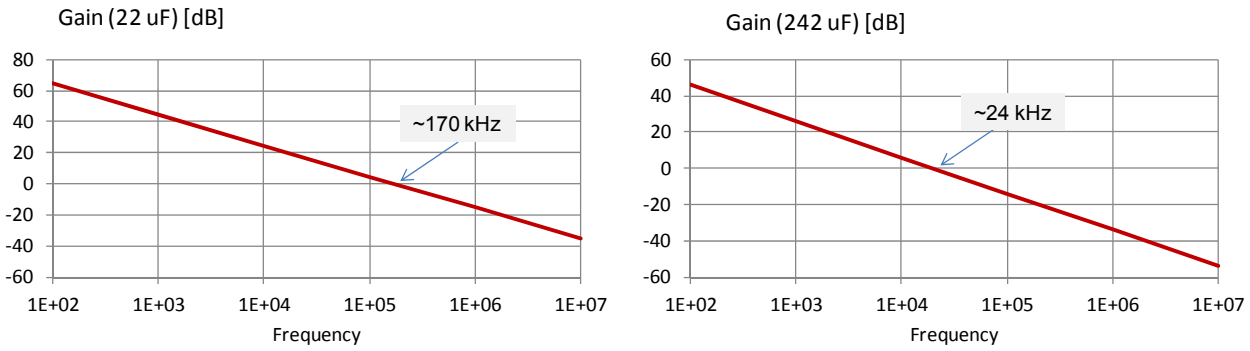

***Figure 2:** Gain and Cross-Over Frequency Estimates for Current Mode Controller*

Figure 2 shows the difference in the cross-over frequency values based on the PDN chosen, and the gain is also lowered with increasing bulk capacitance. The first corner frequency is based on the load resistance and the bulk capacitance value. The second corner frequency is determined by the combined ESR of the bulk capacitance and the total capacitance.

$$FC1 = 1/(2 * \pi * RLoad * C) \quad (1)$$

$$FC2 = 1/(2 * \pi * ESR * C) \quad (2)$$

Figure 2 also shows that the error amplifier control range is limited to the cross-over frequency in each case, the step loading voltage due to a step change in current is then is basically determined by the impedance of the PDN beyond the cross-over frequency. Below the cross-over frequency, the resulting voltage due to a step loading is within the range of control of the error amplifier. An example of the effects of a step load, consider in *Figure 1*, the left chart is the PDN characteristics of just a 22 µF capacitor. With a step load current of 50% of maximum load, we have 2 amperes, this multiplied by the impedance at a frequency of 170 kHz, having a value of about 36 mΩ, is about 72 mV. With a PDN of 242 µF, and with the same loading conditions, the voltage resulting from the step loading is also 72 mV. However, at 20 kHz for the 22 µF case, the voltage resulting from a step load is 720 mV as a result of much higher impedance, by a factor of 10!
The ripple voltage due to the switching action of the regulator can be quickly estimated from the PDN itself. The switching frequency of our converter is about 1 MHz. If we refer to *Figure 1*, the impedance of either graph shows a value of about 3 mΩ. Therefore the inductor current, which is usually about 30% of the load current, when multiplied by the PDN impedance at the switching frequency will estimate a voltage ripple. For each case shown in *Figure 1*, the resulting ripple voltage is about 3.6 mV. If the switching frequency was much lower, 400 KHz, then the resulting ripple voltage would be very different. For the case of the 22 µF capacitor, the impedance is about 18 mΩ, resulting in a ripple voltage of 21.6 mV. Compare this to the 242 µF capacitor, the impedance is 10 mΩ and will result in a ripple voltage of about 12 mV.

The choice of the design of a PDN matters based on expected operating conditions. To consider a "Big V" design or a flat impedance design requires about the same amount of effort to realize a working design. There may be clear advantages to either, such as cost and/or space requirements.

Power Filter Application

Ask a circuit designer what filter inductor would be chosen for a 500 mA design, and the answer would be a high impedance ferrite bead with a low DCR value. High impedance meaning hoping for enough attenuation, and low DCR so that the DC converter voltage doesn't have to be tweaked up in voltage to cover the voltage drop. The basic considerations for an adequate filter is based on how well we match the target impedance of the regulator, and how well we manage to match the impedance of the load. The attenuation requirement is met when we can attenuate the ripple voltage to an acceptable level. The target impedance of the PDN is what drives the type, size and quantity of various types of capacitors. If a "V" design is chosen, there will be many ceramic capacitors, for a flat design concept, the types of capacitors used will be many such a polymer type of tantalum capacitors and a few ceramics. The target impedance is basically determined by the assumed allowable transient voltage resulting from a step load, usually 50% of load current. The quotient of these 2 factors determines the valuation of target impedance.

As an example, our 4 A converter, set for 1.800 volt output, has the following features:

1. Set point accuracy over time and temperature 1% .....±18 mV
2. Line and Load regulation total over time and temperature 1%.....±18 mV
3. Maximum deviation 5%.....±90 mV

The maximum deviation for ripple voltage and transient voltage is ± 54 mV. We can assume that the ripple voltage will be about 20 mV, leaving just 34 mV for transient voltage. The target impedance then estimated by dividing 34 mV by the step load current. If the step load is 50% of the total load current, then the target impedance is estimated to be 17 mΩ. The target impedance is shown in *Figure 3*.

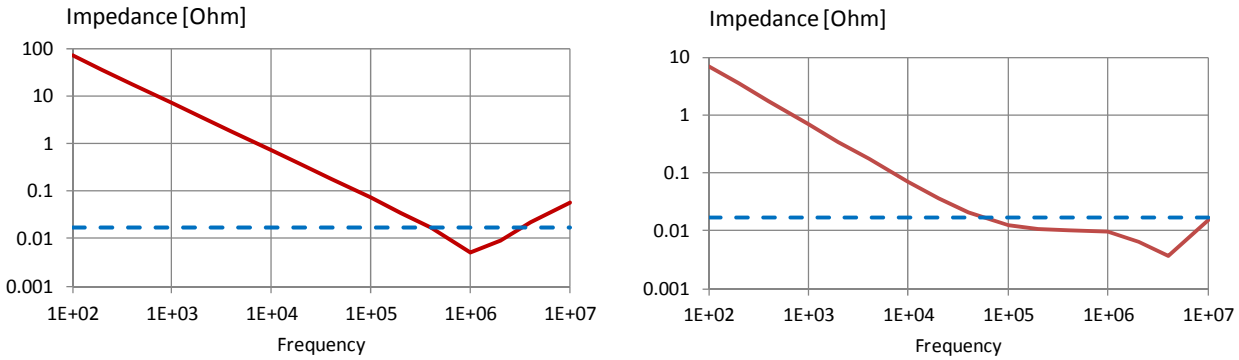

***Figure 3**: PDN with Target Impedance Included*

Figure 3 shows that the PDN for the 22 µF capacitor case, to be limited and perhaps just beyond the range of the error amplifier. In the second case, the impedance of the capacitor is lower resulting in a wider effective range.

If we estimated the ripple voltage based on the target impedance, this would suggest a value of 20 mV. However, if our filtered voltage requirement is just 1 mV, then the ripple voltage needs to be attenuated by a factor of 20 or about -26 dB. Due to component variation, we should provide somewhat more attenuation; a good number in general is about -3 dB. Our design requirement should be -30 dB. If the transient loading affects are to be considered, the effective transient voltage is the sum of the transient voltage as a result of the step loading and ripple voltage. This value is 54 mV and the attenuation needed for 1 mV at the load, the attenuation required is 34.6 dB and tolerance of -3 dB suggests a need for - 37 dB of attenuation. The required noise voltage of 1 mV at the load is set based on a frequency of 1 MHz, and that the noise voltage may increase by + 20 dB at 100 kHz and at 100 MHz. The problem of the 22 µF capacitor case is now showing a very real problem, the value of impedance at 100 kHz clearly is significantly higher than the target impedance, the other case, the 242 µF capacitor, the impedance is lower than the target impedance at 100 kHz. Matching the target impedance is one of the basic requirements for an adequate filter application, and we can see from these 2 design considerations, only the second case meets the requirement. Another consideration in any filter design is the requirement that the attenuation of the filter have minimal gain in the attenuation. Usually, at the corner frequency of a filter, there is some lift where the gain goes positive before going negative. The positive gain indicates a multiplication of the noise voltage at those frequencies. *Figure 4* shows gain of almost 5 in the region of 50 kHz to 70 kHz, ideally this should be nearly 1.

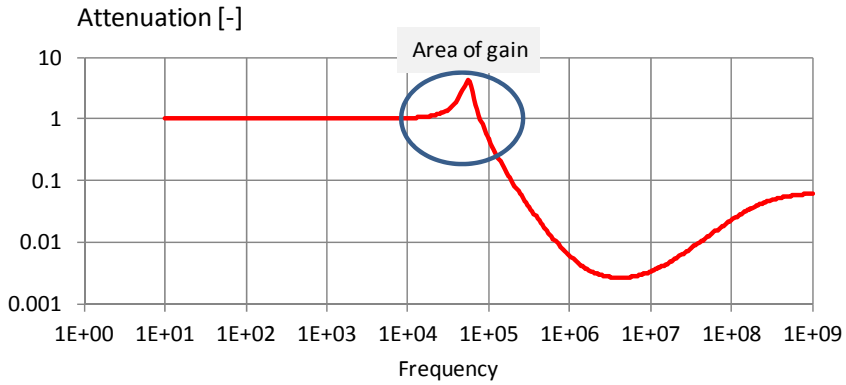

***Figure 4**: Attenuation with Gain*

Filter input impedance, converter looking toward the load

What the DC converter sees when a filter is implemented, should be just the load itself at DC, that is what it was designed to power up. Figure 5 shows what the regulator should see.

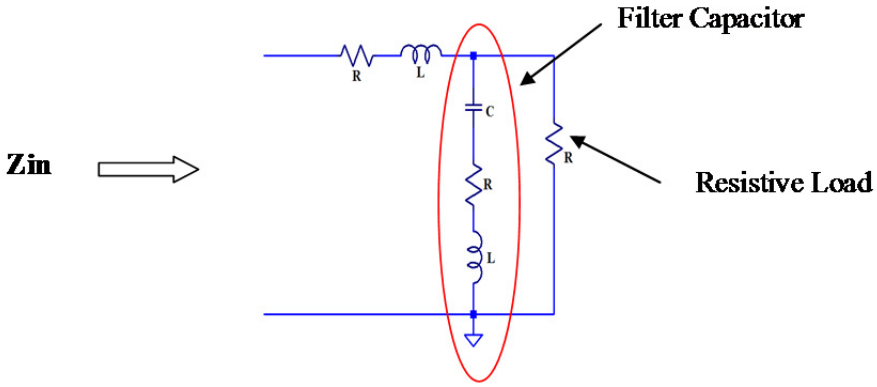

***Figure 5**: Filter Circuit as Seen by the Regulator*

From the regulators point of view the input impedance of the filter network as well as the filters load, should be seen as resistive as possible, it also should see just the target impedance when an AC signal is presented. The series *R* and *L* represent the inductor itself. The filter should now look like a resistive load of 450 mΩ if we provide 4 amps of current into the filter. In reality, there is the DCR of the inductor which will add to the effective total DC resistance of the load. The attenuation of the filter should be set to -34 dB. The attenuation should be at 1 MHz, the corner frequency where the filter begins to work is not based on -40 dB/ decade, it is close to -20 dB/decade. There is sufficient inductance in the output capacitor and the printed circuit board's etch from the filter to the target chip, effectively reducing the generally accepted thought of an L-C filter providing -40 dB/decade. The corner frequency is then calculated:

$$Fcorner = 0.707 * 1MHz * 10^{(Attenuation\ Required/20)} \quad (3)$$

where ***Attenuation Required*** is given as negative value.

The corner frequency as calculated is 14.1 kHz, the point where the filter should start to attenuate. It is also this frequency where the impedance of the inductor should look like the intended target impedance for the regulator, 17 mΩ. The inductance value required is 206 nH. To keep the inductor and its series resistance from oscillating, creating an unstable condition of operating, a general rule is to set the series Q_s of the R-L network to 0.3. While stability can be maintained with a Q_s value up to 0.5, it will be close to be under damped and will allow for over shoot. By choosing a value of 0.3 for the series Q as a starting point allows for some flexibility in the choice of the inductor or by adding additional resistance in series with the inductor. The series Q of an inductor is given as:

$$Qs = \frac{\omega L}{R} \tag{4}$$

The damping factor which indicates the stability of the circuit needs to be equal or greater than 1.0. If the damping factor δ is less than 1, the system is under damped and will exhibit a damped oscillatory condition. The damping frequency is given as:

$$\omega_d = \omega_r \sqrt{1 - \delta^2} \tag{5}$$

where ω_d is the damped frequency and ω_R is the resonant frequency. There is a relationship between the value of the series Q and the damping factor:

$$\delta = 0.5Q^2 - 1.75Q + 1.75 \tag{6}$$

If the series Q is equal to 0.5, the resulting damping factor is equal to 1.0. In choosing the series Q to equal 0.3 provides for a damping factor of 1.27 which indicates that the system is over damped and minimal oscillation will occur. Given that the series Q is 0.3 to start; the suggested value of the series resistance of the inductor can be determined. Using (4), the value of DCR is 57 mΩ based on the corner frequency calculated in (3) of 14.1 kHz. The calculated results of what the regulator will see at DC, 1 kHz or less, is the DCR of the series inductor of 57 mΩ and an impedance of the inductor of less than 2 mΩ. With an equivalent load resistance of 450 mΩ, the total series impedance is 507 mΩ. The circuit will be over damped and should help provide an attenuation that has little if any positive gain.

Filter input impedance, the load looking toward the converter

The load under normal situations where there is no filter would see from an AC perspective, just the target impedance as presented by the PDN. From a DC perspective, it would see the output source impedance of the regulator. With a filter present, the expectation of the load is to see the target impedance, capable of supplying AC current. *Figure 6* shows what the load should see. *Figure 6* shows that the target impedance *Zt* is in series with the filter inductor *Lf*. If we assume that Zt is purely resistive, then the total series resistance as seen by the filter inductor is the sum of the DCR and the target impedance. The series Q of this part of the circuit will be less than 0.3 which indicates good stability. The valuation of *Zt* however, may show a true impedance with some DCR, which impedance maybe capacitive or inductive. *Figure 6* also shows that there is a probable parallel resonance between the filter inductor, *Lf* , and the capacitor *C*. This is to be avoided!

From the load looking into the filter, it should see just the target impedance as if the filter was not present. To cause the load to see just the target impedance can be accomplished by setting the series resistance *Rc* of the capacitor to equal the target impedance of 17 mΩ. The parallel resonance issue can be solved if the value of capacitance is chosen wisely. To understand this problem we need to look at the characteristics of the parallel circuit. Unlike a series resonant circuit which has a defined resonant frequency, the parallel resonance is not well defined, it is depended on the equivalent value of the parallel R of the circuit.

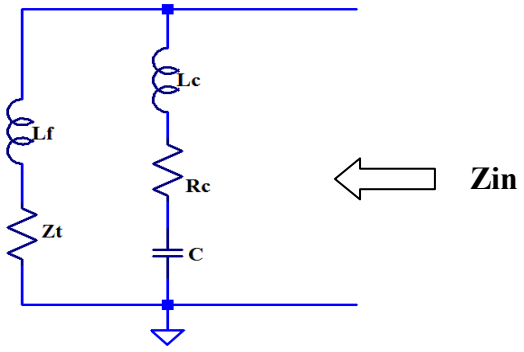

***Figure 6**: Filter Circuit as Seen by the Load*

Figure 7 shows a parallel resonant circuit. At resonance, the impedance value of the *L* and *C* are identical but of opposite signs. The current drawn by the impedances will be nearly 0 amperes and the source which is connected to the circuit will see just the value of *R*.

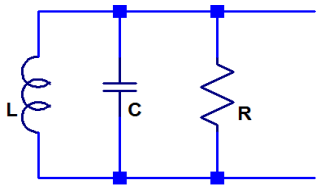

***Figure 7**: A Parallel Resonant Circuit.*

The parallel resonance of circuit in Figure 7 is not merely just the square root of *L* and *C*, although it is a part of the equation. The resonant frequency is given in (7).

$$Fr = \frac{1}{2\pi\sqrt{LC}}\sqrt{1-\frac{CR^2}{L}} \qquad (7)$$

If the value under the radical $\sqrt{1-\frac{CR^2}{L}}$ is set to 0, then there is no resonant frequency! Going one step further, if we set $1 = \frac{CR^2}{L}$, the value of *L* is already known, the value of *R* is set to the target impedance, therefore the value of *C* can be determined! To realize the condition of no resonance, the effective value of *R* must be first determined. *R* in *Figure 7* is the parallel resistance of the circuit and this value must be determined. The equivalent parallel resistance of each leg of the parallel circuit can be shown to equal:

$$Rp = Rs(1 + Qs^2) \qquad (8)$$

Each leg then has an equivalent parallel resistance. On the far left side of the circuit we have a series resistance equivalent to the sum of the DCR and target impedance, making the assumption that the target impedance is resistive. The total series resistance is then 57 mΩ and 17 mΩ for a total of 74 mΩ. The series Qs is given in (4) and at 14.1 kHz is 0.23, the equivalent parallel *R* is then is 78 mΩ. If the value of *Rc* in *Figure 6* is the target impedance of 17 mΩ, then the total equivalent parallel resistance would be dependent on either the inductance Lc of the capacitor, or on the value of capacitance *C*. Estimating that the capacitance value would be greater than what could be realized in a single ceramic capacitor, the capacitor is likely to be a polymer tantalum whose typical inductance is in the range of 1.5 nH to 2.5 nH. Using (4) and the corner frequency of 14.1 kHz, the value of the series Q for the capacitor using 2.5 nH for the inductance of the capacitor is 0.013. The equivalent value of *Rp* for the capacitor is then basically the series resistance of 17 mΩ. The equivalent parallel resistance of both legs is 14 mΩ. From (7) having the equivalent parallel resistance, using the value of the filter inductance of 207 nH and setting the radical to 0, the value of capacitance required is 1056 μF.

Filter Inductor

The filter inductor chosen is assumed to maintain its inductance value with a full load current present. The inductor chosen by the circuit designer, maybe a gapped ferrite inductor or a ferrite bead, depending on the load current. The ferrite bead will change its inductance to a lower value due to the current being passed through it. Characterization of the ferrite bead or any other inductor, needs to be done. Selecting the value of inductance should start with a no load current basis, this will set the maximum series Q of the circuit. The selection of the capacitor *C* can be decreased if it is known how much the inductor will drop in value due to a load current bias. The decrease in capacitance is limited. It should not be decreased below the series resonant corner frequency (14.1 kHz) created by the filter inductor and the capacitor. The series impedance of the capacitor and the inductor with no loading will cause that impedance to be equal to the target impedance. For this series of calculations, the minimum value of capacitance is 615 μF.

II. Actual Circuit Used and Measurements Actual Circuit Components

The actual circuit used to verify the concepts depicted thus far consist of an evaluation board for the chosen converter, to which a filter network was added, and modified the bulk capacitors to create a flat impedance type of PDN whose target impedance was set to 22.5 mΩ.

The components used are:

1. Current-mode non-isolated converter, 4A rated [39].
2. Bulk PDN
    a. (1) 220 μF, polymer tantalum capacitor, ESR = 25 mΩ.
    b. (2) 22 μF, ceramic X5R capacitors, ESR = 4 mΩ total.
    c. (1) 2.2 μF, ceramic X5R capacitor, ESR = 10 mΩ.
3. Filter Network
    a. (1) Ferrite Bead, 4 ADC rated, 30 ohms impedance.
    b. (1) 220 μF, polymer tantalum capacitor, ESR = 25 mΩ.
    c. (2) 22 22 μF, ceramic X5R capacitors, ESR = 4 mΩ total.

The original evaluation board was provided with a PDN of (2) 22 µF, ceramic X5R capacitors located near the controller. *Figure 8* shows the set up of the evaluation board with the output filter added.

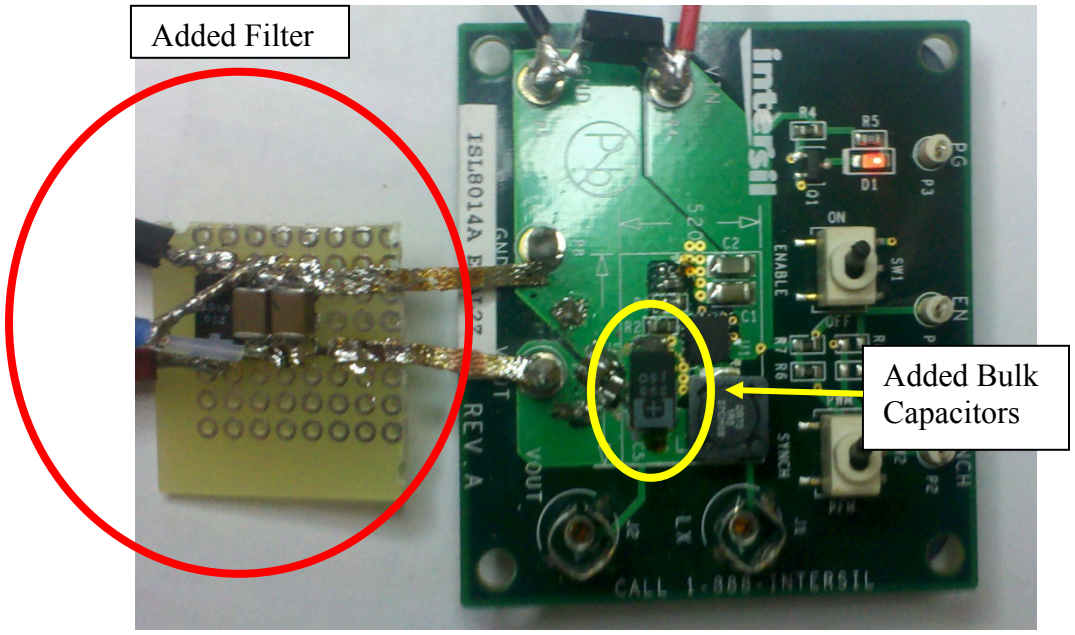

***Figure 8**: Photo of the Evaluation Board and the added Filter Network*

Measurement of the output PDN

With the regulator off, the bulk capacitors were measured at the terminals of the evaluation board with the filter present. *Figure 9* shows the impedance profile of the bulk capacitors using a VNA. *Figure 10* shows the impedance of the bulk capacitors with the regulator on. The impedance profile shows a relatively flat profile from about 15 kHz to 1 MHz.

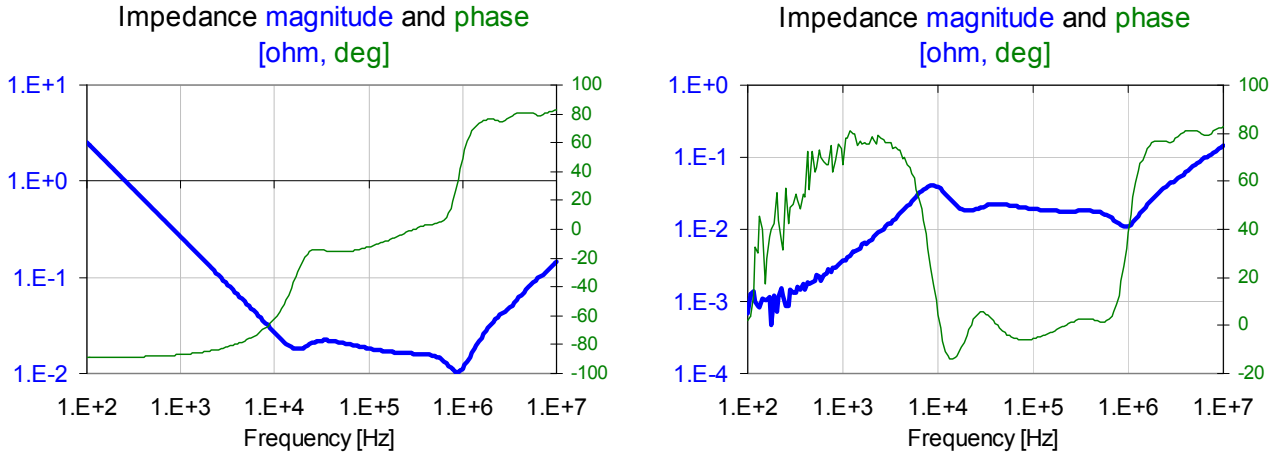

***Figure 9**: With the regulator Off, the impedance of the bulk capacitors (on the left).*
***Figure 10**: Regulator On with 0 Ampere Load Current (on the right)*

Figure 11 shows the attenuation of the filter. The measurement made by using the VNA ports of "A" to "B" and the reference port. The regulator was ON but with no current being drawn from the load.

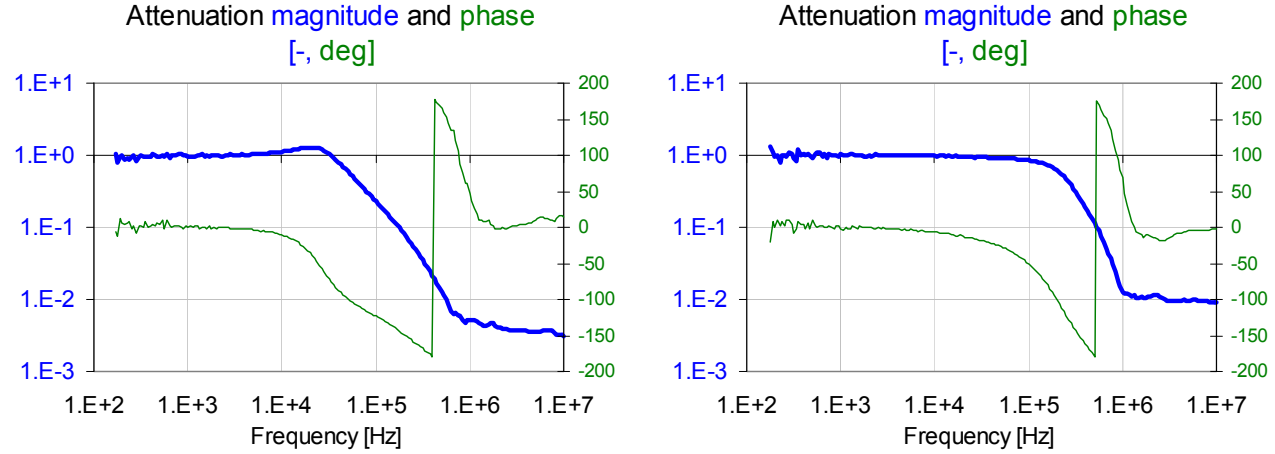

***Figure 11**: Attenuation of the filter with no load current (on the left)*
***Figure 12**: Full load current of 4 A (on the right)*

Figure 11 shows a slight elevation in the attenuation near the 20 kHz area. The overall attenuation at 1 MHz is -45 dB. The phase show relative flatness out to 20 kHz. The corner frequency is 22 kHz. With a 4 A load, the filter was again measured, see *Figure 12*. With the full load current of 4A, the attenuation shows good stability. Notice also the phase is very close to 0^{o} all the way out to 20 kHz. Roll-off of the attenuation begins at 100 kHz and the maximum attenuation is -40 dB and occurs at 1MHz. *Figure 11* shows the corner frequency of 22 kHz, and with an output filter capacitor of 264 µF, we can estimate that the inductance of the ferrite bead is at no load current is 191 nH. In *Figure 12*, the corner frequency moved to about 100 kHz at full load current of 4 A, and the inductance of the ferrite bead is approximately 10 nH. The maximum current rating of the ferrite bead is 4 A, we are at its maximum capability.

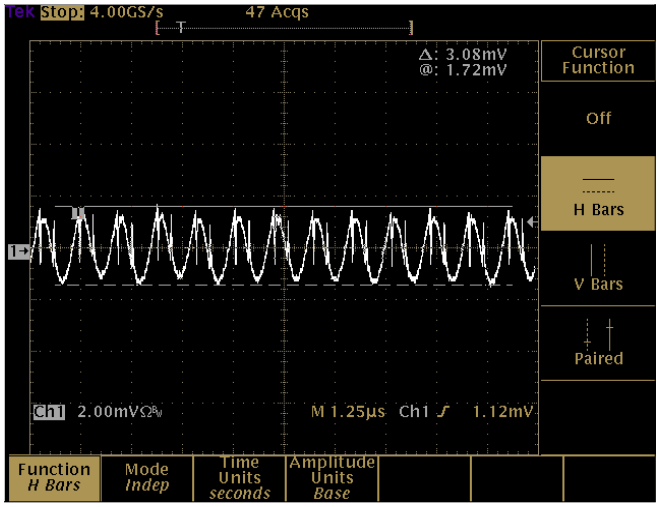

***Figure 13**: Ripple voltage before the filter*

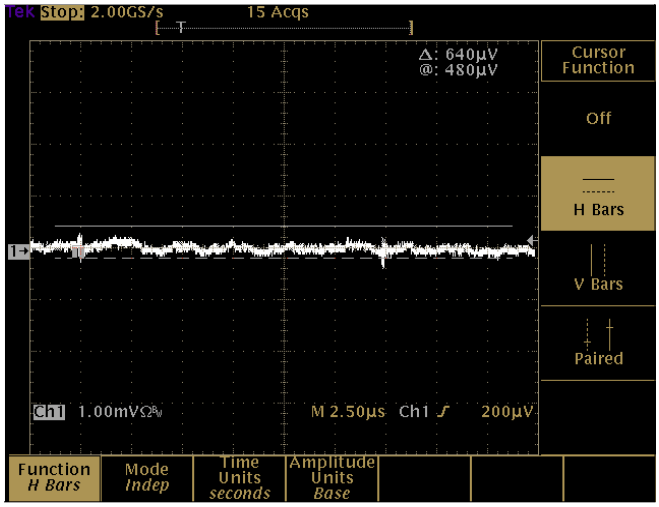

***Figure 14**: Ripple voltage after the filter*

Figure 13 shows the ripple voltage before the filter with a 4 A load present. The magnitude of the ripple voltage is approximately 3.1 mV. *Figure 14* shows the ripple voltage after the filter with the same load current of 4 amperes. The magnitude of the voltage in *Figure 14* is 640 µV. The resultant attenuation factor is about -14 dB. The assumed requirement of 1 mV or less at the load has been met. *Figures 15* and *16* show the ripple voltage before the filter and after the filter with a no load current on the output of the filter. The magnitude of the ripple voltage before the filter is 5.4 mV and the magnitude of the attenuated ripple after the filter is 640 µV shown in *Figure 16*. The attenuation factor is about -18.5 dB.

Figures 9 through *16* were measured with the sense lines of the regulator before the filter.

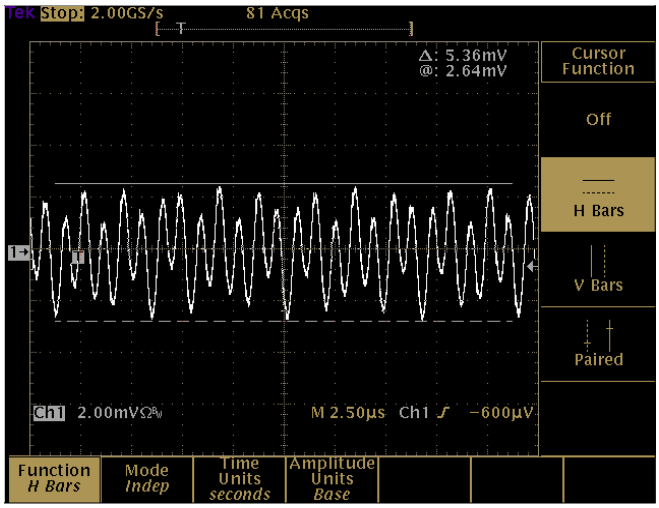

***Figure 15**: Ripple voltage before the filter*

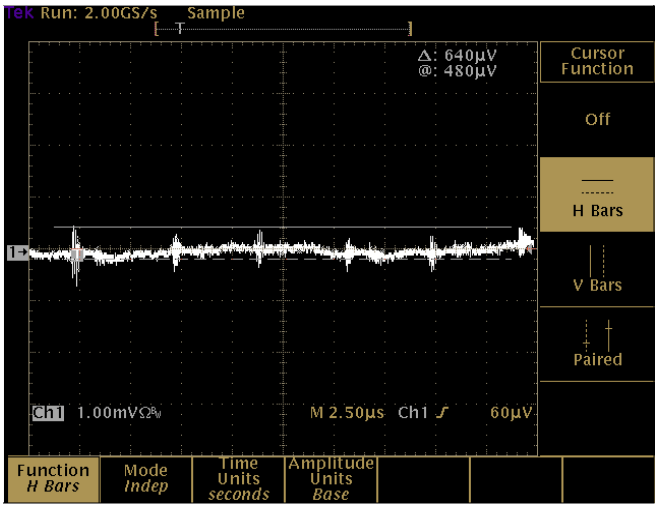

***Figure 16**: Ripple voltage after the filter*

With the sense lines of the regulator moved to the output of the filter, *Figures 17* through *24* show the effects of the location of the sense lines has on the regulators performance.

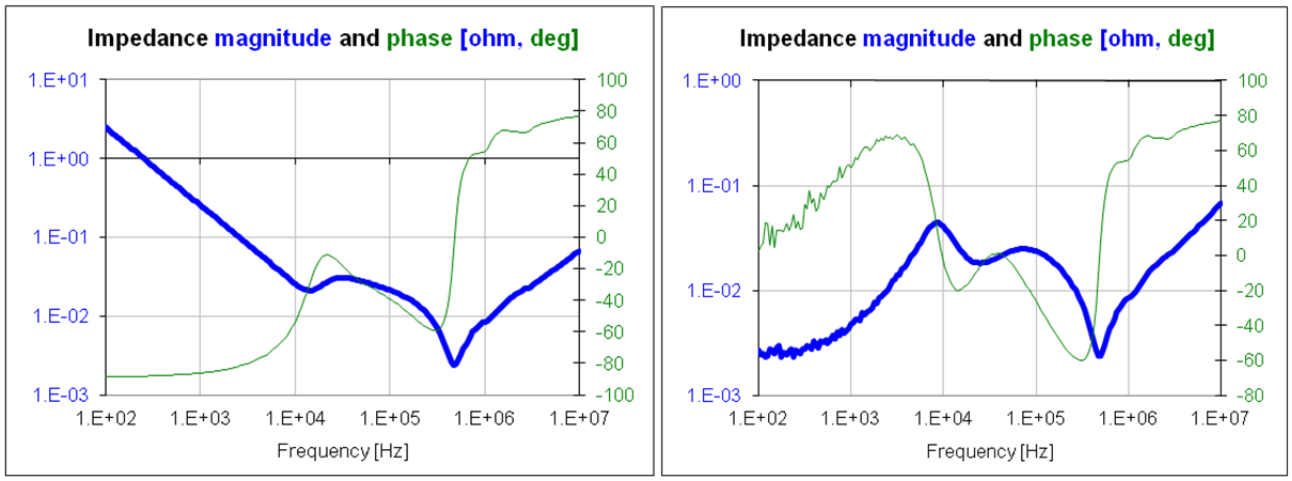

***Figure 17**: Impedance of the bulk and filter with the regulator OFF (on the left)*
***Figure 18**: Impedance of the bulk and filter with no load current (on the right)*

The difference between *Figures 9* compared to *17*, and *Figure 10* compared to *18* are quite different and shows the effect of the filter impedance on the regulator. *Figure 19* shows the regulator with a 4 ampere load. *Figure 20* shows the regulator with the sense lines before the filter and with a 4 ampere load.

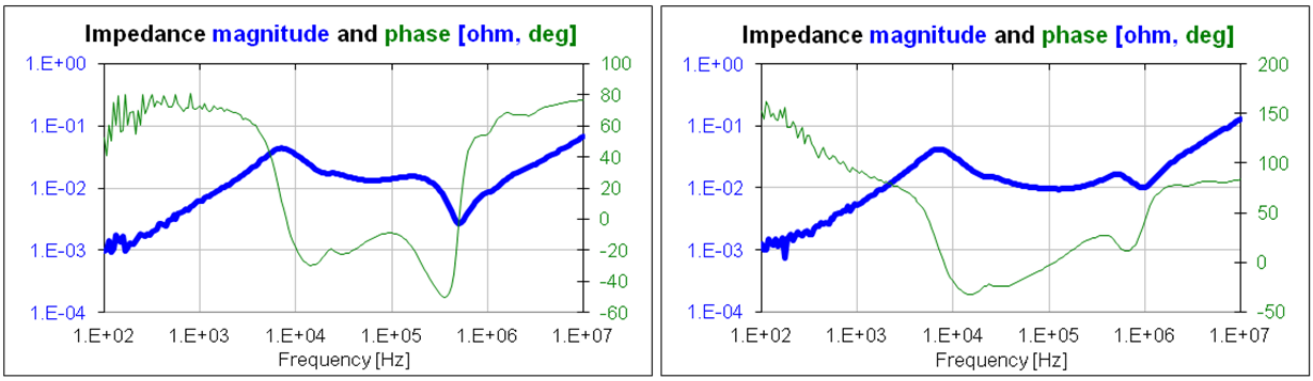

***Figure 19**: Impedance of the bulk and filter with a 4 Ampere load, sense lines after filter*
***Figure 20**: Impedance of the bulk with a 4 Ampere load, sense lines before filter*

With loading in this example, the difference due to the location of the sense lines is little. However, with less than a full load current, the differences are more pronounced.
The filters ability to attenuate the ripple voltage is shown in *Figures 21* to *24*.

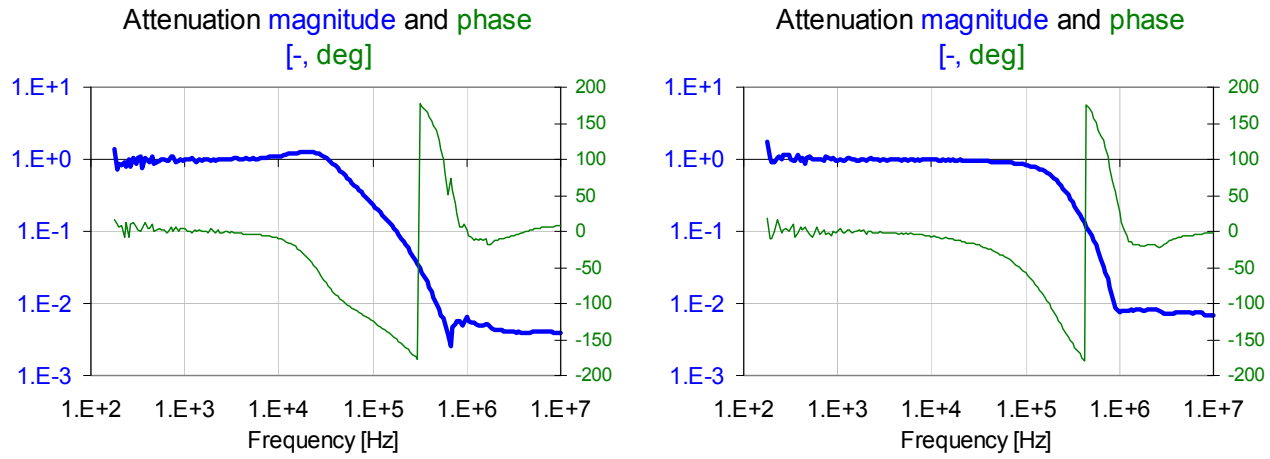

***Figure 21**: Sense Lines Connected After the Filter, No Load*
***Figure 22**: Sense Lines Connected After the Filter, 4 Ampere Load*

Figures 21 and *22* show little difference in the attenuation characteristics of the filter with the sense lines connected at the output of the filter. From the point of the attenuation, there is little difference as to where converter sense lines are connected. *Figures 23* and *24* show the ripple voltage with the sense lines connected after the filter under no load conditions, the attenuation is still quite good. *Figures 25* and *26* show the results with 4 ampere load again with the sense lines after the filter.

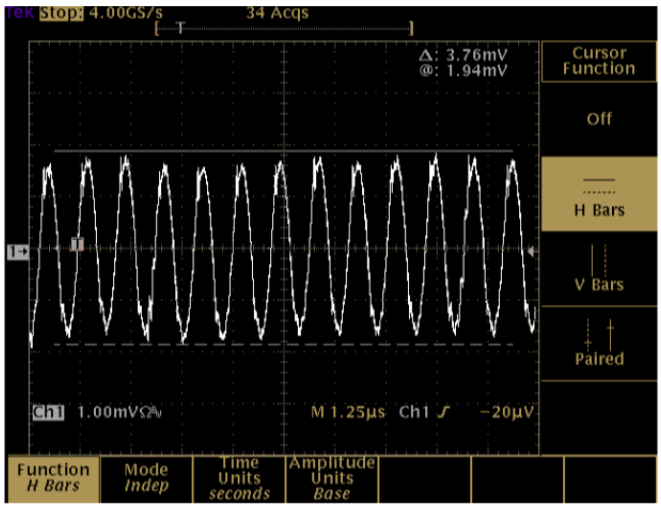

***Figure 23**: Ripple voltage before the filter*

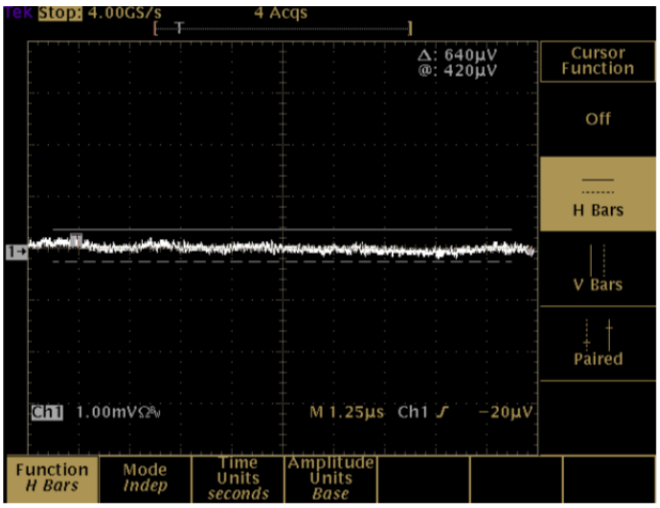

***Figure 24**: Ripple voltage after the filter*

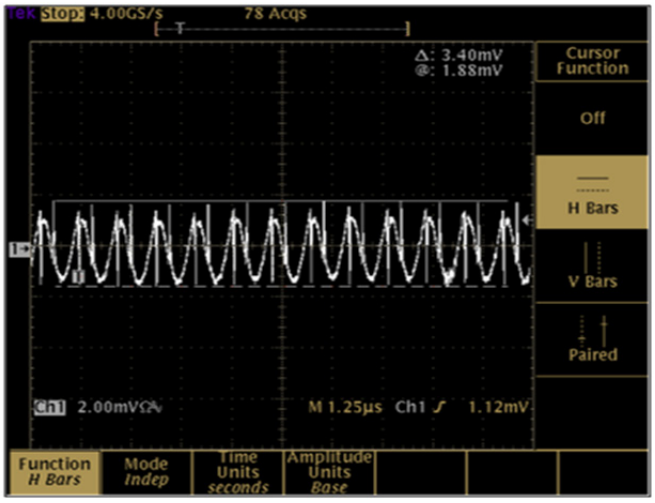

***Figure 25**: Ripple voltage before the filter*

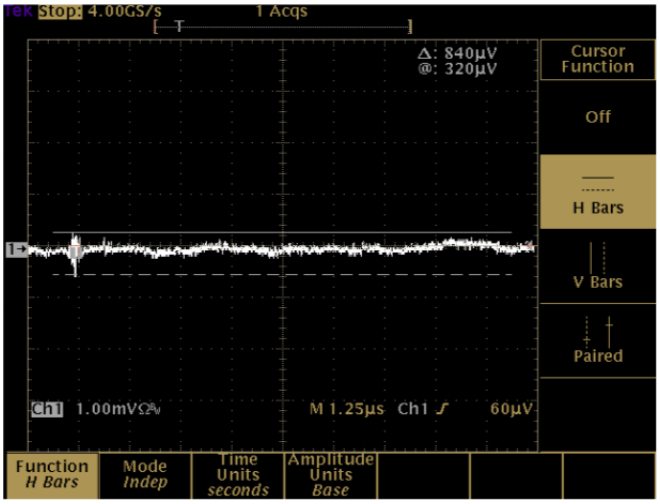

***Figure 26**: Ripple voltage after the filter*

Added Bulk Capacitors Removed

The bulk capacitor of 220 µF was removed, leaving just (1) 22 µF capacitors as the PDN. The filter components remain. The cross-over frequency of the regulator has been simulated with the first with the (1) 22 µF implemented. *Figure 27* shows the cross-over frequency with just 1 capacitor, the cross-over frequency is about 200 kHz which is well beyond the corner frequency of the filter even at full load current of 4 amperes. *Figure 28* shows the impedance profile with no load, converter off and with the sense lines located before the filter. This figure clearly shows the filter having and overall effect on the PDN. Figure 29 shows the same condition with the sense lines located after the filter.

Figures 30 and *31* show the impedance profile with the converter on but at no load conditions. *Figure 30* shows impedance profile with the sense line connected before the converter while *Figure 31* shows the impedance profile with the sense lines connected after the filter.

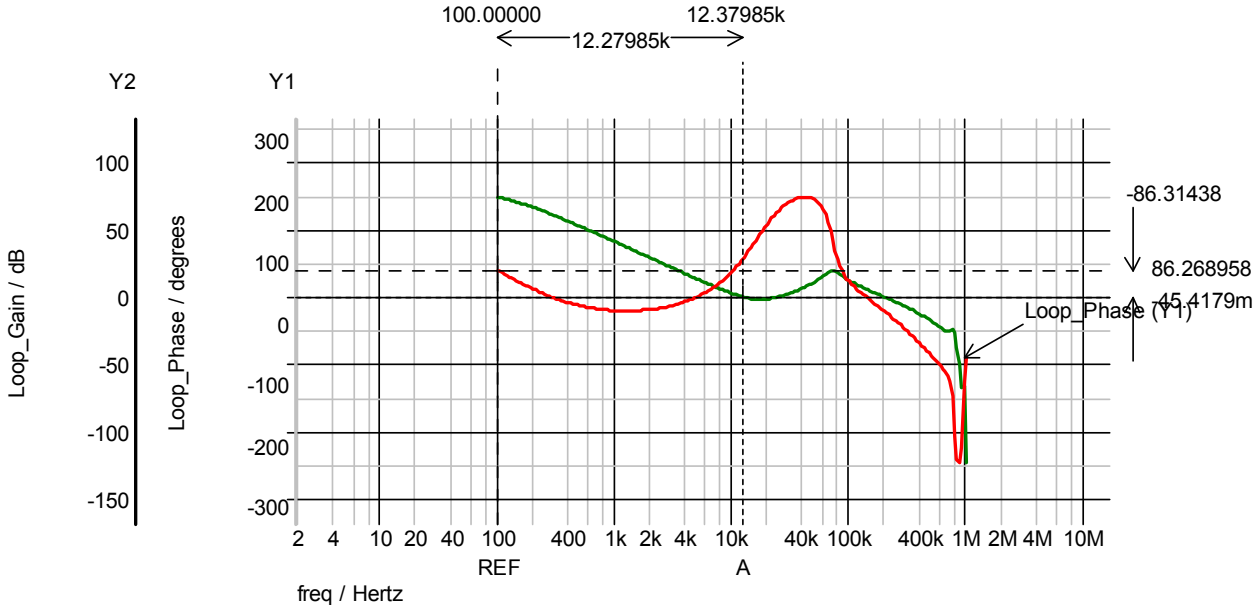

***Figure 27**: ISims simulation [38] with 22 µF of Capacitance for Bulk Capacitor*

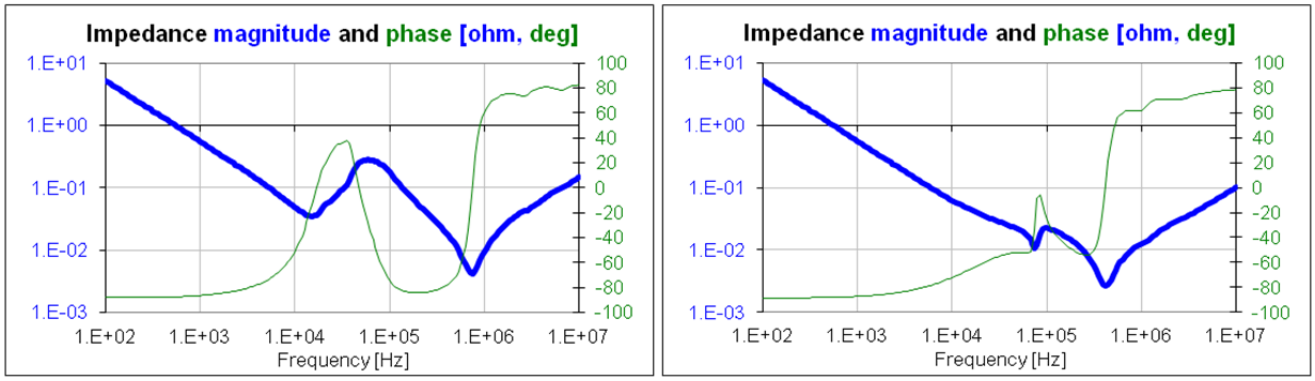

***Figure 28**: Impedance profile with converter OFF, sense lines before filter (on the left)*
***Figure 29**: Impedance profile with converter OFF, sense lines after filter (on the right)*

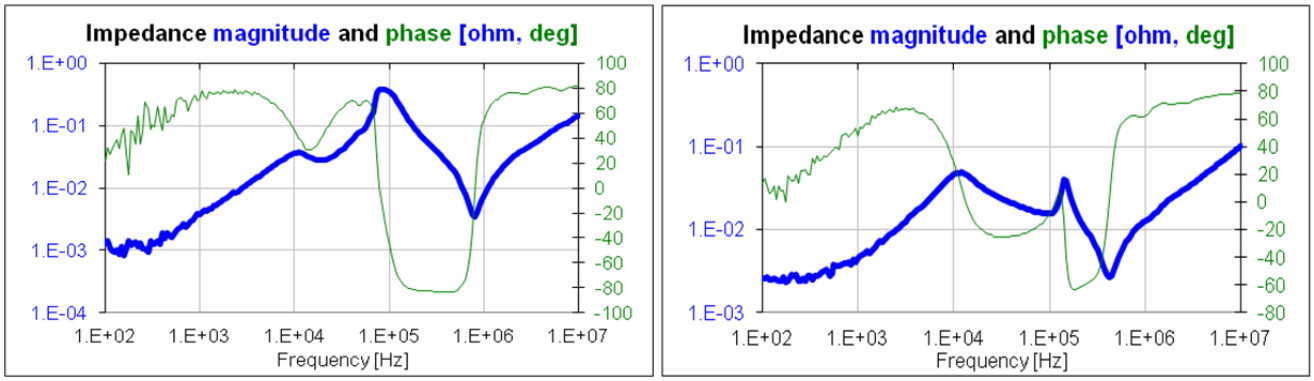

***Figure 30**: Impedance profile with converter ON, no load, sense lines before filter (on the left)*
***Figure 31**: Impedance profile with converter ON, no load, sense lines after filter (on the right)*

Figures 32 and *33* show the impedance profile with full load current of 4 amperes and with the sense lines located before and after the filter.

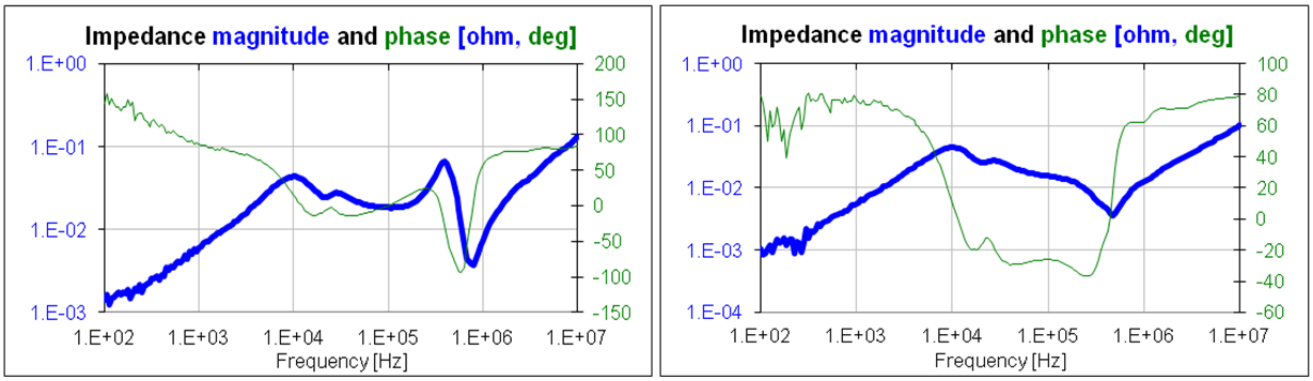

Figure 32*: Impedance profile full load current of 4 Amperes, sense lines before filter (on the left)*
Figure 33*: Impedance profile full load current of 4 Amperes, sense lines after filter (on the right)*

With no load conditions *Figure 34, 35* and *36* show the attenuation of the ripple voltage. *Figure 35* shows the ripple voltage with a sub-harmonic frequency indicating stability problems. *Figure 36* shows that the attenuation just meets the 1 mV requirement. The sense lines are connected after the filter in each case.

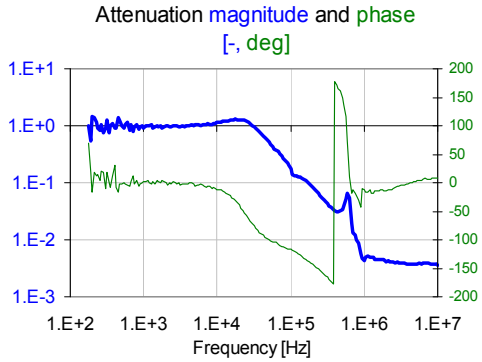

Figure34*: Attenuation profile with no load on the output, sense lines after filter*

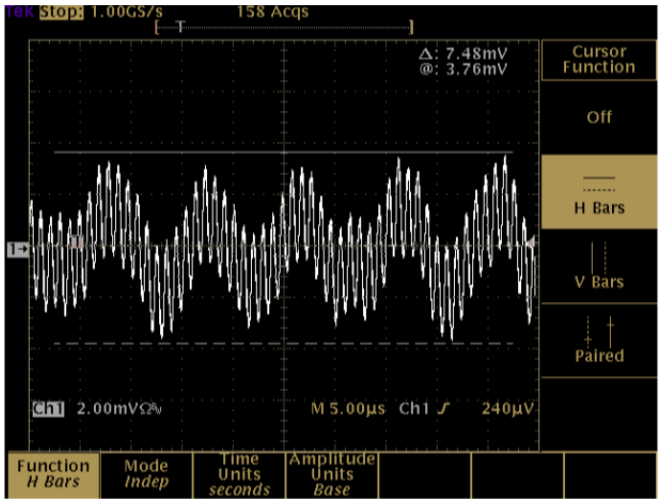

Figure 35*: Voltage ripple before filter*

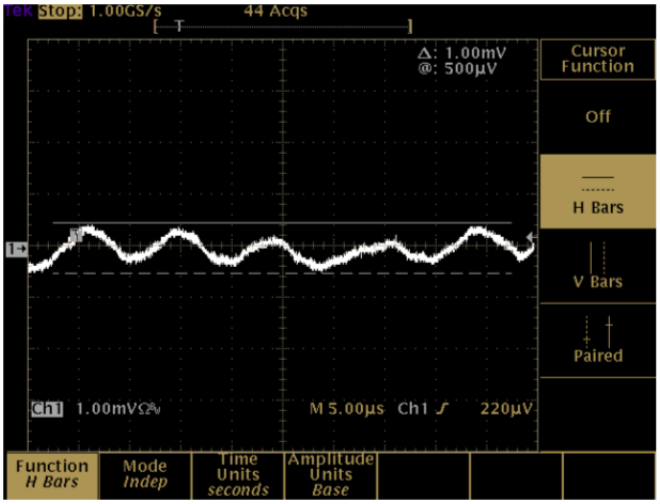

Figure 36*: Voltage ripple after filter*

Figure 35 shows a ripple voltage of 7.5 mV, and *Figure 36* shows the output ripple voltage after the filter of 1.0 mV. The sub harmonic frequency in *Figure 35* is about 20 KHz, approximately the corner frequency of the filter. Full load conditions of 4 amperes shown in *Figures 37, 38* and *39*, show similar results, but because the inductance of the filter is lower, the corner frequency has moved out toward 100 kHz.

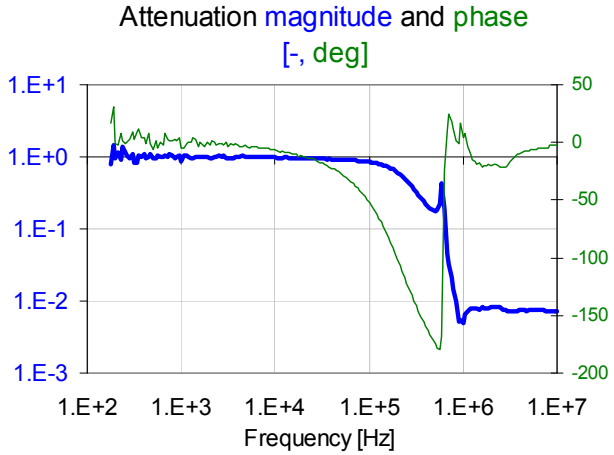

***Figure 37**: Attenuation with full load current, 4 Amperes, sense lines after filter*

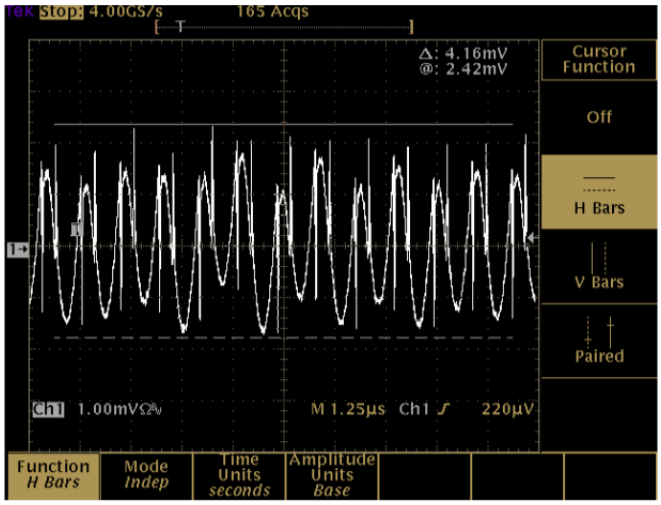

***Figure 38**: Voltage ripple before filter*

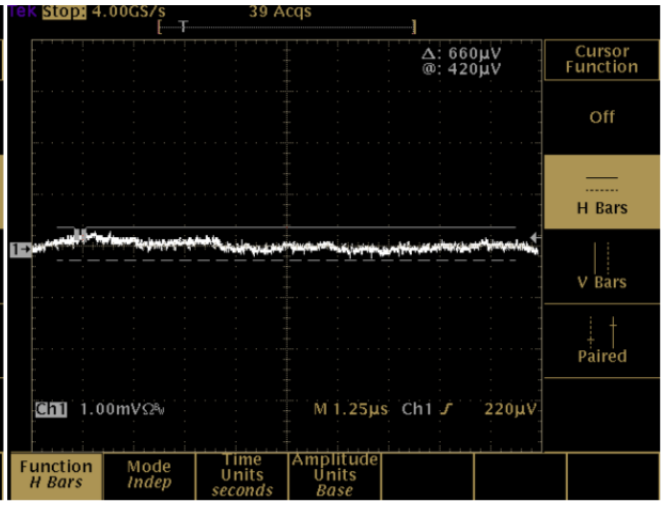

***Figure 39**: Voltage ripple after filter*

Figures 38 and *39* still show some instability of the regulator although to a lesser degree. The magnitude of the voltage ripple before the filter has dropped to just over 4 mV and the output ripple has been reduced to 640 µV.

Summary

The usage of power filters for the purpose of attenuation of ripple voltages to a level of 1 mV or less can be accomplished by matching the filter to the power supply. With a proper PDN employed at the converter level, and with matched filter design, it has been demonstrated that the behavior of the regulator remains stable. It has also been shown, that inductor used needs to be characterized or have a knowledge of its operation with a load bias current is very important. Placing of sense lines of the converter after the filter may cause unstable operation of the converter itself, particularly at no load conditions.

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