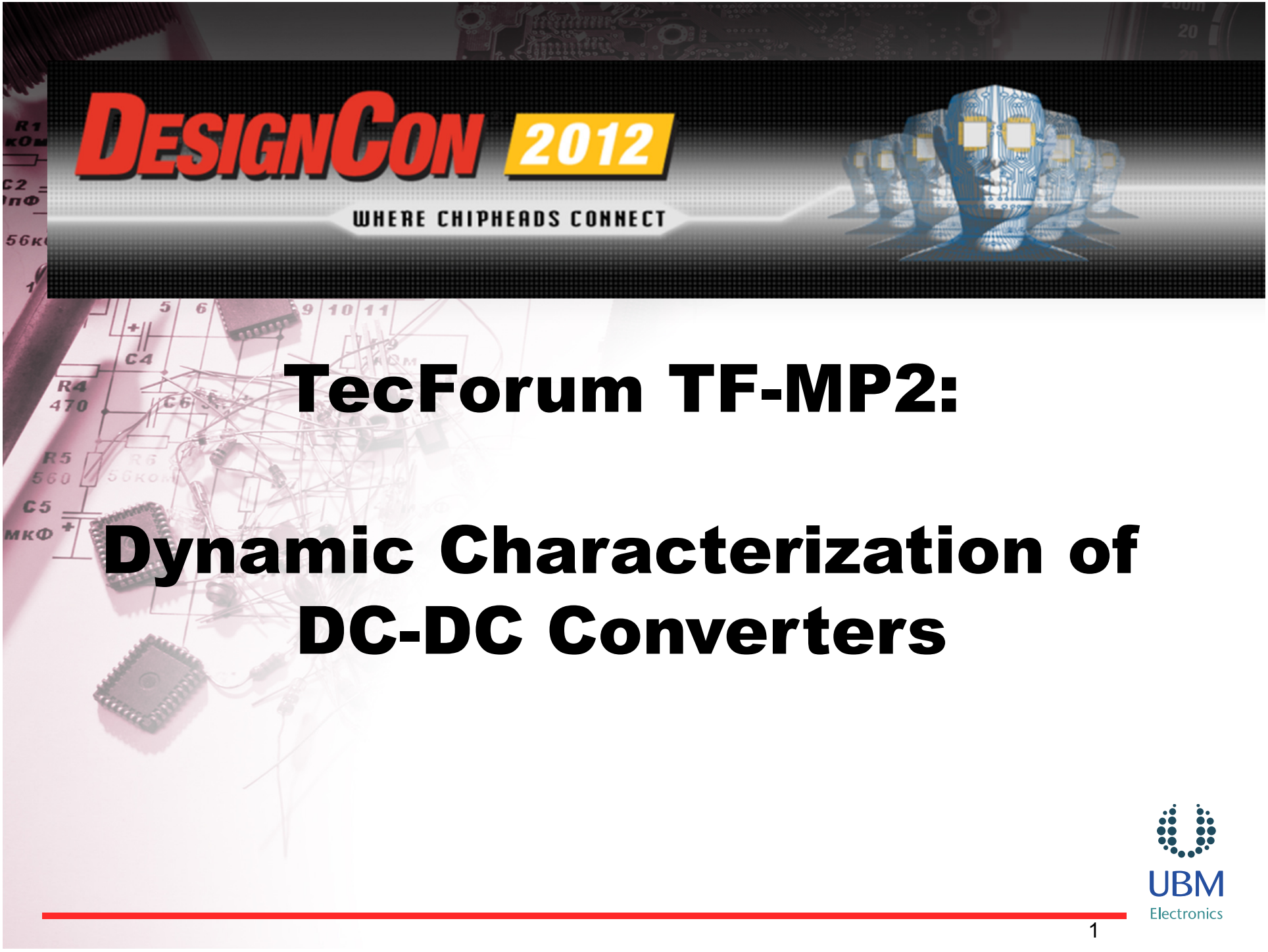

TecForum TF-MP2:

Dynamic Characterization of DC-DC Converters

UBM Electronics

Disclaimer:

This presentation does not constitute as an endorsement for any specific product, service, company, or solution.

Part I: Dynamic Characterization of DC-DC Converters from a System's Perspective

Istvan Novak, Oracle-America Inc.

Kendrick Barry Williams, Oracle-America Inc.

Chris Young, Intersil Corporation

Brandon Howell, Intersil Corporation

Jason R. Miller, Oracle-America Inc.

Gustavo Blando, Oracle-America Inc.

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Part II: Power Filter Network and its Effect on DC-DC Converters

Kendrick Barry Williams, Oracle-America Inc.

Istvan Novak, Oracle-America Inc.

Brandon Howell, Intersil Corporation

Chris Young, Intersil Corporation

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Outline

Part I: Dynamic Characterization of DC-DC Converters from a System's Perspective

- **I. Introduction and background**
  - Dynamic specification items
  - Output filter
  - Modulator
  - Error amplifier and Loop compensation
- **II. Dynamic parameters of DC-DC converters from a system's perspective**

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Outline (continued):

- **III. Output impedance of DC-DC converters**
  - How source impedance influences output impedance
  - Multiple Converters in Parallel
  - Observations and Assumptions
  - Digital Control
- **IV. Measurements, Modeling, Simulations**
  - Measurements
  - Modeling, simulations
- **Conclusions**

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Outline

Part II: Power Filter Network and its Effect on DC-DC Converters

- **I. Introduction and Background Information**
  - DC Converters Introduction
  - Power Filter Introduction
  - DC Converter Specifications
  - Filter Specifications
  - The DC Converter Application
  - Cross-Over Frequency

Outline (continued)

- Power Filter Application
- Filter input impedance, converter looking toward the load
- Filter input impedance, the load looking toward the converter
- Filter Inductor

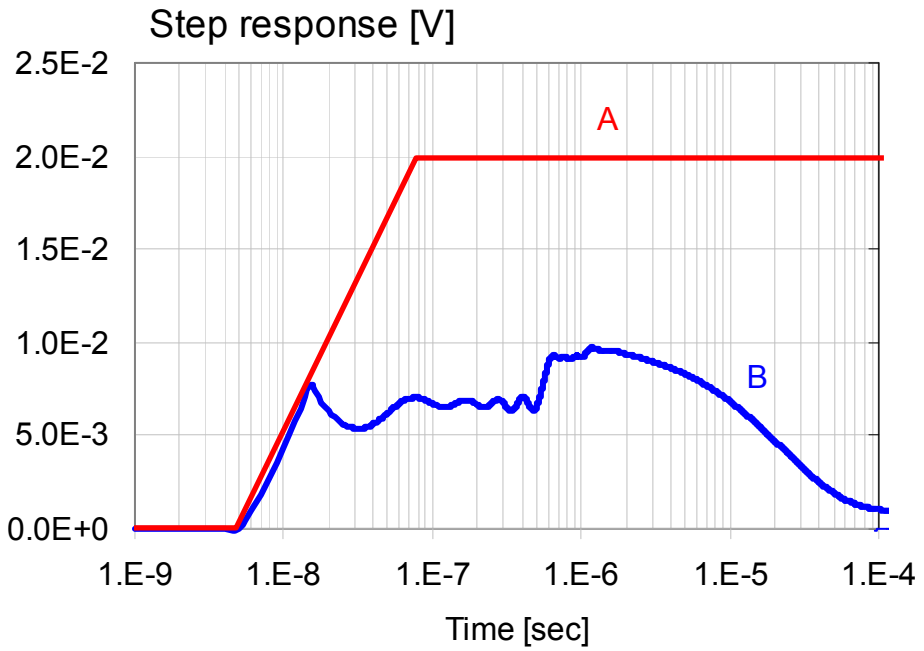
- **II. Actual Circuit Used and Measurements**
  - Added Bulk Capacitors Removed
- **Summary**

Motivation

- Number of DC-DC converters is on the rise
- Dynamic noise allowance keeps shrinking
- Recent converter trends offer new solutions

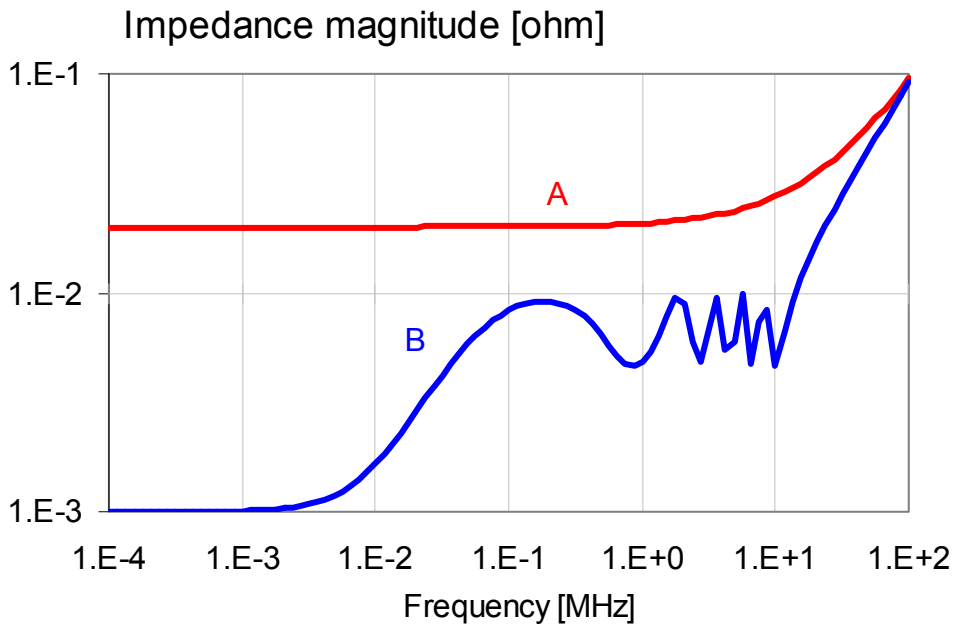
Quiz Question 1

- **Which step response will guarantee smaller worst-case noise A or B?**



Quiz Question 2

- **Which impedance profile will guarantee smaller worst-case noise, A or B?**



Quiz Question 3

- **In what frequency range will the converter loop influence transient response and output impedance?**
  - Up to 10x the cross-over frequency
  - Not above the cross-over frequency
  - Up to 2x the cross-over frequency

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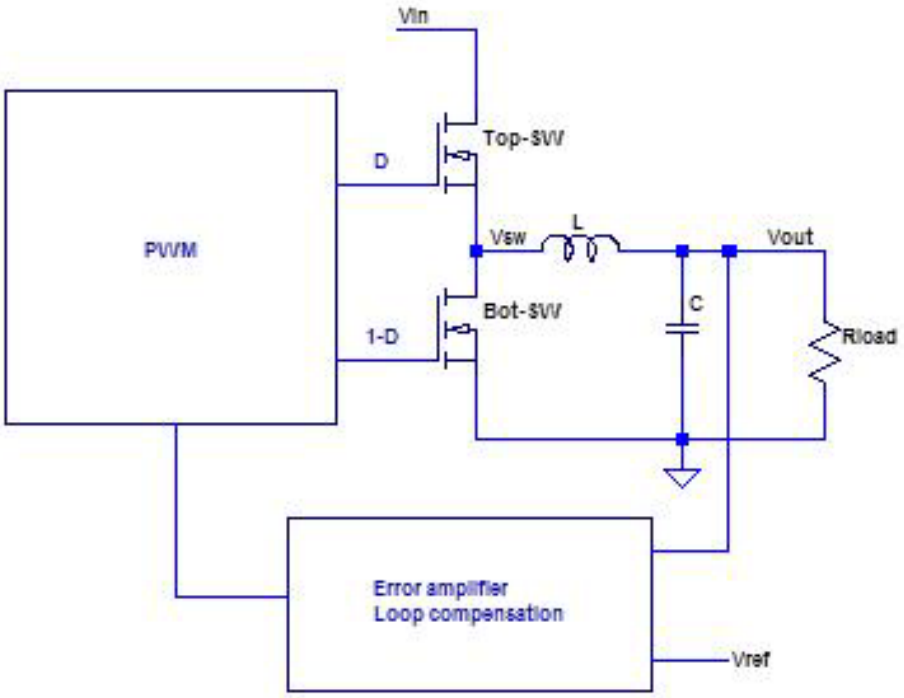
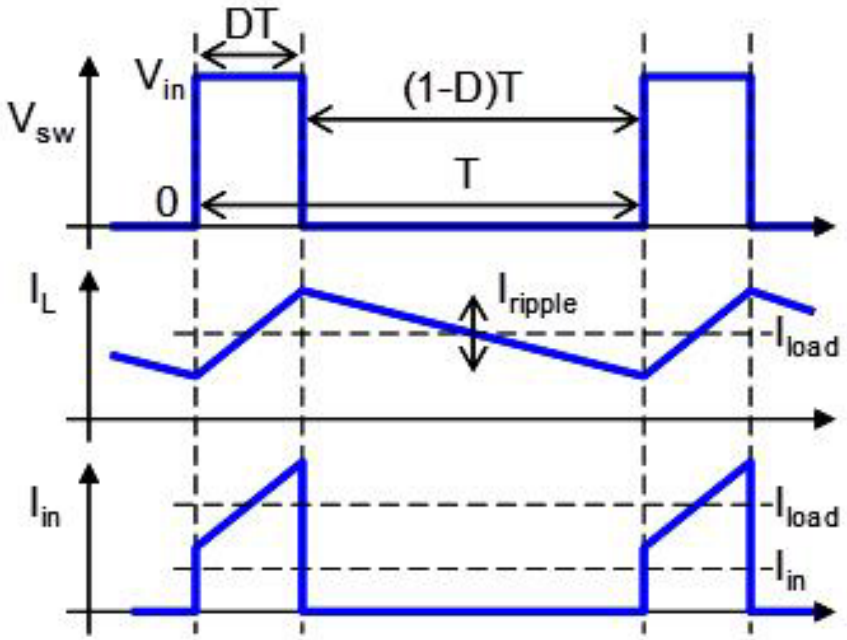
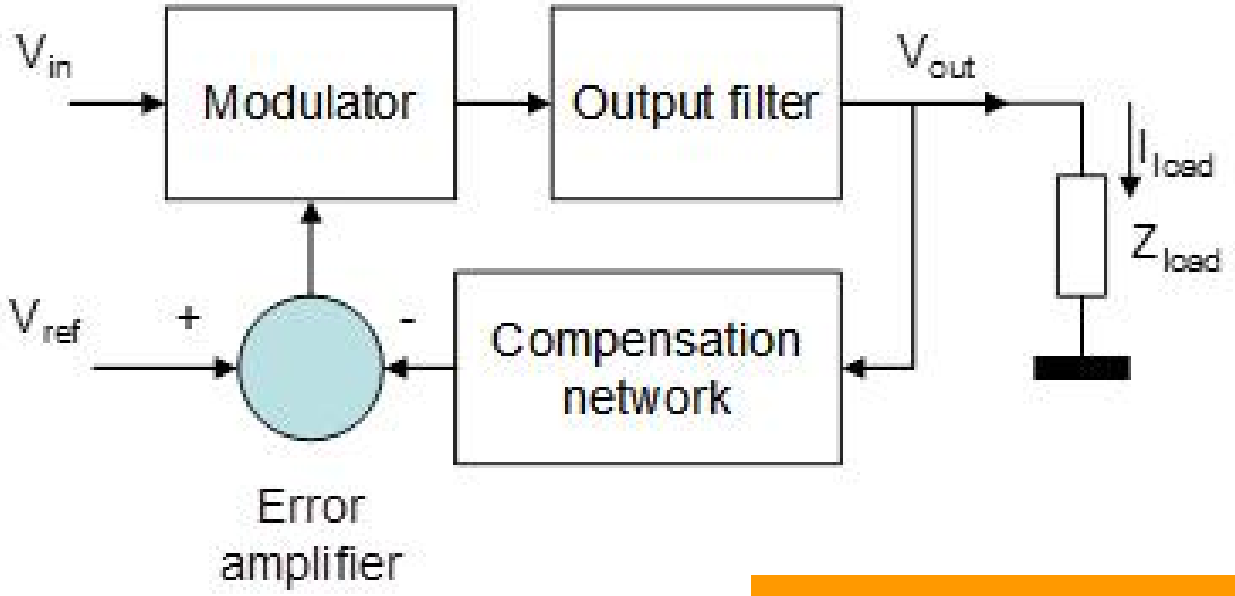
Non-isolated Buck Converter





$$V_{out} = D\,V_{in}$$

The Feedback Loop

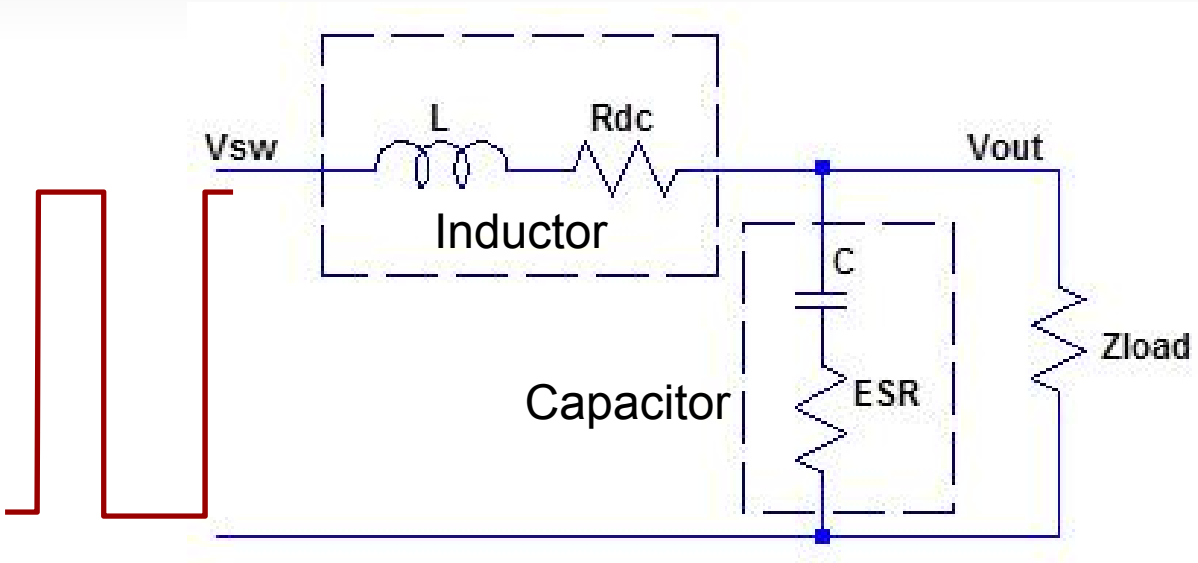


$$G_{loop} = G_M G_F G_C G_{EA}$$

Dynamic Parameters

- Loop stability is the most important
- Load response or output impedance
- Line response, input impedance
- Output ripple, ringing noise

Output Filter in Voltage-Mode Control



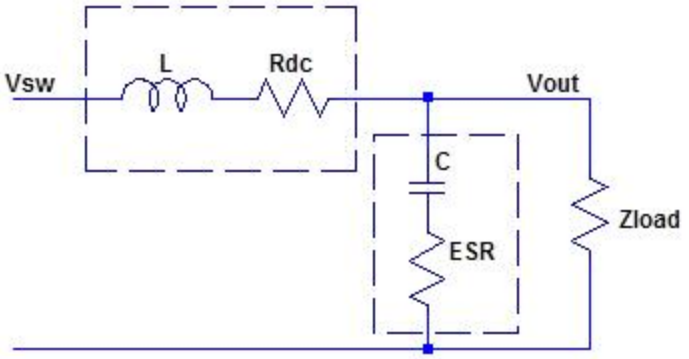
$$G_F = \frac{Z_{Load} \parallel Z_C}{Z_L + Z_{Load} \parallel Z_C}$$

G_F Transfer Function

Assume infinite load impedance

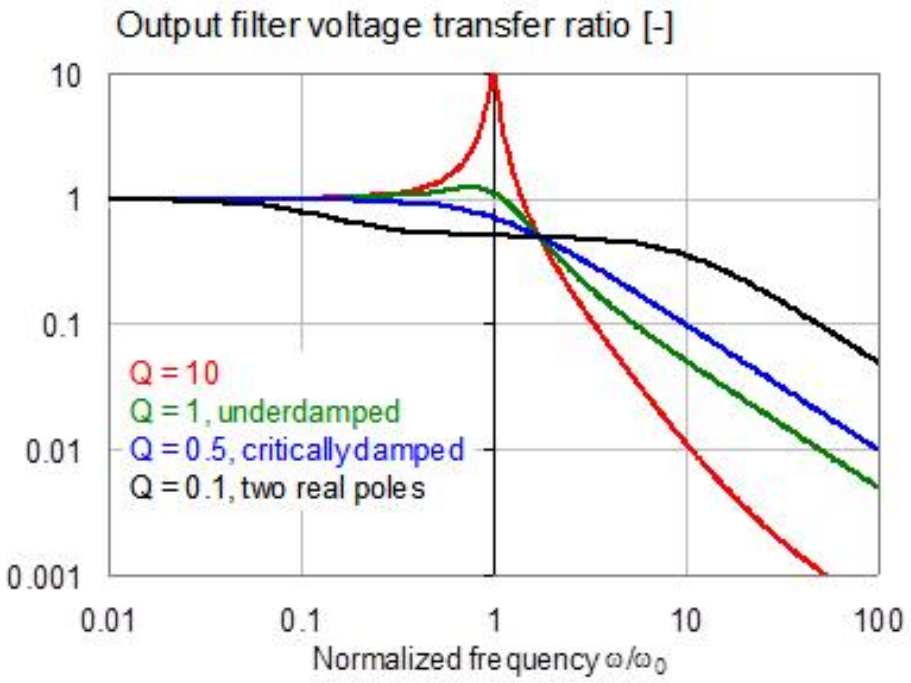
$$G_F = \frac{1 + j\omega ESR\,C}{1 + j\omega(R_{dc} + ESR)C - \omega^2 LC} = \frac{1 + j\omega ESR\,C}{1 + jQ^{-1}\frac{\omega}{\omega_0} - \left(\frac{\omega}{\omega_0}\right)^2}$$

$$Q = \frac{\sqrt{L/C}}{R_{dc} + ESR} \qquad \omega_0 = \frac{1}{\sqrt{LC}}$$

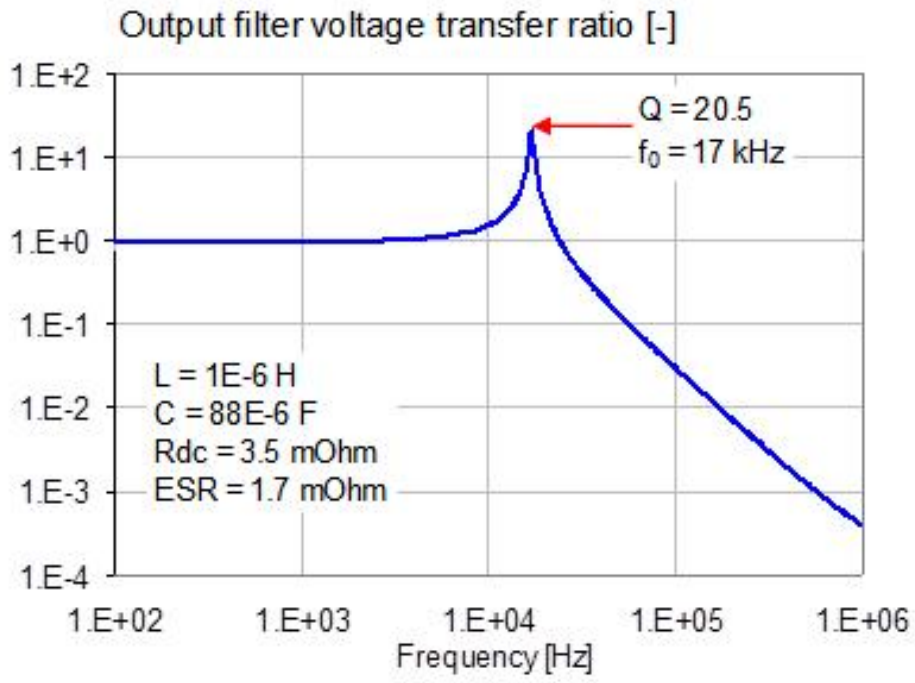


G_F Transfer Function

Normalized view:

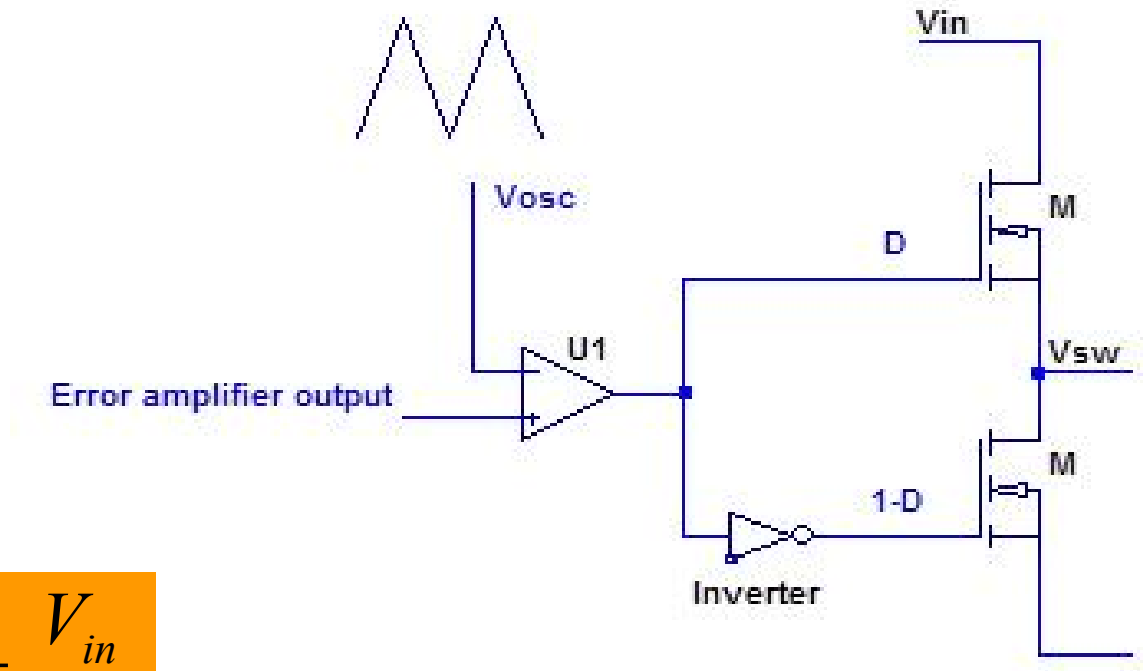


A typical plot:



Assume infinite load impedance

Modulator

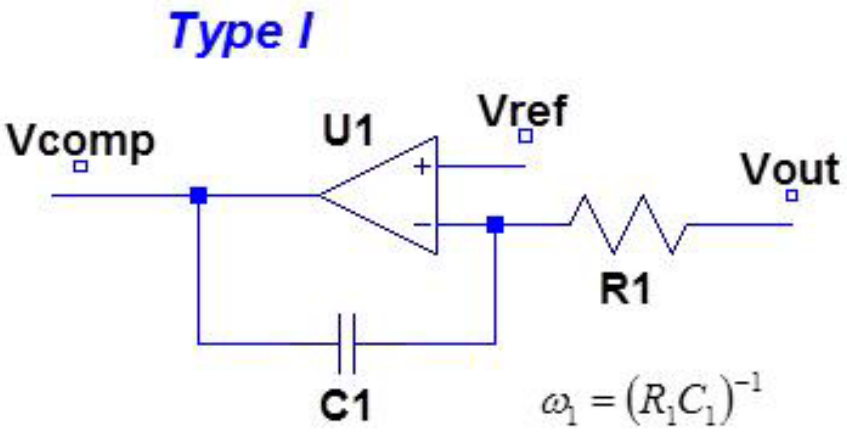


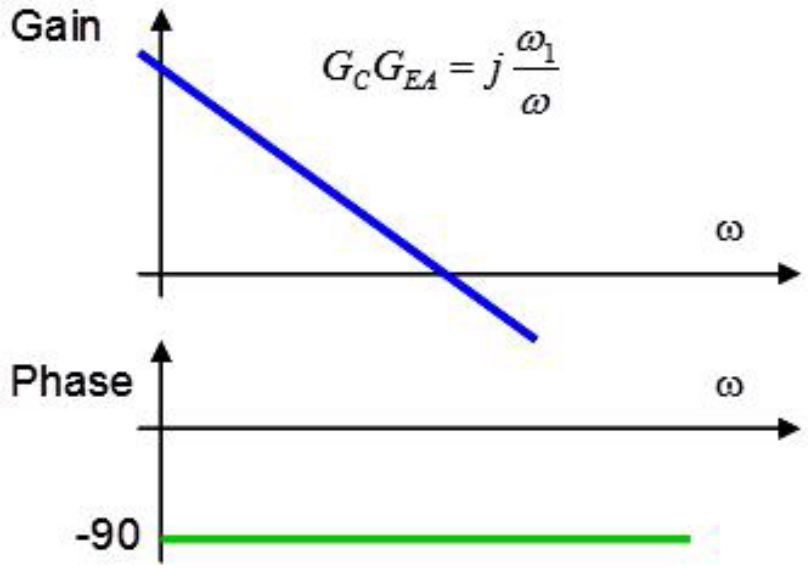
$$G_M = \frac{V_{in}}{V_{osc}}$$

Error Amplifier and Loop Compensation

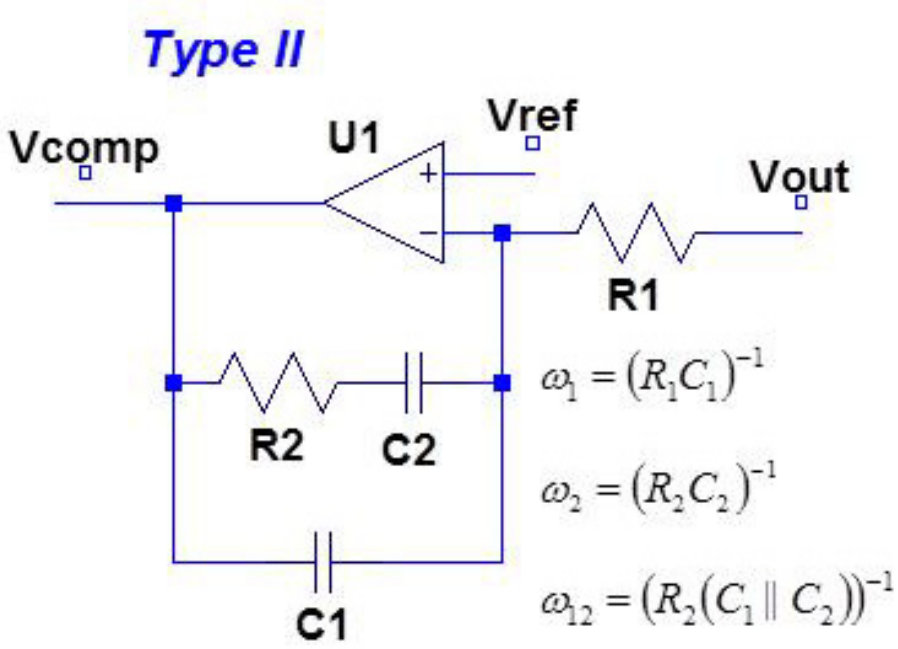
- **PID (P**roportional**-I**ntegral**-D**erivative**)**
- **Type I (Integral)**
- **Type II (Integral-Proportional)**
- **Type III (Integral-Proportional-Derivative)**

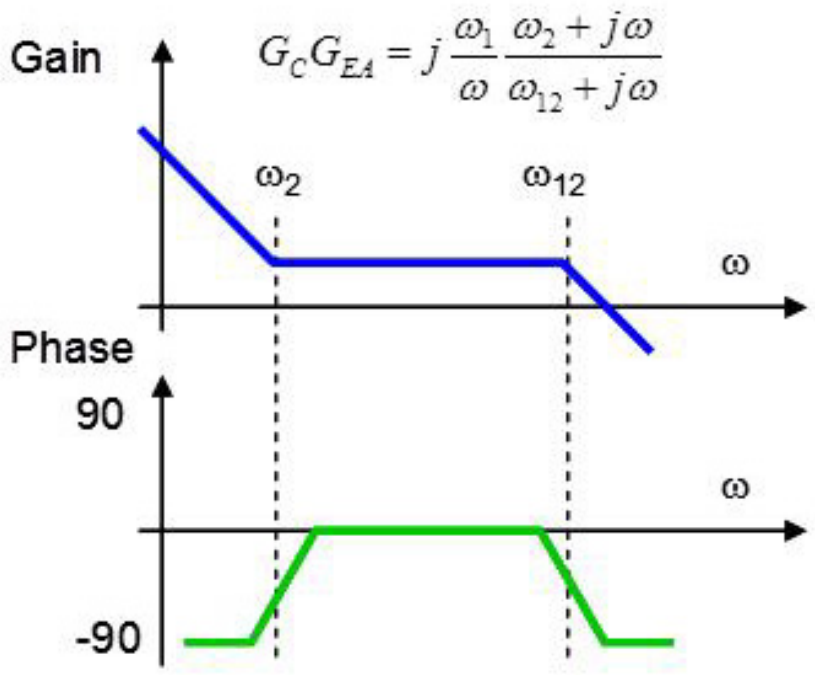
Type I Compensation



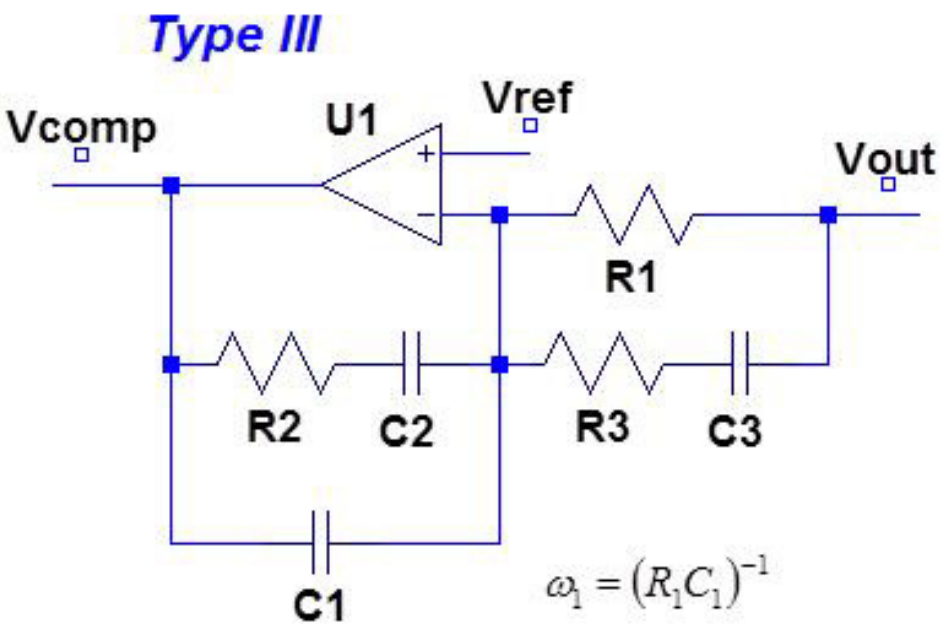


Type II Compensation





Type III Compensation

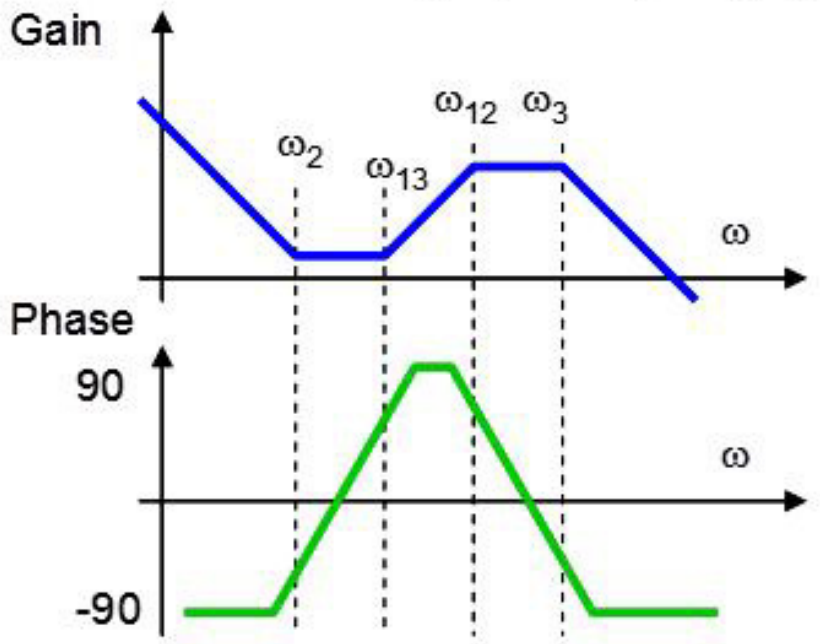


$$\omega_1 = (R_1 C_1)^{-1}$$

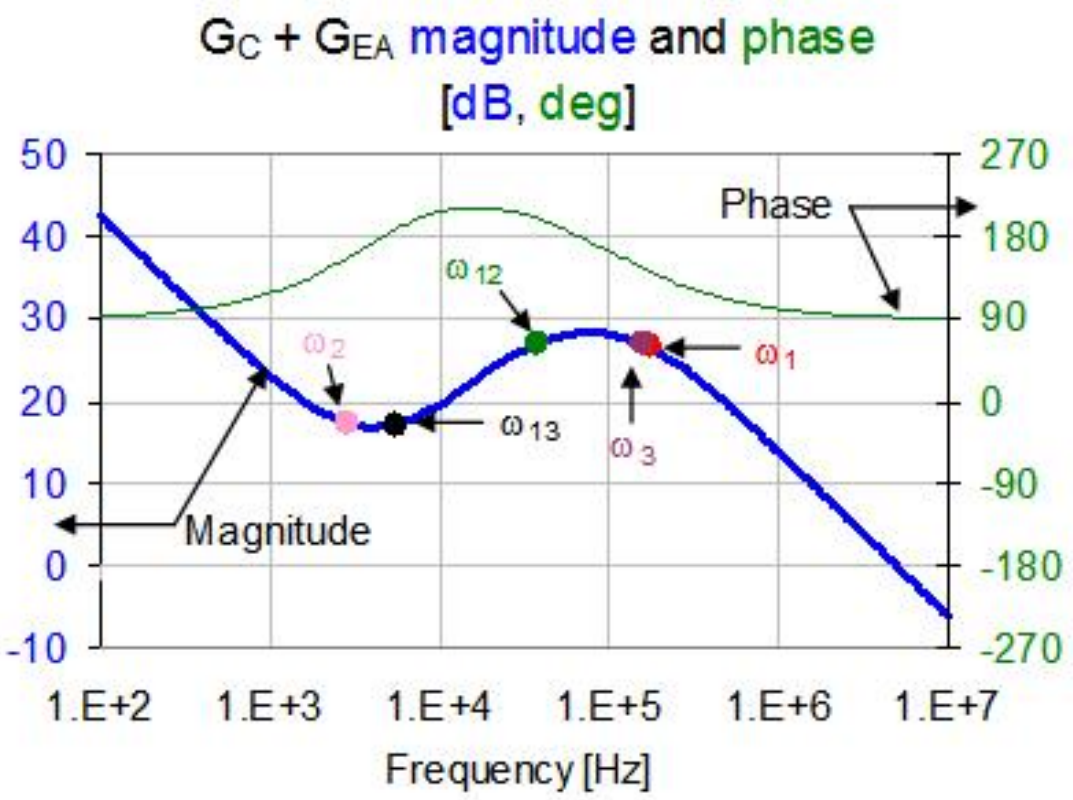
$$\omega_{12} = (R_2 (C_1 \parallel C_2))^{-1} \qquad \omega_2 = (R_2 C_2)^{-1}$$

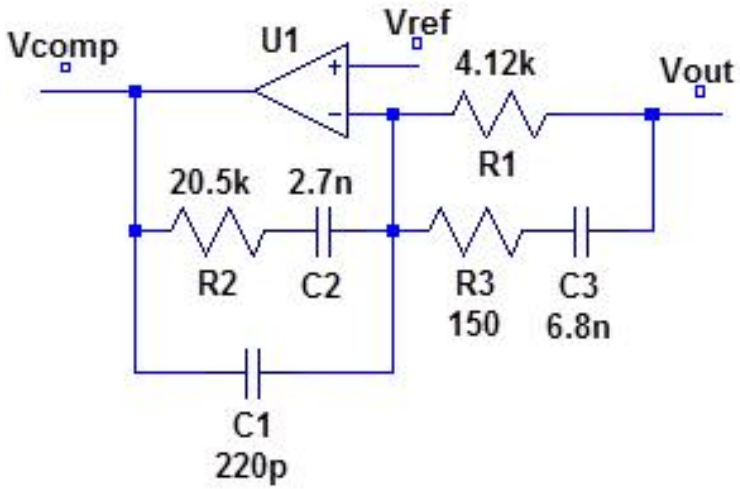
$$\omega_{13} = (C_3 (R_1 + R_3))^{-1} \qquad \omega_3 = (R_3 C_3)^{-1}$$

$$G_C G_{EA} = j \frac{\omega_1}{\omega} \frac{\omega_2 + j\omega}{\omega_{12} + j\omega} \frac{R_1 + R_3}{R_3} \frac{\omega_{13} + j\omega}{\omega_3 + j\omega}$$

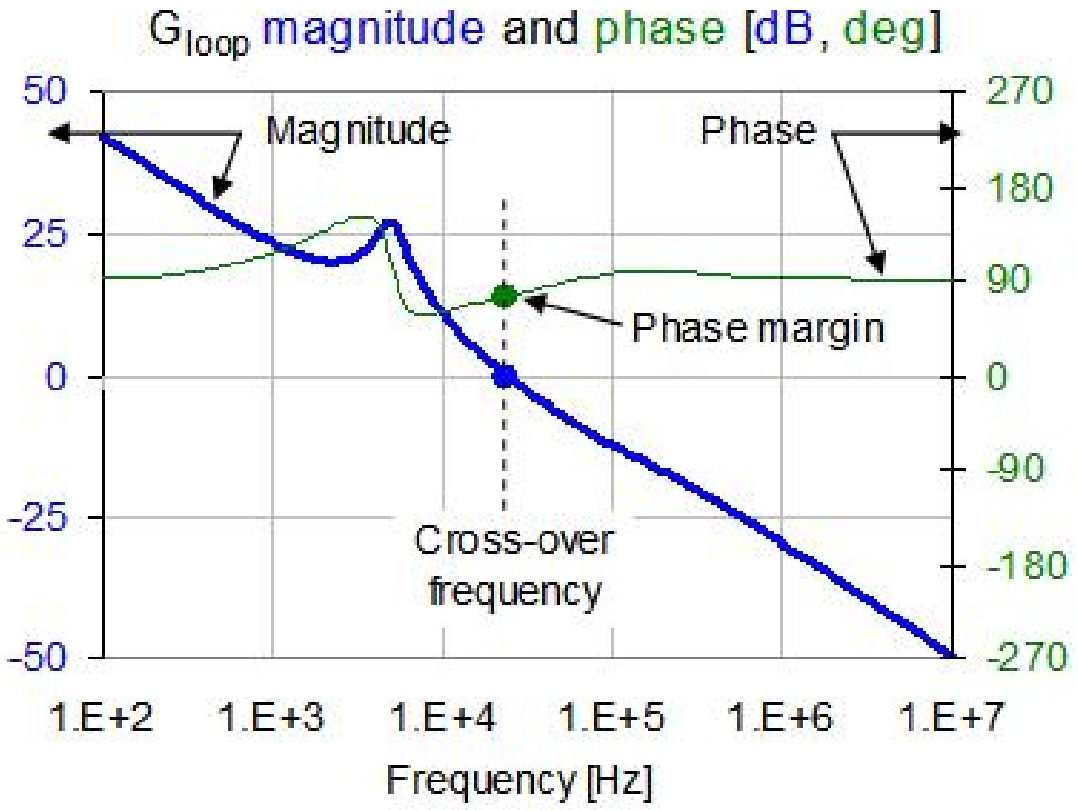


A Type III Implementation





Putting the Loop Together

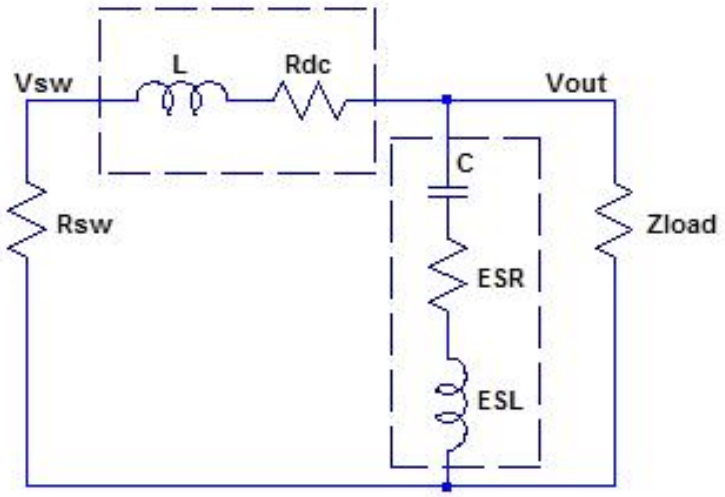


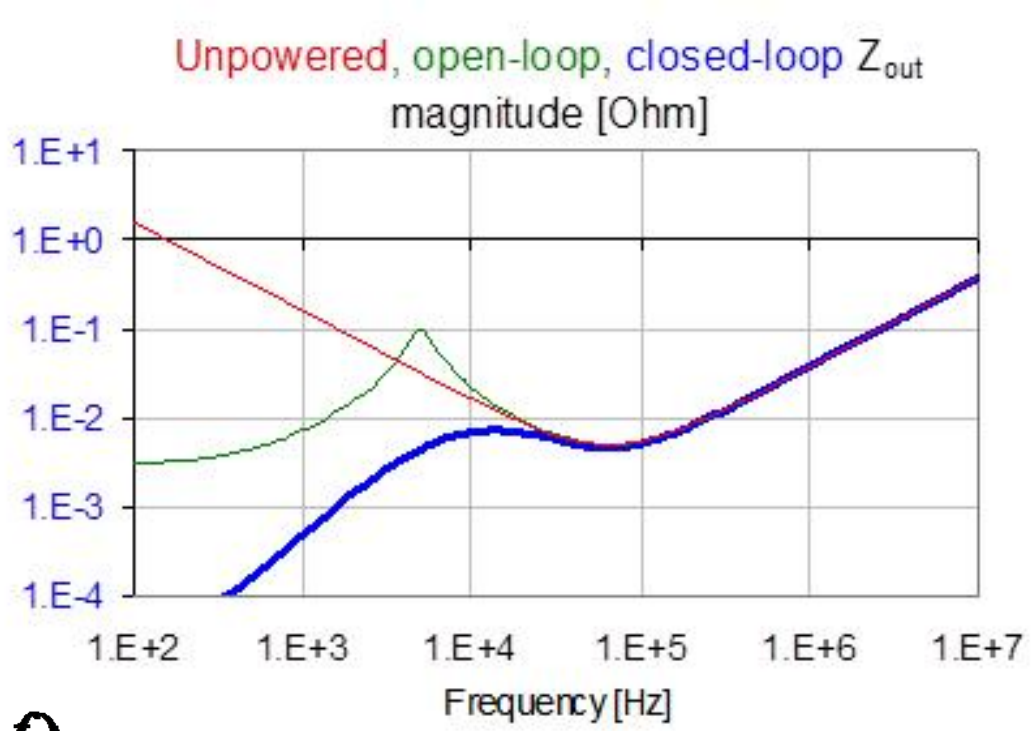
A typical loop gain plot for voltage-mode control with Type III compensation.

Important parameters:

- Cross-over frequency
- Phase margin
- Gain margin

Closed-Loop Output Impedance





$$Z_{out-closed-loop}(f) = \frac{Z_{out-open-loop}(f)}{1 + G_{loop}(f)}$$

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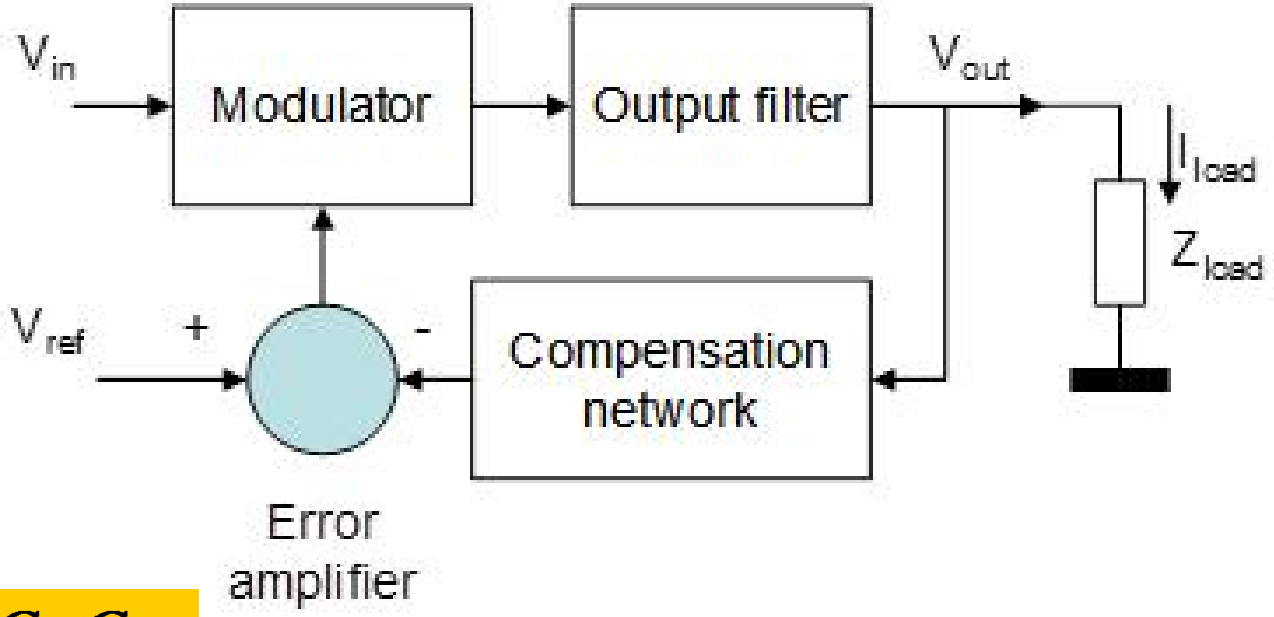
Line Regulation



$$\frac{V_{out}}{V_{in}} = \frac{G_M G_F}{1 + G_{loop}}$$

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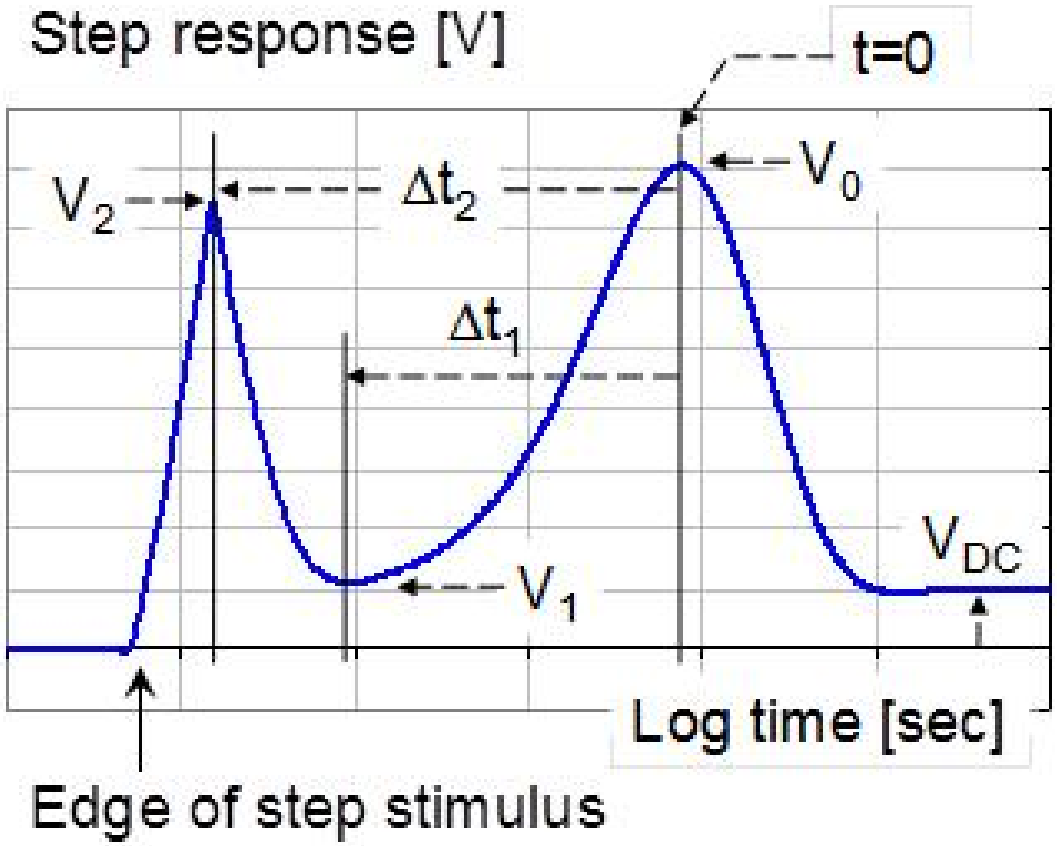
The Reverse Pulse Technique

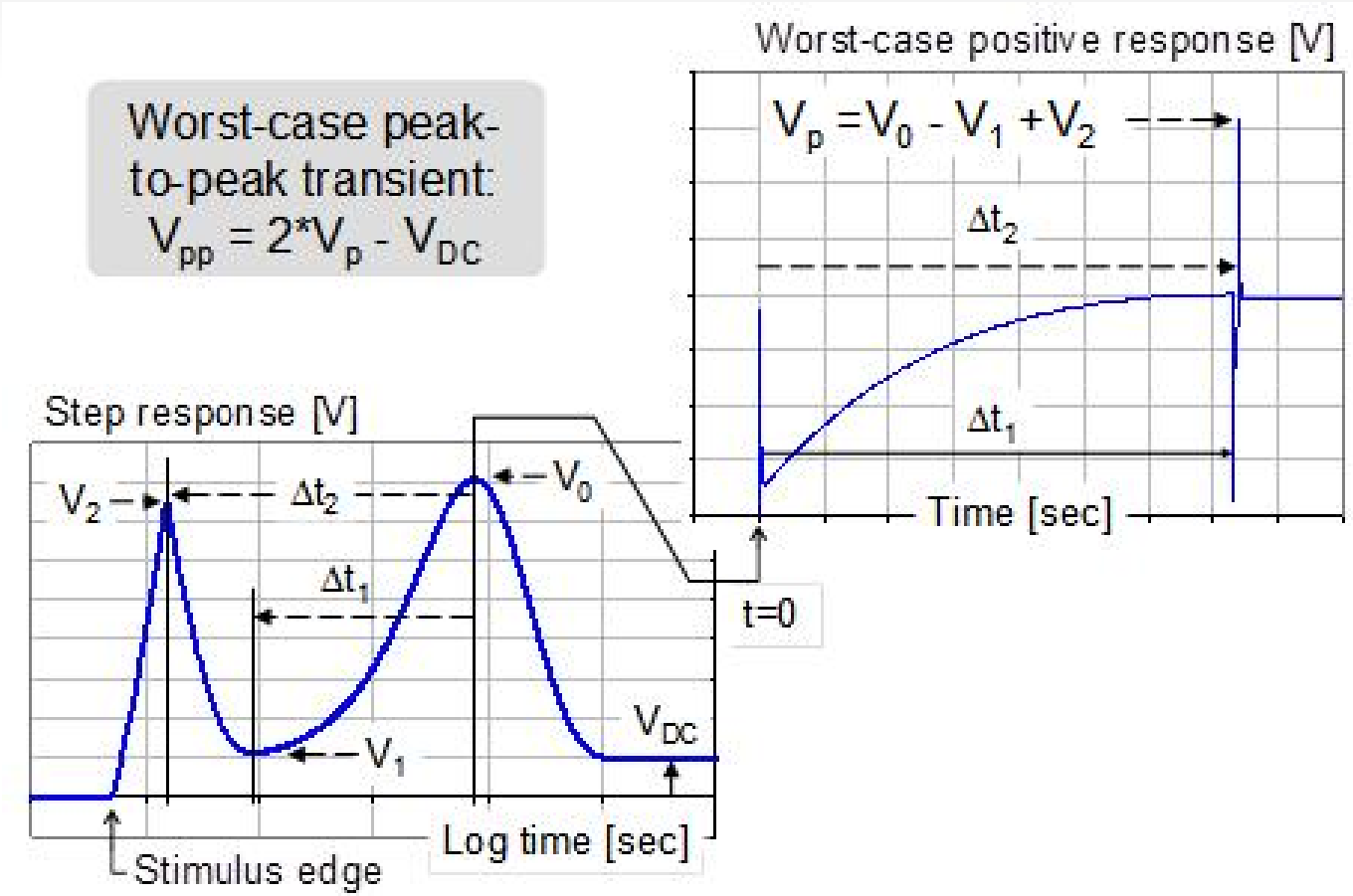


Assumptions:

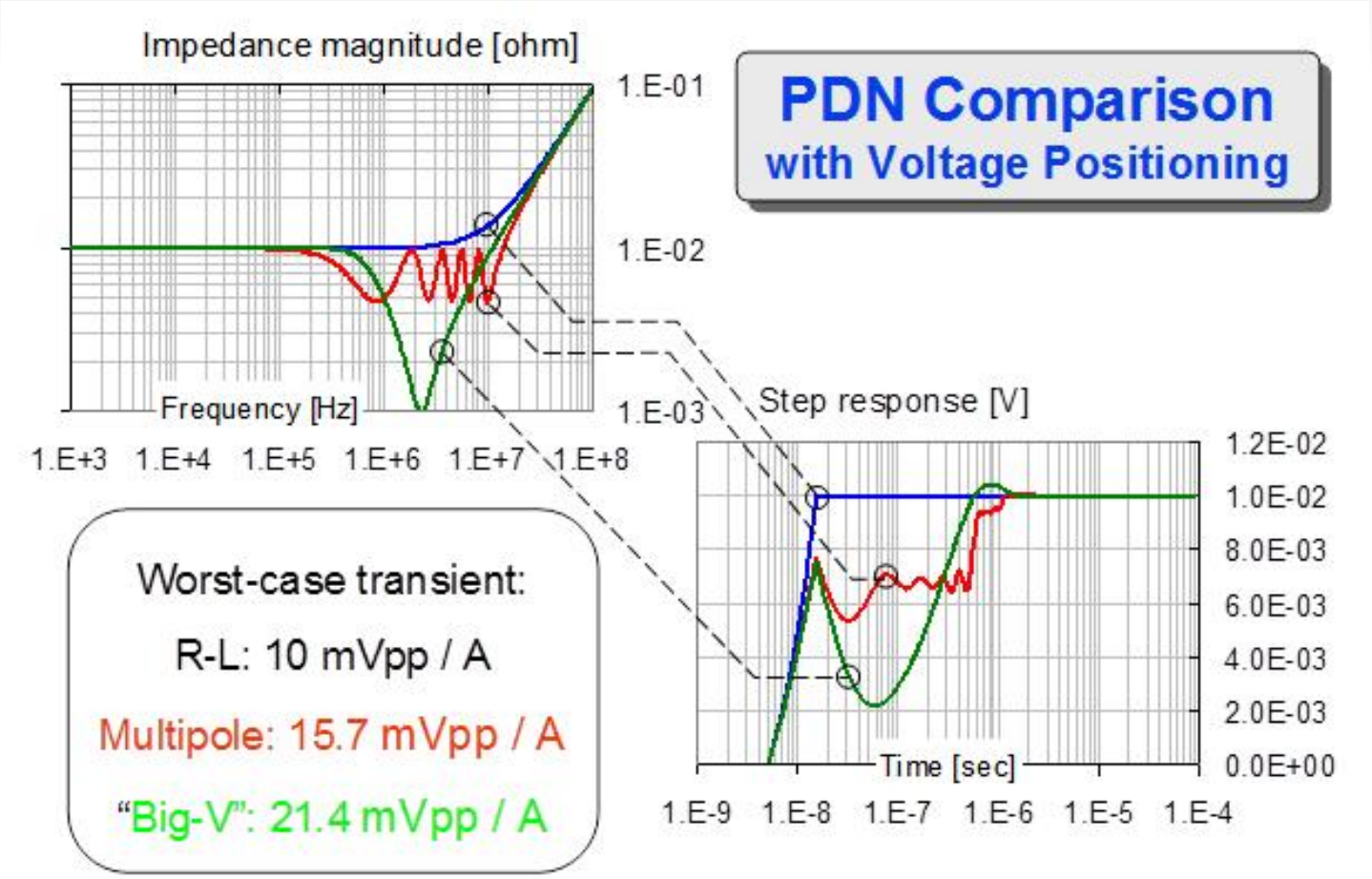
- PDN is LTI
- Random current steps
- Bounded step size
- Bounded step speed

The Reverse Pulse Technique

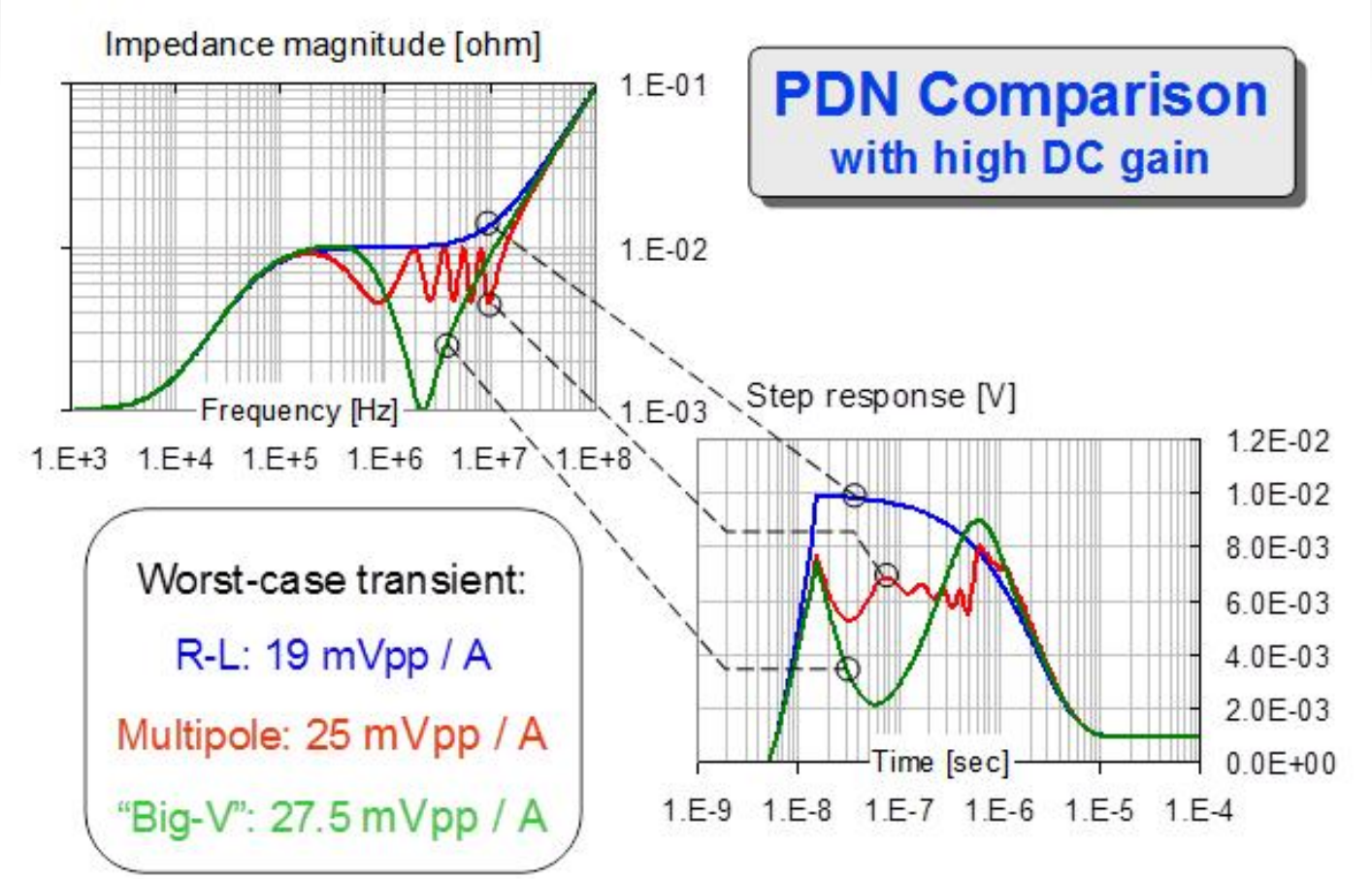
Worst-case peak-to-peak transient:
$V_{pp} = 2*V_p - V_{DC}$



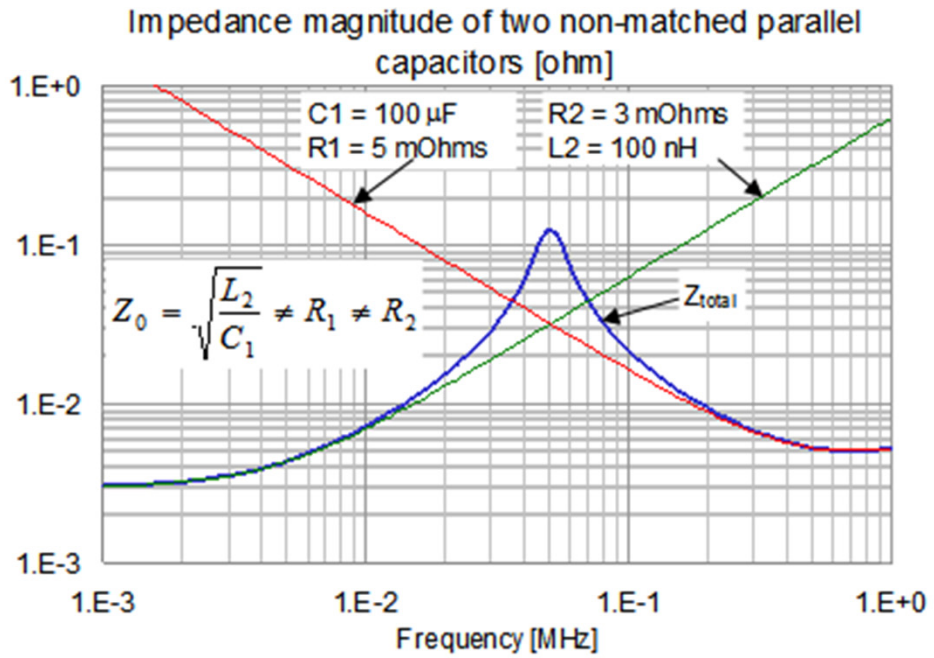
Noise vs. Impedance Profile

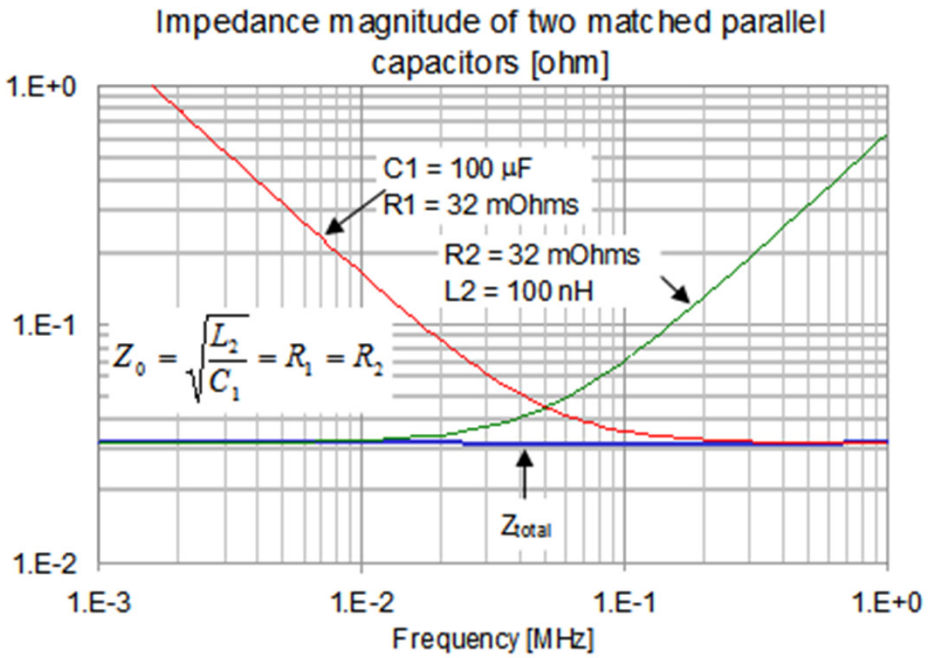


Noise vs. Impedance Profile



Impedance Matching in PDN





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Outline (continued):

- **III. Output impedance of DC-DC converters**
  - How source impedance influences output impedance
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  - Measurements
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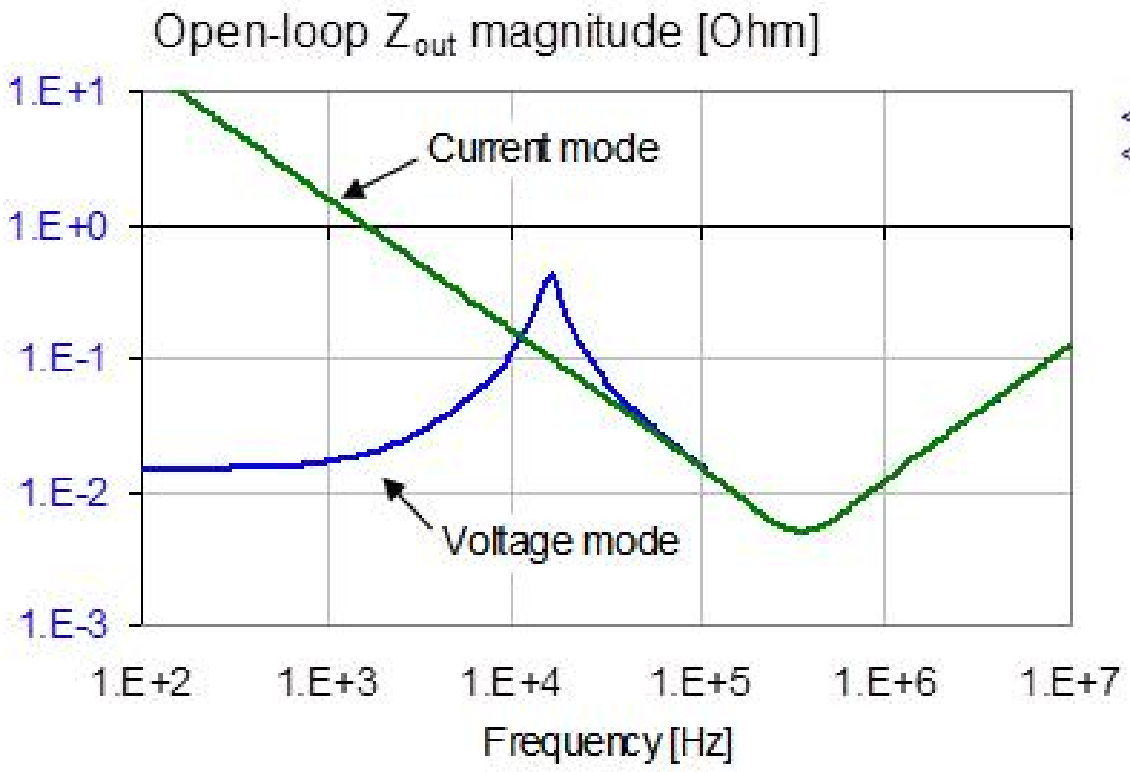
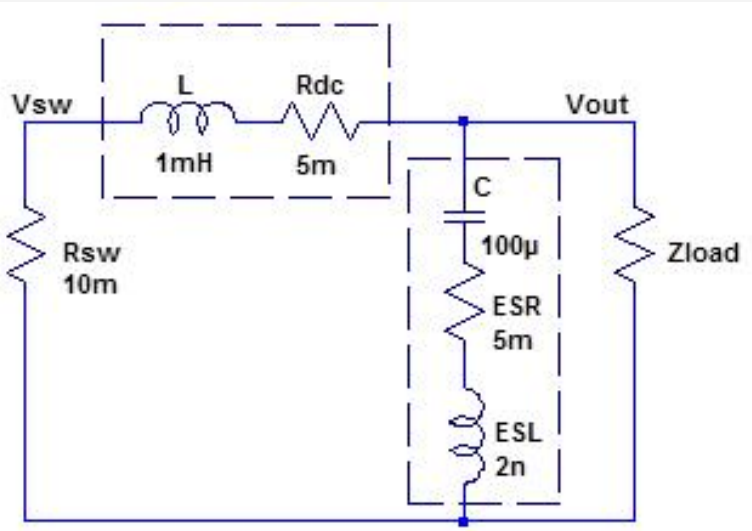
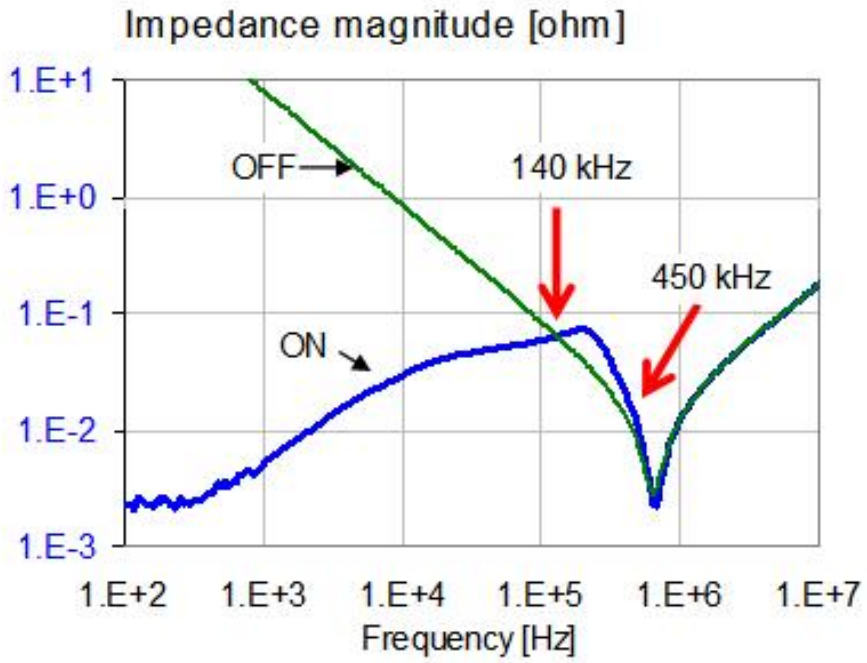
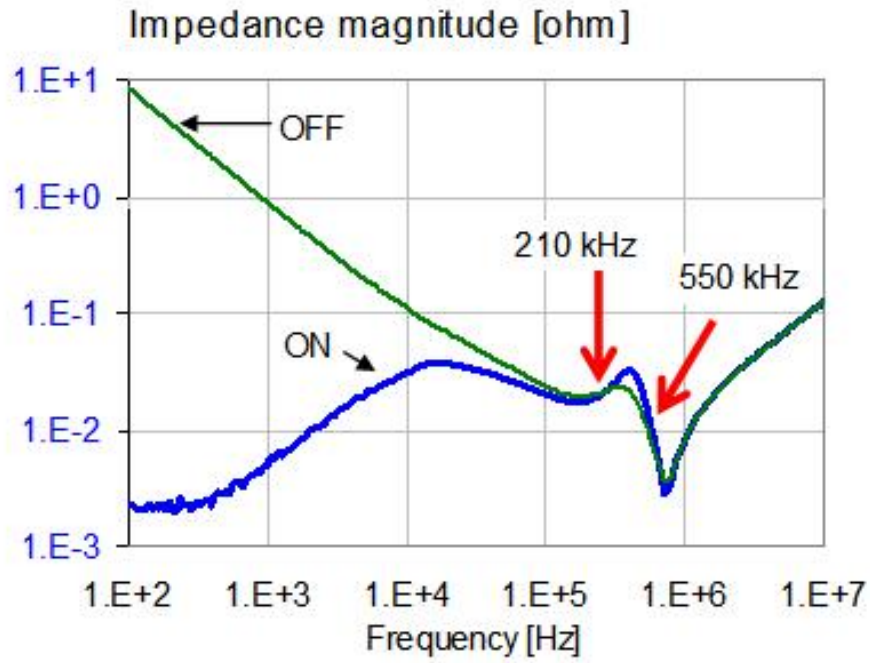
Open-Loop Output Impedance





Closed-Loop Output Impedance





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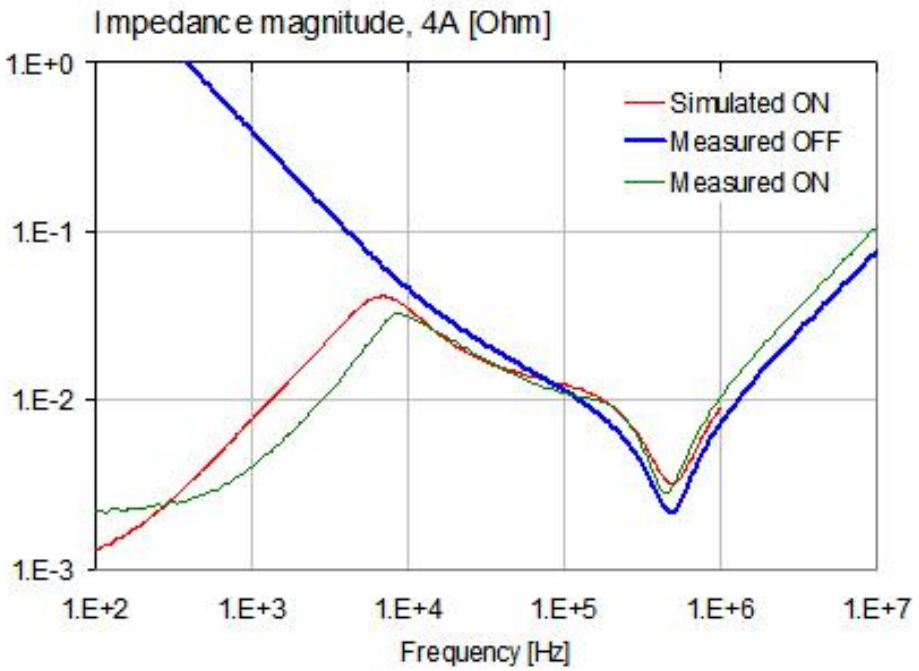
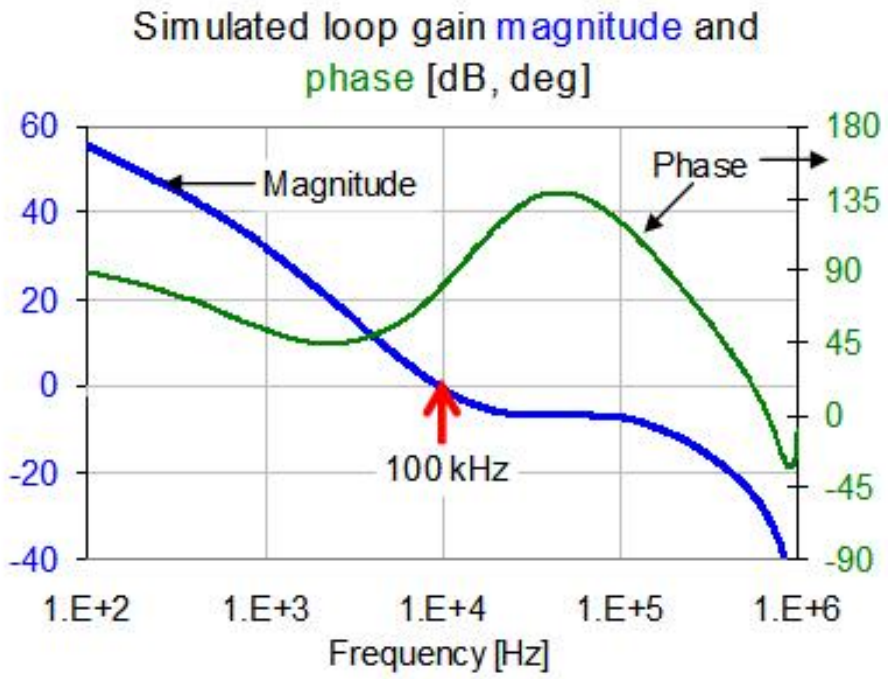
Closed-Loop Output Impedance vs. Crossover Frequency





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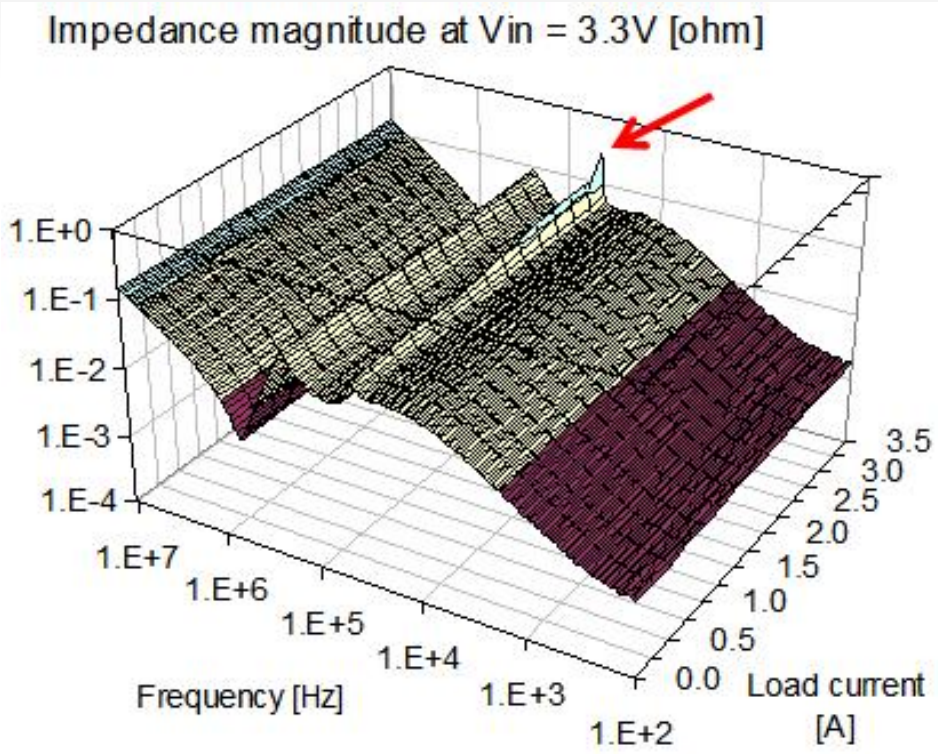
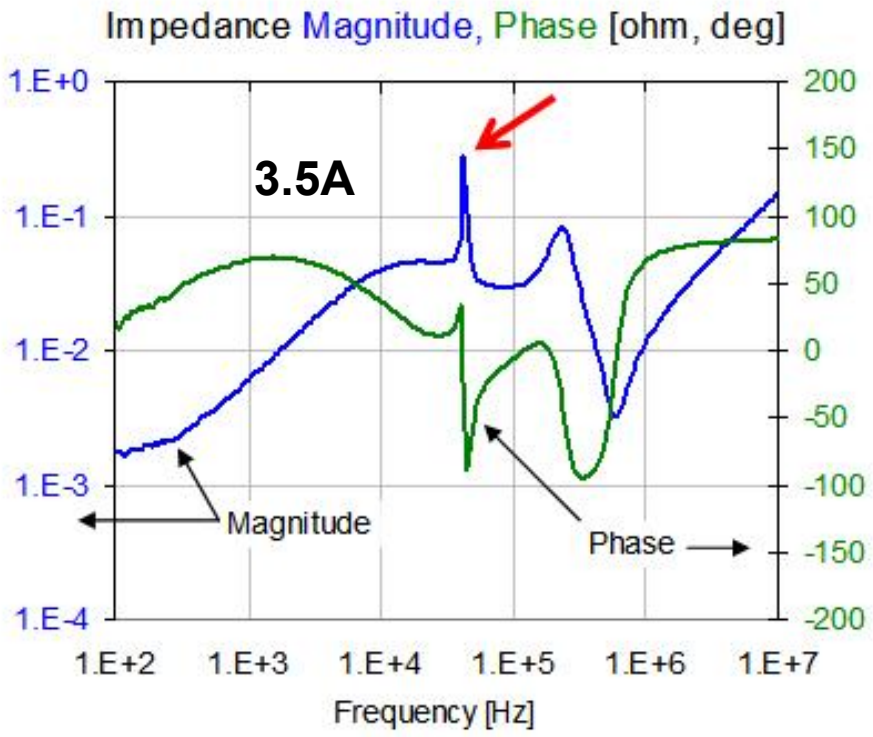
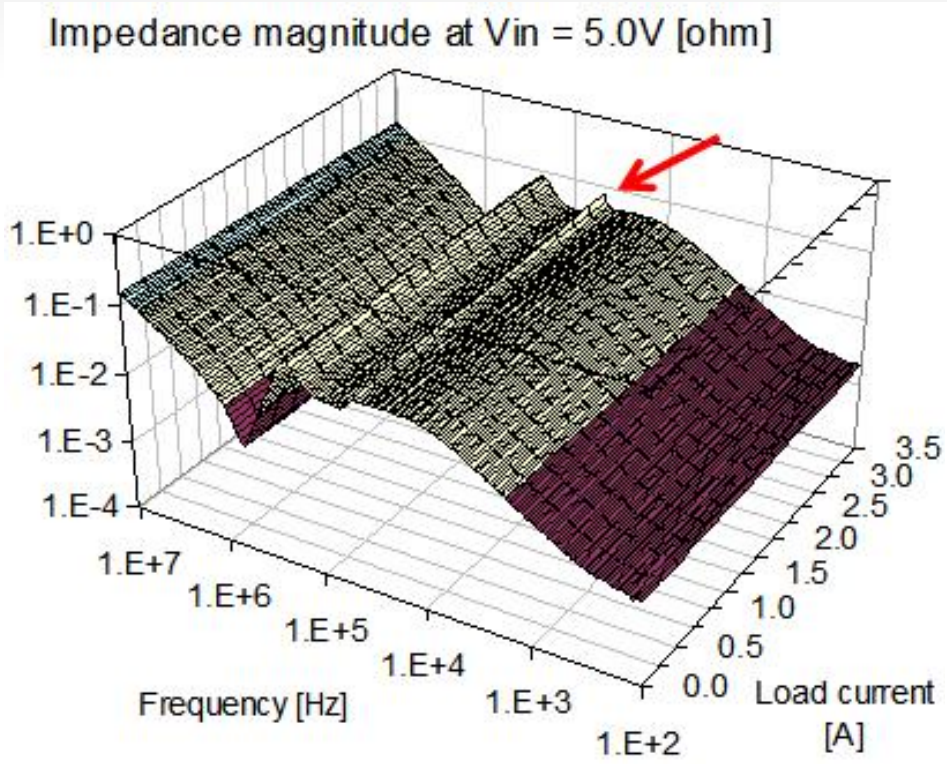
Output Impedance, Vin = 3.3V

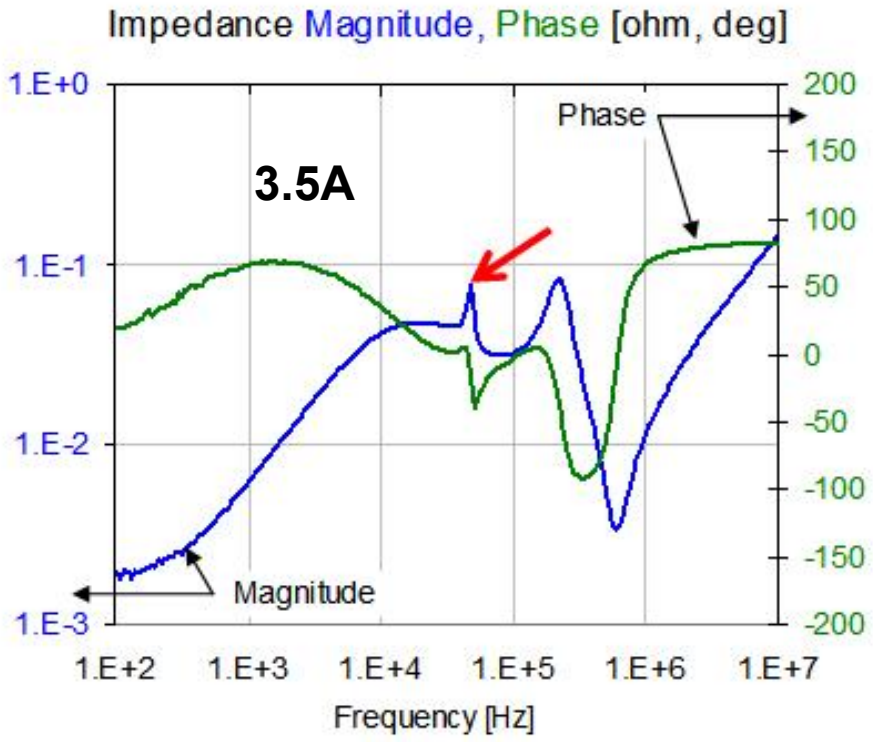




Vout = 1.8V, 4A max rated current

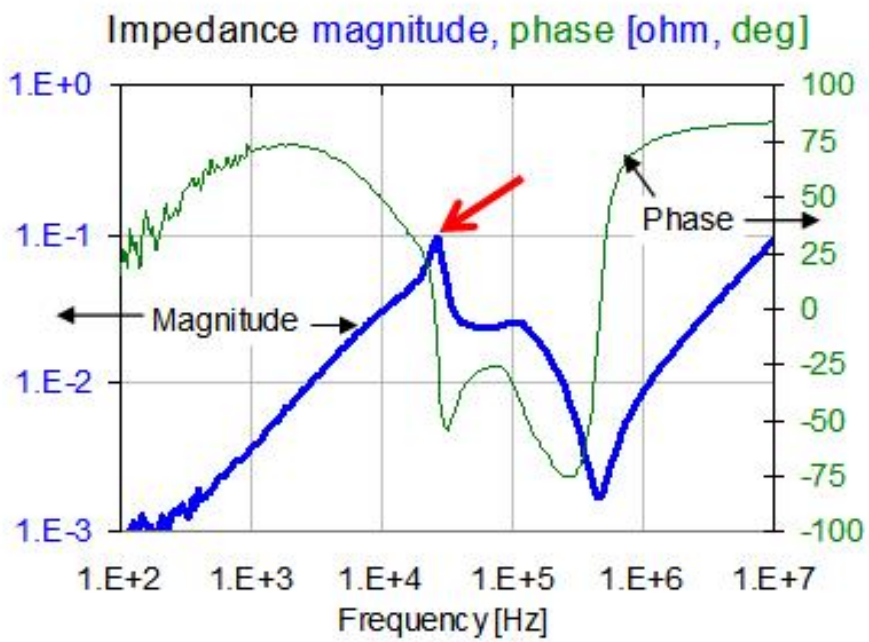
Output Impedance, Vin = 5.0V

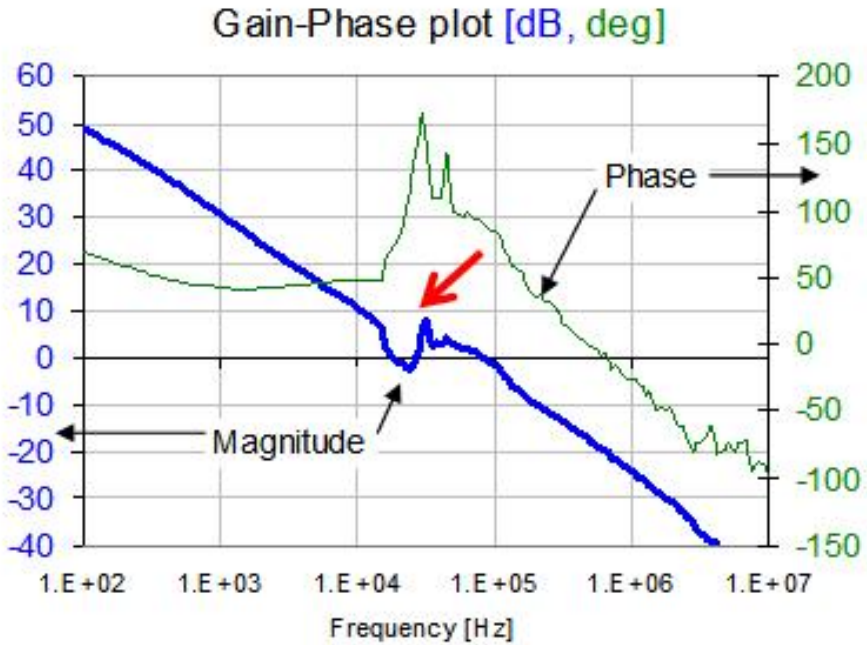




Vout = 1.8V, 4A max rated current

Output Impedance vs. Gain-Phase





Vin = 3.3V, Vout = 1.8V, 2A max rated current

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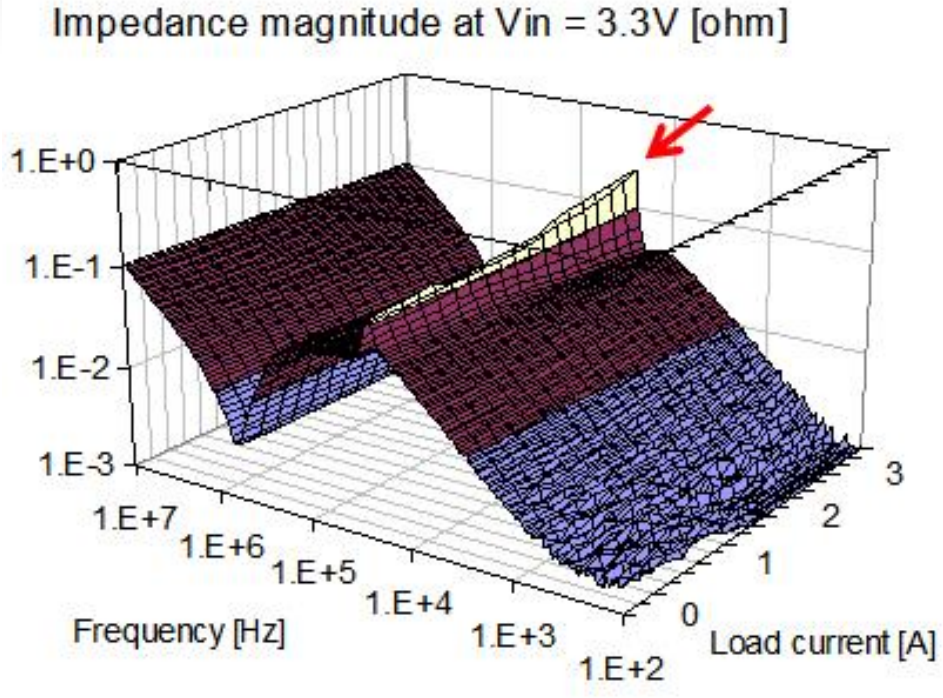
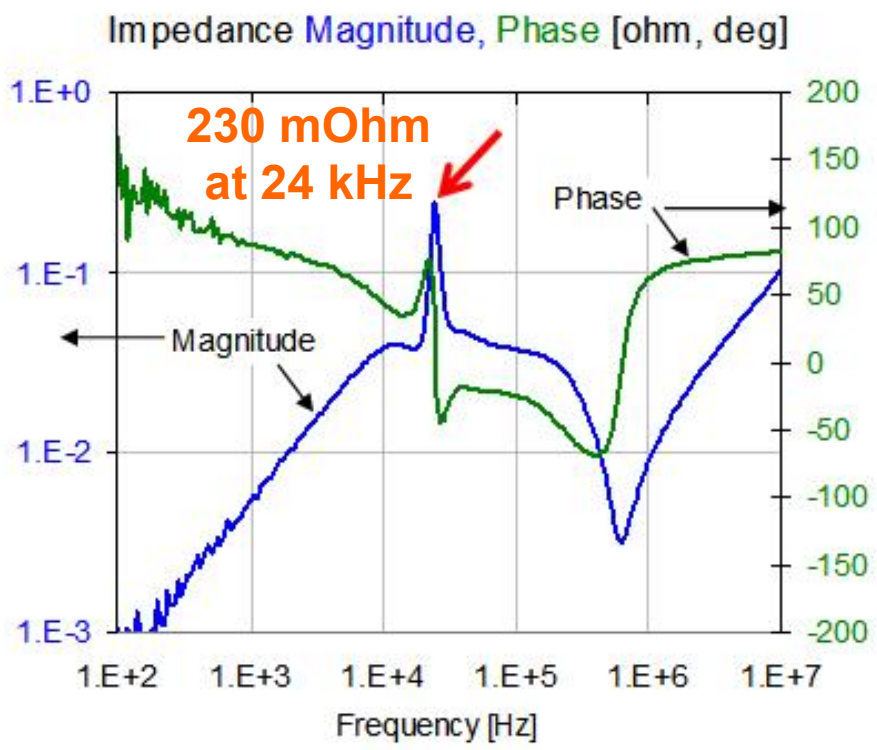
Output Impedance vs. Time Domain





Vin = 3.3V, Vout = 1.8V, 6A max rated current

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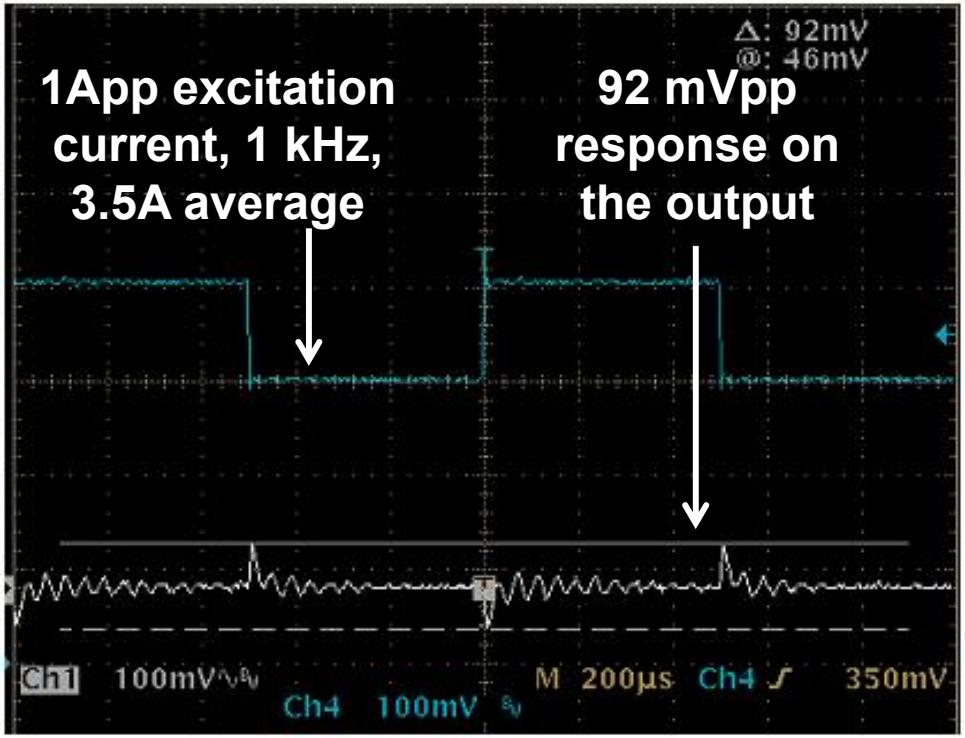
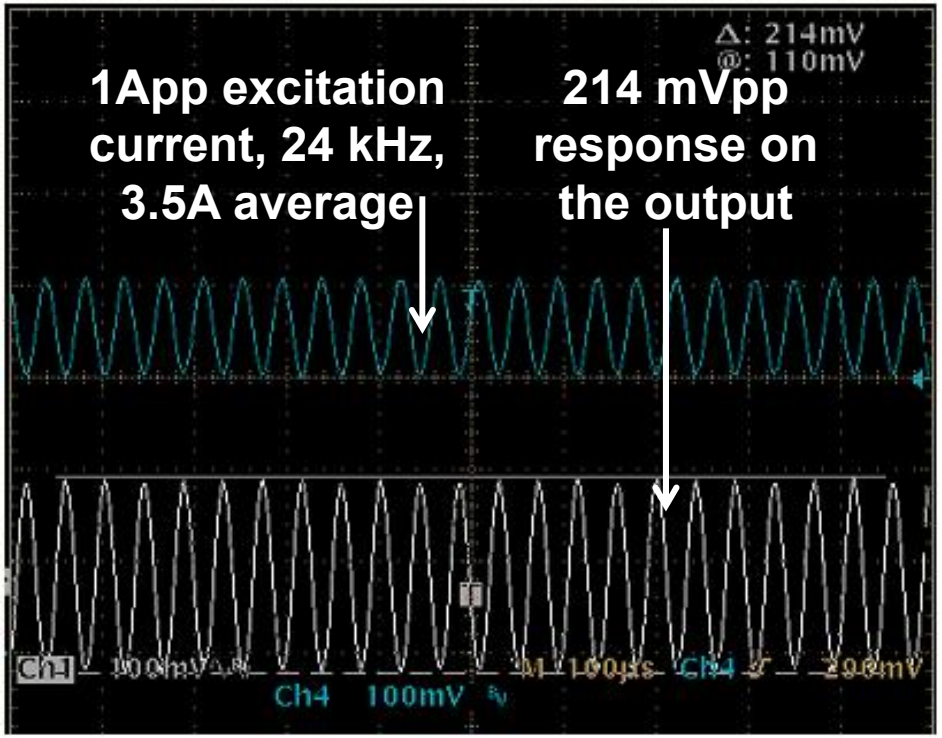
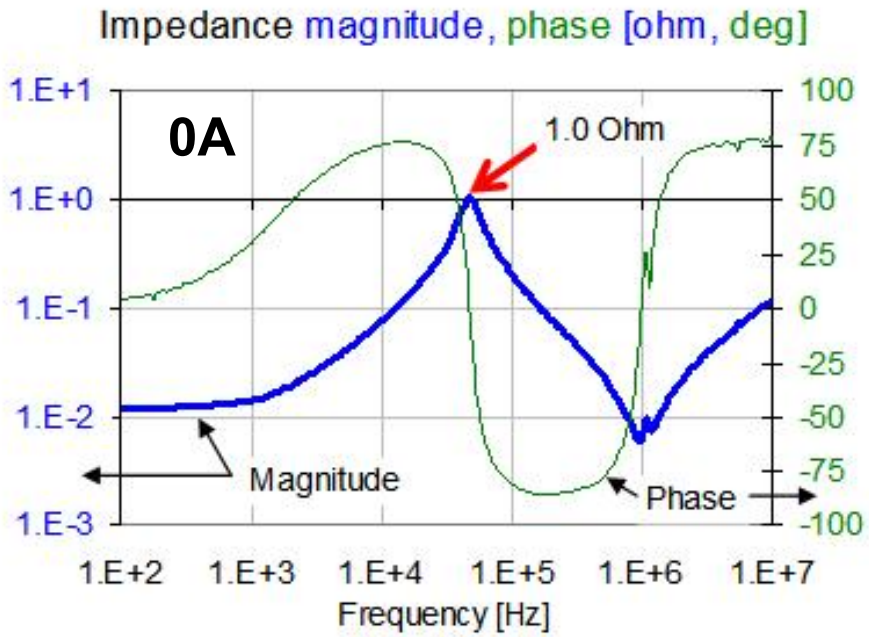
Output Impedance vs. Time Domain

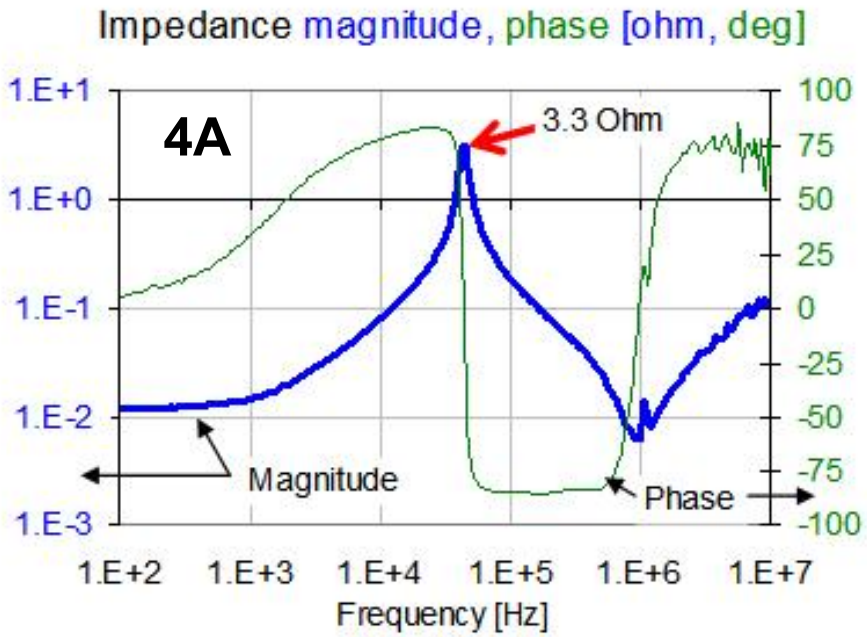




Vin = 3.3V, Vout = 1.8V, 6A max rated current

Impedance Across Input

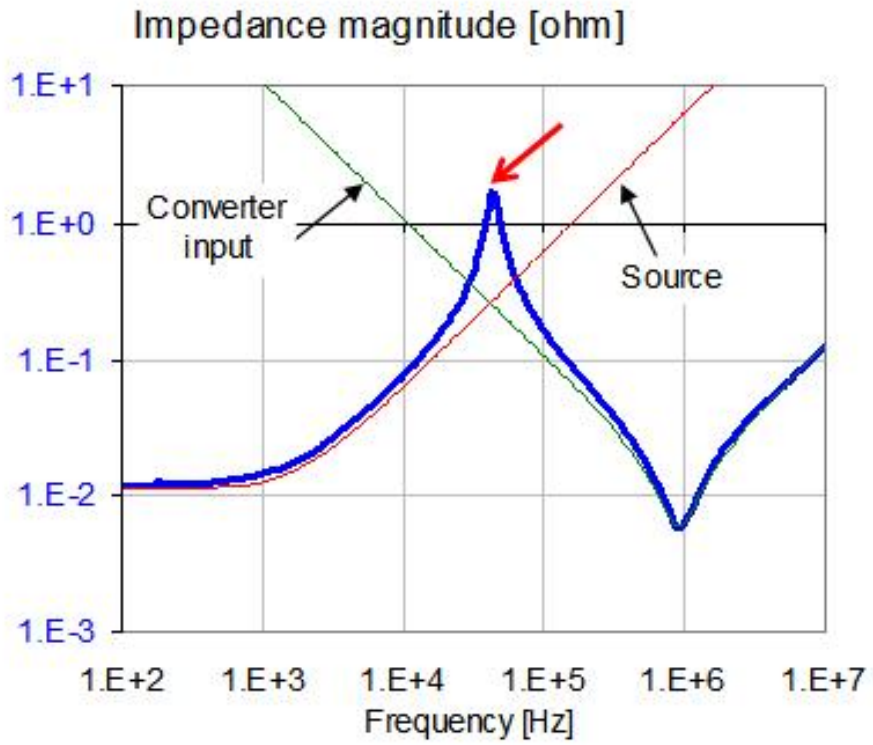


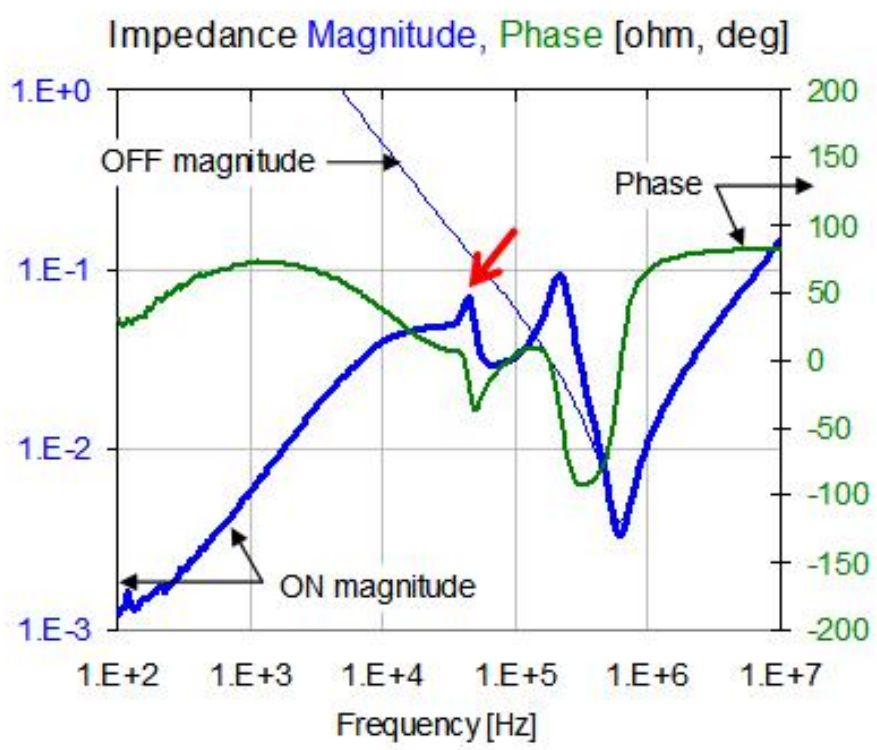


Vin = 3.3V, Vout = 1.8V, 4A max rated current

Peak increases with load current

Input vs. Output Impedance





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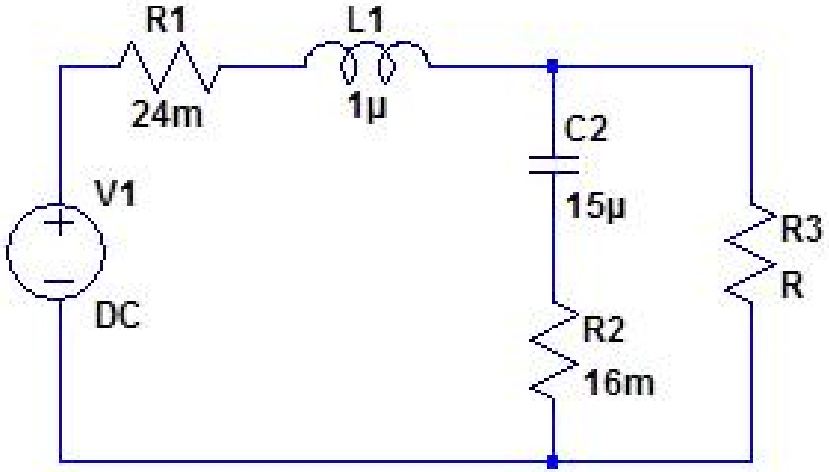
Impedance Model of Source/Input

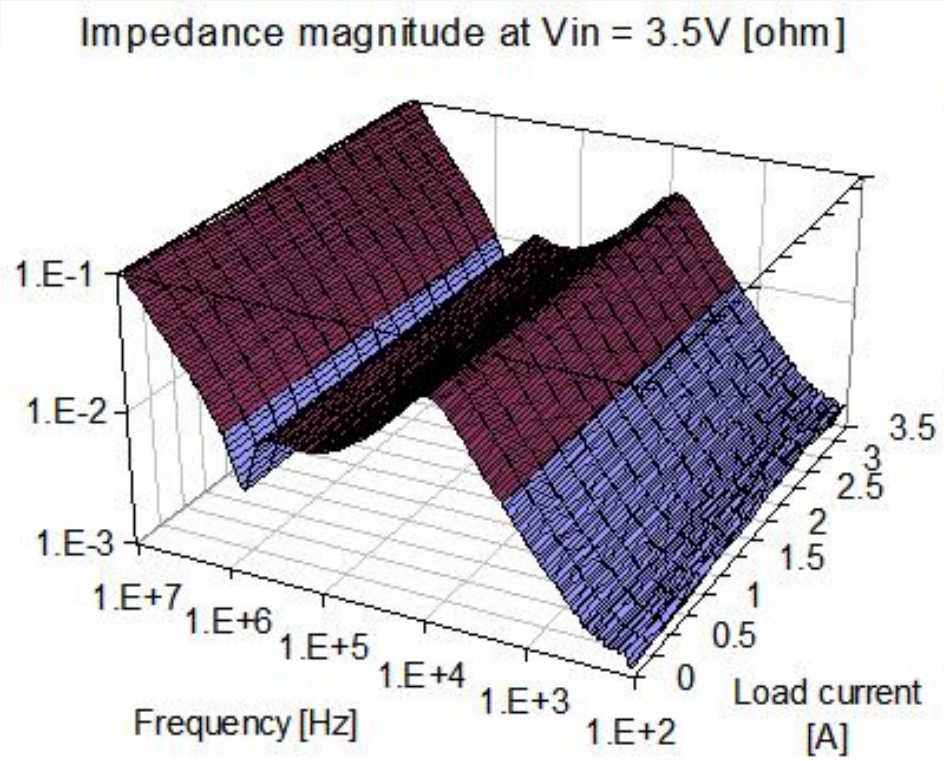


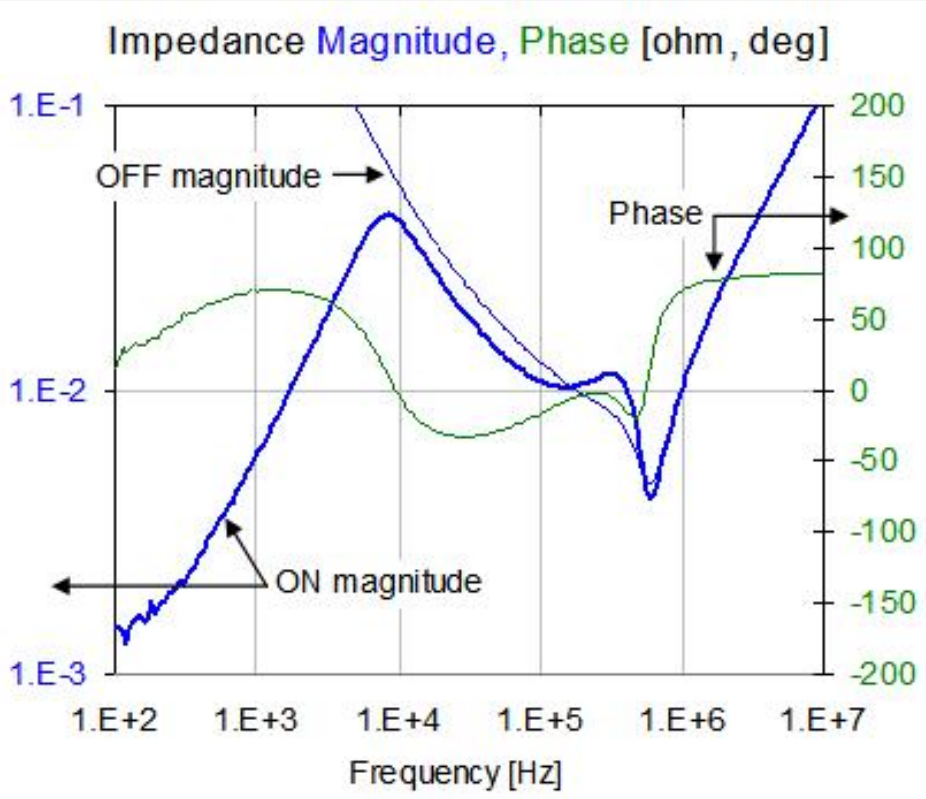
Critical negative load resistance:

$$R_3 = -\frac{R_1 R_2 C + L}{C(R_1 + R_2)}$$

$$r_{in} = \frac{\Delta V}{\Delta I_{in}} = \frac{\Delta V}{\frac{V_{out}\, I_{load}}{\eta(V_{in} + \Delta V)} - \frac{V_{out}\, I_{load}}{\eta V_{in}}} = -\eta \frac{V_{in}^2}{V_{out}\, I_{load}} = -R_{DC}$$

Input Peaking: The Solution



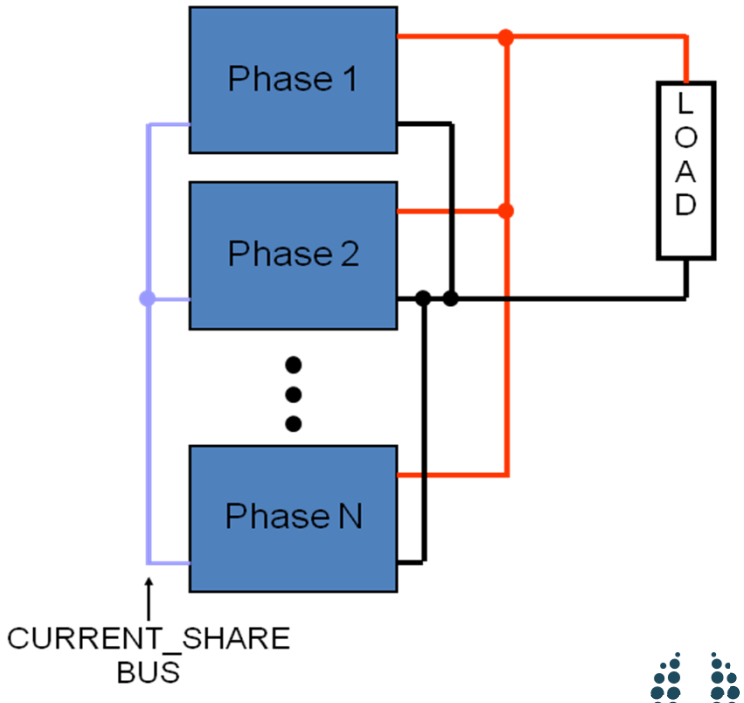


330 uF 25 mOhm polymer capacitor across input

Multiple Converters in Parallel

Multiple Converters in Parallel

- In Multi-phase systems, each phase must share current.
- Current share eases design requirements on each phase
- Current share is both a static and dynamic requirement.



Multiple Converters in Parallel

- In a multi-phase system, each phase can be represented by its Thevenin equivalent

- This allows the system to be simplified into the parallel combination of source impedances, Z_i.

$$\frac{1}{Z_S} = \frac{1}{Z_1} + \frac{1}{Z_2} + \cdots \frac{1}{Z_N} = \frac{N}{Z_i}$$

Multiple Converters in Parallel

- The power system and load share a common voltage (across the load). At medium frequencies the impedance of the passive output network scales with the number of phases.

Or

$$Z_S = \frac{Z_i}{N}$$

$$N \cdot Z_S = Z_i$$

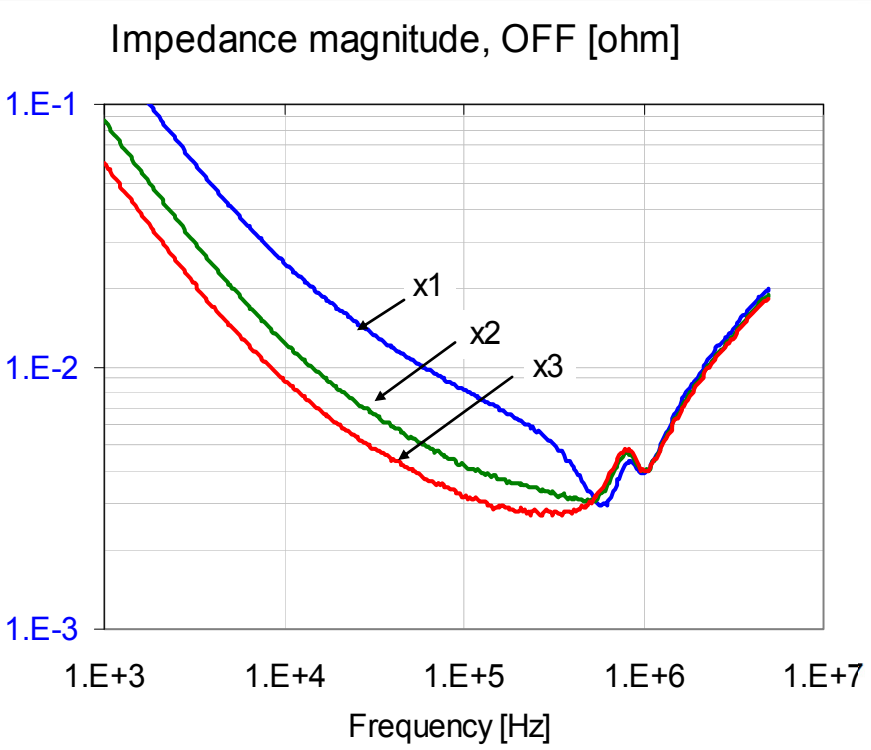
Multiple Converters in Parallel

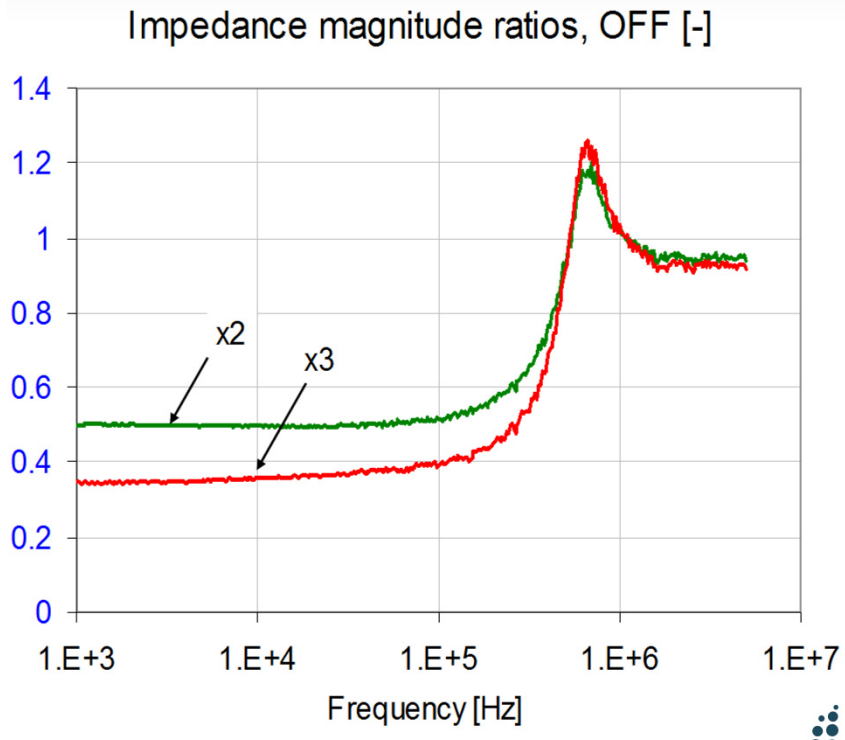
- So what does this mean?

$$N \cdot Z_S = Z_i$$

- … the dynamics of a multiphase system can be scaled to the dynamics of a single phase system with load impedance, Z_L, scaled by the number of phases!

Supplies OFF Output Impedance





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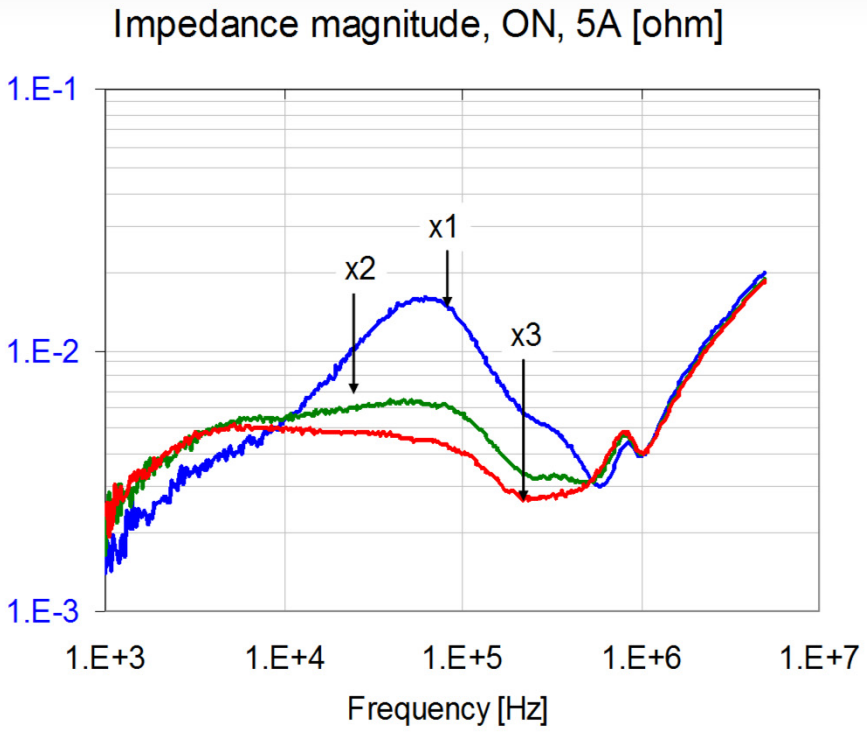
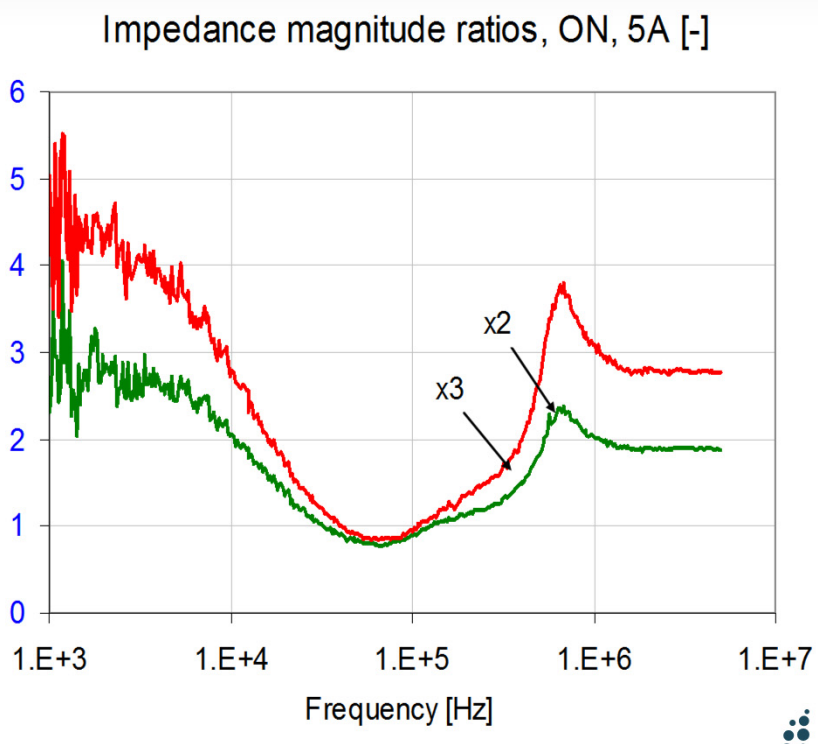
Supplies OFF – Main Points

- For low frequencies, OFF impedance scales with number of supplies added
- As frequency increases, series parasitic inductance between supplies isolates supplies, so parallel supplies have diminishing effect.
- What happens when the supplies are turned on?

Supplies ON, 5A Load





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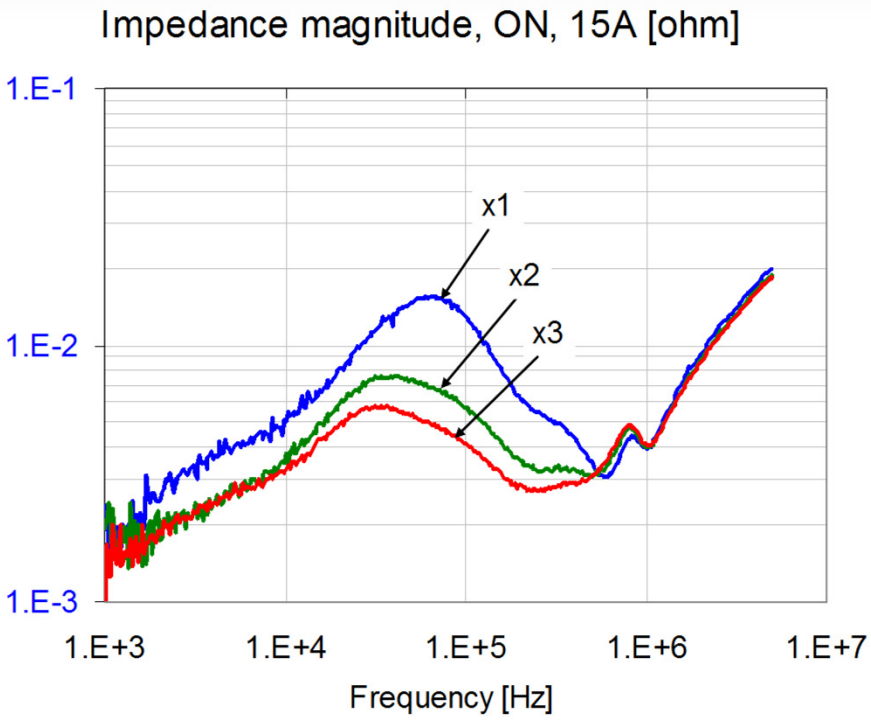
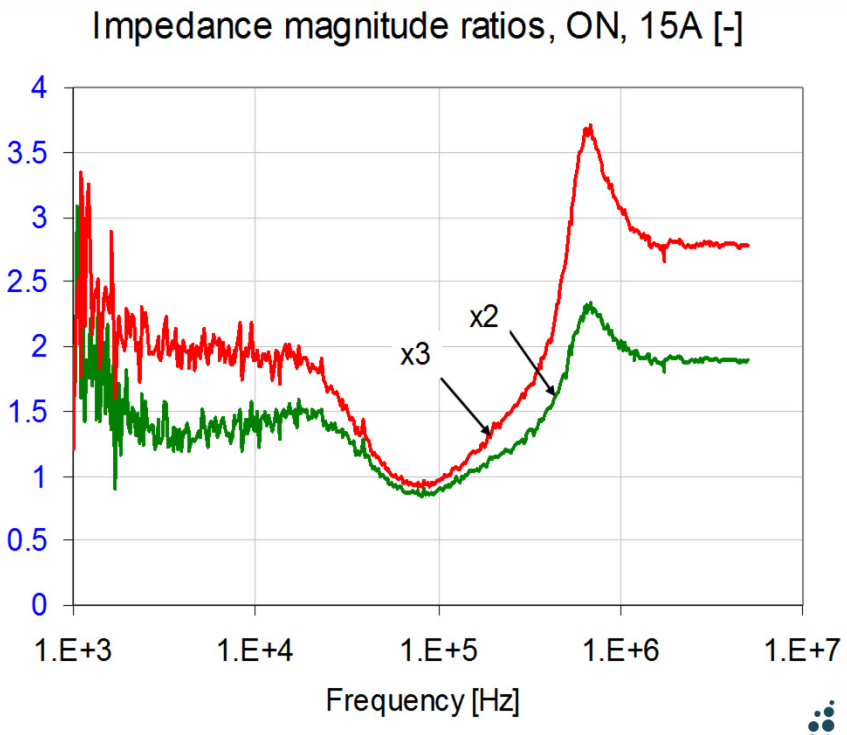
Supplies ON, 15A Load





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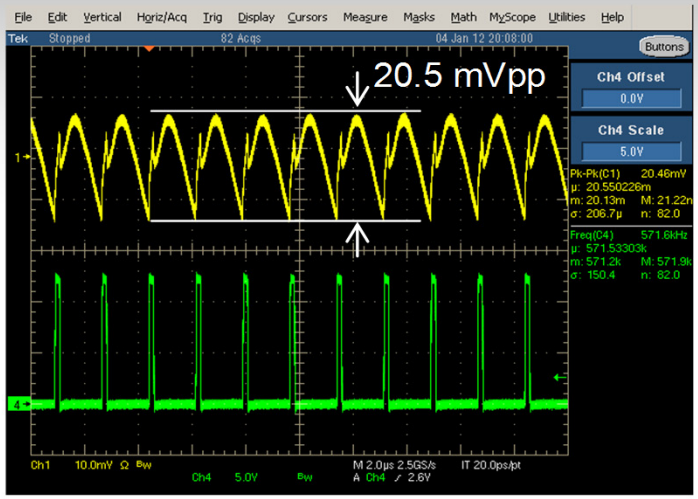
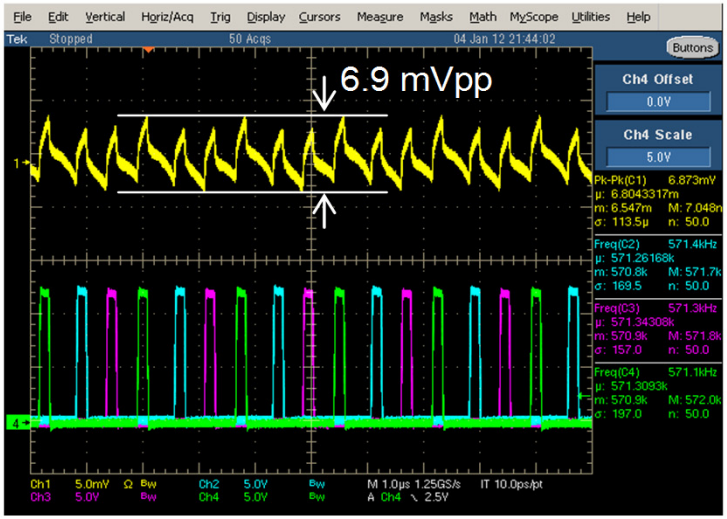
Supplies ON – Main Points

- At low frequencies the high DC loop gain establishes very low impedance, which gets masked out by residual connection resistance - no difference in single, two or three phase plots.
- As frequency increases, loop gain decreases, and impedance distributes according to passive impedance of each phase.
- At high frequencies, parastics dominate.

Multiple Converters in Parallel

- What about the time domain?
- Switching of paralleled converters are typically phase shifted by 360˚/N, where N is the number of supplies
- Do we see similar scaling in output voltage ripple?





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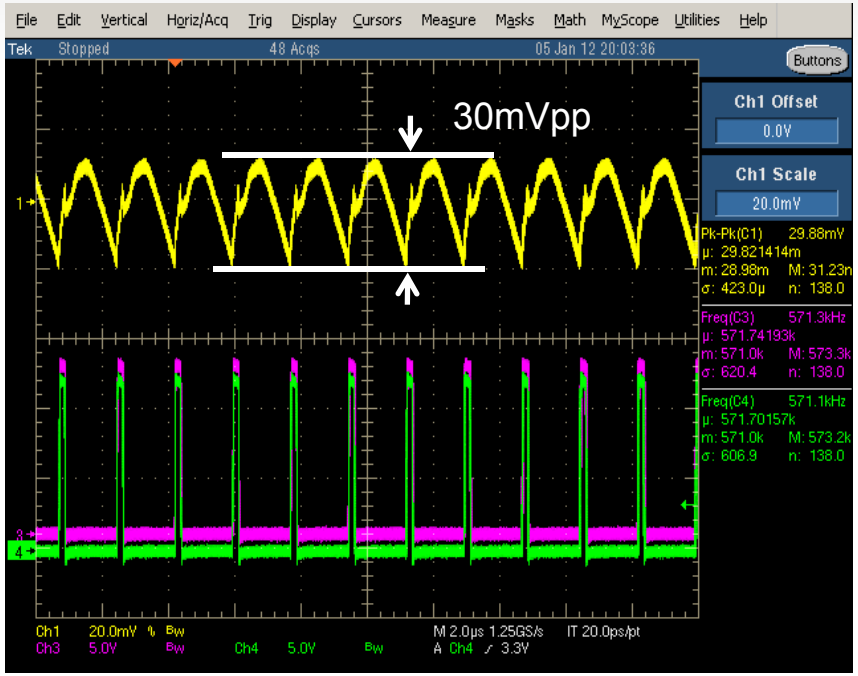
Vout Ripple Scaling

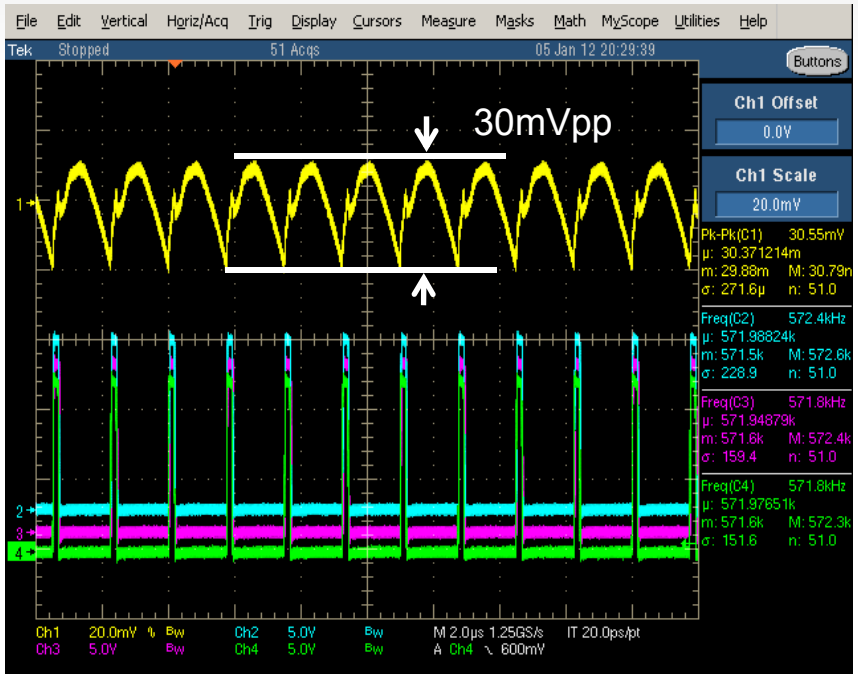
- Dominate contribution of Vout ripple is inductor ripple current multiplied across output capacitor ESR.

$$V_{out\_ripple} = I_{L_{Pk-pk}} \bullet ESR_{C_{out}}$$

- By phase shifting the switching by 360˚/N, effective switching frequency increases, resulting in a decrease in Vout ripple.

- What if phase shifting is disabled?


File Edit Vertical Horiz/Acq Trig Display Cursors Measure Masks Math MyScope Utilities Help
Tek Stopped 48 Acqs 05 Jan 12 20:03:36
Buttons
30mVpp
Ch1 Offset
0.0V
Ch1 Scale
20.0mV
Pk-Pk(C1) 29.88mV
μ: 29.821414m
m: 28.98m M: 31.23m
σ: 423.0μ n: 138.0
Freq(C3) 571.3kHz
μ: 571.74193k
m: 571.0k M: 573.3k
σ: 620.4 n: 138.0
Freq(C4) 571.1kHz
μ: 571.70157k
m: 571.0k M: 573.2k
σ: 606.9 n: 138.0
Ch1 20.0mV Bw
Ch3 5.0V Bw
Ch4 5.0V Bw
M 2.0μs 1.25GS/s
A Ch4 3.3V
IT 20.0ps/pt


File Edit Vertical Horiz/Acq Trig Display Cursors Measure Masks Math MyScope Utilities Help
Tek Stopped 51 Acqs 05 Jan 12 20:29:39
Buttons
30mVpp
Ch1 Offset
0.0V
Ch1 Scale
20.0mV
Pk-Pk(C1) 30.55mV
μ: 30.371214m
m: 29.88m M: 30.79m
σ: 271.6μ n: 51.0
Freq(C2) 572.4kHz
μ: 571.98824k
m: 571.5k M: 572.6k
σ: 228.9 n: 51.0
Freq(C3) 571.8kHz
μ: 571.94879k
m: 571.6k M: 572.4k
σ: 159.4 n: 51.0
Freq(C4) 571.8kHz
μ: 571.97651k
m: 571.6k M: 572.3k
σ: 151.6 n: 51.0
Ch1 20.0mV Bw
Ch3 5.0V Bw
Ch2 5.0V Bw
Ch4 5.0V Bw
M 2.0μs 1.25GS/s
A Ch4 600mV
IT 20.0ps/pt

Why multiphase?

- When properly designed, current is divided between phases – makes design of 30A+ buck converters realizable and cost effective.
  - Distributes the thermal loading
  - Small, cost effective inductors
- Output impedance scales with number of phases added.
- When phases are phase shifted, Vout ripple scales with number of phases.

Digital Control

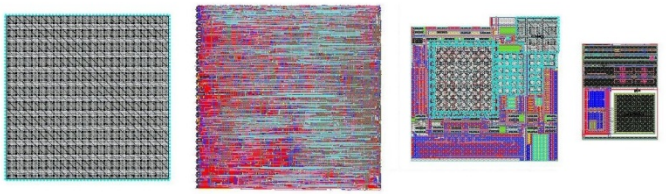
Digital Control

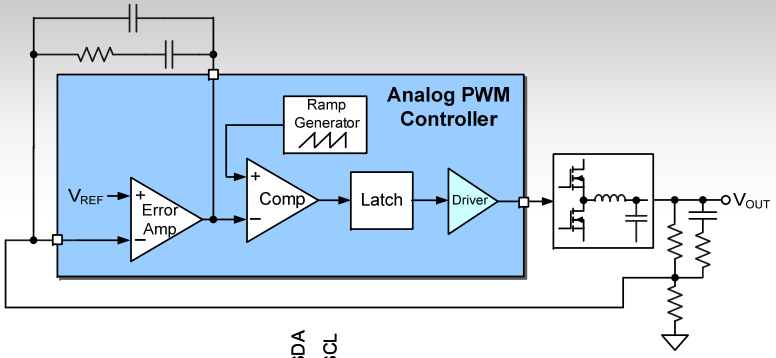
- Digital Control is rising in popularity
- Many different techniques, but same basic result – produce PWM pulse using digital techniques.
- Analog control uses analog filters in control loop; Digital control uses digital filters, which combine current and historical gained values.

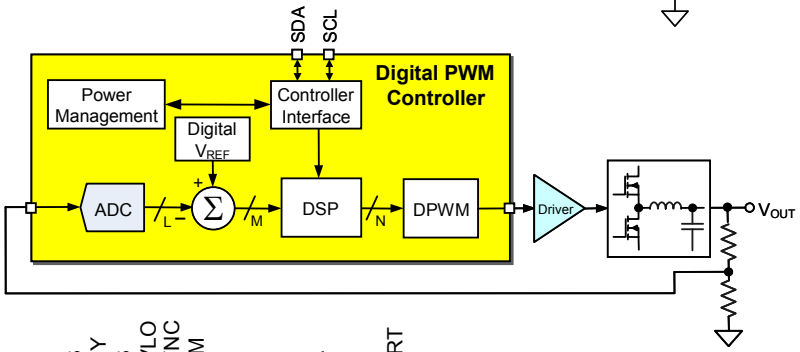
Advantages to Digital Power

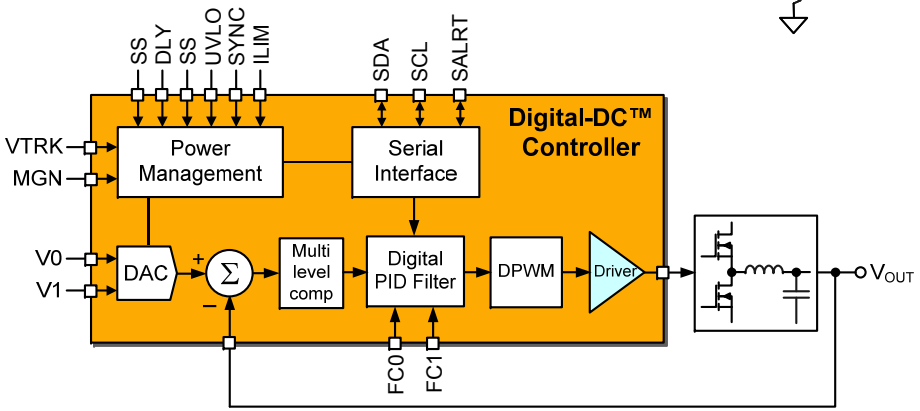
- **Programmability/Configurability**
  - Software and Hardware
  - More sophisticated algorithms
  - Control
  - Monitoring
- **Components**
  - Storage
  - Math operations
- **Numerical Stability (e.g. drift)**
  - Calibration
- **Silicon Processes**
- **Resistance to noise**

Reduced component count
Higher Density
Lower (system) cost
Better reuse
Faster time to market









- **Analog**
  - Well understood
  - External control and compensation components
- **"Textbook" Digital**
  - DSP – brute force=$
- **Power Optimized Digital**
  - Efficient compensation
  - Strap configurable

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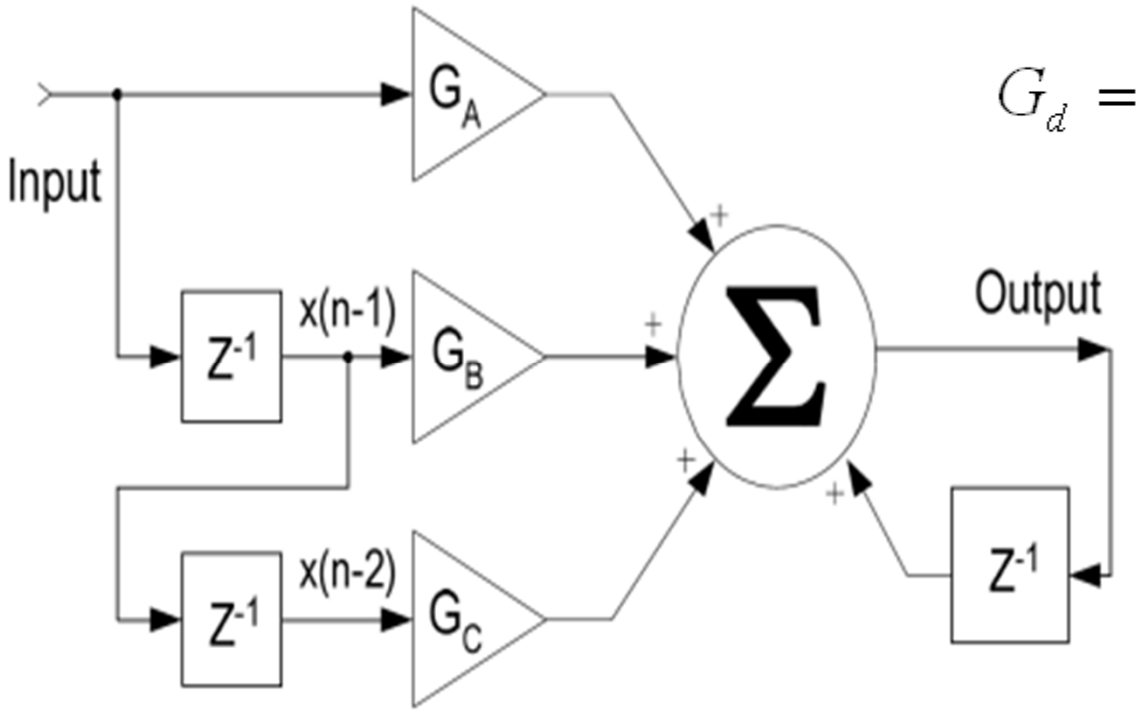
Digital PID Filter



$$G_d = \frac{A + Be^{-sT} + Ce^{-2sT}}{e^{-sT}\left(1 - e^{-sT}\right)}$$

Digital PID Filter

$$G_d = \frac{A + Be^{-sT} + Ce^{-2sT}}{e^{-sT}\left(1 - e^{-sT}\right)}$$

- A, B and C are gain coefficients for various “taps”.
- First term in denominator is due to delays in signal path
- T is the switching frequency of the PWM

Digital PID Filter

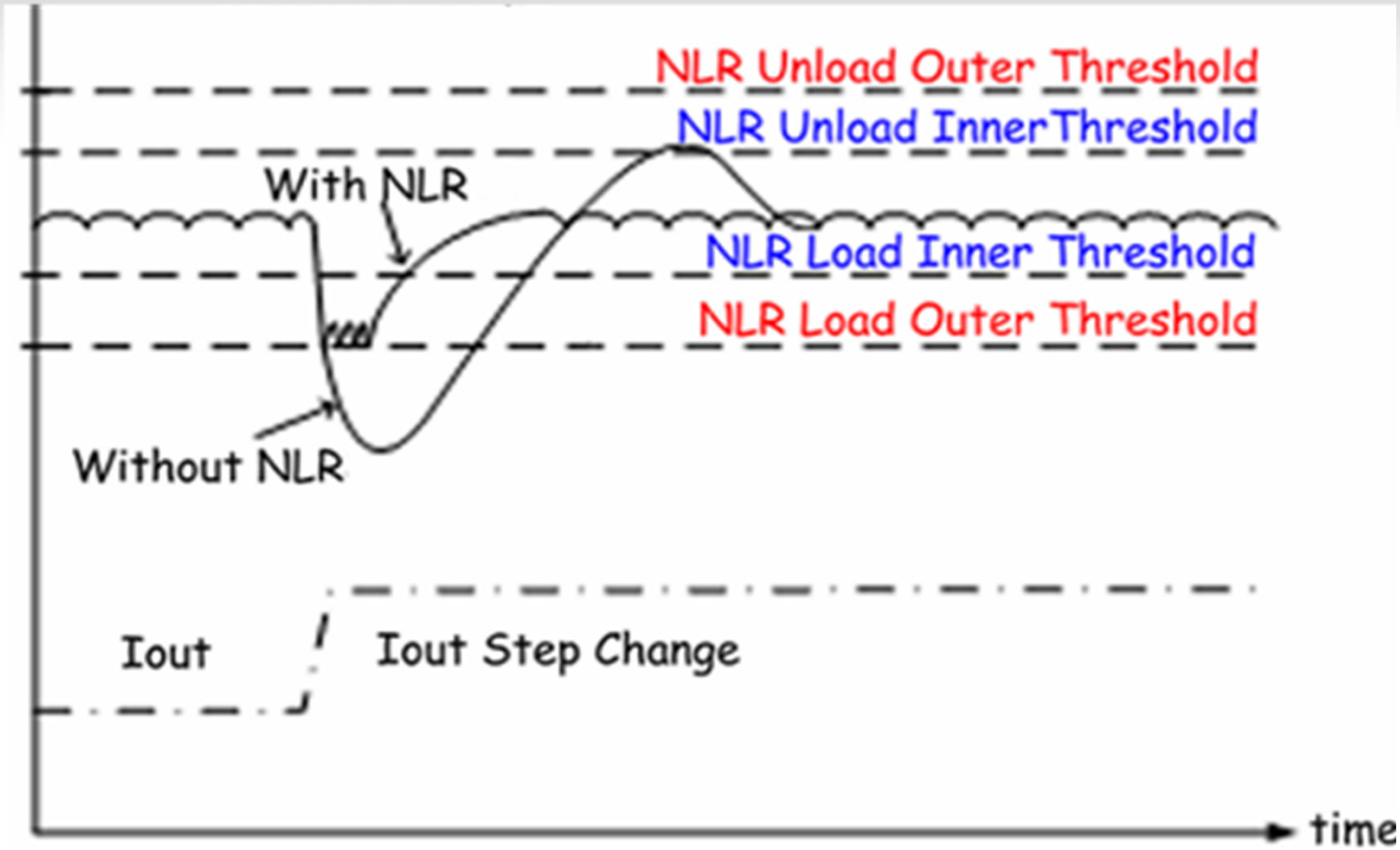
- Digital PID compensator has two Zeros, a pole at zero and a pole at infinity.
- Two zeros can be either real or a complex conjugate pair.
- Not limited to just real zeros like in a Type III analog compensator!

Other Advantages…

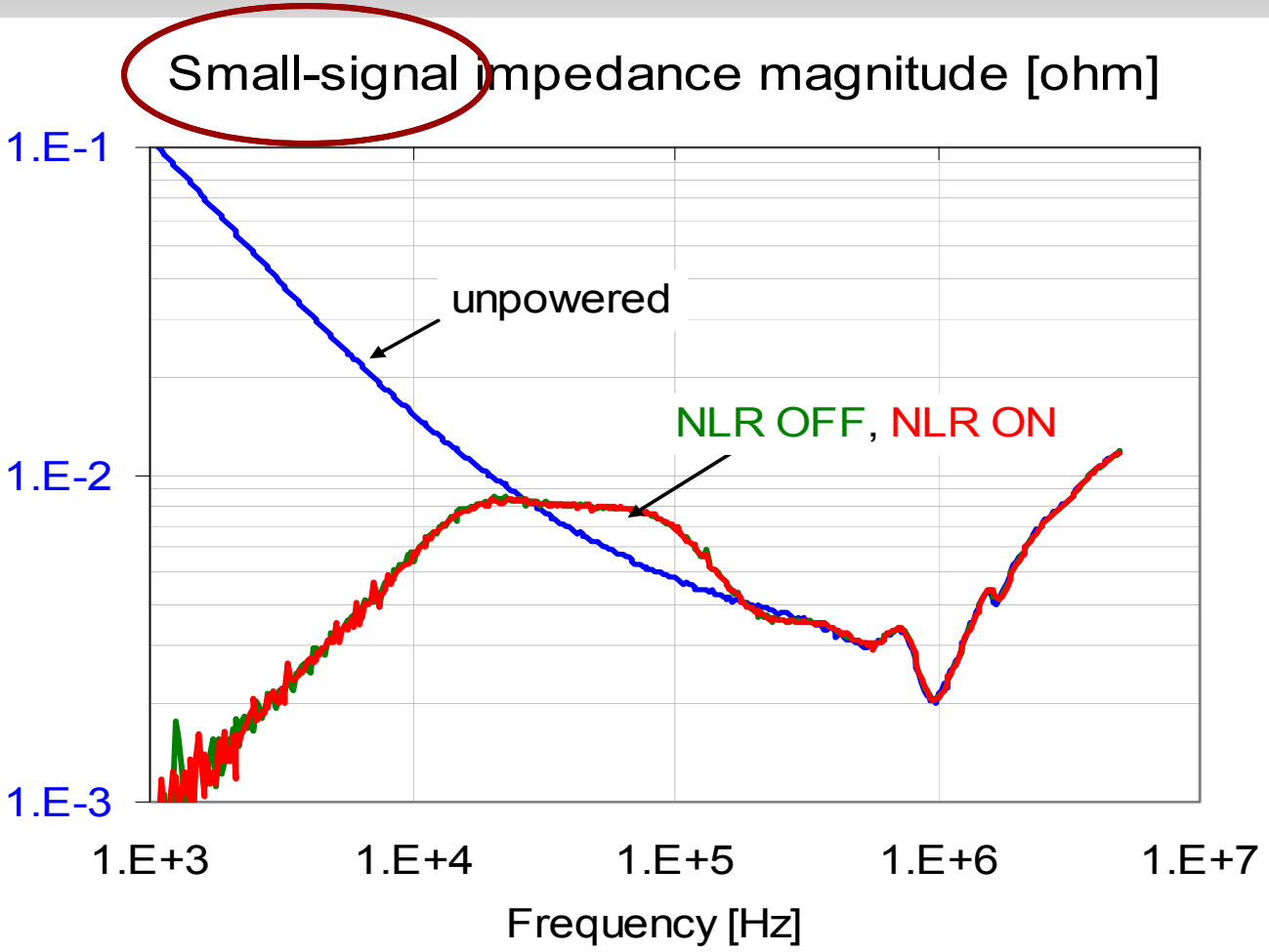
- Compensation values are stored in digital registers – no need for solder iron to change compensation!
- Automatic compensation algorithms – controller can automatically characterize and compensate plant.
- Non-linear control algorithms can easily be implemented.

What is Non-linear Control?

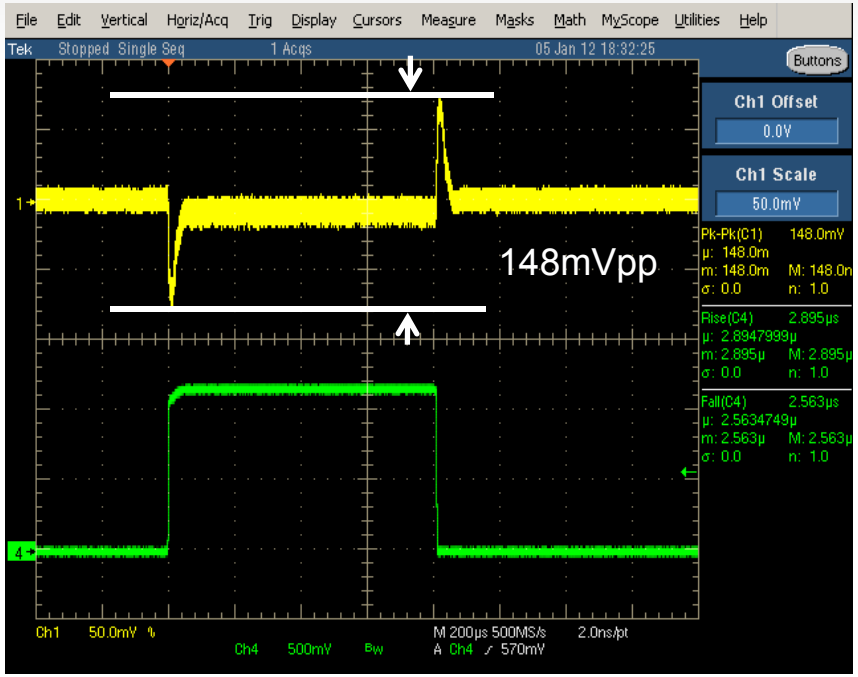
- Fast control loop which by-passes normal, slower, PID control loop.
- Many ways to implement – one example is a threshold based approach.
- Net effect is to increases effective control loop bandwidth.

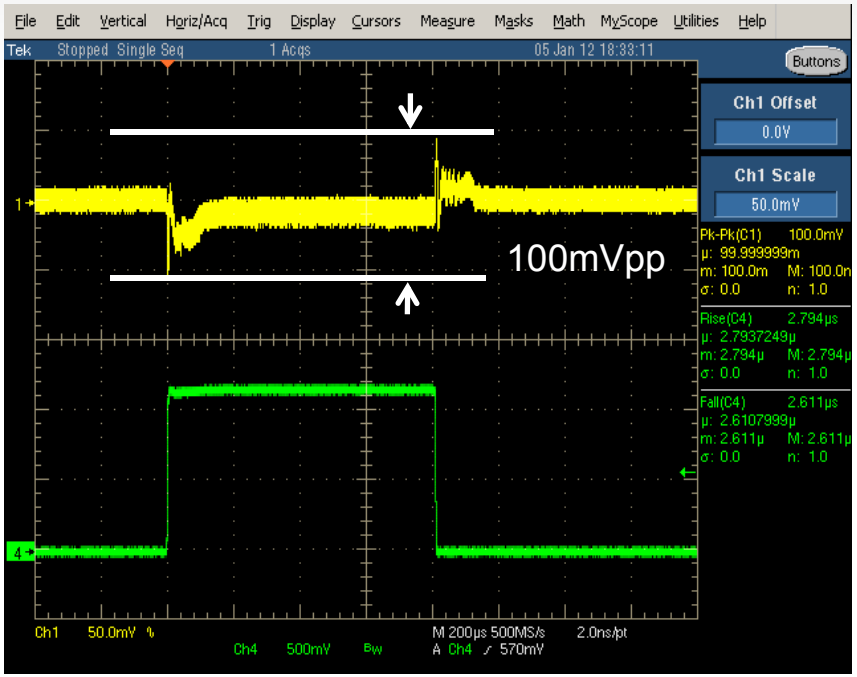

NLR Unload Outer Threshold
NLR Unload InnerThreshold
With NLR
NLR Load Inner Threshold
NLR Load Outer Threshold
Without NLR
Iout
Iout Step Change
time

- **Neat, but does it show up in output impedance measurements?**


Small-signal impedance magnitude [ohm]
1.E-1
1.E-2
1.E-3
unpowered
NLR OFF, NLR ON
1.E+3
1.E+4
1.E+5
1.E+6
1.E+7
Frequency [Hz]

- No, not in small signal output impedance measurements.
- Excitation signal is not large enough to excite NLR response.
- What about time domain?





- **33% Reduction in output deviation with NLR!**

Outline (continued):

- **III. Output impedance of DC-DC converters**
  - How source impedance influences output impedance
  - Multiple Converters in Parallel
  - Observations and Assumptions
  - Digital Control
- **IV. Measurements, Modeling, Simulations**
  - Measurements
  - Modeling, simulations
- **Conclusions**

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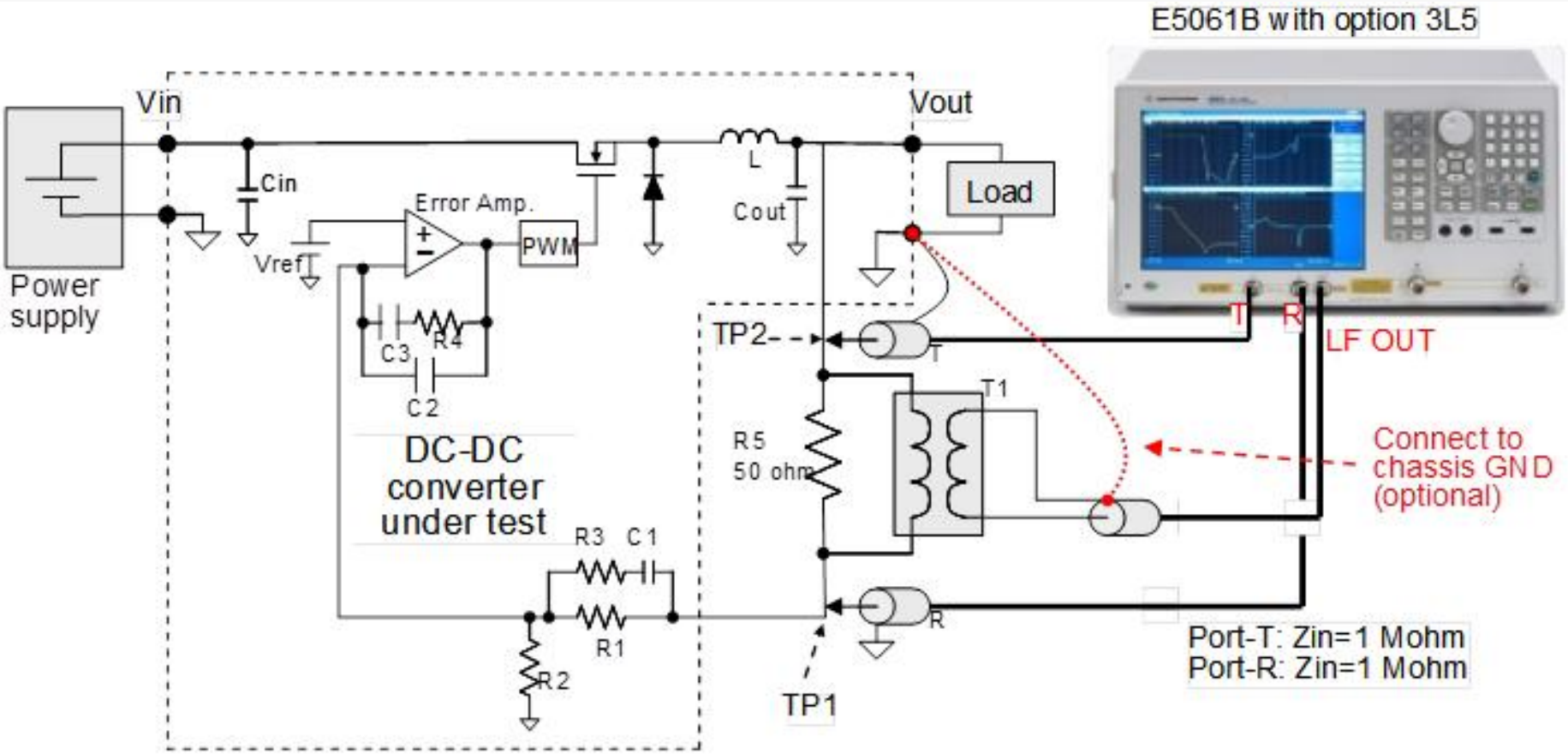
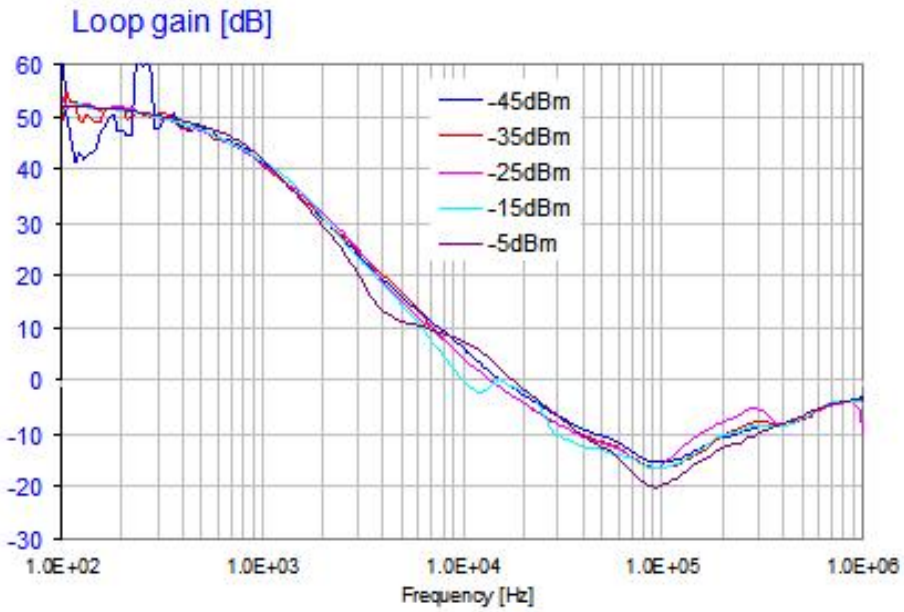
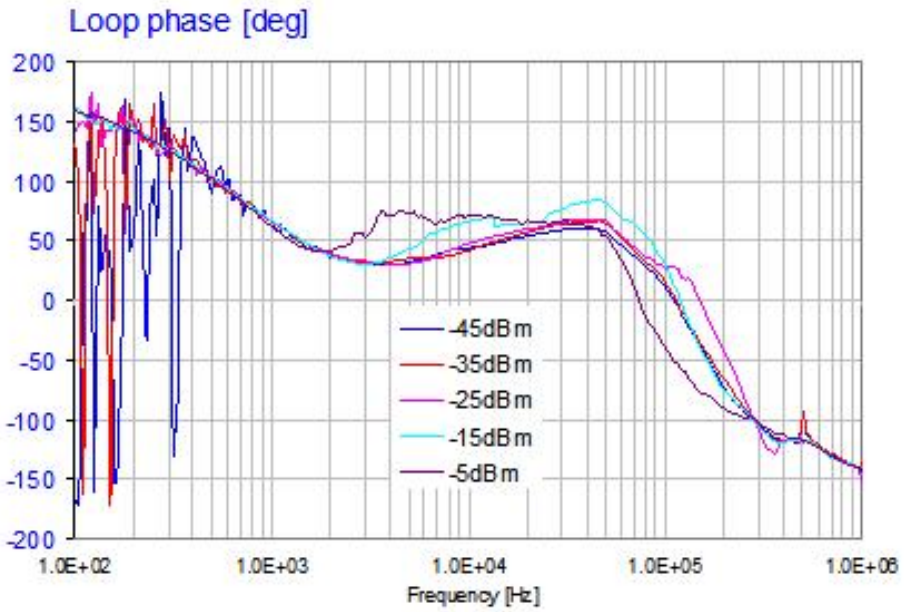
Gain-Phase Measurement

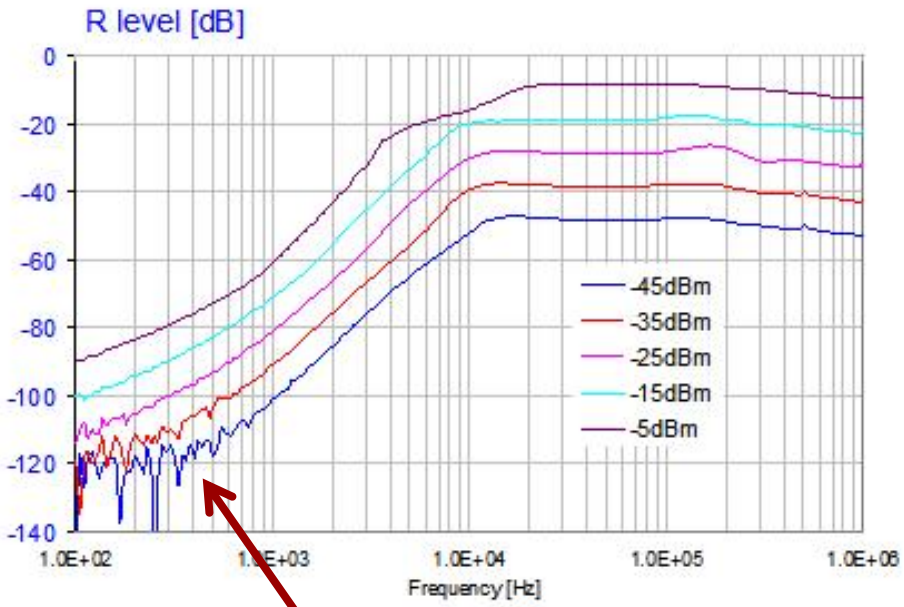


Gain-Phase Results (1)



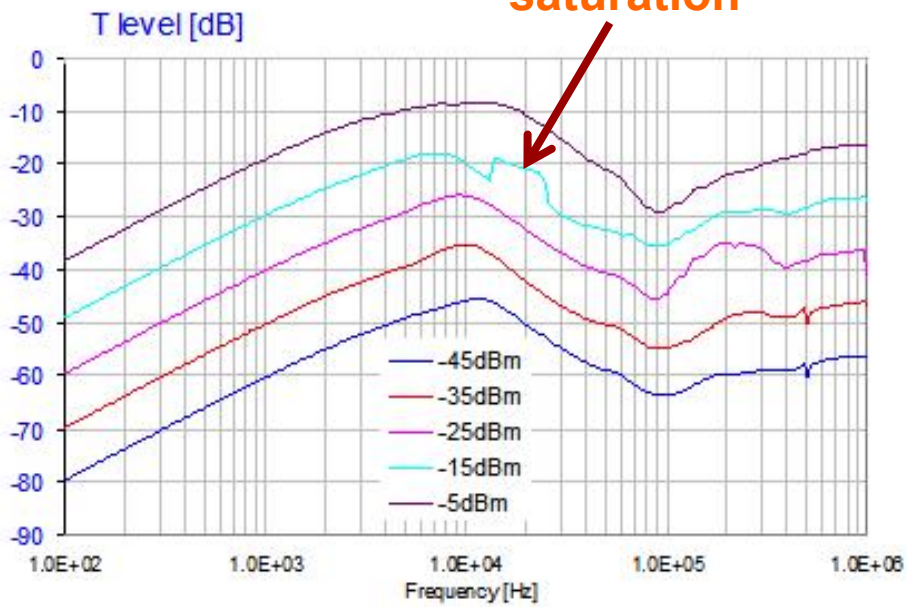


Gain-Phase Results (2)



Instrument noise floor

Error amplifier saturation



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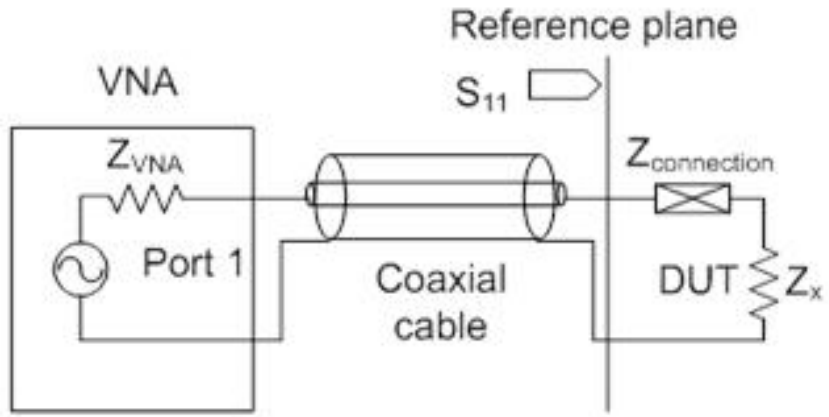
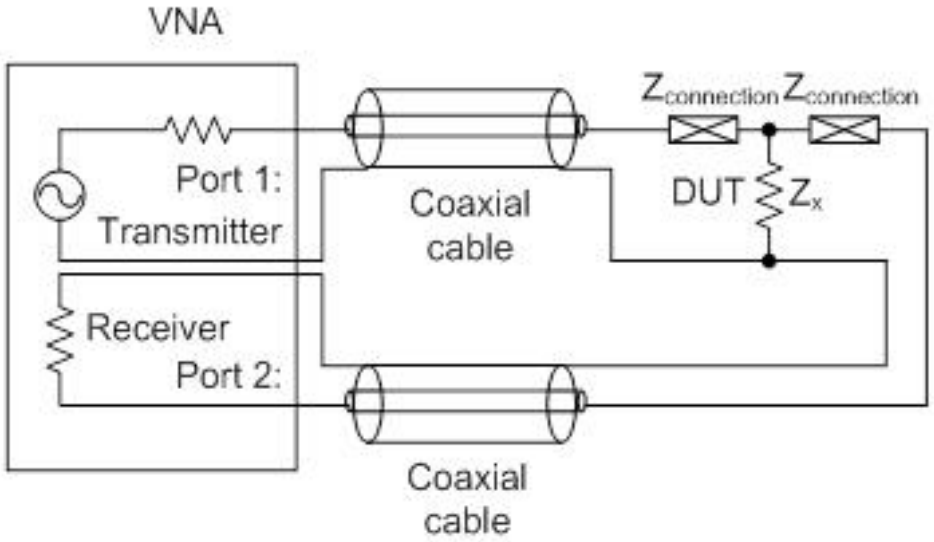
Measuring Low Impedances
The Problems



Problems with one-port impedance measurements:

- Discontinuity is in series to the unknown low impedance
- Reflection reading is not accurate for large reflections

Measuring Low Impedances
The Solution

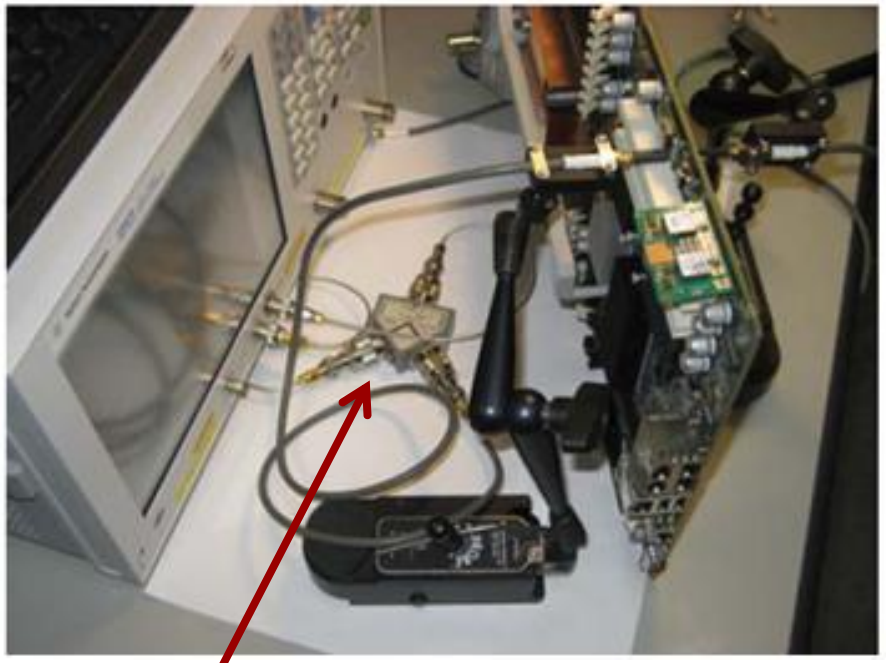


Benefits of two-port impedance measurements:

- Discontinuity is in series to the 50-Ohm VNA impedance
- Small DUT voltage is measured by a separate input (Kelvin connection)

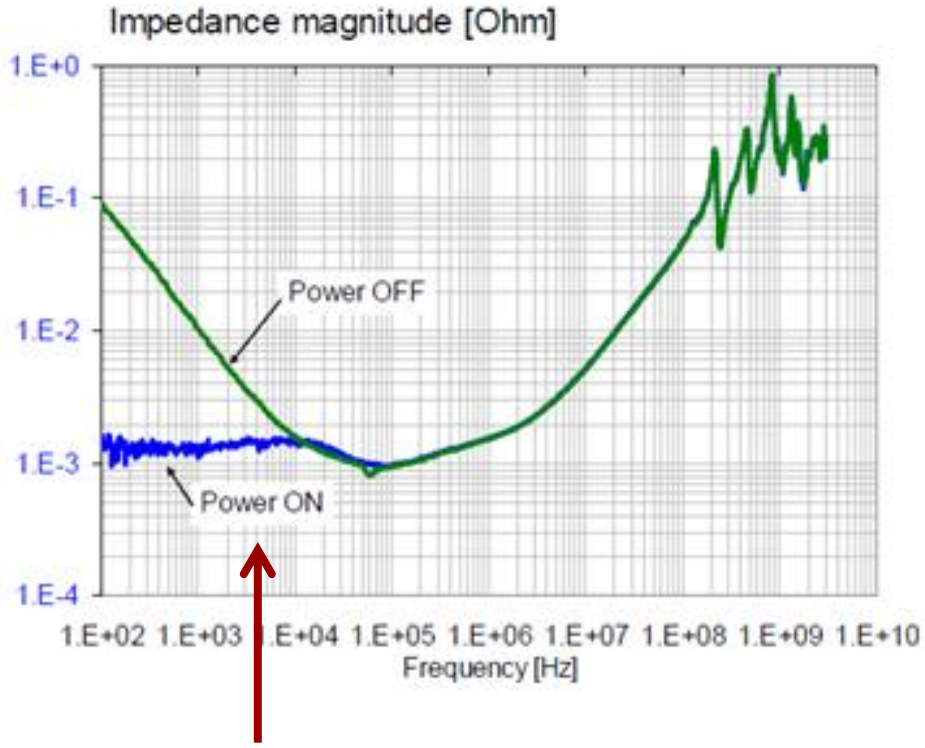
Measuring Full Systems (1)

Ferrite isolation with grounded ports

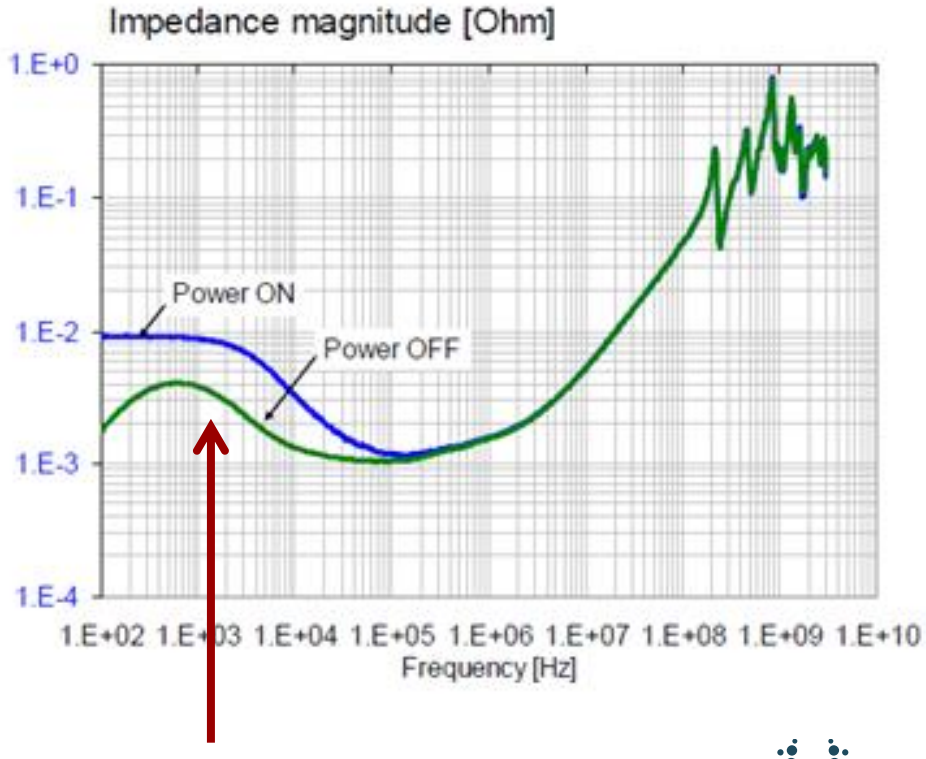


DC power splitter with floating-ground inputs

Measuring Full Systems (2)



Correct reading with ferrite isolation



Incorrect reading without ferrite isolation

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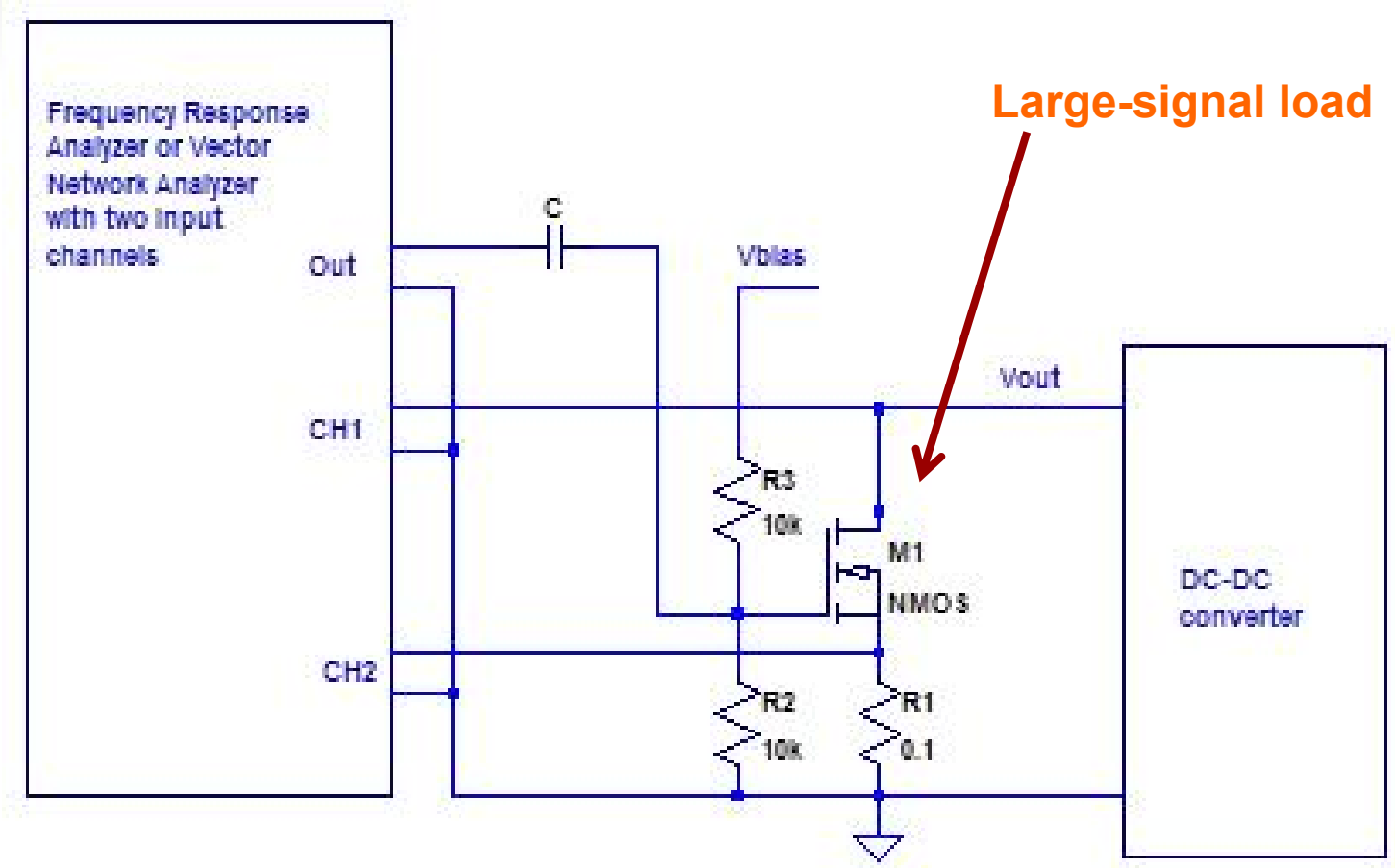
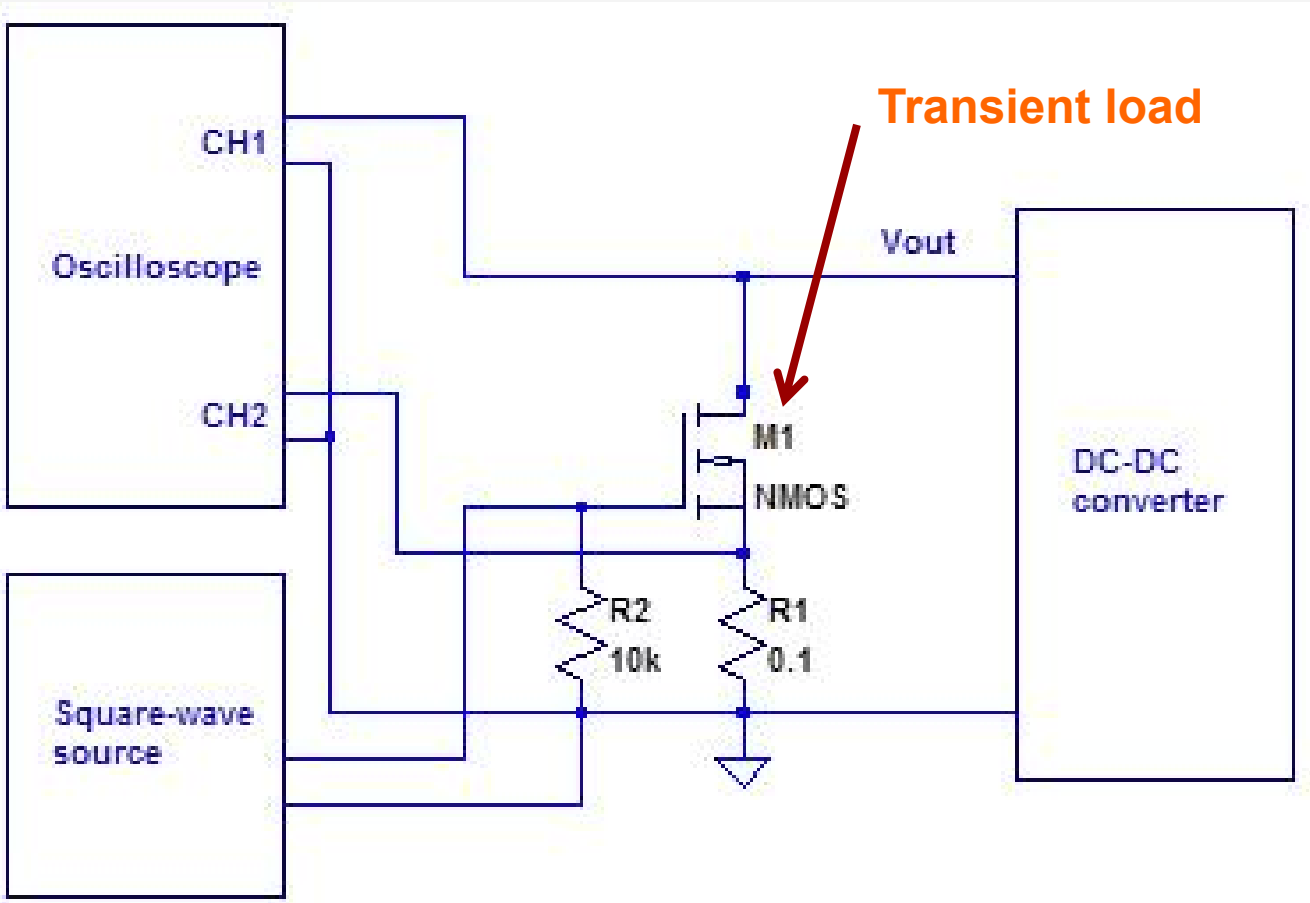
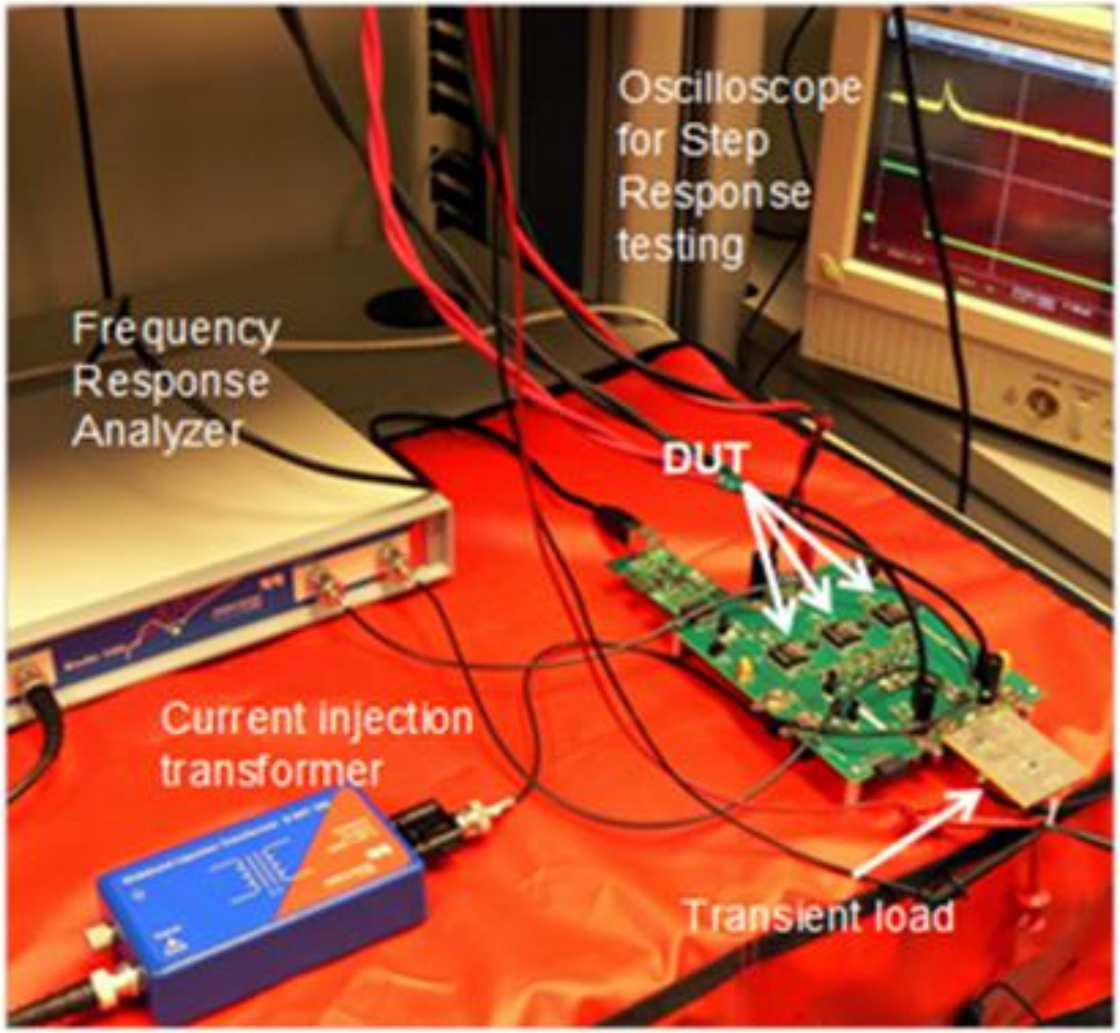
Large-Signal Z_{out} Measurement

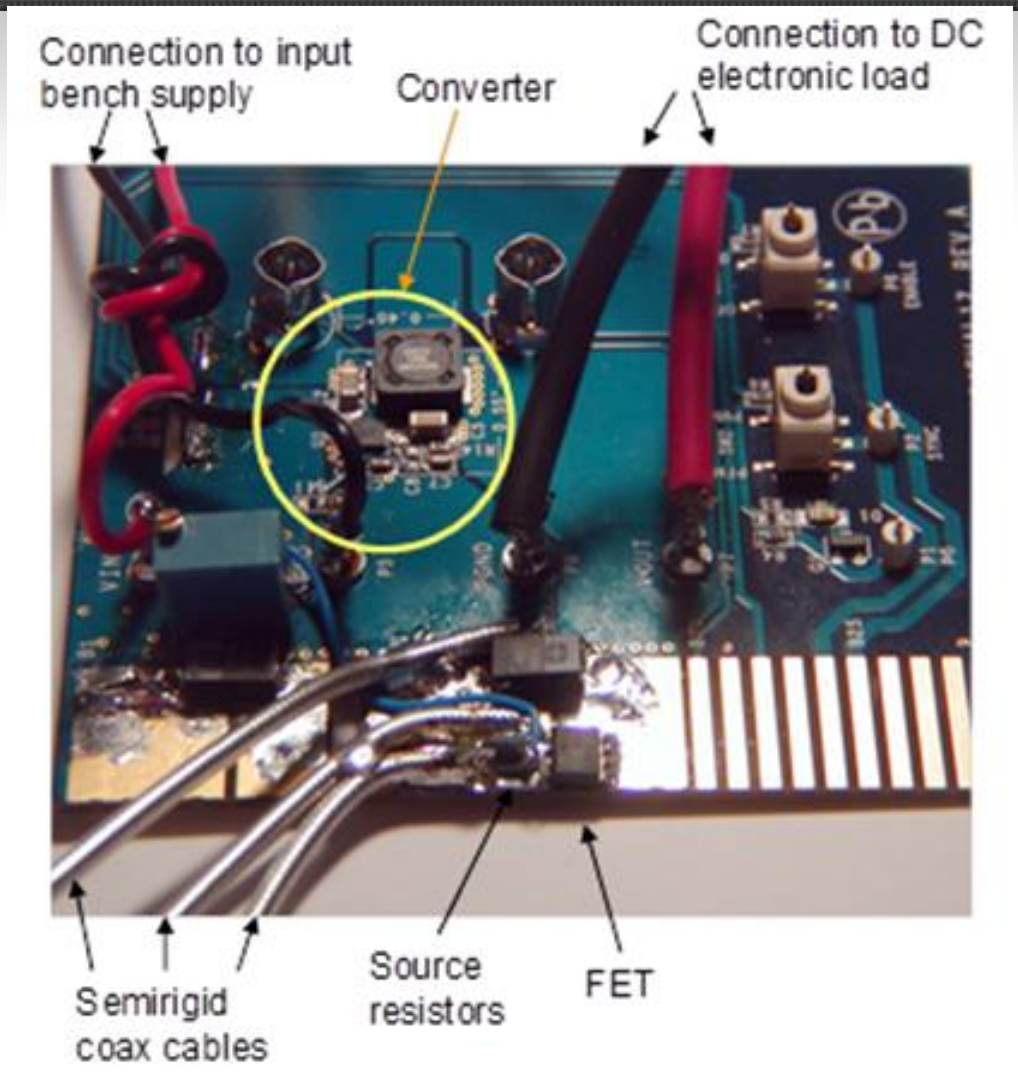


Load Transient Measurement

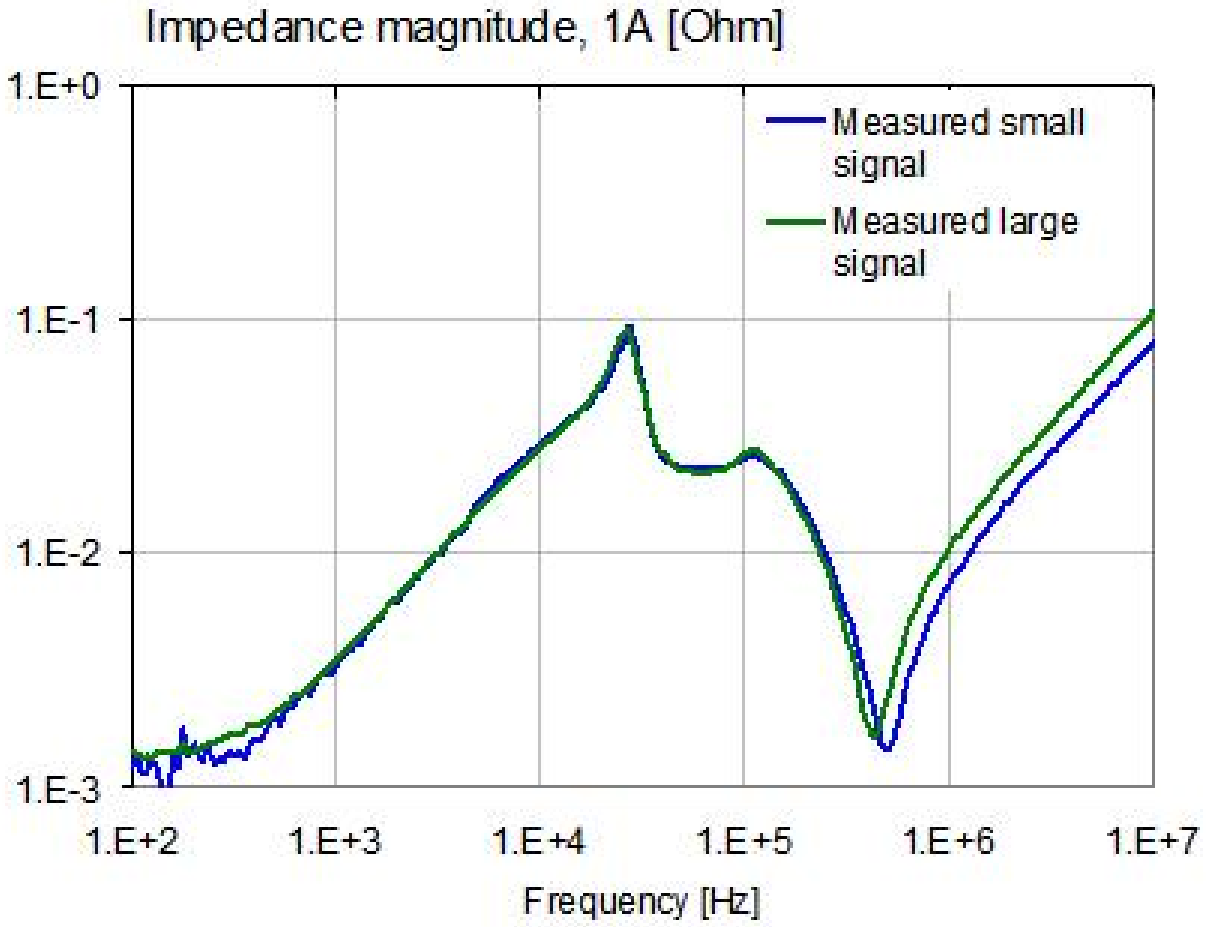




Multi-Purpose Test Setup

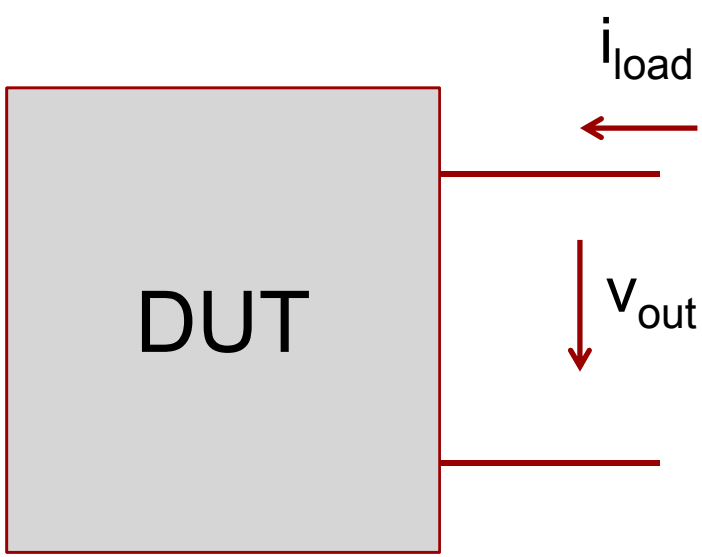


Large-Signal Output Impedance Measurement Setup

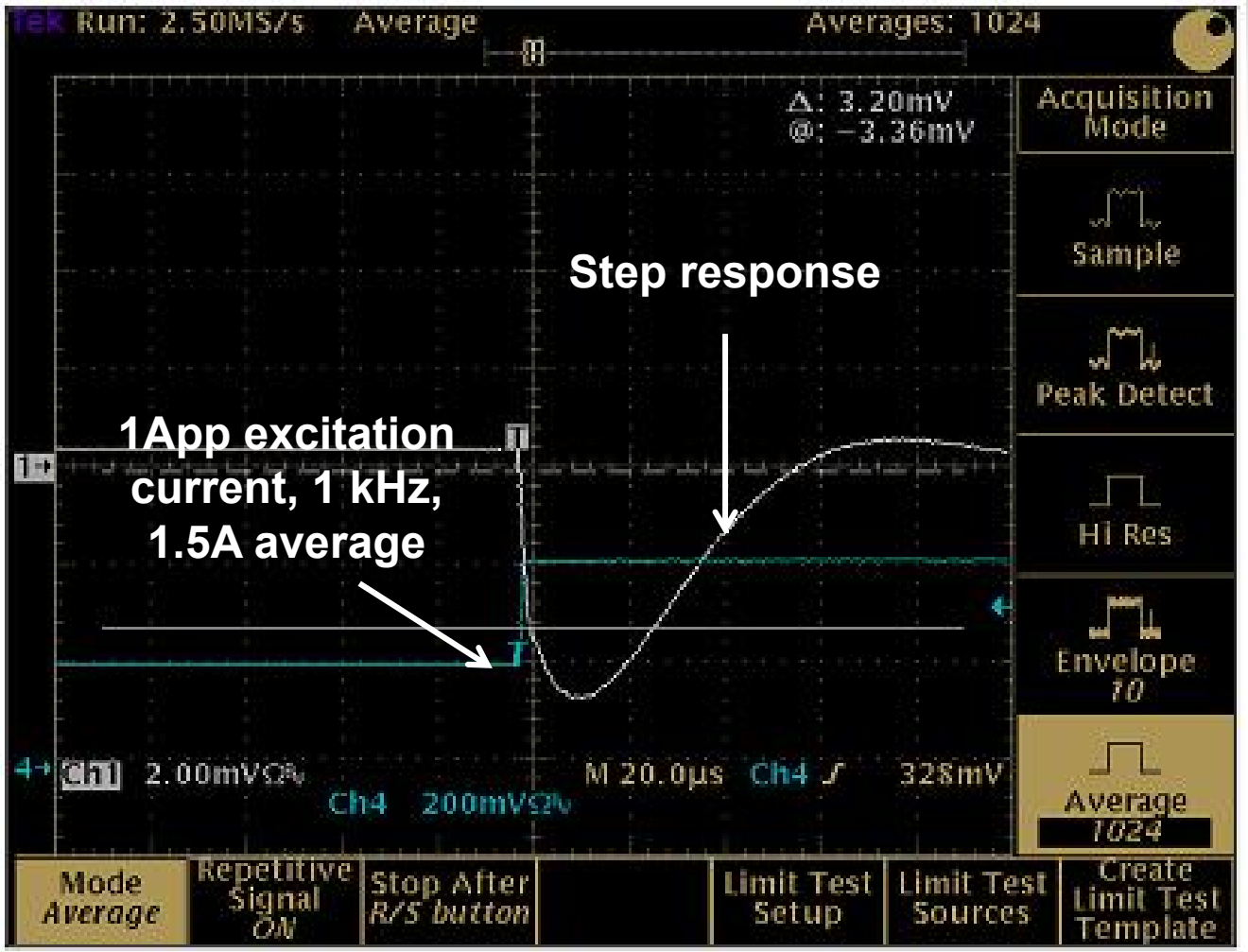


Small-Signal vs. Large-Signal Output Impedance

Output Impedance from Step Response

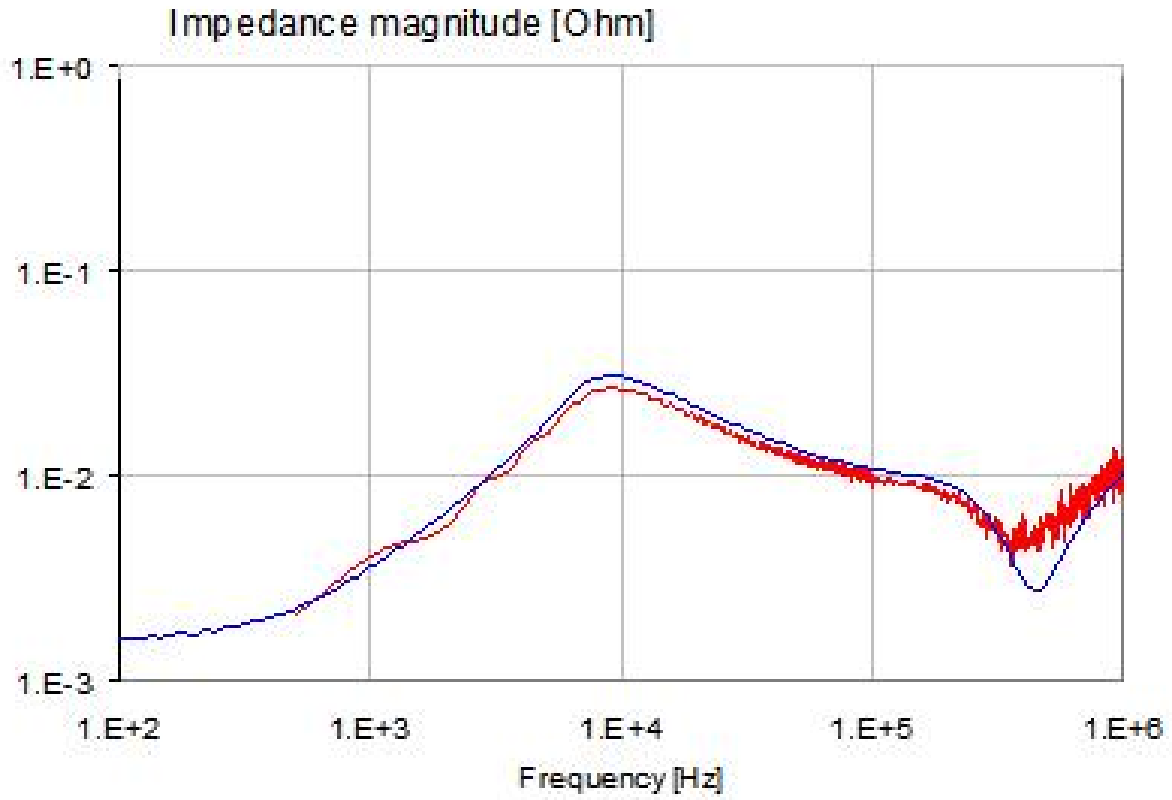


- The noise transfer function is v_{out}/i_{load}
- The Fourier Transform of the transfer function is the Impulse Response
- The Step Response is the integral of the Impulse Response



Step Response

Z_{out} from Step Response



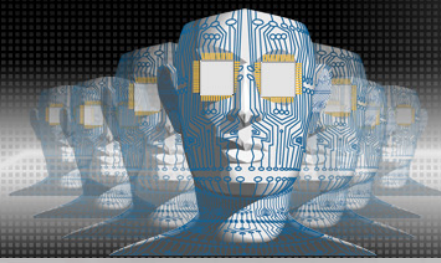
- Blue trace: small-signal Z_{out}
- Red trace: Z_{out} from Step Response

Conclusions

- **For linearized behavior**
  - Dynamic converter parameters can be based on the Gain-Phase function
  - Output impedance is a good measure for dynamic response
  - Output impedance can be measured or simulated by
  - Swept-sine small signal
  - Swept-sine large signal
  - Derivative of the Fourier Transform of the Step Response
  - Source impedance can greatly influence output impedance
  - Output impedance can go above OFF impedance (peaking) for several decades beyond the crossover frequency

Conclusions (continued)

- **Paralleled converter outputs will**
  - Reduce output impedance proportional to the number of phases
  - Not change crossover frequency
- **Nonlinear control can reduce the magnitude of instantaneous transient response**
- **Gain-Phase and output impedance measurements can be achieved with a unified setup**



Part II: Power Filter Network and its Effect on DC-DC Converters

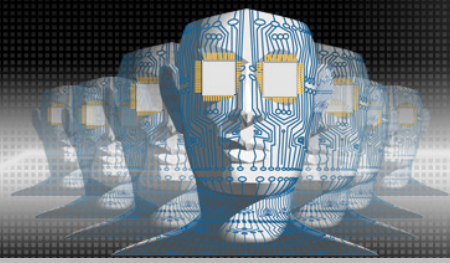
Kendrick Barry Williams, Oracle-America Inc.

Istvan Novak, Oracle-America Inc.

Brandon Howell, Intersil Corporation

Chris Young, Intersil Corporation

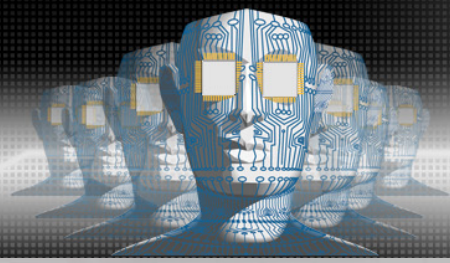
UBM Electronics



Outline

Part II: Power Filter Network and its Effect on DC-DC Converters

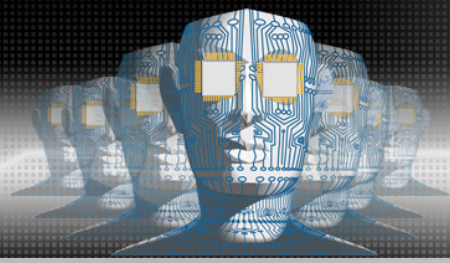
- **I. Introduction and Background Information**
  - DC Converters Introduction
  - Power Filter Introduction
  - DC Converter Specifications
  - Filter Specifications
  - The DC Converter Application
  - Cross-Over Frequency



Outline (continued)

- Power Filter Application
- Filter input impedance, converter looking toward the load
- Filter input impedance, the load looking toward the converter
- Filter Inductor

- **II. Actual Circuit Used and Measurements**
  - Added Bulk Capacitors Removed
- **Summary**



Outline

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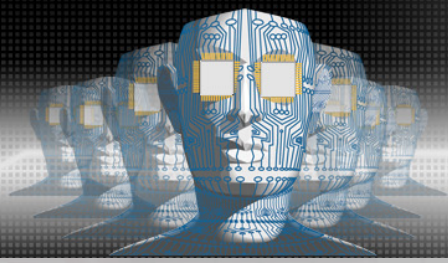
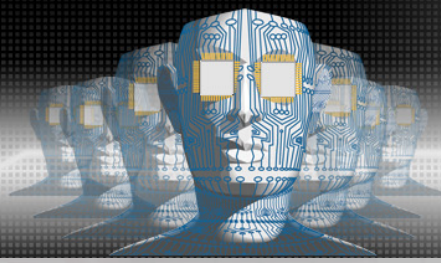


Why Do We Need More Filtering?

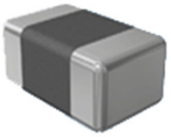
- I/O frequencies are increasing beyond 10Gb/s
- Sensitive circuits need reduced noise levels – less than 5 mV Pk – Pk
- Chips with PLL circuits operating at frequencies of 1 MHz and above



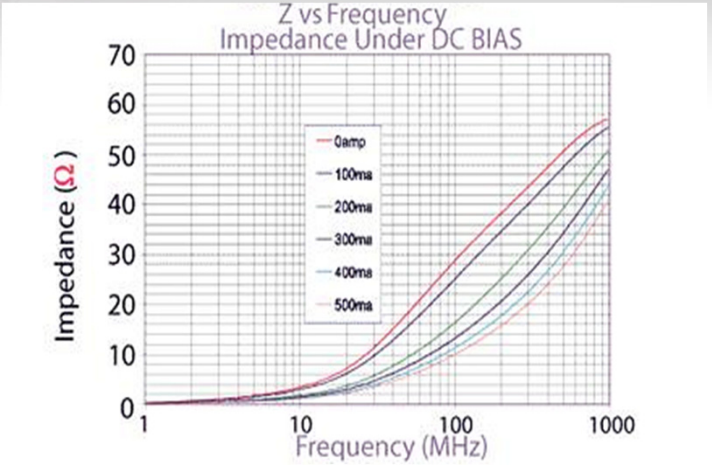
A Brief Survey – What Inductors Were Chosen?

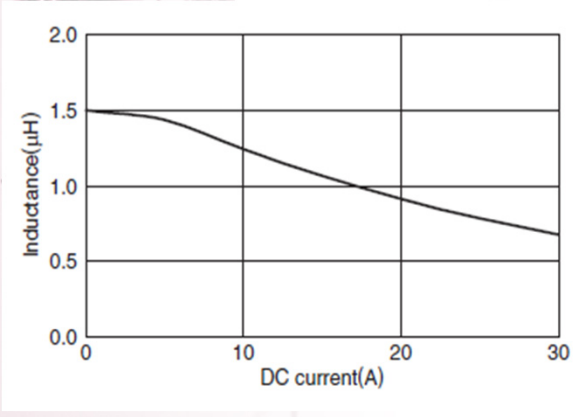
- Ferrite Beads for applications up to 6 Amperes
- Gapped Inductors for larger currents > 6 Amperes
- Need for low resistive loss to keep efficiencies high
- Small Size

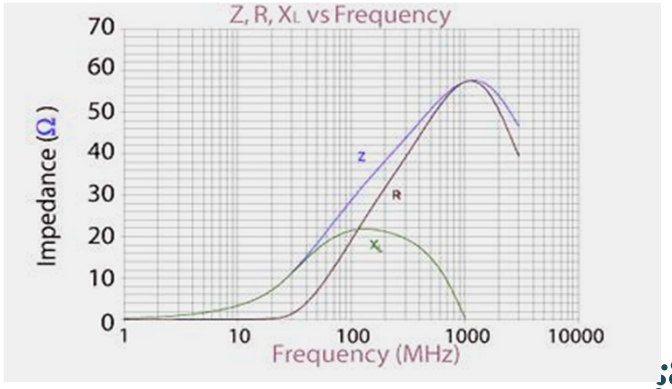
Gapped Inductors



Ferrite Beads







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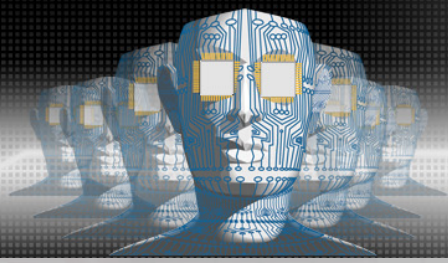


Important Things About Inductors

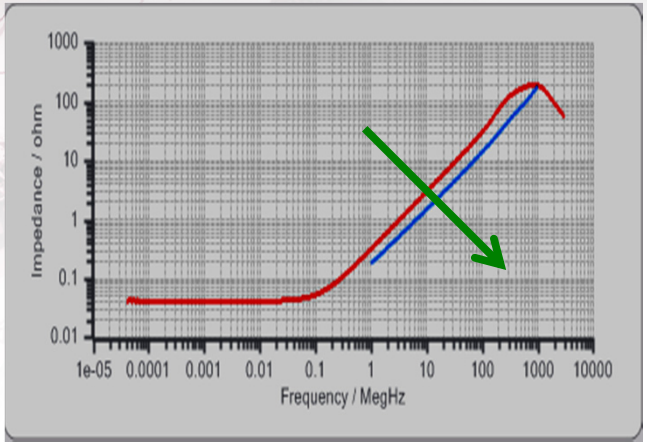
- Signal Inductors are very sensitive to DC bias currents
- Power Line Ferrite Beads

  Resistive value decreases with increasing current

  Inductance decreases with increasing current

  Not all ferrite beads are created equally!

Ferrite Bead DC Bias



Ferrite Bead, 30 Ω
Red, DC Current = 0.0 A
Blue, DC Current = 1.8 A

The effects of DC bias is dependent on the materials used in the manufacturing of the product

Not all suppliers provide DC Bias Information!!

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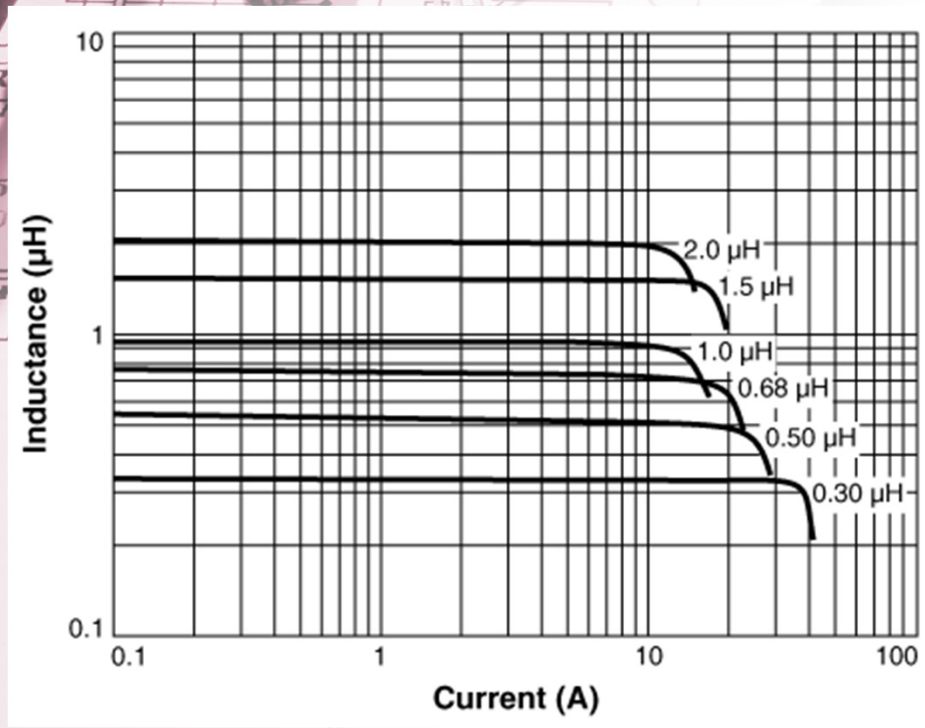
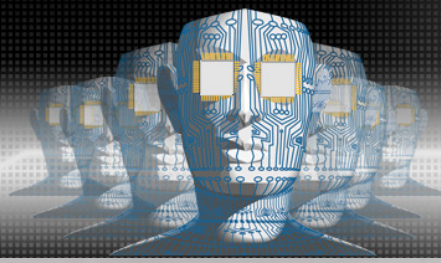
We could of course use a big power inductor !!



The larger inductors behave more in line with our expectations



Power Supplies – Where is the Industry going?

Integrated Power Solutions

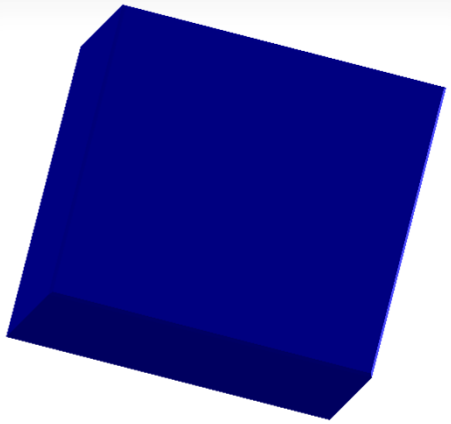
- FETs and Inductor integrated with controller
- Compensation loops integrated with the package
- User adds voltage divider to set output voltage

Digital Control Systems

- PID Controllers offer a means to alter the behavior through firmware instead of added components.

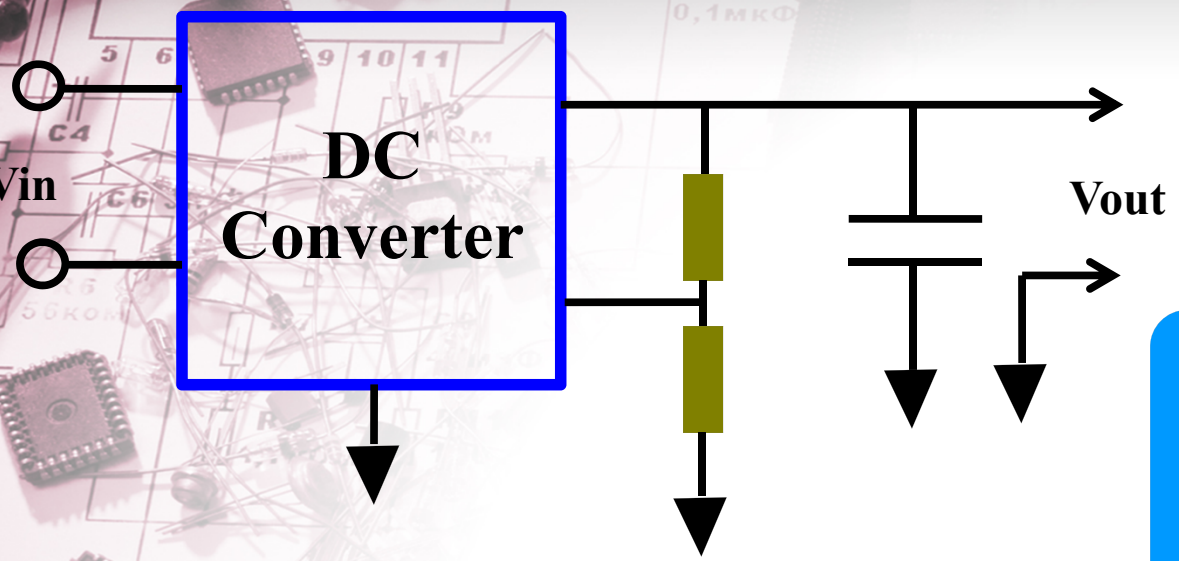
DC Converters

Typical Buck Regulator
Non – Isolated 10 Amp
15 mm x 15 mm x 3.5 mm



Fully Integrated, PID Control

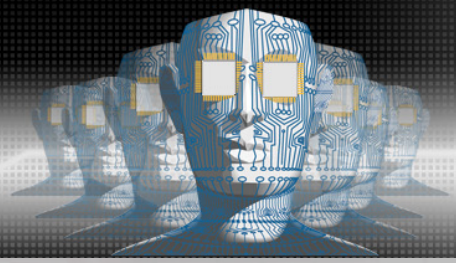
What information do we need to know about this regulator?



Converter Consists Of

(2) Power FETs
(1) Power Inductor
(1) Digital Controller

Basic DC Converter Implementation



The converter vendor does provide information about:

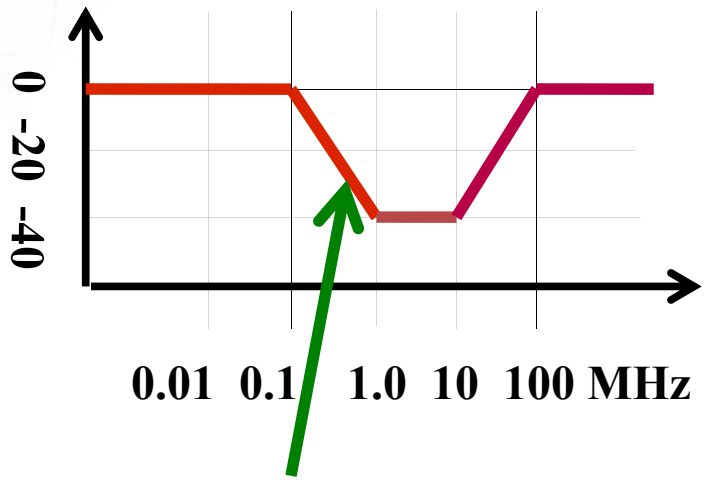
- Input Voltage Range
- Output Voltage Range
- Output Current
- Switching Frequency
- Line and Load Regulation
- Set Point Accuracy

The converter vendor does not provide information about:

- Type of Controller:
  - Voltage Mode
  - Current Mode
- Bandwidth of Loop Compensation
- Cross – Over Frequency
- Output Inductor & DCR

Filter Requirements, What are they?

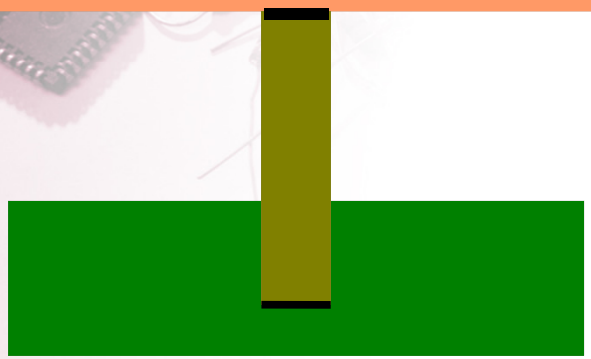
Vendors in general don't provide information on what the max noise voltage that can be tolerated, nor the frequency range needed



Filter Requirements – General Rule of Thumb

Remember!!!!

General Rules of Thumb make certain assumptions that may or may not be true!



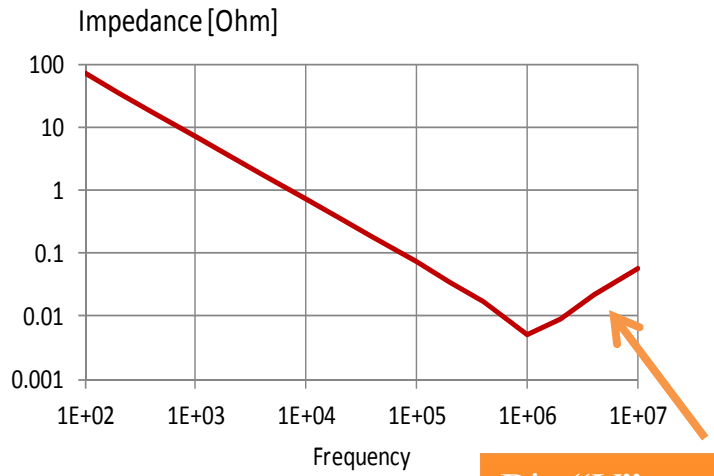
Assumed Filter Requirements

Assumptions

1. **Nominal Noise Voltage of 1mV**
2. **Attenuation -20dB/decade**
3. **Corner Frequency 100 KHz And 100 MHz**

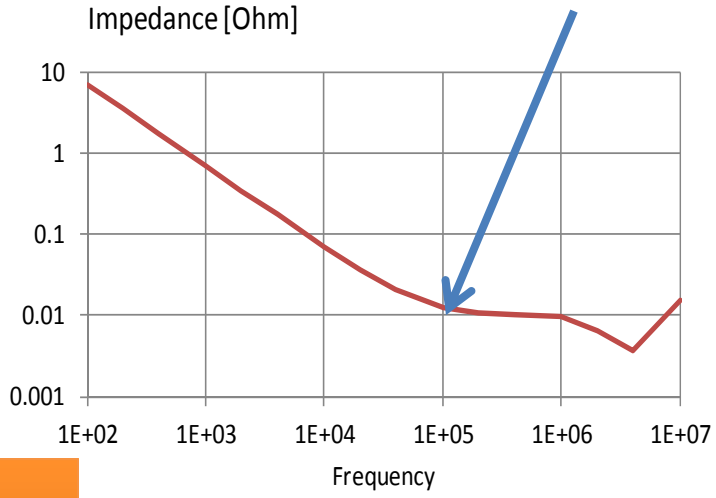
DC Converter—PDN

Big "V" PDN



Big "V" resulting from usage of many of the same capacitor

Flat Z PDN



Flat Region resulting from several different types of capacitors

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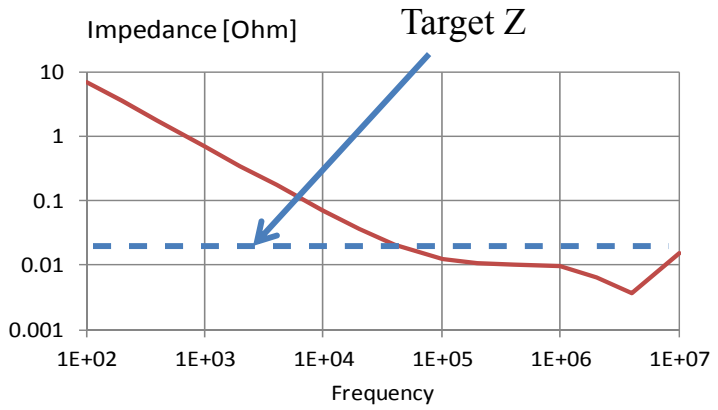
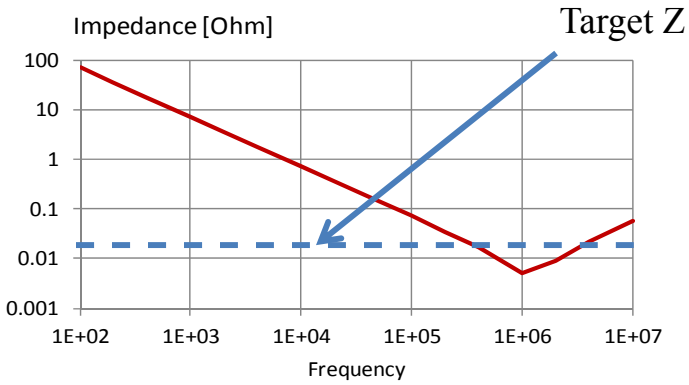
DC Converter — Target Impedance

Example

Vout = 1.800 V
Iout = 4.000 A
Set Point Accuracy = 18 mV
Max deviation = 90 mV (5%)
Inductor Ripple Current = 1.200 A





Allowances

90 mV – 18 mV = 72 mV
Ripple Voltage = 37.5% or 27 mV

Target Z = 27 mV/ 1.200A = 22.5 mΩ

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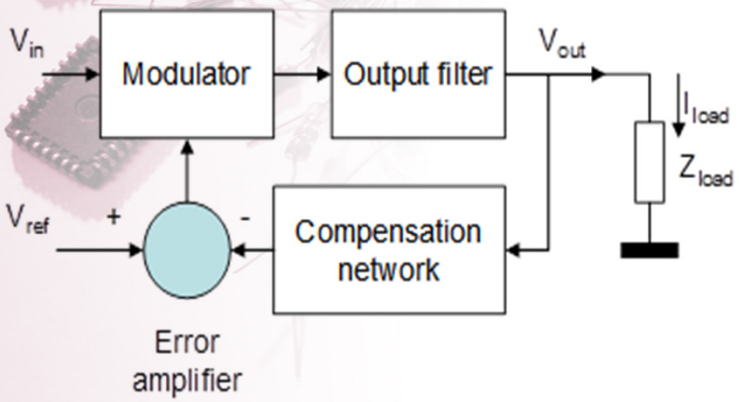
DC Converter Loop Cross – Over Frequency Problem

Issues:

An integrated regulator.
No information about the internal inductor.
No information on the type of controller.
No information about the loop compensation



Solutions:

Ask the vendor or….
Assume both Voltage Mode and Current Mode Controller

Estimating The Cross – Over Frequency For a Current Mode Controller

Estimated Corner Frequencies

$F_{c1} = 1 / (\omega R_{load} C_{bulk})$

$F_{c2} = 1 / (\omega R_{ESR} C_{bulk})$

Estimated Error Amplifier Gain

0 dB @ 1 MHz

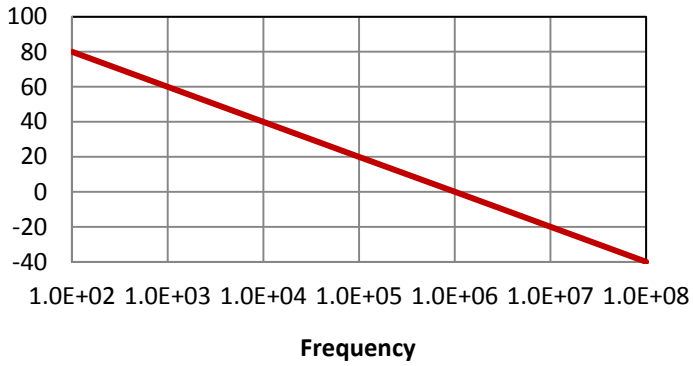
+ 120 dB @ 1 Hz.

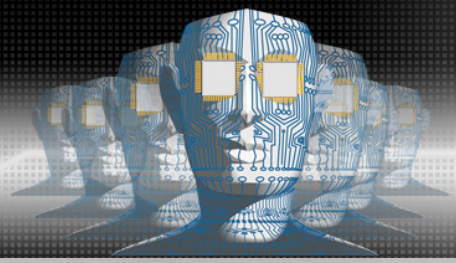
Estimated Gain Needed

Gain Needed $\sim 10^{((120 - G) / 20)}$

Where $G = 20\text{Log}(V_{out} / V_{ripple})$

Error Amp Gain (dB)

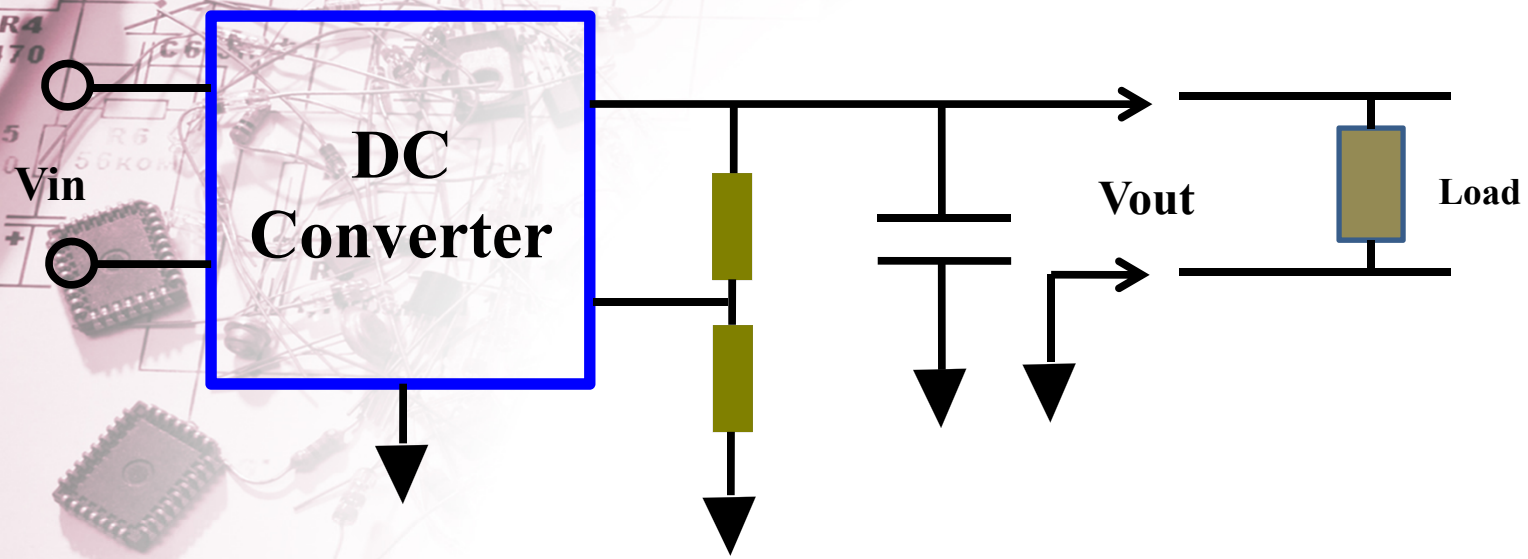




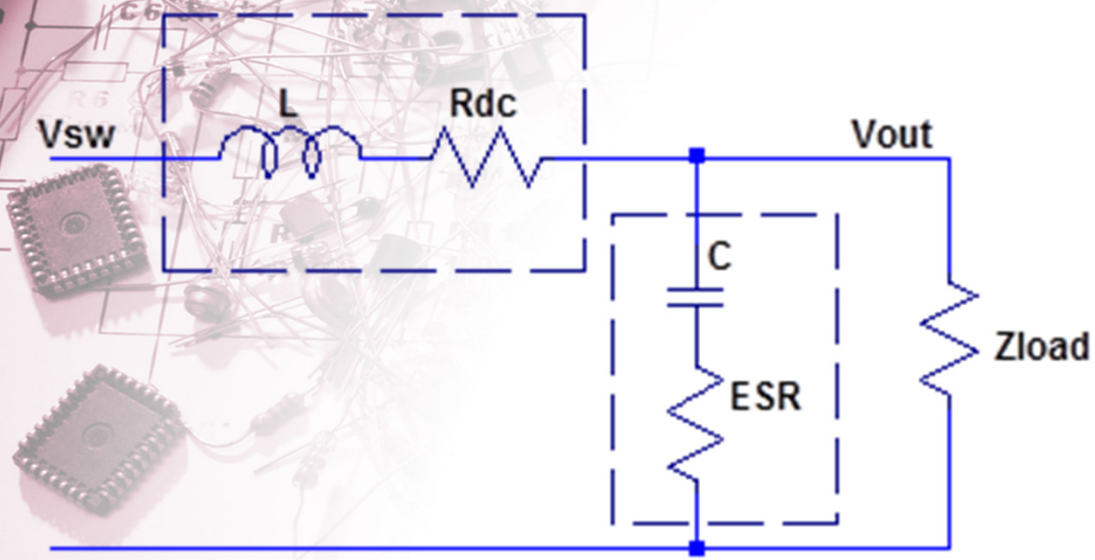
Power Filter Application – What is it that we need to Accomplish?

- Just as in Signal Integrity work, we need to match the load to the source.
- We also must match the source to the load.
- We need to have sufficient attenuation to meet the requirement of the target device, without gain.
- We shall not cause instability of the regulator with the additional filter.

Matching the Source to the Load



What the Regulator Will See With a Filter



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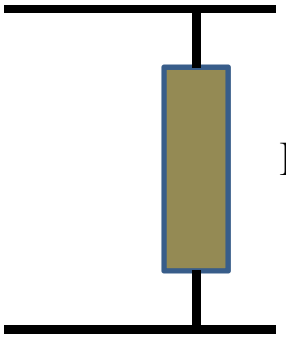
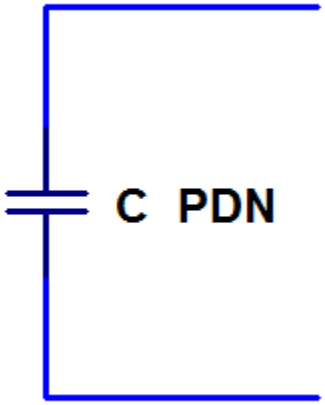
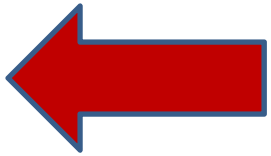


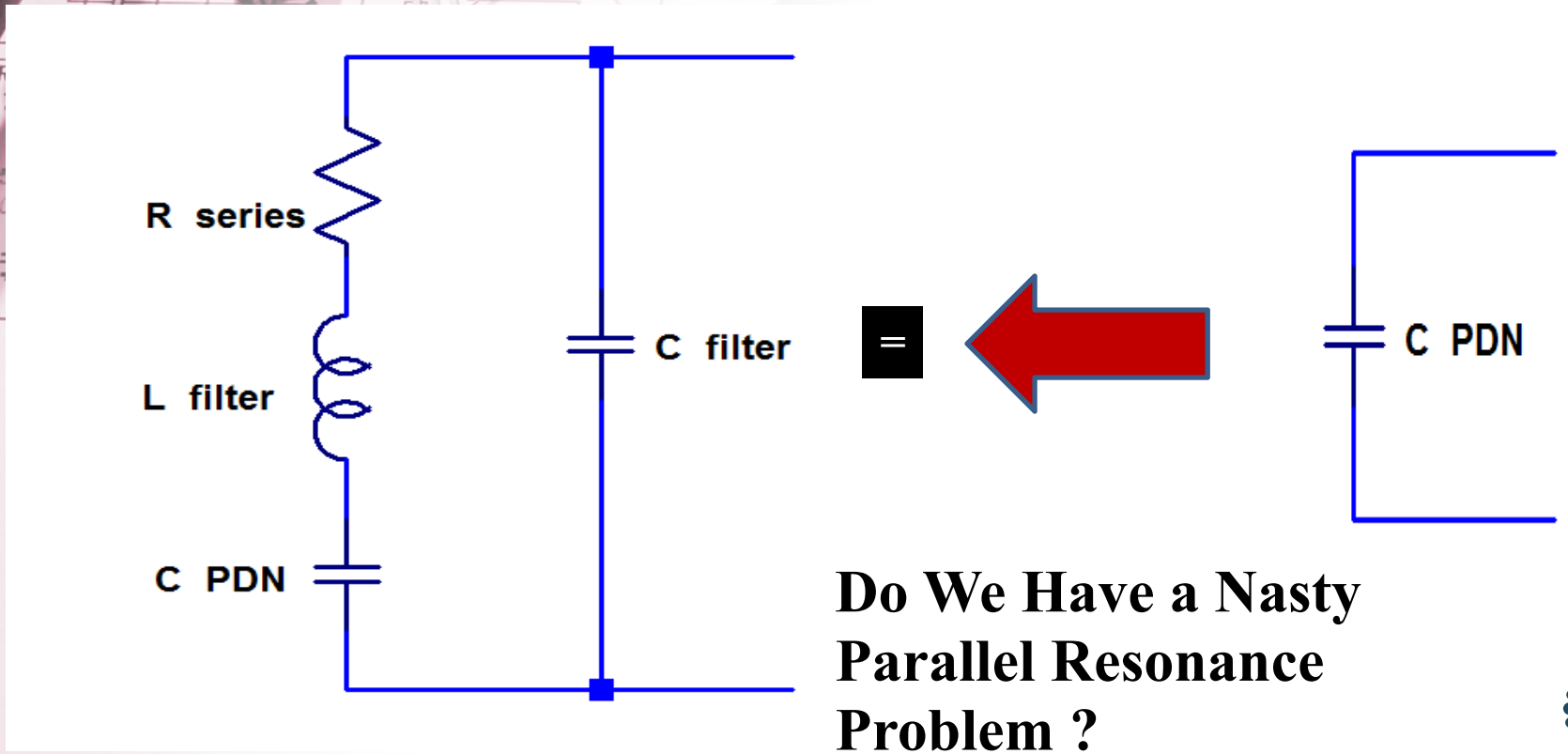
What Will The Load See?





The Load Sees Just the PDN

What The Load Sees With A Filter



Do We Have a Nasty Parallel Resonance Problem ?

Parallel Resonance – Defining Its Value

Isn't its frequency just …..

$$Fr = \frac{1}{\omega\sqrt{LC}}$$

Actually, it is more than that ….

$$Fr = \frac{1}{\omega\sqrt{LC}}\sqrt{1 - \frac{CR^2}{L}}$$

And if the radical is set to "0", then there is no resonance!!

Suggesting that …

$$\frac{1}{Q} = RYo$$

Outline (continued)

- Power Filter Application
- Forward Impedance, converter looking toward the load
- Reverse Impedance, the load looking toward the converter
- Stability Analysis
- **II. Actual Circuit Used and Measurements**
  - Added Bulk Capacitors Removed
- **Summary**

DESIGN EXAMPLE -- 1

Design Requirements # 1:

Ripple and Noise Voltage …… 1 mV @ Load
Attenuation Profile
- -20dB starting at 100 KHz
- +20 dB starting at 10 MHz

Ripple Voltage from regulator …. .27 mV
Target Impedance ……. 22.5 mΩ
PDN – Flat Impedance Design
- (1) 220 µF, Poly. Tant. ESR = 25 mΩ
- (1) 22 µF, Ceramic, 10 V, X5R ESR = 4 mΩ
- (1) 2.2 µF, Ceramic, 10 V, X5R ESR = 10 mΩ

DESIGN EXAMPLE -- 2

Design Requirements # 2:

Ripple and Noise Voltage …… 1 mV @ Load
Attenuation Profile
- -20dB starting at 100 KHz
- +20 dB starting at 10 MHz

Ripple Voltage from regulator …. .27 mV
Target Impedance ……. 22.5 mΩ
PDN – Big "V"
- (1) 22 µF, Ceramic, 10 V, X5R ESR = 4 mΩ

DESIGN EXAMPLE -- 3

Regulator Specifications:

1. Switching Frequency…… 1 MHz
2. Controller Type ….. Current Mode (Asked Vendor)
3. Set Voltage ….. 1.800 V
4. Output Current …. 4.0 A
5. Minimum Bulk Capacitance …22 µF

Error Amp Cross – Over Frequency Estimation

Gain Needed = 20Log(Vout /V ripple) = 32.64 dB

$F_{c1} = 1/(2\pi(0.45)(22\ \mu F)) = 16.1$ KHz

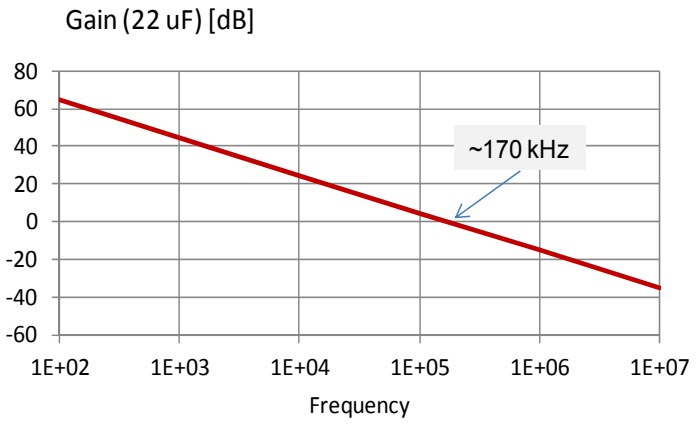
$F_{c2} = 1/(2\pi(0.004)(22\ \mu F)) = 1.81$ MHz

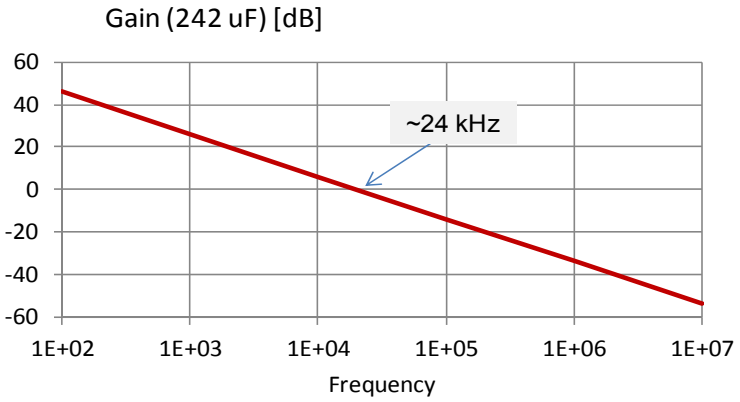
$F_{0dB} = ((F_{c1})(F_{c2}))^{0.5} = 170$ KHz

$F_{c1} = 1/(2\pi(0.45)(242\ \mu F)) = 1462$ Hz

$F_{c2} = 1/(2\pi(0.002)(242\ \mu F)) = 329$ KHz

$F_{0dB} = ((F_{c1})(F_{c2}))^{0.5} = 22$ KHz





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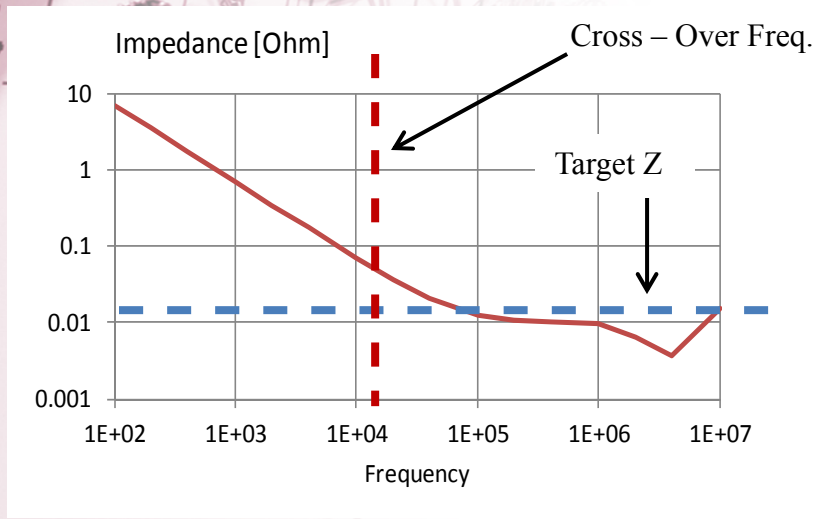
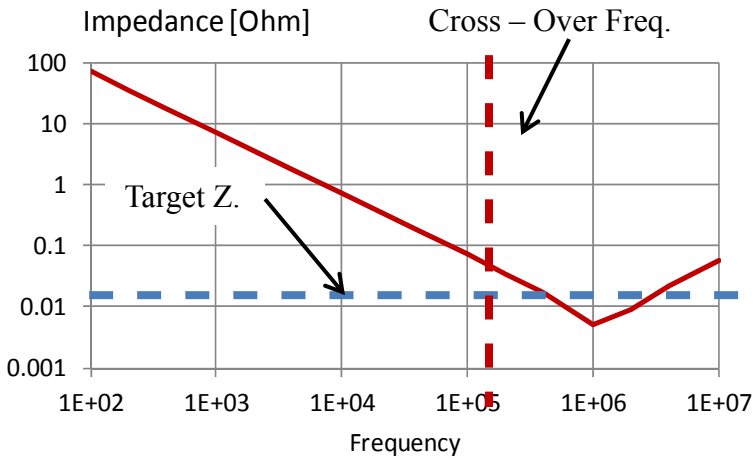
Regulator OFF, Quick Estimates of PDN Impedance, Cross – Over Frequency, and Target Impedance

Case #1 Bulk C = 242 µF



Case #2 Bulk C = 22 µF



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Filter Design

Looking From Converter to Load

Attenuation Needed is base on -20 dB/decade

Ripple Voltage = 27 mV,
(Maximum Noise Voltage)(0.5)/Ripple Voltage = -34.6 dB

Specified attenuation to occur at 1 MHZ; therefore, ……
Corner Frequency = (1 MHz)($10^{(Attenuation/20)}$) = 13KHz

Initial value of Inductance = Target Z/(ω F_{corner}) = 274 nH

Initial value of Capacitance = Inductance/(Target Z)^2 = 540 µF

Filter Design Continued

Our survey indicated a need for small parts.

With an inductance value of 274 nH in a ferrite bead rated for our maximum current of 4 Amps is tough to get.

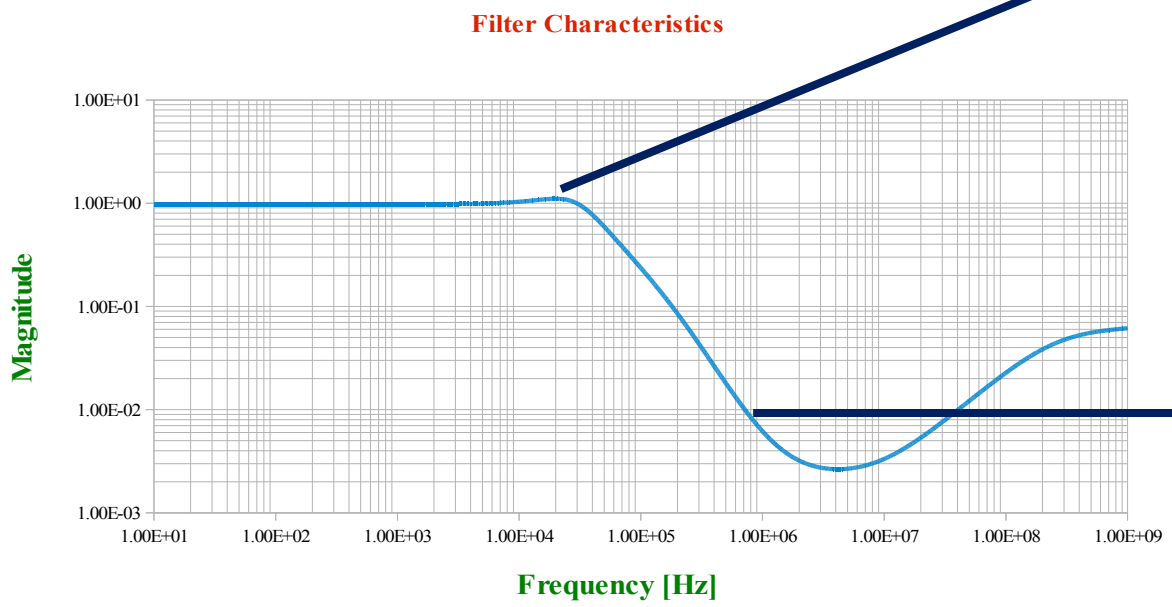
Lowered the value of inductance to 120 nH which is readily available and is small, 0603 package.

In lowering the inductance, the capacitance needs to be valuated, the new value based on the Z_o of the filter suggests a value of 270 µF,
220 µF has been selected, a poly Tantalum, ESR = 25 mΩ.

To extend the bandwidth, (2) 22 µF ceramic capacitors were added.

How well did we do?

Met the corner frequency requirement



Virtually NO Gain!

Met the Attenuation factor at 1 MHz

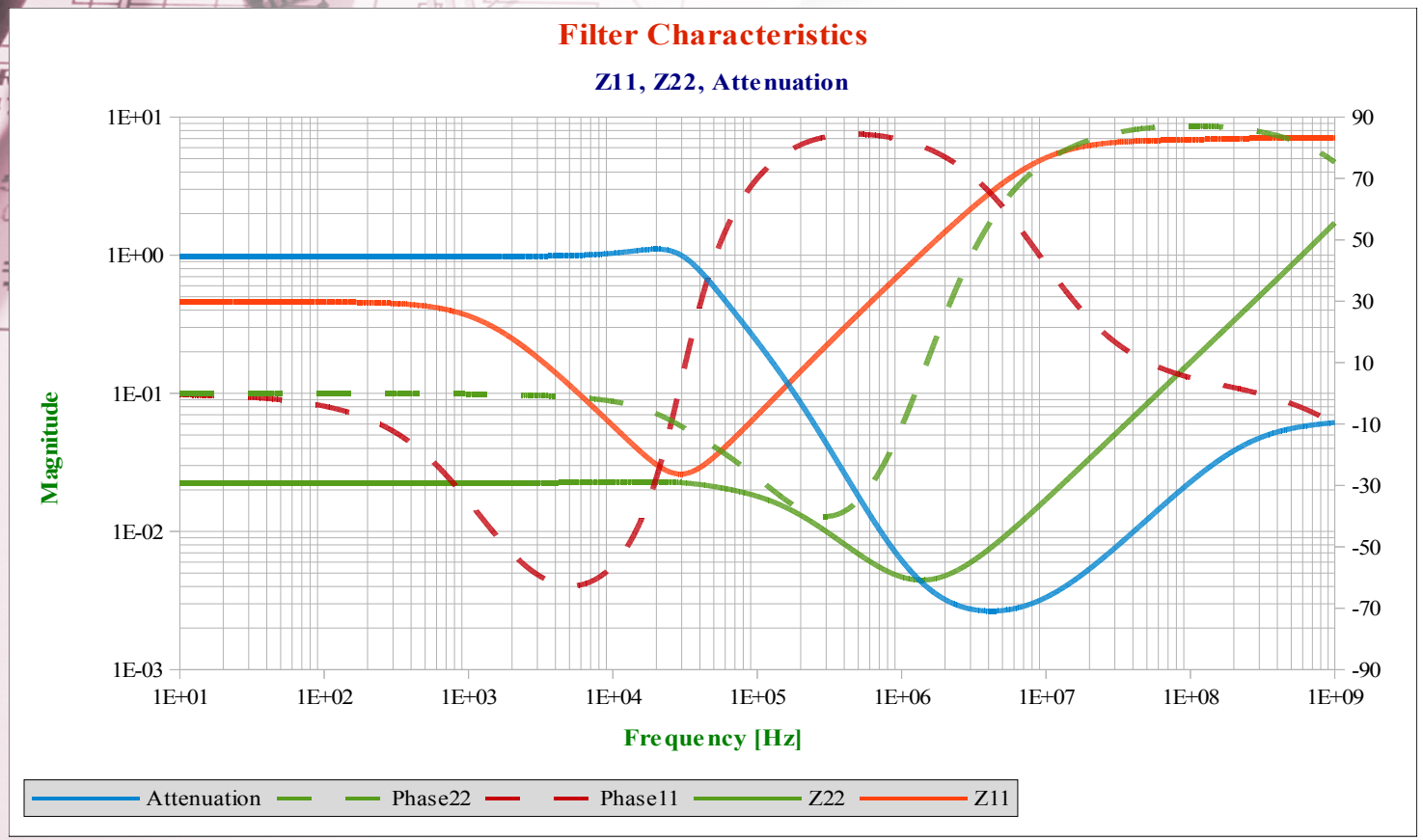
Filter Design Continued

From The Load Side, Looking Toward The Regulator

The requirement is that the load should see the PDN at the regulator, this value is 22.5 mΩ. We chose a 25 mΩ poly tantalum capacitor which is sufficient in terms of the ESR of the capacitor.

However, the tantalum capacitor turns inductive at about 1 MHz, it needs to be countered with ceramic capacitors that will extend the attenuation bandwidth towards 10 MHz.

Total Design Solution



Green, looking from the load to the converter.

Red, looking from the converter to the load

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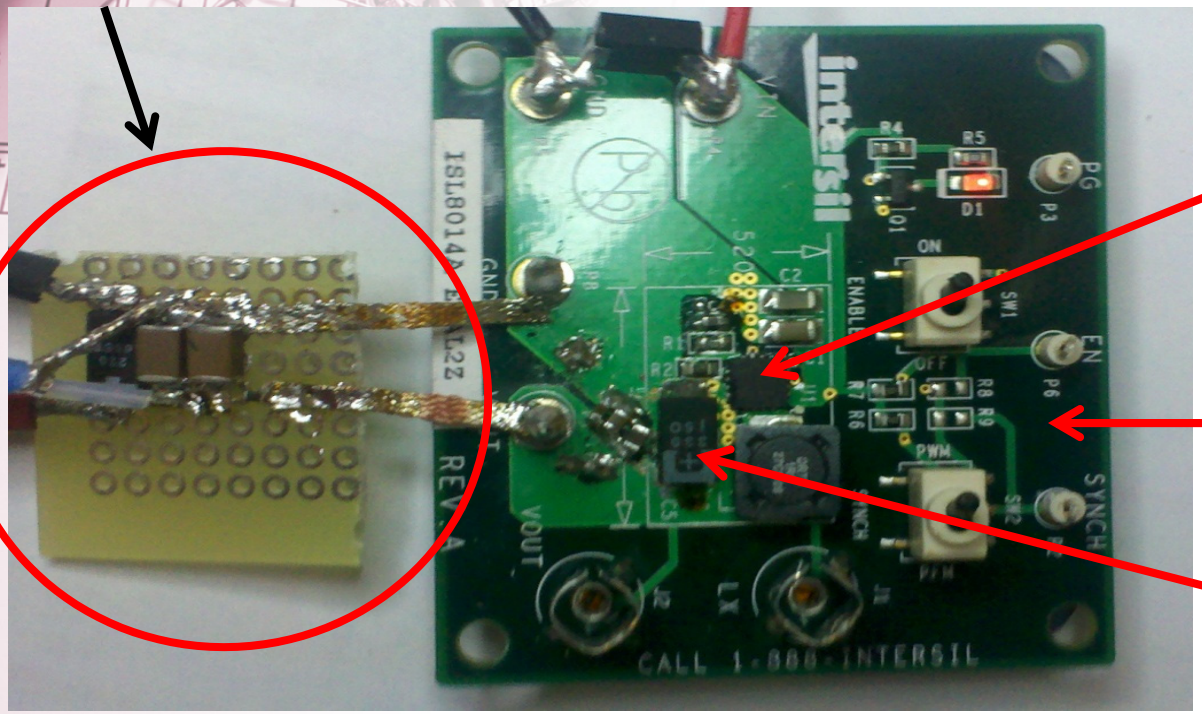
Measurements

Measurements in the following section, were done with the filter added

Added Filter



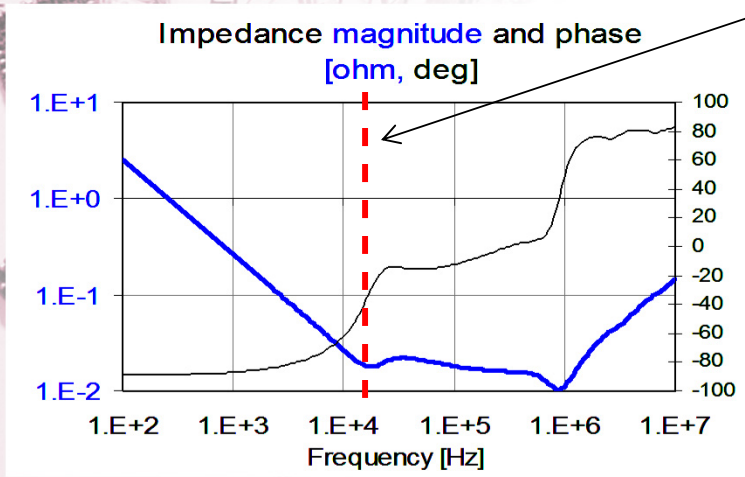
Current Mode Controller

Regulator Evaluation Board

Bulk Capacitance added

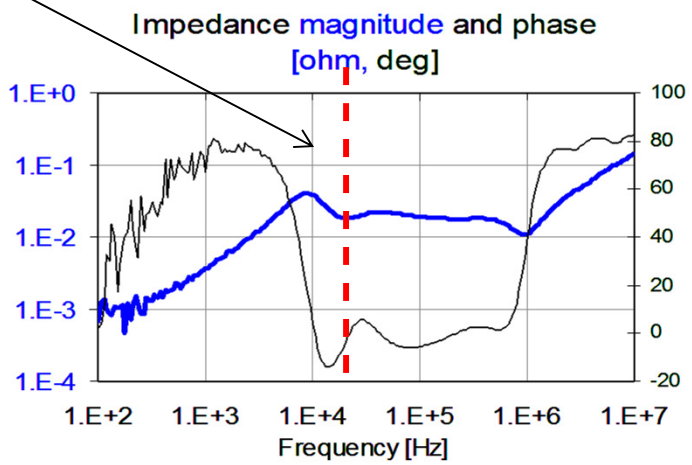
Measured Output PDN – Case # 1

Regulator OFF



Regulator ON, 0 Ampere Load

Cross – Over Frequency Regulator



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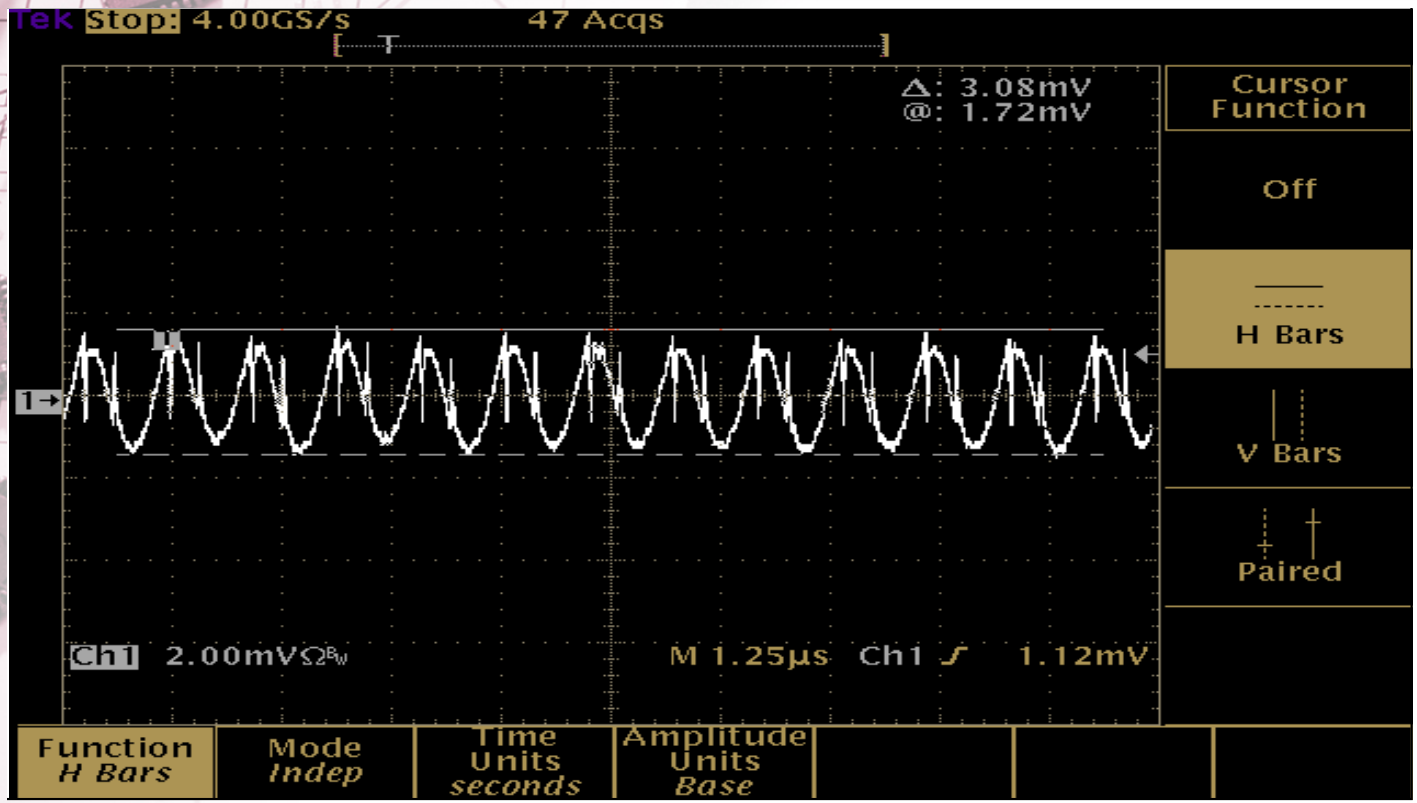
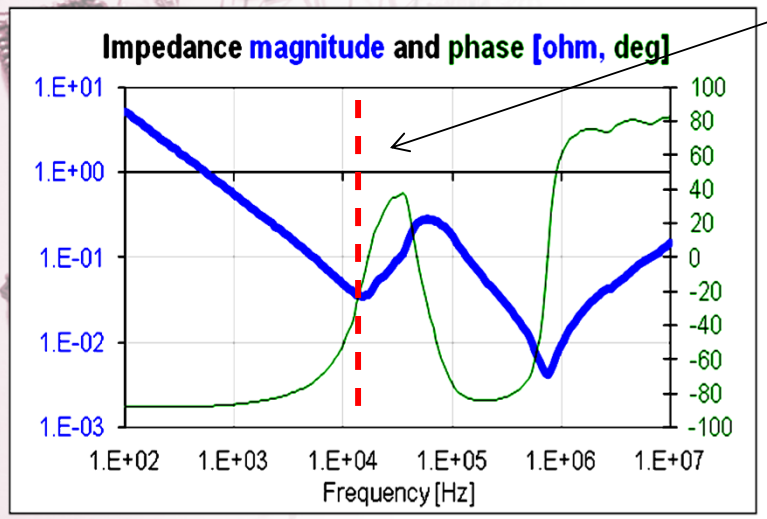
Measured Ripple Voltage



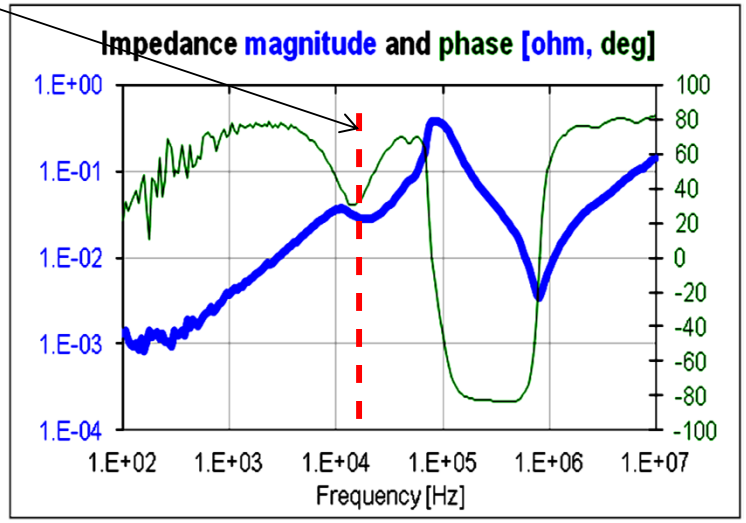
Measured Output PDN – Case # 2

Regulator OFF

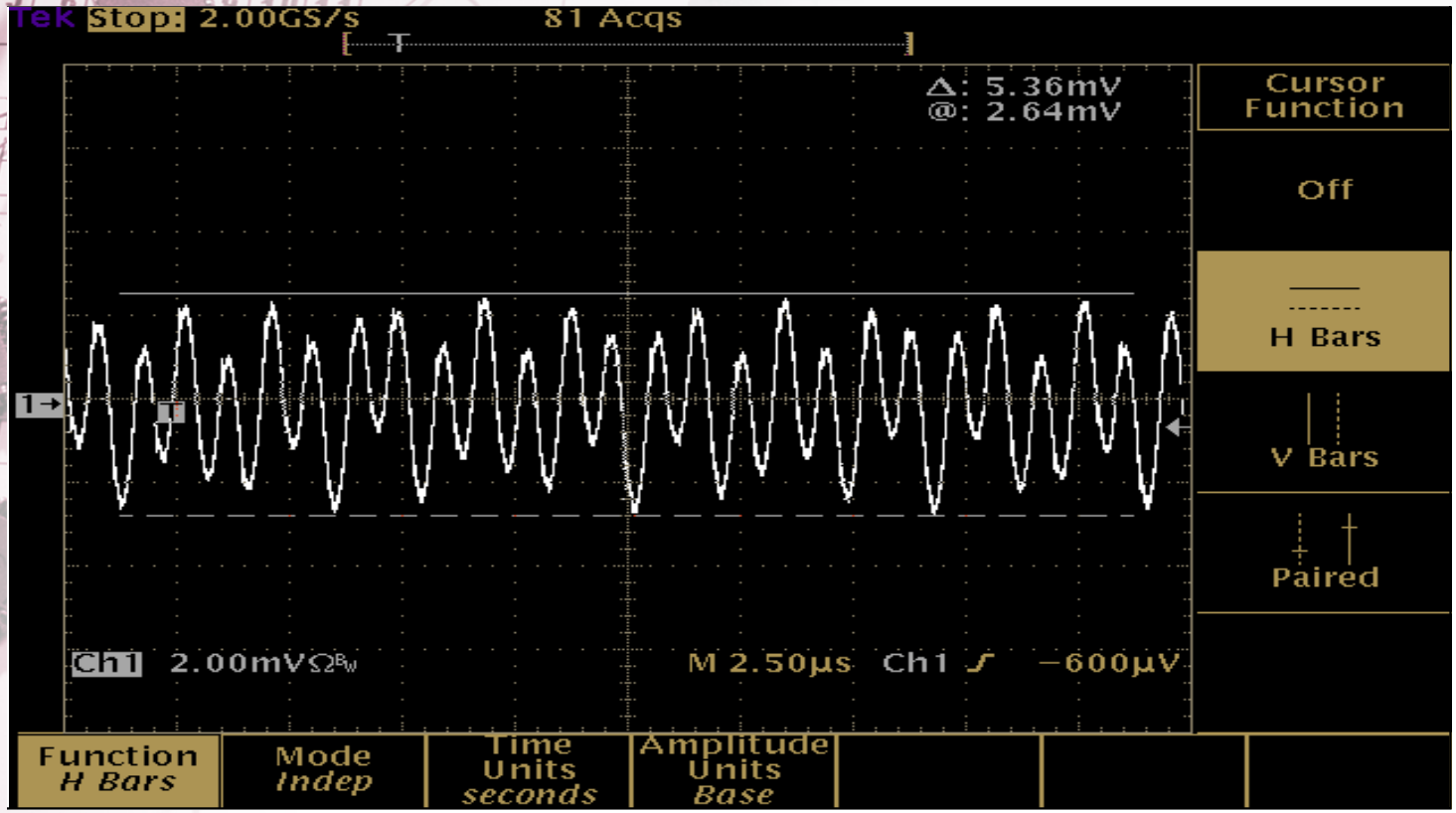


Regulator ON, 0 Ampere Load

Cross – Over Frequency Regulator

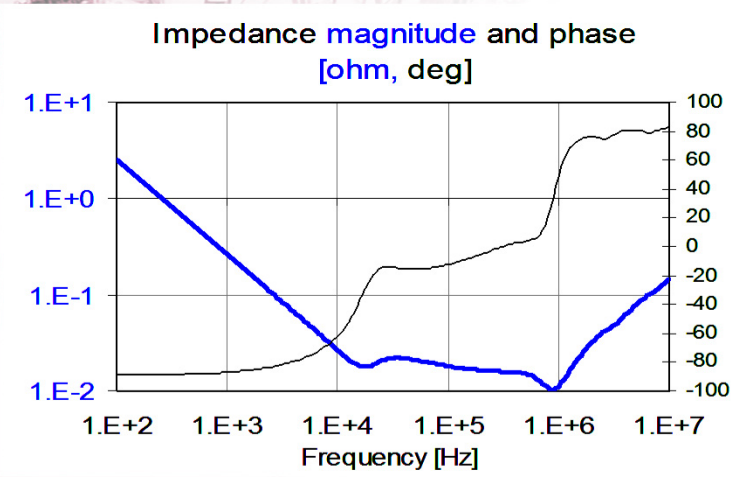


Measured Ripple Voltage Case #2

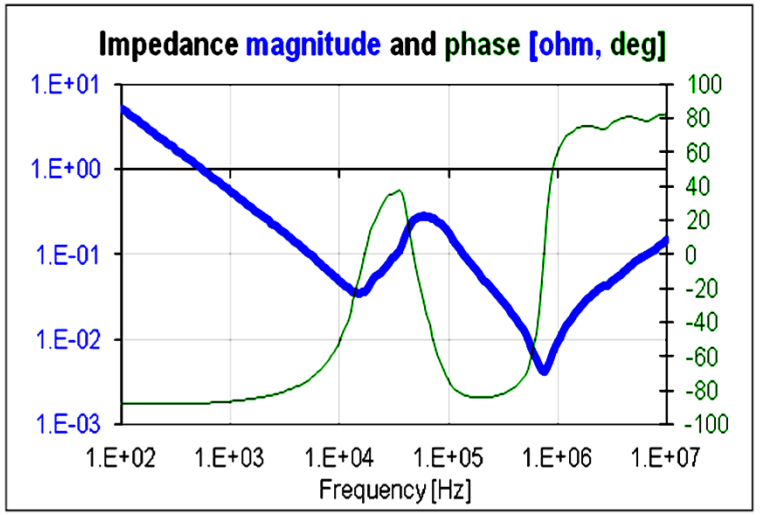


Comparison Of Measured Output PDN Case # 1 & # 2

Regulator OFF, Case # 1

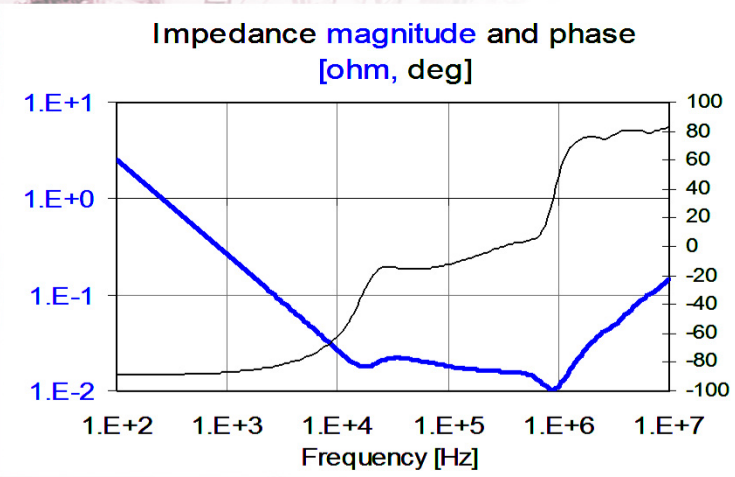


Regulator OFF, Case # 2

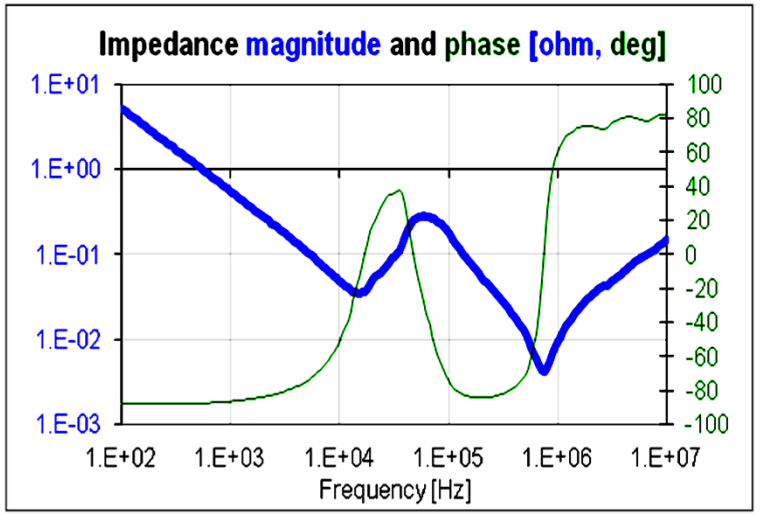


Comparison Of Measured Output PDN Case # 1 & # 2

Regulator OFF, Case # 1

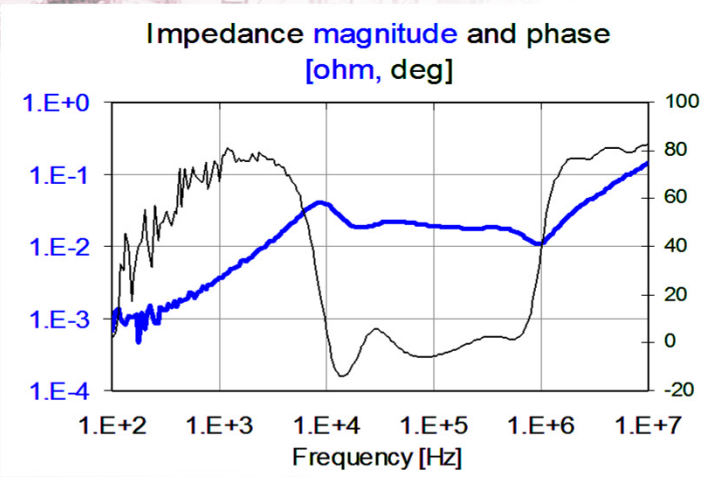


Regulator OFF, Case # 2

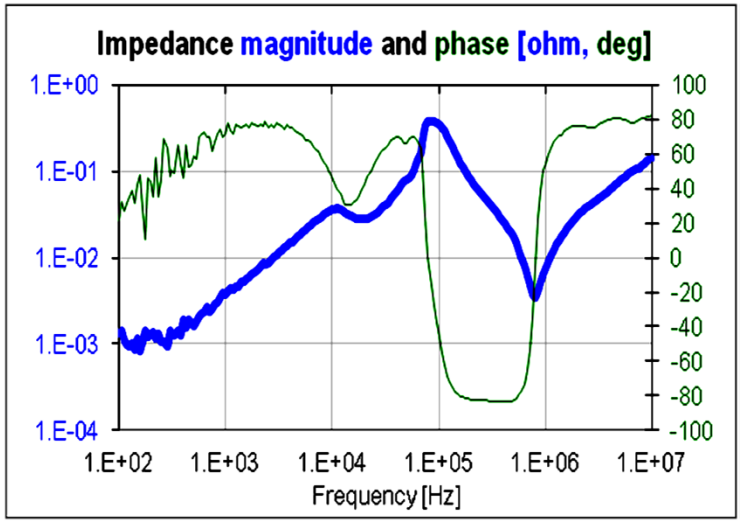


Comparison Of Measured Output PDN Case # 1 & # 2

Regulator ON, 0 Ampere, Case # 1



Regulator ON, 0 Ampere, Case # 2



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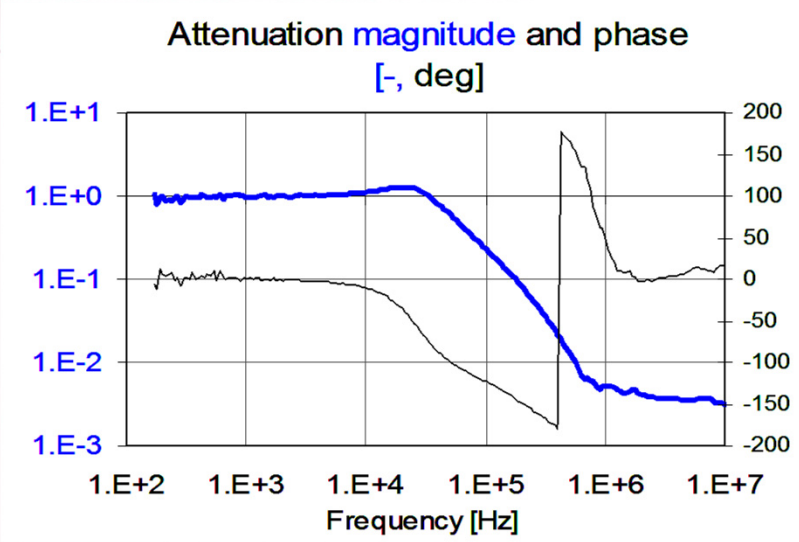
Attenuation Measurements

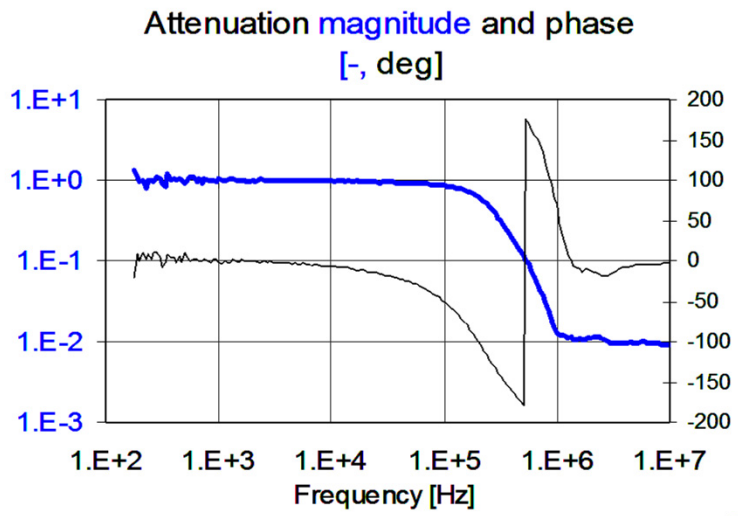
Case # 1, 0 Ampere Load

Filter appears to have a slight lift, and the corner frequency is about 30 KHz, somewhat higher than simulation results.



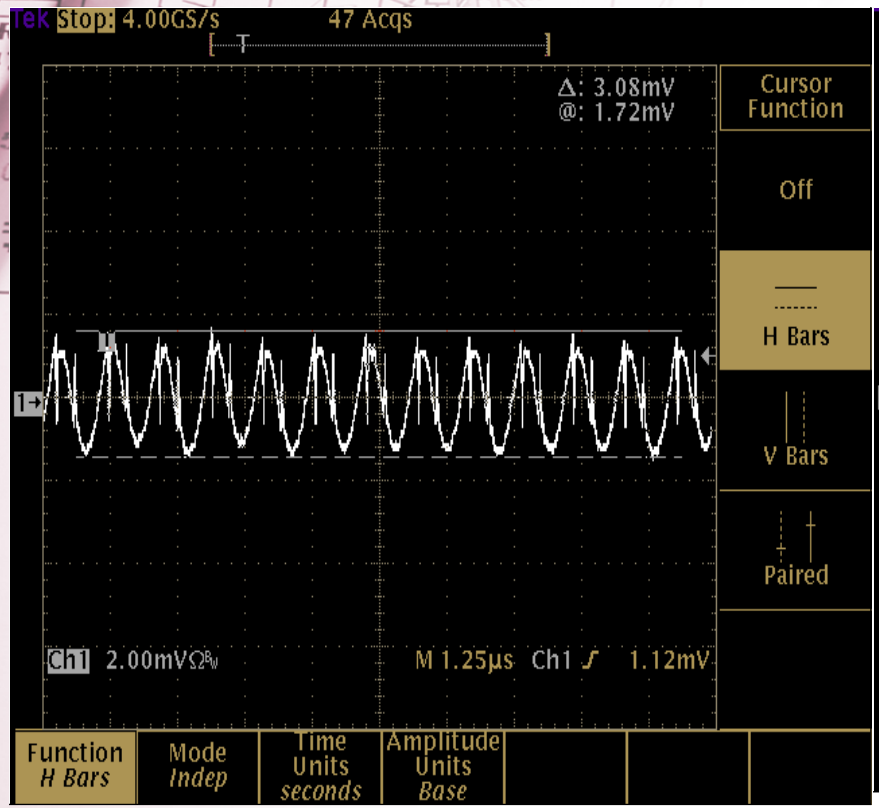
Case # 1, 4 Ampere Load

Filter Inductance appears to have dropped by a factor of about 4, shows that the ferrite bead is affected by DC bias current.

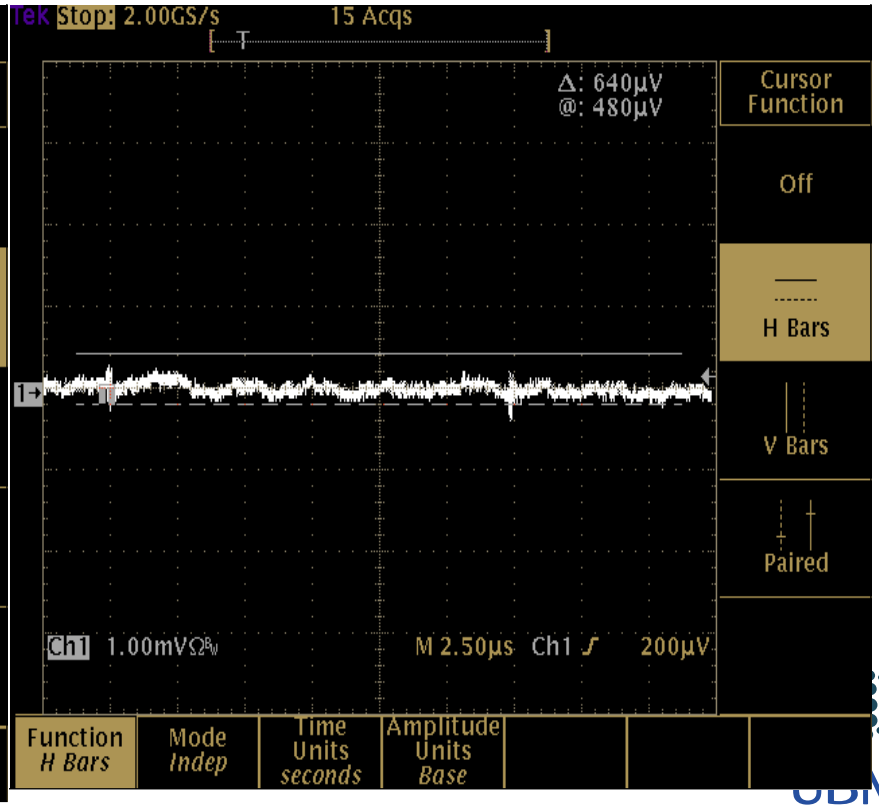


Measured Ripple Voltage Before /After the Filter, 4 Amp Load

Ripple Voltage Before Filter



Ripple Voltage After Filter



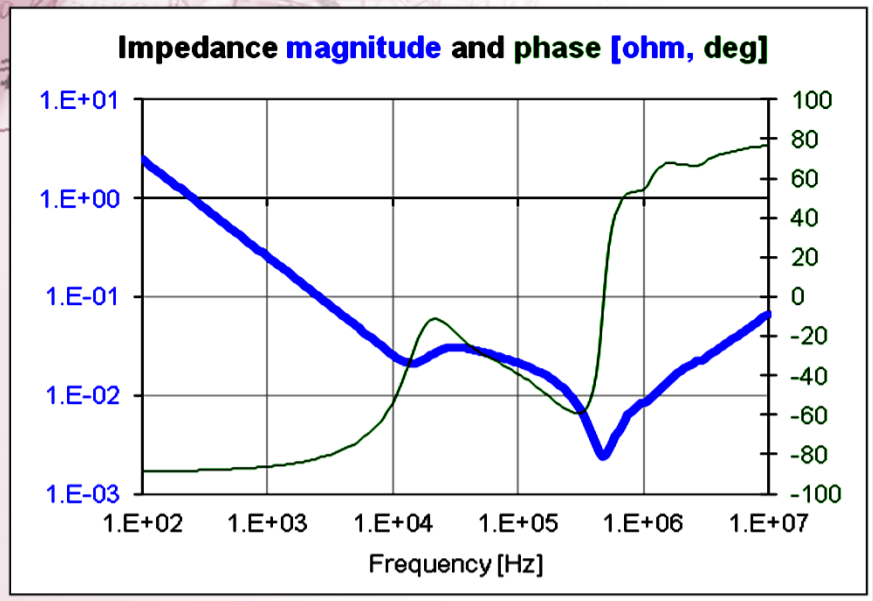
Moving The Converter Sense Lines

All the measurements made thus far, have the sense lines connected at the filter.

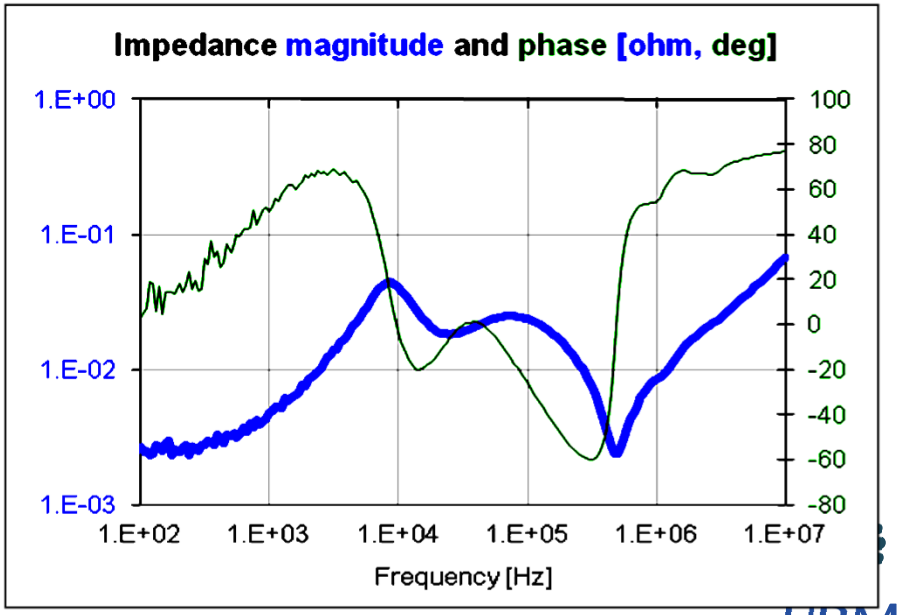
What if we move the sense lines to a point after the filter components, would we see any difference in performance?

Investigation of the movement of the sense lines begins by first looking at the output impedance of the regulator, that is at the bulk capacitors.

Regulator OFF



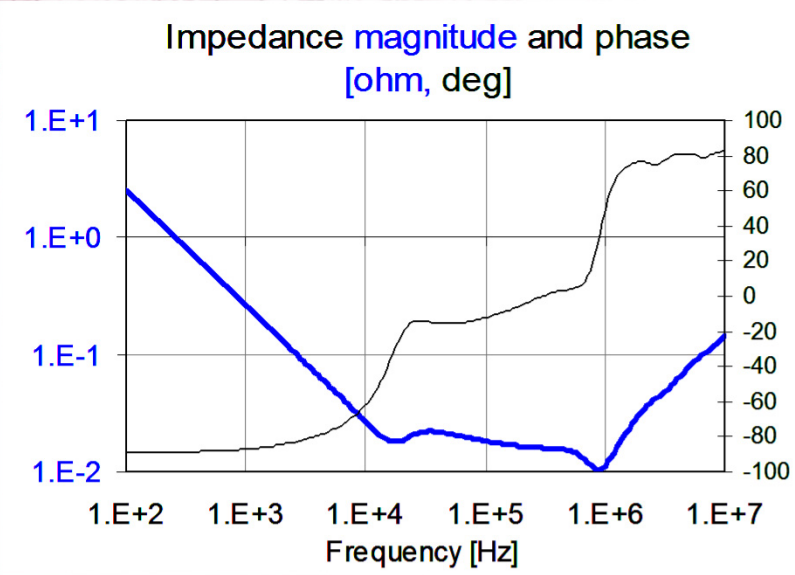
Regulator ON, 0 Ampere Load



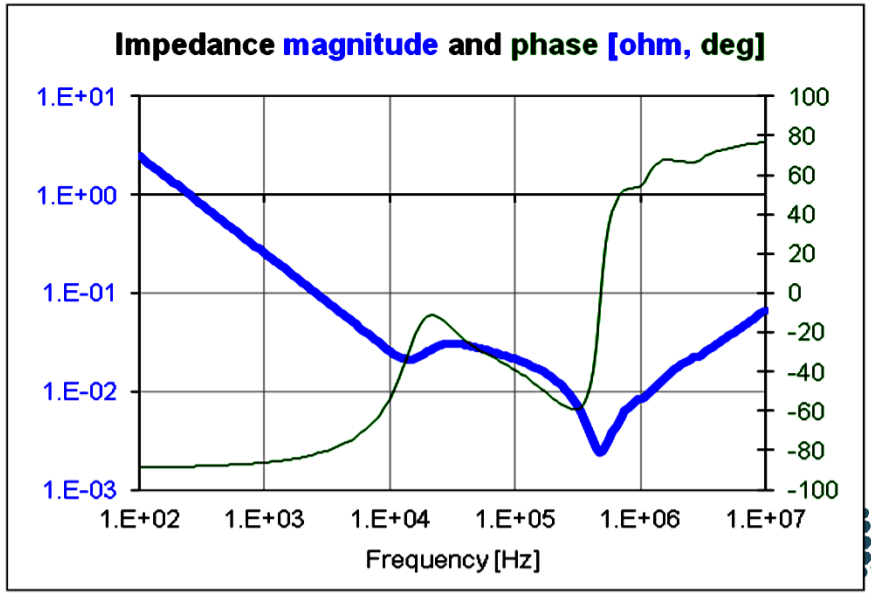
Comparative Output Impedance, Before / After Sense Line Change

Regulators OFF

Sense Lines Before Filter



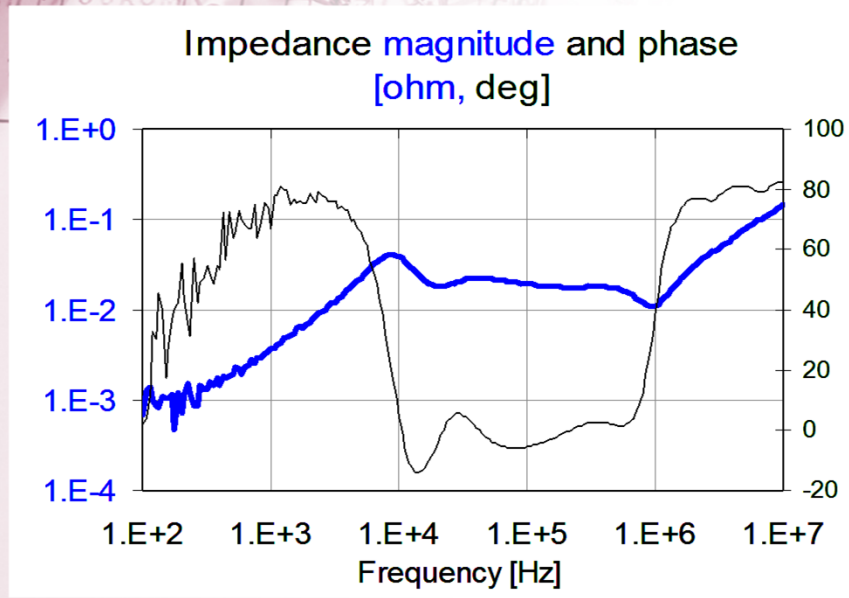
Sense Lines After Filter



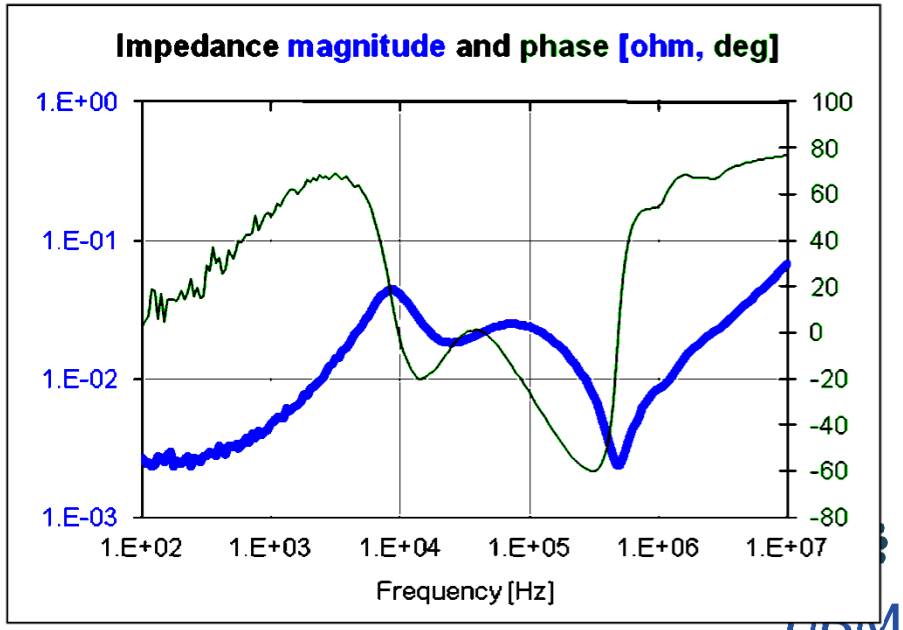
Comparative Output Impedance, Before / After Sense Line Change

Regulators ON

Sense Lines Before Filter



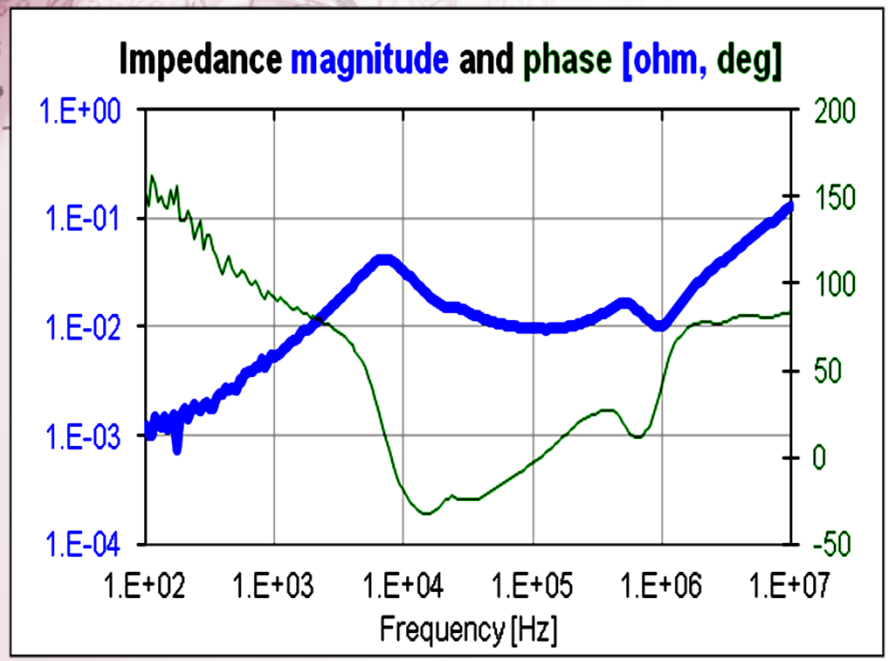
Sense Lines After Filter



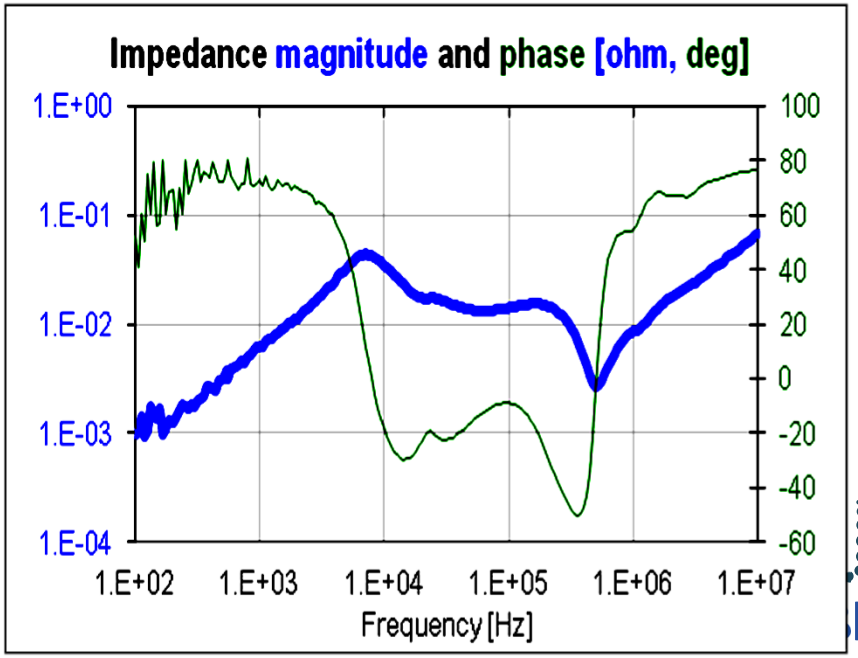
Comparative Output Impedance, Before / After Sense Line Change

Regulators ON, 4 Amp Load

Sense Lines Before Filter



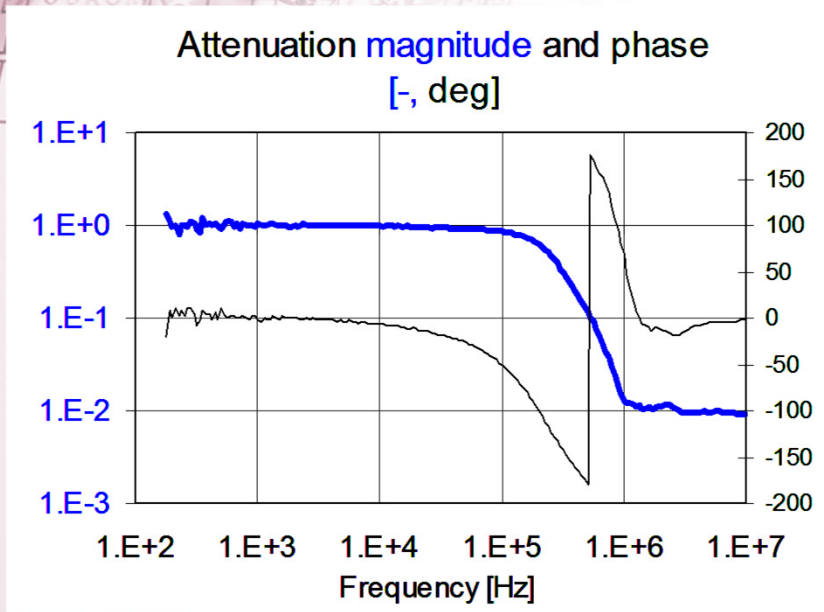
Sense Lines After Filter



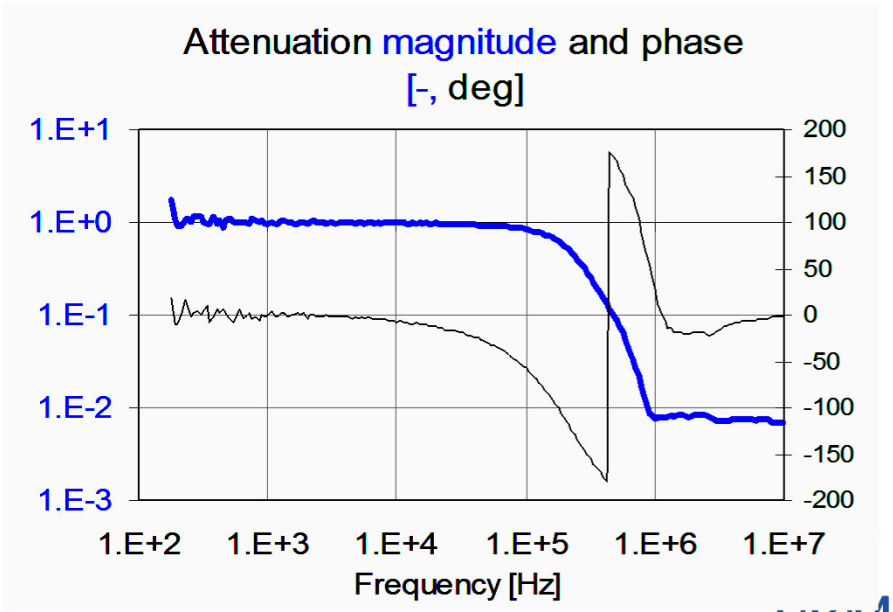
Comparative Attenuation, Before / After Sense Line Change

Attenuation, 4 Amp Load

Sense Lines Before Filter



Sense Lines After Filter



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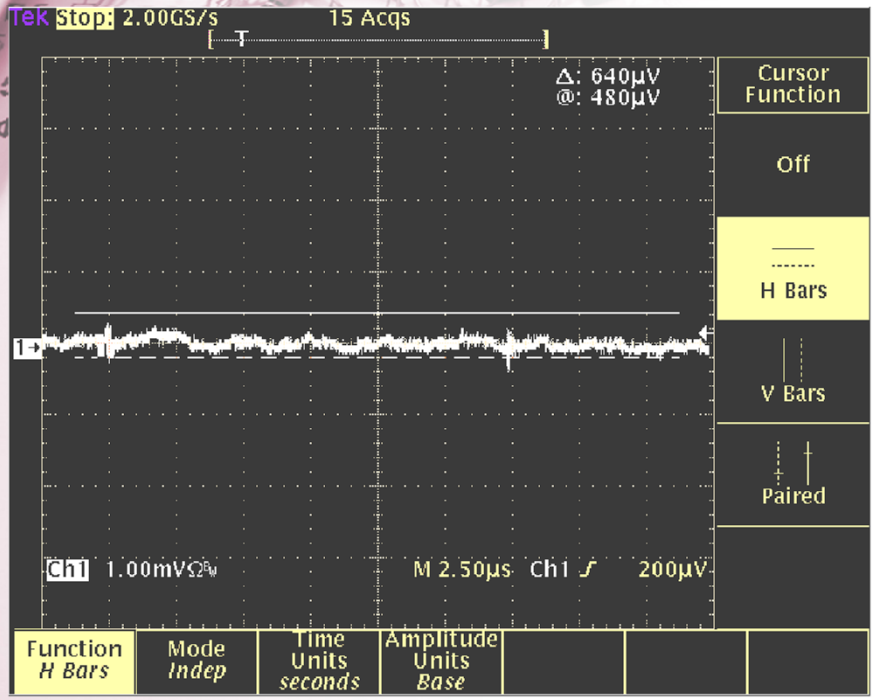
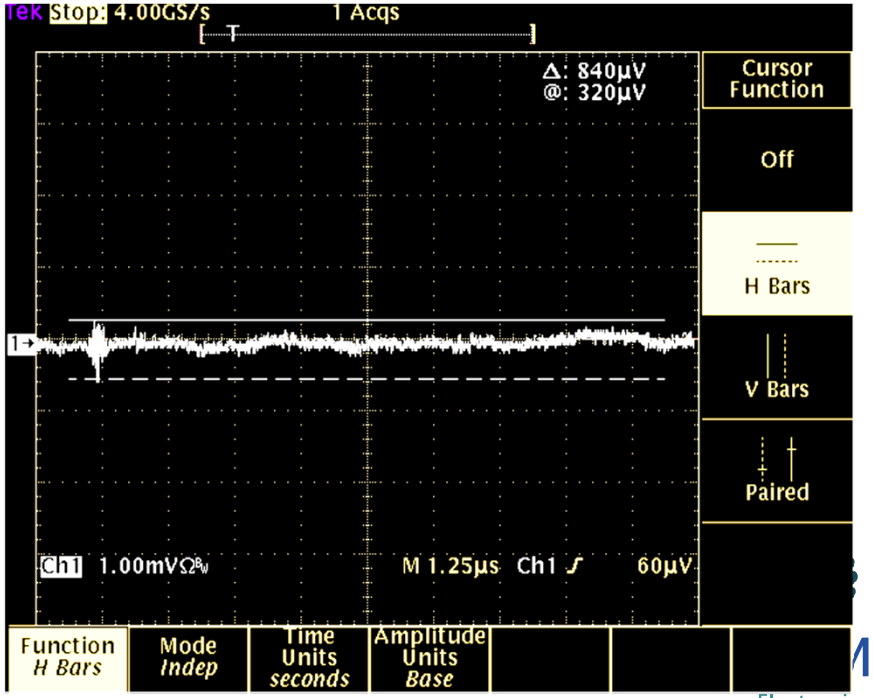
Comparative Attenuation, Before / After Sense Line Change

Ripple Voltage Attenuation, 4 Amp Load

Sense Lines Before Filter



Sense Lines After Filter



Change to Case #2, where the Bulk Capacitor is 22 µF. A comparison of the location of the sense lines, before and after the filter.

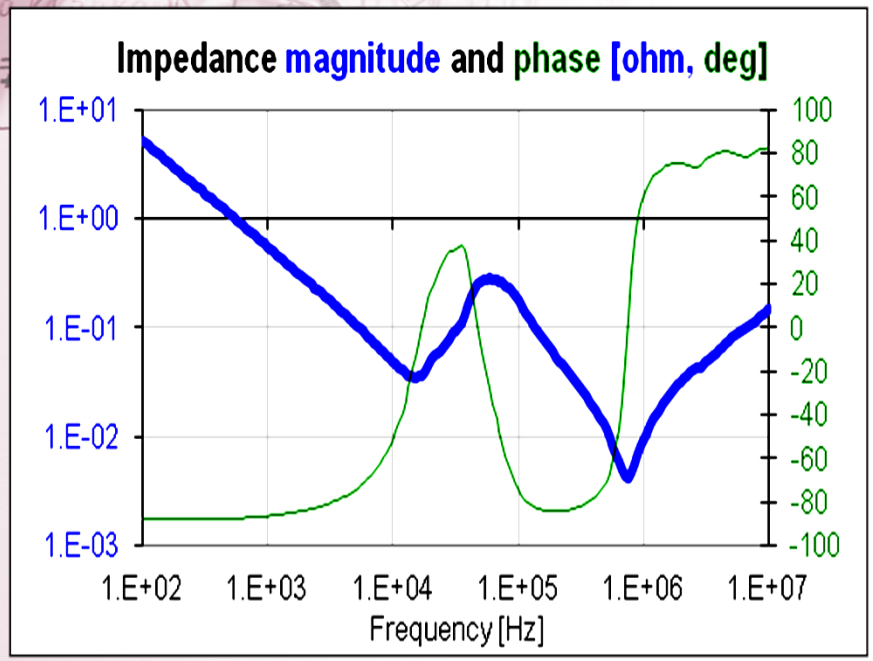
What are differences in Output Impedances with the change in the sense line location?

Is there any differences in Attenuation?

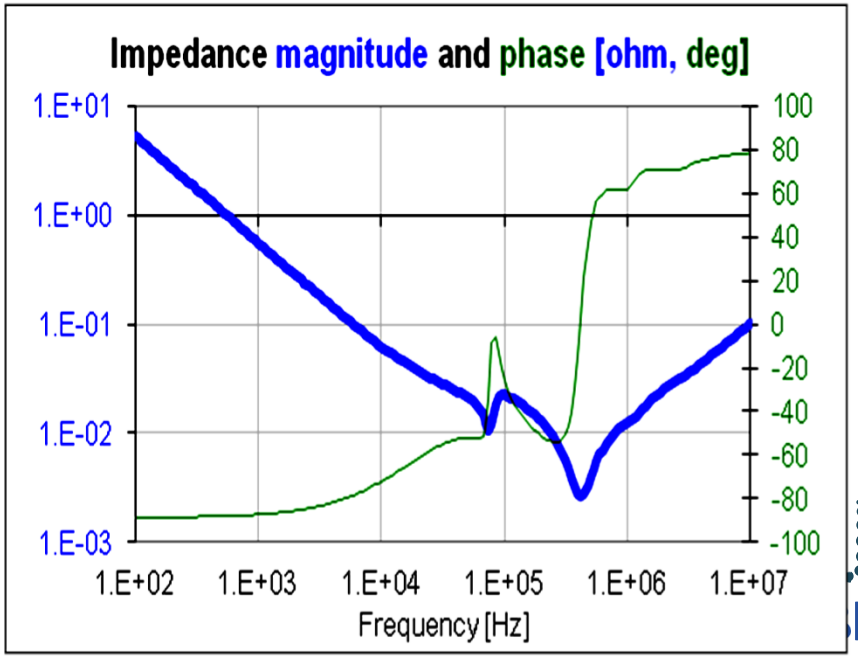
Is there any differences in the measured ripple voltages?

Comparison of Output Impedances

Regulator OFF, Before Filter

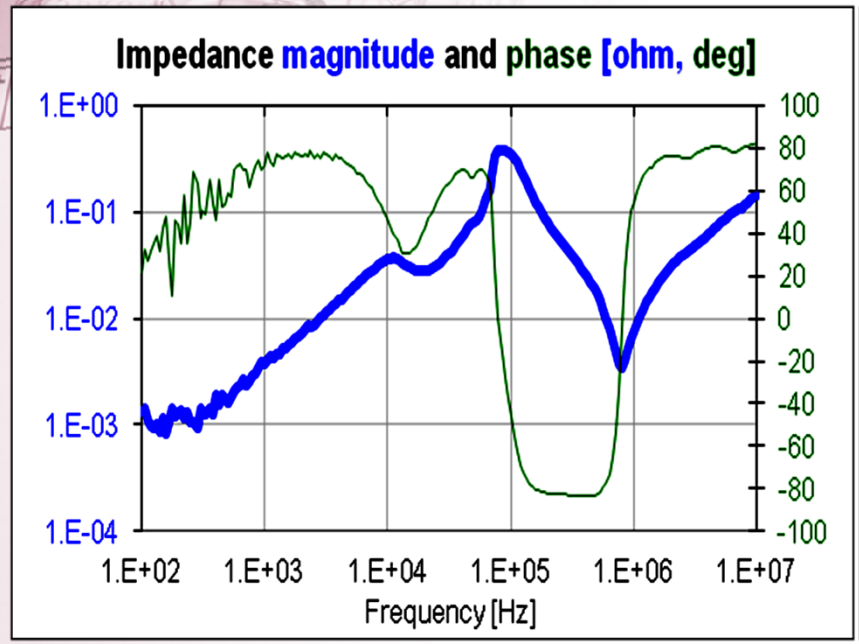


Regulator OFF, After Filter

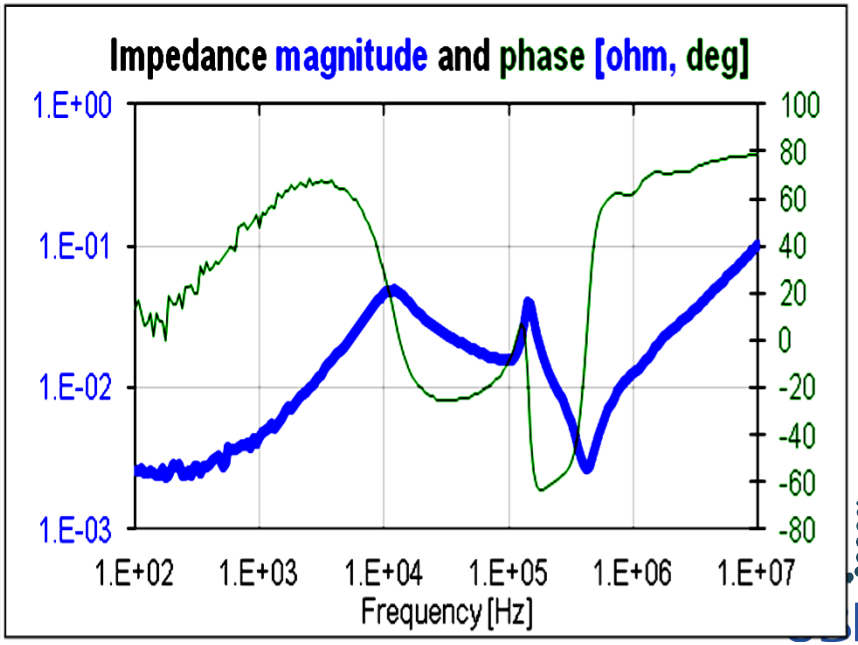


Comparison of Output Impedances

Regulator ON, 0 Amp Load, Before Filter

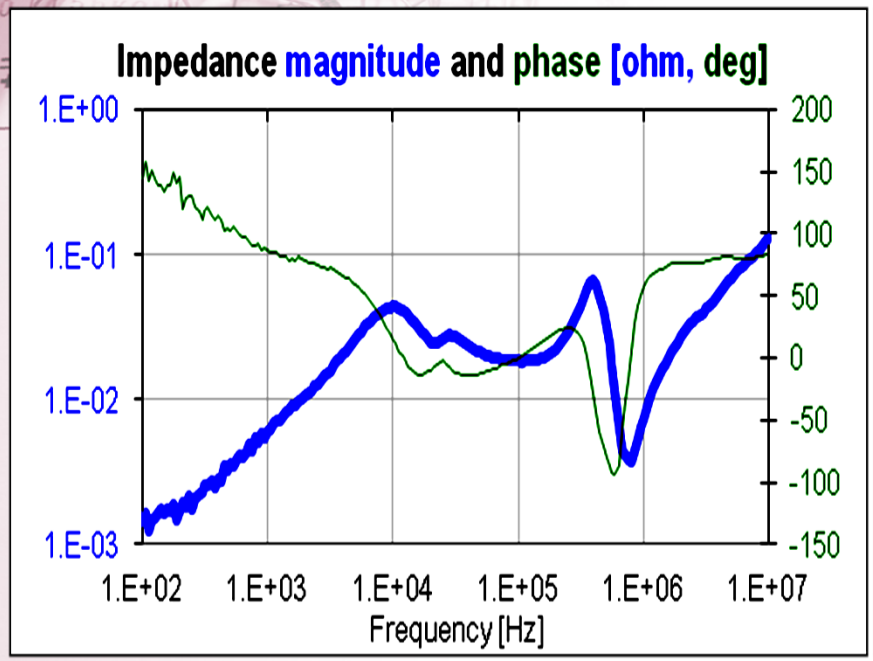


Regulator ON, 0 Amp Load, After Filter

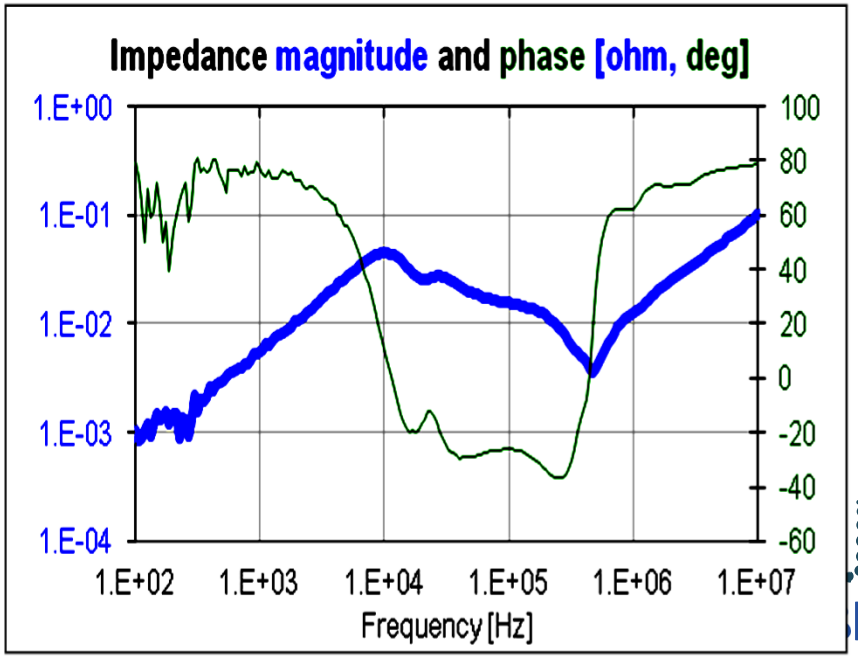


Comparison of Output Impedances

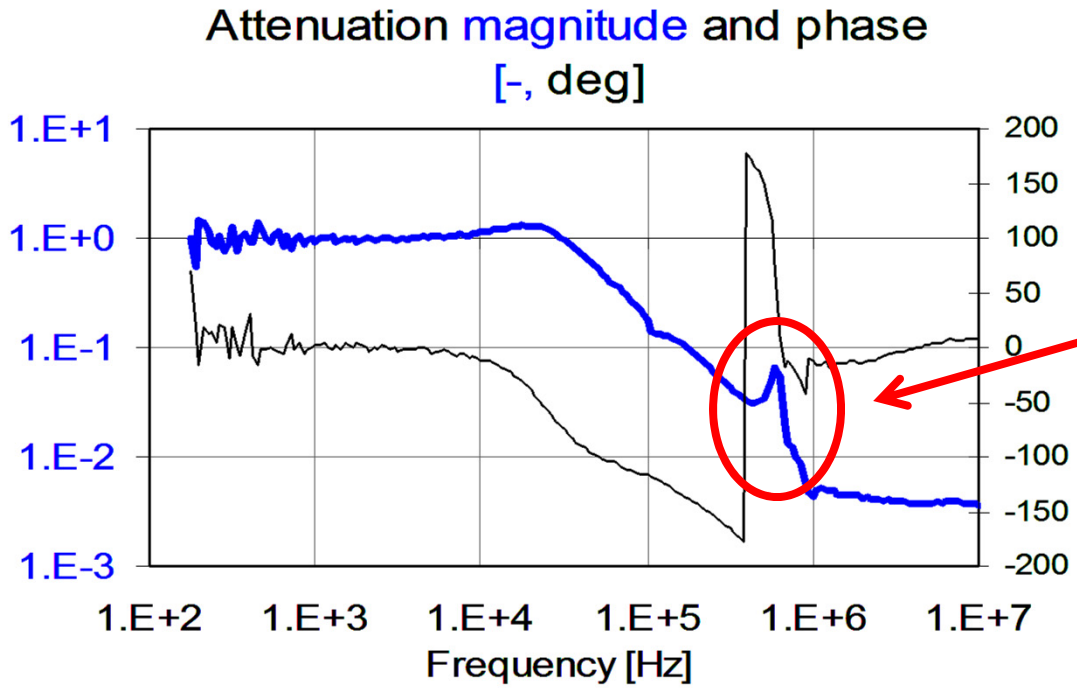
Regulator ON, 4 Amp Load, Before Filter



Regulator ON, 4 Amp Load, After Filter



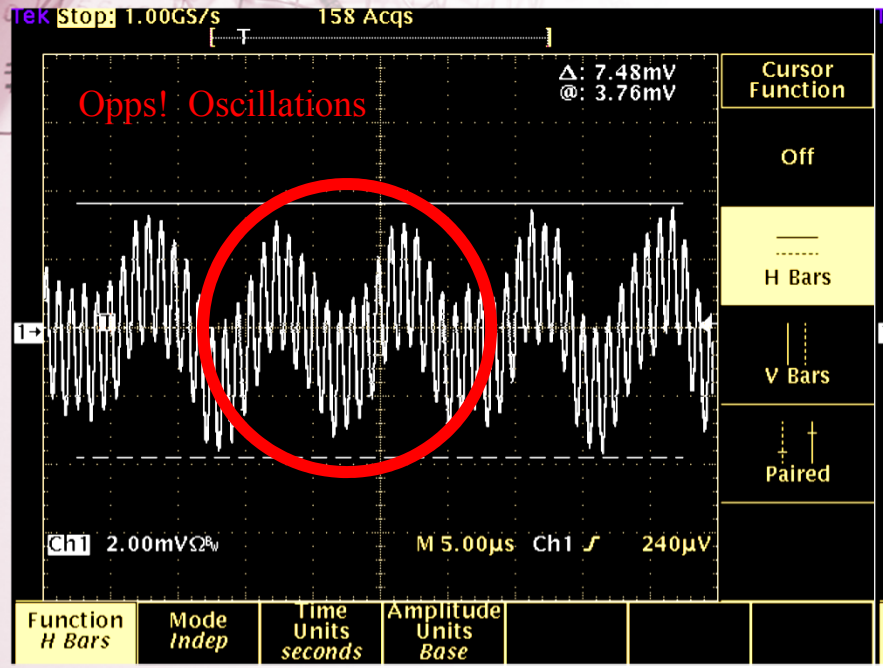
Measured Attenuation With 0 Ampere Load



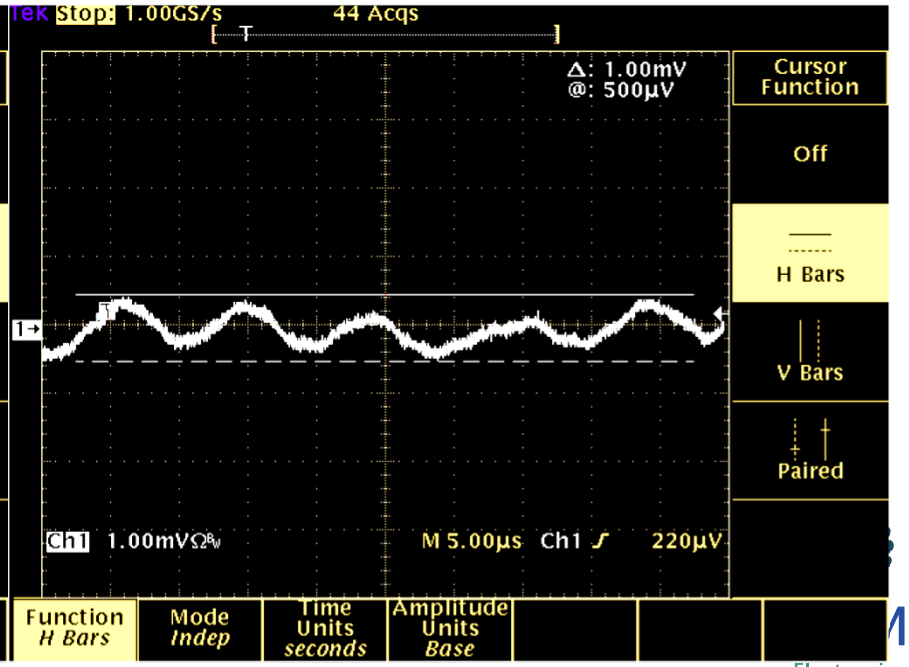
Some Strange event going on here!

Comparison of Ripple Voltages

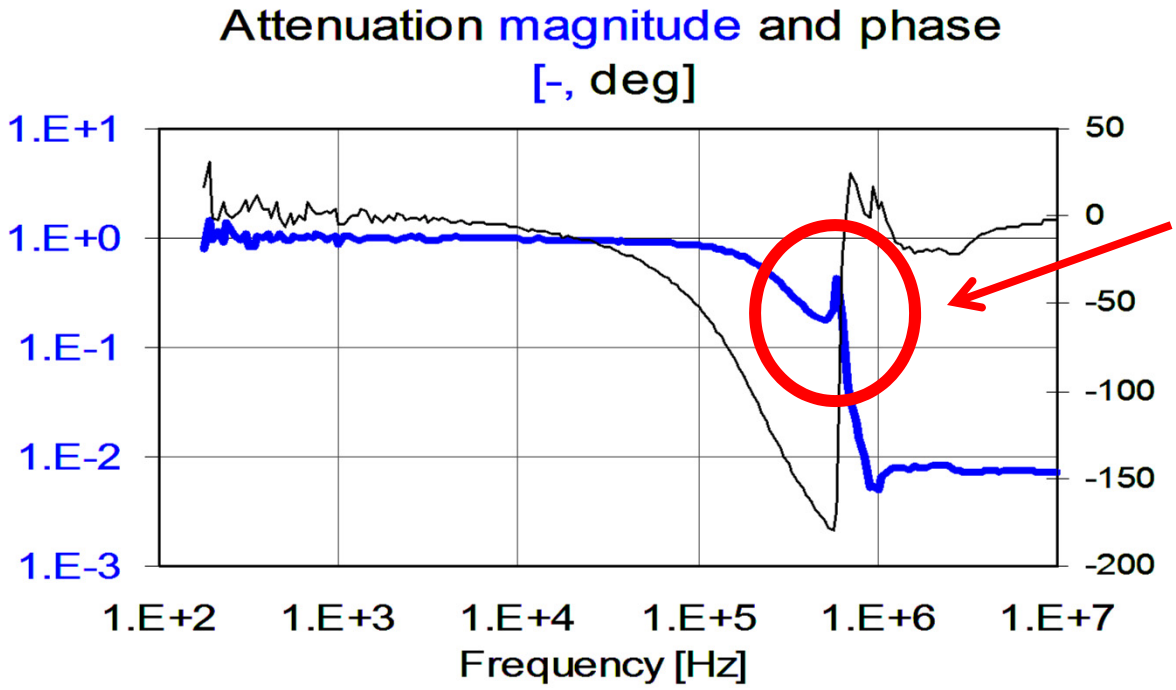
Regulator ON, 0 Amp Load, Before Filter



Regulator ON, 0 Amp Load, After Filter



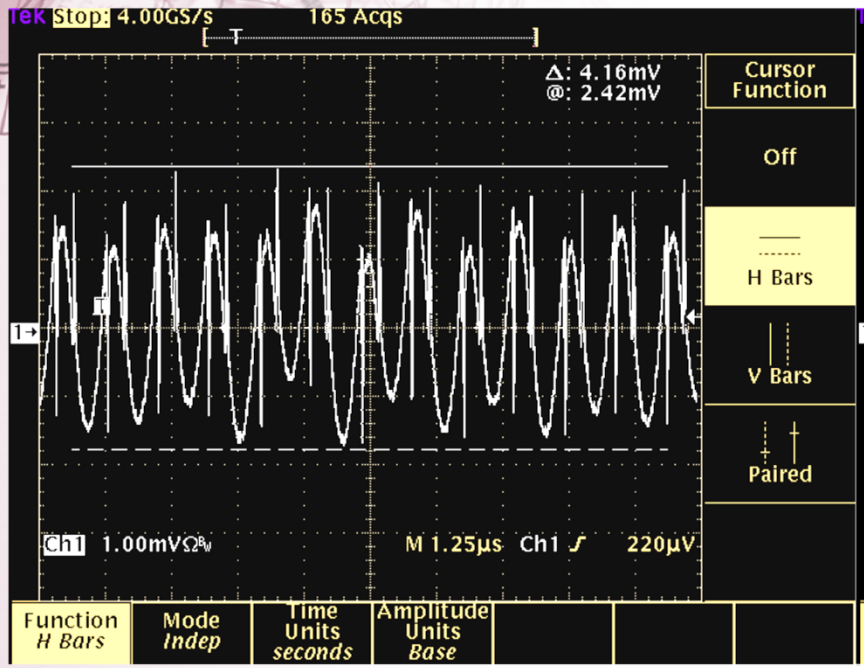
Measured Attenuation With 4 Ampere Load



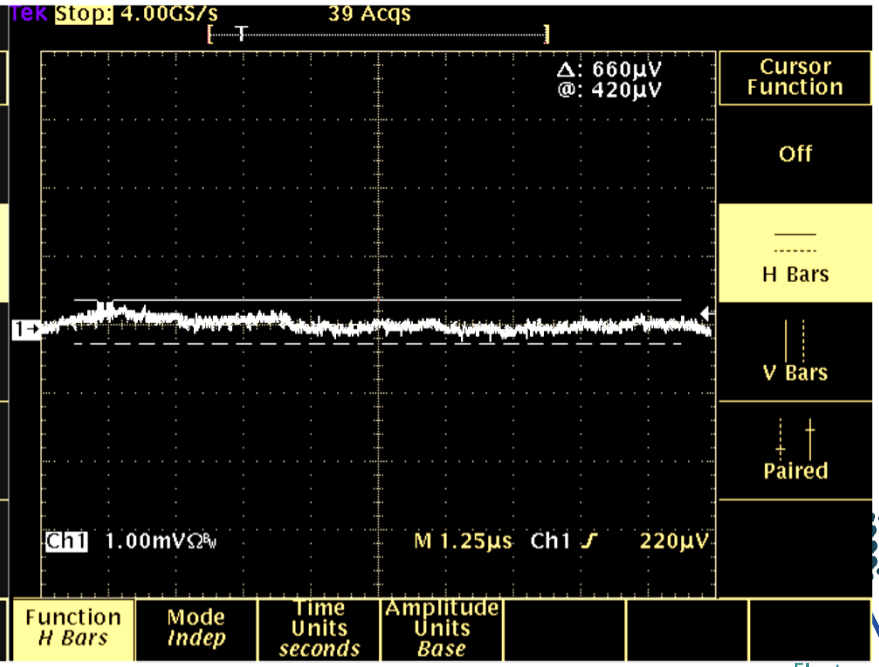
Here it is again!

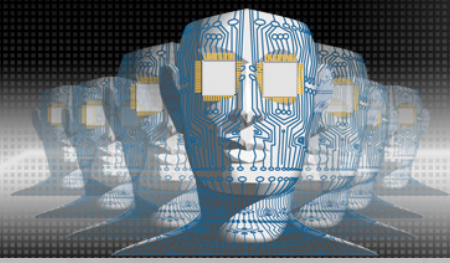
Comparison of Ripple Voltages

Regulator ON, 4 Amp Load, Before Filter



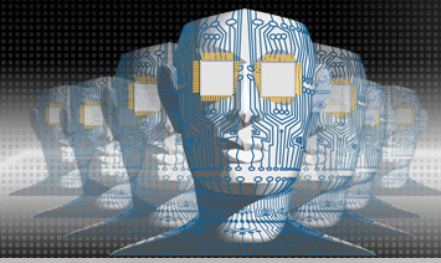
Regulator ON, 4 Amp Load, After Filter





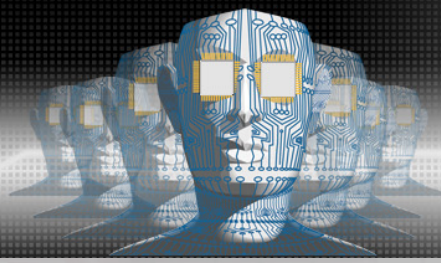
Summary of the Design Challenge

- Using a Current Mode Controller, without knowledge of any information about the compensation loop, we designed a power filter network that required a 1 mV noise level at 1 MHz.
- The resulting design using a target impedance that is basically flat;
  - The corner frequency of the filter occurs approximately where the simulation indicated
  - The resulting attenuation of the ripple noise was below the maximum assumed level required of 1 mV. Typical results show 500 – 800 µV of noise voltage.
  - The DC converter showed no ill effect from having a power filter attached, it appears to be stable, indicating:
    - Matching the source to the load was accomplished
    - Matching the load to the source was also accomplished



Summary Continued – Surprises!

- Observation of the effects of a ferrite bead used to it maximum rated value of current indicates that the bead saturates, reducing its inductance and series resistance significantly.
- Use of a ferrite bead may cause the attenuation requirements not to be met even with a flat output impedance.
- Use of a target impedance that is constructed by using the concept of a Big "V", with minimal amount of capacitance can be a significant problem.
  - It may cause instability of the DC converter.
  - Attenuation requirements may not be met.
- Sense lines for the DC converter should be located before the filter to avoid instability issues for the DC converter.



Other Observations

- In the design of the power filter, the corner frequency should be higher in frequency than the cross – over frequency of the compensation loop.
  - There will be no interference between the 2 systems, the compensation loop does not necessarily maintain the output impedance beyond the point where the gain goes below 0 dB.
  - Using a corner frequency inside the compensation loop control may alter the phase and should it fall so that there is no phase margin, may cause instability issues for the DC converter.
- Placing the sense lines of the converter before the filter helps to avoid the issue of interference between the 2 systems.

THANK YOU!

ANY QUESTIONS?

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