DesignCon 2012

Temperature and Moisture Dependence of PCB and Package Traces and the Impact on Signal Performance

Jason R. Miller, Oracle Corp.
Jason.Miller@Oracle.Com, (781) 442-2774

Ying Li, Oracle Corp.
Kevin Hinckley, Oracle Corp.
Gustavo Blando, Oracle Corp.
Bruce Guenin, Oracle Corp.
Istvan Novak, Oracle Corp.

Aykut Dengi, Alto Technogies, Inc.
Aykut.dengi@alto-tec.com

Ashley Rebelo, LSI Corp.
Ash.Rebelo@LSI.Com , (610) 712-7234

Scott McMorrow, Teraspeed Consulting Group, LLC
Scott@Teraspeed.Com, (401) 284-1827

Abstract

As link speeds continue to increase and operating margins are in the tens of millivolts and picoseconds, many engineers have lingering questions about the robustness of their links when one considers manufacturing, material, and temperature variation. Most hardware systems are required to reliably operate over a wide range of environmental conditions. In this paper, we examine the impact of temperature and humidity variation on the electrical properties of typical printed circuit boards traces (PCBs) and organic package traces. Test structures will be measured and the temperature-dependent, dielectric material properties, Dk(T, f) and Df(T, f), will be extracted for organic packaging materials and several PCB materials. By using two different methods, the extracted dielectric material properties can be compared and the dielectric component of loss can be isolated from the conductive loss. With the added dimension of temperature as an input parameter in our simulation environment, a temperature dependent multi-pole Debye model will be introduced to capture the dependence of the s-parameters on temperature.

Author Biographies

Jason R. Miller is a Principal Hardware Engineer at Oracle Corporation where he works on ASIC development, ASIC packaging, interconnect modeling and characterization, and system simulation. He has published over 40 technical articles on the topics such as high-speed modeling and simulation and co-authored the book “Frequency-Domain Characterization of Power Distribution Networks” published by Artech House. He received his Ph.D. in electrical engineering from Columbia University.

Ying Li is a Hardware Engineer at Oracle Corporation where she works on signal and power integrity of ASIC packaging interconnects simulation and measurement validation. In previous graduate studies, her research work focused on computational electromagnetics, sensitivity analysis and optimization. She received her Masters degree in electrical engineering from McMaster University. She is pursuing her Ph.D. degree at University of Washington.

Kevin Hinckley is a Principal Signal Integrity Engineer at Oracle Corporation with more than 15 years in the industry. Kevin has spent the last 12 years at Oracle in various product design groups and is currently responsible for all aspects of signal integrity modeling, analysis and validation for Oracle's x86 based servers. Prior to his time at Oracle, Kevin worked in the Defense Industry with a focus on semiconductor device modeling, simulation and measurement. He received a BSEE from Rensselaer Polytechnic Institute.

Gustavo J. Blando is a Principal Hardware Engineer with over ten years of experience in the industry. Currently at Oracle Corporation, he is responsible for the development of new processes and methodologies in the areas of broadband measurement, high speed modeling and system simulations. He received his M.S. from Northeastern University.

Bruce Guenin is a Principal Hardware Engineer at Oracle. He specializes in the development of advanced packaging technologies and in thermal and mechanical simulation and testing. He is Chairman of the JEDEC JC-15 Thermal Standards Committee and an Associate Editor of Electronics Cooling Magazine. His contributions to the thermal sciences have been recognized by receiving the Harvey Rosten Award in 2004 and the Thermi Award in 2010. He received the B.S. degree in Physics from Loyola University, New Orleans, and the Ph.D. in Physics from the University of Virginia.

Istvan Novak is a Senior Principal Engineer at Oracle. Besides signal integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is a Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies.

Aykut Dengi received the B.S. degree from Bilkent University in Ankara, Turkey in 1992 and the Ph. D. degree from Carnegie Mellon University in 1997, both in electrical and computer engineering. He is currently a founder and the President of Alto Technologies, Inc., a privately owned electronic design automation company. Before that he worked at Cadence Design Systems, Neolinear, and Motorola, leading research teams in design automation, interconnect modeling and electromagnetic field solvers.

Ashley Rebelo is a Staff Engineer in the packaging characterization group of LSI Corporation where he is responsible for Signal and Power integrity modeling of packaging interconnects. Prior to LSI he was Senior Member of Technical Staff in Agere System (formerly Lucent Technologies) where he was responsible for modeling and measurement validation of ASIC package and Interconnects. He holds a B.S in Electrical & Computer Engineering from Rutgers University and graduate studies at Lehigh University.

Scott McMorrow is President and Founder of Teraspeed Consulting Group. Mr. McMorrow is an experienced technologist with over 20 years of broad background in complex system design, interconnect & Signal Integrity engineering, modeling & measurement methodology, engineering team building and professional training. Mr. McMorrow has a consistent history of delivering and managing technical consultation that enables clients to manufacture systems with state-of-the-art performance, enhanced design margins, lower cost, and reduced risk. Mr. McMorrow is an expert in high-performance design and signal integrity engineering, and has been a consultant and trainer to engineering organizations world-wide.

Introduction

As link speeds continue to increase and operating margins are in the tens of millivolts and picoseconds, many engineers have lingering questions about the robustness of their links when one considers manufacturing, material, and temperature variation. The challenges are considerable: links must remain operational across the entire product lifespan which means that manufacturing and material variation must remain in a predetermined range over the span of years and engineers must be able to account for this tolerance range in the link budget or compensate for it using adaptive equalization. In addition to manufacturing and material variation, most hardware systems are required to reliably operate over a wide range of environmental conditions. For example, a typical system operating range is 5-35 ˚C (41-95 ˚F) and a relative humidity of 10-90 %.

The complex permittivity of many package [1] and PCB materials has been shown to be temperature dependent. For this reason, accurate determination of the complex permittivity of dielectrics is needed for package and PCB modeling across operational temperature extremes. The complex permittivity impacts many important electrical parameters including the speed of signal propagation, channel loss and impedance matching. Field solvers and analytic formulas require an estimate of the complex permittivity to provide accurate simulation data. In this paper we seek to understand the temperature and humidity dependence of the complex permittivity for various packaging and PCB materials and explore ways of capturing this variation in our simulation environment.

The paper is divided into five sections. In the first section, we review our measurement set up and present measurement data of packaging and PCB materials as a function of temperature and humidity. The second section dives into a discussion and analysis of how moisture penetrates into packaging substrates. This will also include empirical data on the water absorption of the materials measured in the first section. Next, in the third section, an approach will be presented to extract and match the material properties across temperature. This method fits the complex propagation constant at each temperature between a transmission line model and the measurement data. In the fourth section, with the realization that often models are provided directly from vendors (and usually extracted at room temperature), we provide a method for directly scaling solved s-parameters such that temperature and humidity effects can be accounted for. Finally, in the fifth section, we examine the real-world impact of temperature variation on operating margin including eye diagrams.

1 Temperature & Humidity Measurements

Package and PCB test structures were measured as a function of temperature and humidity. For all measurements, a 40 GHz 4-port network analyzer was used to measure S-parameters and an Electronic Calibration Module, 10 MHz to 40 GHz, was used to perform the calibration. After calibration, soaked or baked samples were placed in a test

chamber and the S-parameters were measured as a function of temperature. Both the short and long stripline structures were measured simultaneously using all four ports of the network analyzer (i.e. measuring two, two-port structures simultaneously) to ensure both structures were measured at the precisely the same environmental conditions. Figure 1 shows the entire test setup.

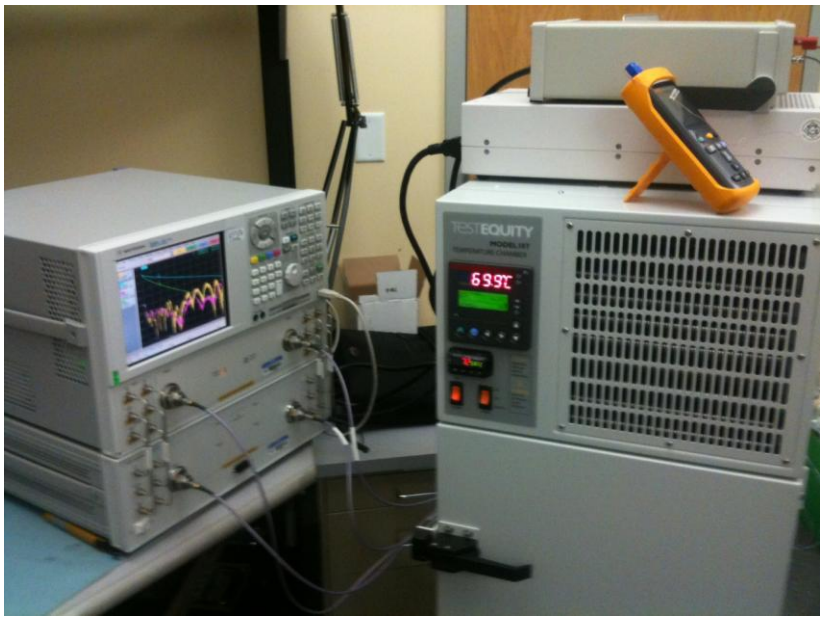

Figure 1 Measurement setup for the temperature dependent s-parameter measurements.

Once the soaked or baked out samples were inserted into the chamber, the temperature was typically varied from 0 ˚C to 100 ˚C in 10 ˚C steps. During some of the measurements, the coaxial connections became unreliable at the temperature extremes. In those cases, the temperature characterization may have been performed over a slightly narrower range.

Since measurements includes the presence of connectors, and it's impossible to know exactly the trace characteristic impedance, it's very difficult and sometimes even misleading to extract the material loss and delay based directly on the raw s-parameters. Instead a methodology [2] was used that extract Generalized S-parameters (GMS). With this method two traces of different lengths are measured, and with the assumption that the characteristics of these two traces and the connectors are identical, the parasitic effect of the connectors can be removed, and the complex propagation constant, independent of characteristic impedance can be extracted for the delta between the traces. This method will be used throughout the paper.

1.1 Package Measurements

A suite of structures were designed by Teraspeed Consulting for the identification of material parameters of package dielectrics and for benchmarking various electromagnetic

and signal integrity simulators using advanced VNA measurement techniques. There are 19 test structures on the board, comprising calibration structures, transmission line segments, and resonant structures, in addition to typical elements of single-ended and differential multi-gigabit package data channels. All test structures are equipped with optimized transitions from 2.92 mm edge-launch connectors to microstrip and stripline lines that minimize measurement impedance discontinuities and extend the effective measurement bandwidth to 40 GHz. These transitions were designed to have a modal cutoff frequency of 55 GHz, well beyond the measurement bandwidth of the VNA.

The test structure stackup consisted of five build-up layers and one core layer, for a total of 12 plane layers. The build-up material (where the traces were routed) is a resin material used in organic buildup packages and we will identify it going forward as Material A. The build-up layers are non-reinforced. Trace dimensions are 15 μ thick and 21 μ wide.

For the purposes of this study two of the test structures were simulated and measured. This structure consists of two single-ended stripline having a length of 98,218 um and 48,218 um. There are two 2.92 mm edge-launch connectors on each board.

Soaked samples were exposed to 1 week of 30 ˚C and 60 % RH, measured and then baked for 1 week of 125 ˚C and remeasured.

Figure 1 shows the measured S21 GMS s-parameters for the soaked and baked out packaging sample. We see two clear trends; first, as temperature increases the loss increases (both conductive and dielectric). Second, we observe that the range of S21 values for the soaked samples is larger than the baked out sample. **This is an observation we will consistently see throughout the measured data: the presence of moisture accentuates the temperature dependence of the complex permittivity.**

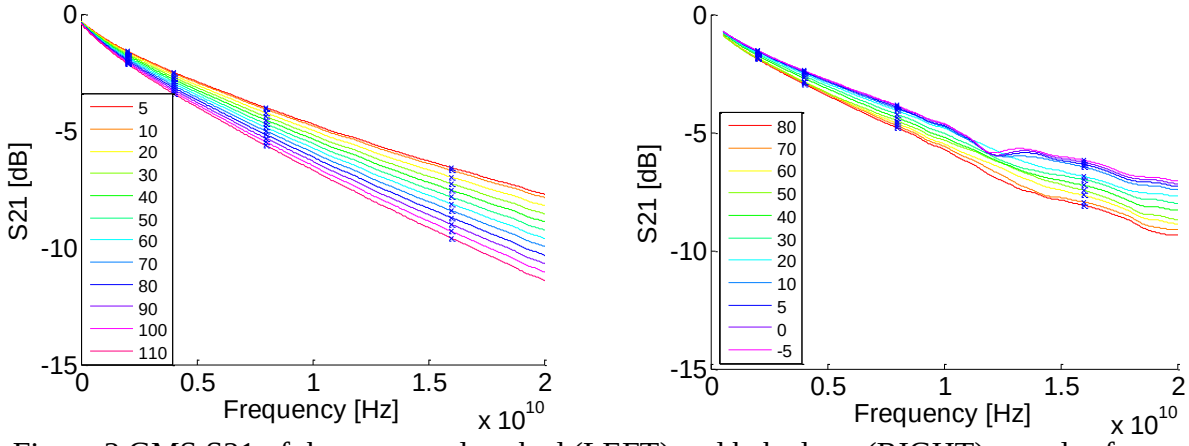

Figure 2 GMS S21 of the measured soaked (LEFT) and baked out (RIGHT) samples for different temperatures. Markers are shown on the curves at 2, 4, 8 and 16 GHz. Note that the distortion observed in the baked out sample is due to a known cabling issue and is not due to the material characteristics.

Figure 3 shows the measured S21 GMS s-parameters for the soaked and baked out packaging sample as a function of temperature for discrete frequency points. Again, the soaked samples exhibit a steeper slope and hence a greater sensitivity of loss to temperature. **We see that as frequency increases, the loss variation across temperature increases. This means that at higher data rates, where margins get tighter, temperature dependent effects will be much more important to capture.** Figure 4 highlights this trend by plotting the increase in loss relative to 20 ˚C; we see that at 16 GHz, there is about a 25 % increase in loss at 100 ˚C. Note that the measurement data was converted to magnitude from dB before computing the percentage change.

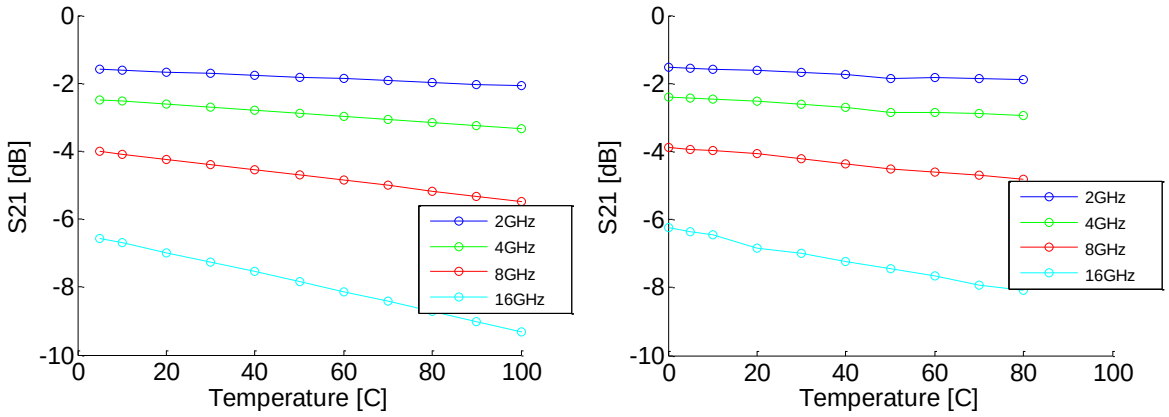

Figure 3 GMS S21 at discrete frequency points of the measured soaked (LEFT) and baked out (RIGHT) samples as a function of temperature.

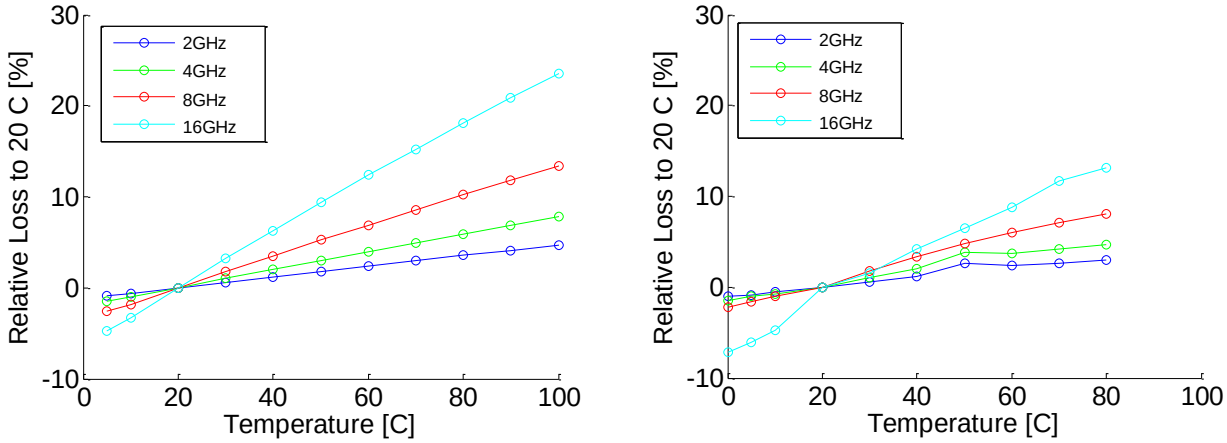

Figure 4 Relative loss to 20 ˚C at discrete frequency points of the measured soaked (LEFT) and baked out samples (RIGHT) as a function of temperature.

Figure 5 shows the measured S21 GMS group delay for the soaked and baked out packaging sample as a function of temperature. The baked out data exhibits a slightly narrower range of group delay variation across temperature. Figure 6 plots the variation across temperature relative to 20 ˚C extracted at a low frequency. Although the group

delay is slightly more sensitive to temperature for the soaked sample, the increase in loss over temperature is much more significant. **Thus we can conclude that that the variation of the dielectric constant over temperature is relatively moderate for this material.** This is observation is consistent with earlier investigations [1].

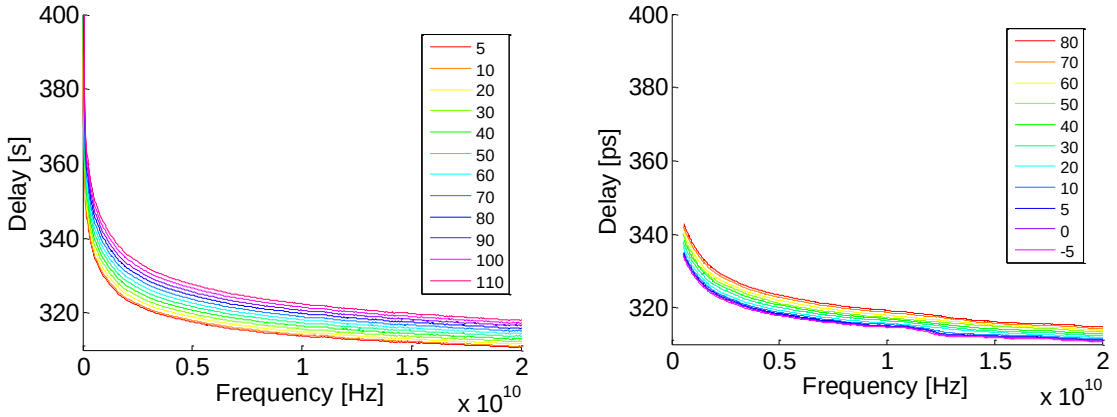

Figure 5 GMS group delay of the measured soaked (LEFT) and baked out (RIGHT) samples for different temperatures.

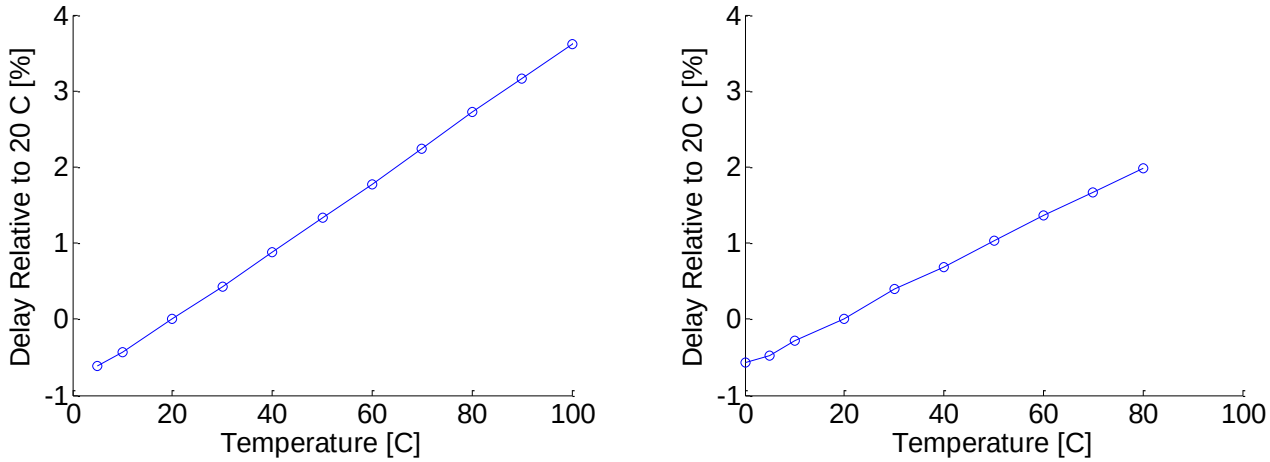

Figure 6 Delay relative to 20 ˚C of the measured soaked (LEFT) and baked out (RIGHT) samples as a function of temperature.

1.2 PCB Measurements

The PCB measurements were made on test coupons with two 2.92 mm edge-launch SMAs on each board. Like the packaging measurements, two single-ended stripline were measured having a length of 9.8 cm and 5.2 cm. Prior to the measurements these samples were kept at room temperature and humidity. Two low-loss PCB materials available commercially were investigated. We will identify these as Material B and Material C. Material C is advertised as having a lower dielectric loss than Material B.

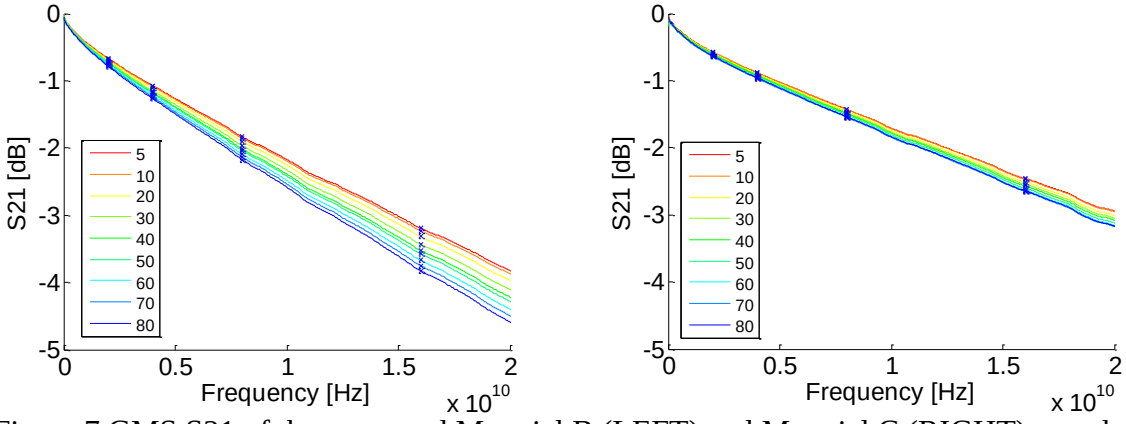

Figure 7 GMS S21 of the measured Material B (LEFT) and Material C (RIGHT) samples for different temperatures. Markers are shown on the curves at 2, 4, 8 and 16 GHz.

Figure 7 shows the measured S21 GMS s-parameters for the Material B and Material C PCB sample. Like the packaging material, we see that as temperature increases the loss increases. Also, we observe significantly less loss variation with temperature for Material C. Figure 8 shows that the frequency dependence of the temperature dependent losses: again, **the temperature dependence of Material C is quite flat compared to Material B material even as high as 16 GHz.**

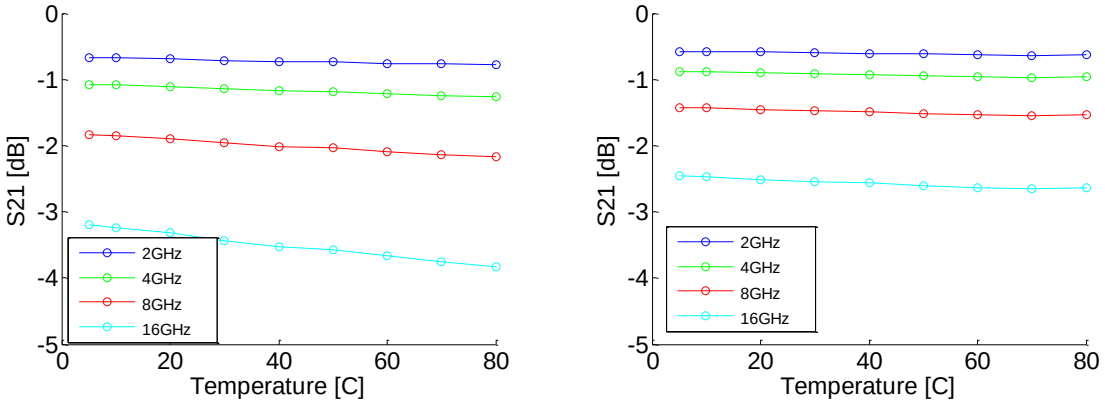

Figure 8 GMS S21 at discrete frequency points of the measured Material B (LEFT) and Material C (RIGHT) samples as a function of temperature.

Looking at Figure 9 we see that although Material B does show an increase in loss relative to 20 ˚C, the variation is significantly less compared to what we observe for the packaging materials in the previous section. With Material C samples, the loss variation is even further reduced. Note that the measurement data was converted to magnitude from dB before computing the percentage change.

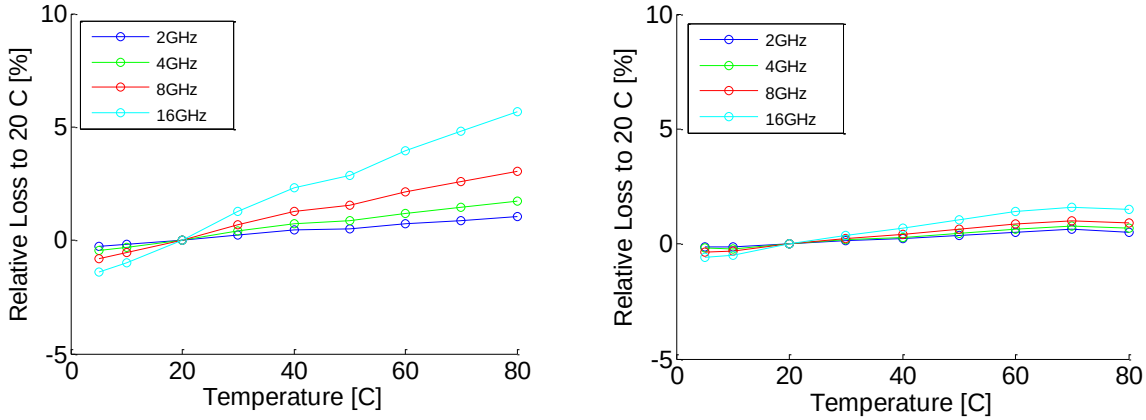

Figure 9 Relative loss to 20 ˚C at discrete frequency points of the measured Material B (LEFT) and Material C (RIGHT) as a function of temperature.

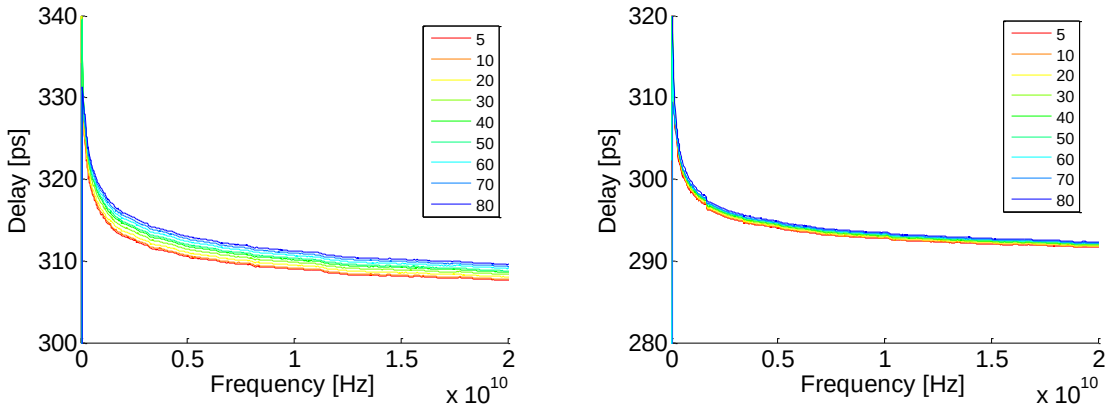

Figure 10 GMS group delay of the measured Material B (LEFT) and Material C (RIGHT) samples for different temperatures.

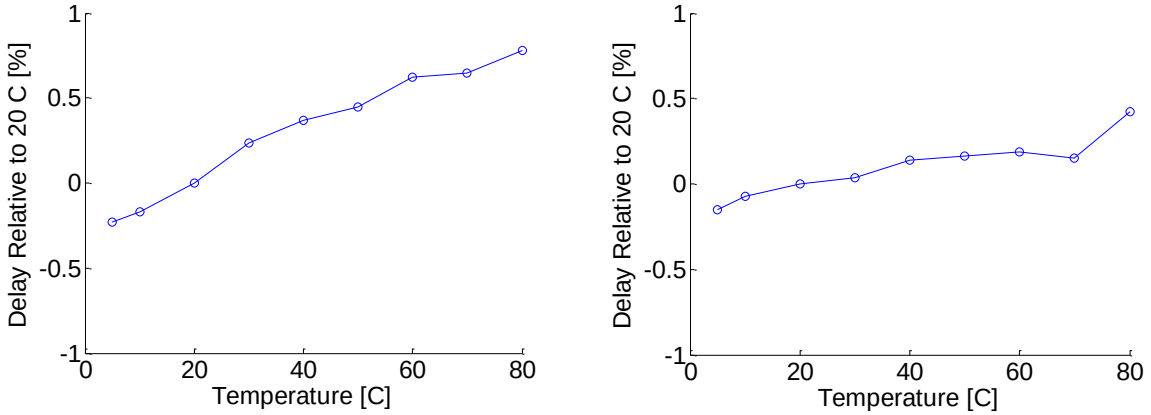

Figure 11 Delay relative to 20 ˚C of the measured Material B (LEFT) and Material C (RIGHT) as a function of temperature.

2 Temperature-Moisture Modeling

This effort is devoted to quantifying the effect of humidity soak and bake out processes on organic substrates. Initially, the intent is to determine the moisture concentration distribution in the test samples analyzed in Section 1.1. **Ultimately, the objective is to apply this analysis to predict moisture levels in actual packages under various field conditions to enable the subsequent prediction of signal attenuation.**

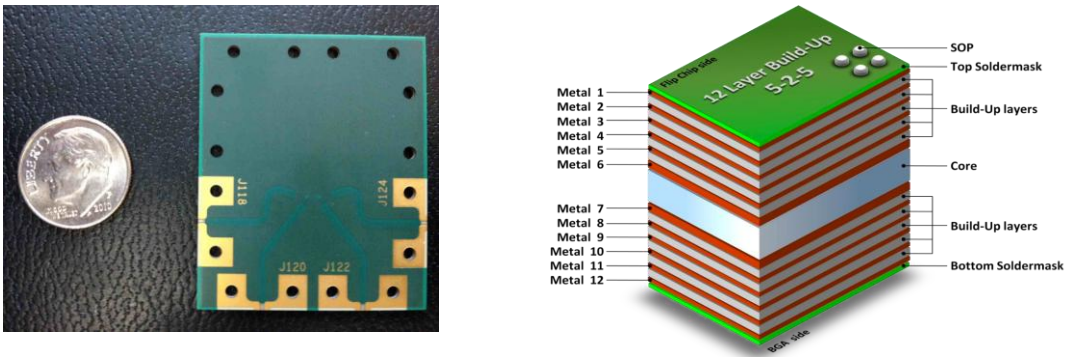

Figure 12 (LEFT) Photo of moisture sample and (RIGHT) diagram of substrate stackup.

Figure 12 shows the moisture sample. Its overall dimensions are 3.6 x 4.3 x 0.13 cm. The stackup diagram shows the substrate construction, consisting of 12 metal planes with 10 buildup layers and 1 core layer sandwiched between them. Since the planes are largely intact, the dominant path for moisture to diffuse into the buildup and core layers is within the plane of each layer beginning at the outer edges of the sample.

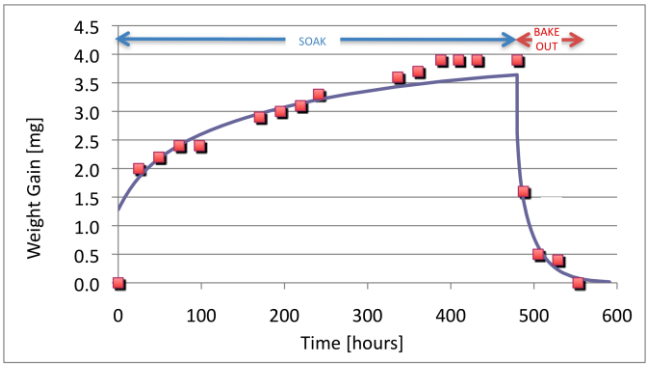

Figure 13 Graph showing weight gain data (symbols) and model (line) during humidity soak and bakeout.

Figure 13 displays a graph of the weight gain of the sample due to moisture during the initial soak process, 30˚C and 60% RH. The total amount of moisture absorbed by the sample stabilizes at 3.9 mg after 388 hours. The subsequent bakeout process at 125˚C produces a more rapid loss of moisture such that the weight gain returns to zero after only

73 hours. The smooth curve represents the results of a numerical diffusion model described below.

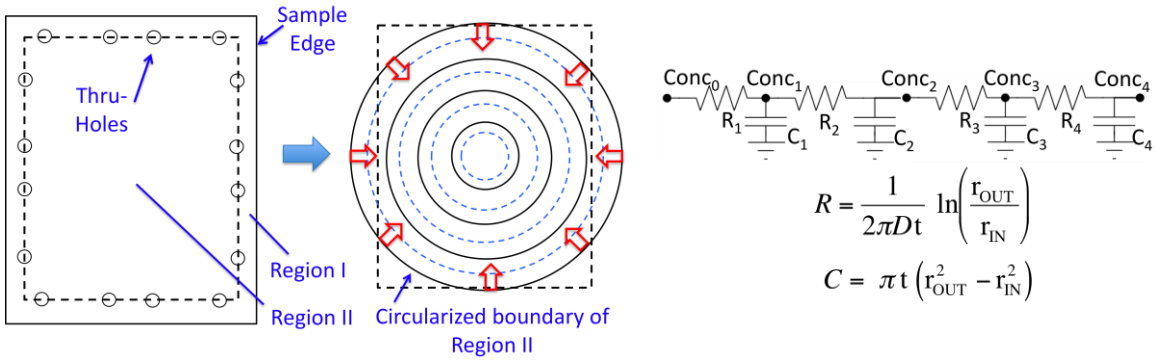

Figure 14 (LEFT) Diagrams of moisture sample and circular region with same area as Region II. Solid (dotted) circles define regions for capacitance (resistance) calculation. Red arrows indicate radial moisture diffusion paths. (RIGHT) 4-stage RC circuit used to calculate moisture concentration versus time and equations to calculate R and C.

Figure 14 illustrates the procedure used to perform the transient diffusion calculation. The first step was qualitative, in observing that at the beginning of the soak and bakeout processes, there was a rapid change in the weight gain, followed by a slower change. This abrupt change is attributed to the rapid saturation of Region I, due to moisture flow from the outer edge and the array of into this narrow region. Once Region I is saturated, all of the moisture entering the sample via the edges or the holes will diffuse toward the center of the substrate. The diffusion of moisture into Region II is a separate process and is the limiting factor in determining the rate of moisture uptake and loss in the two processes. The subsequent effort focused on Region II.

In order to simplify the calculation of moisture diffusion into Region II, the outer boundary is circularized, maintaining the same enclosed area. This region is then subdivided into 4 annular regions, each having the same radial width. As shown in the Figure, in this model geometry, moisture is assumed to diffuse uniformly along the perimeter of Region II, migrating radially inward toward the center of the region.

The rate of diffusion through these 4 regions can be calculated using a numerical method developed for modeling the transient flow of heat [3]. The equations for heat flow can be used if the following substitutions are made: moisture concentration = temperature; diffusion coefficient = thermal conductivity; volume = heat capacity. The R and C parameters are calculated using the indicated equations, where D is the diffusion coefficient, t is the total thickness of the buildup and core layers, equal to 1.1 mm, and r_{OUT} and r_{IN} are the outer and inner radii of the annulus in question. The values of R are calculated using the values of radius indicated by the dotted lines. These lines divide each of the capacitive volumes into 2 equal parts. Hence they represent the mean distance of moisture to diffuse from one of the concentric volumes to the next. The boundary condition, applied to the leftmost node in the RC circuit is that the moisture

concentration of that node equals the saturation concentration for the sample in equilibrium with the ambient environment. For the soak process this is 2.1 mg/cm^3. For the bakeout process it was set to zero. The solution of the numerical model provides a value of concentration at each of the 4 nodes in the model versus time.

Figure 13 shows reasonable agreement between the test and model. Because of the different temperature and humidity levels in the soak and bakeout processes, a separate value of diffusion coefficient was determined for each by fitting the model to the data. The values are: D_{SOAK} = 7.0E-7 cm^2/sec and D_{BAKE} = 7.3E-7 cm^2/sec. Note that these values represent the combined effect of the buildup and core materials, which are present in a certain proportion. Their applicability is limited to substrates with the same stackup.

Having established above a reasonable model for the moisture diffusion, we can now apply this to the stripline samples measured in Section 1.1 Hence, the two values of D were applied to the moisture calculation for the stripline.

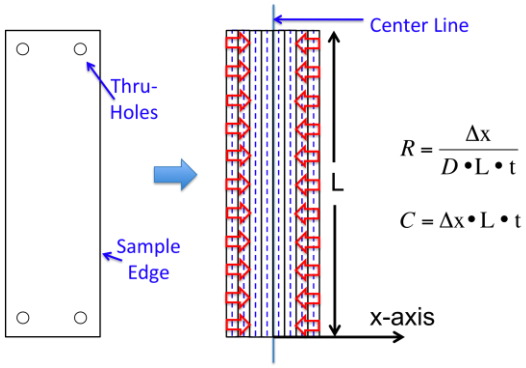

Figure 15 Diagrams of electrical test sample and its representation in 1-D diffusion model. Solid (dotted) lines in right figure define regions for capacitance (resistance) calculation. Red arrows indicate moisture diffusion paths, symmetrical about the sample center line.

A diagram for the stripline sample is shown in Figure 15. The overall dimensions for this sample are 4.9 x 1.4 x 0.13 cm. Since flow from the long edge to the center line is symmetrical, the maximum distance for moisture to diffuse from the other edges is 0.7 cm. Thus, the L/W aspect ratio of each half of the sample is 7:1. This allows end effects to be neglected and a 1-dimensional model to be applied with reasonable accuracy.

The right-hand diagram in Figure 15 shows each half of the sample divided into 4 sections of equal width. These represent the capacitors in the model. As before, the resistors represent the diffusion rate for moisture from the mid-plane of each capacitive volume to the next. The equations for calculating the R and C values for 1-D flow are indicated in the Figure.

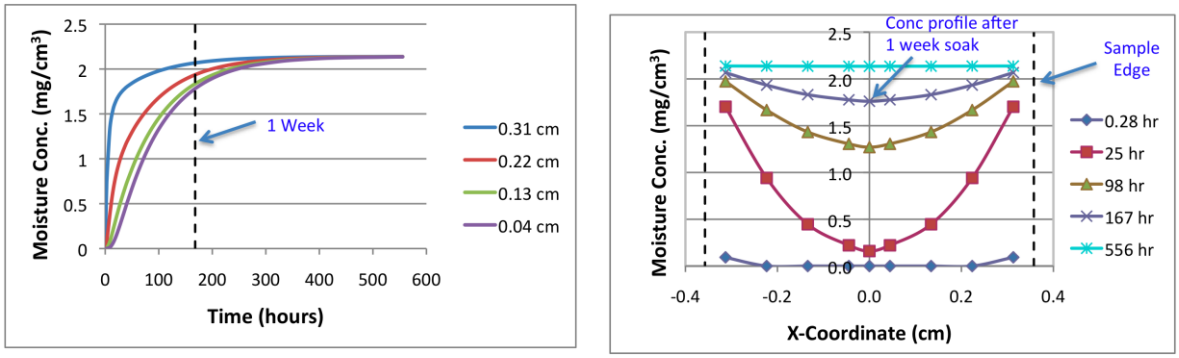

Figure 16 Calculated values of concentration at the capacitor nodes of the stripline sample versus time (LEFT) and versus x-coordinate in the sample (RIGHT) during the soak process. The stripline center conductor is centered at 0 along the x-axis.

Figure 16 shows the calculated results for the stripline sample. The right hand graph illustrates concentration profiles at various values of elapsed time. The concentration near the edges increases much more rapidly than at the center of the sample, where the stripline is located. After 1 week of exposure to the soak process, the moisture concentration of the stripline region is only about 80% of the saturated value, whereas near the sample edges it is 97%. The left hand graph shows that approximately 2 weeks of soak time is needed to saturate the sample throughout its volume.

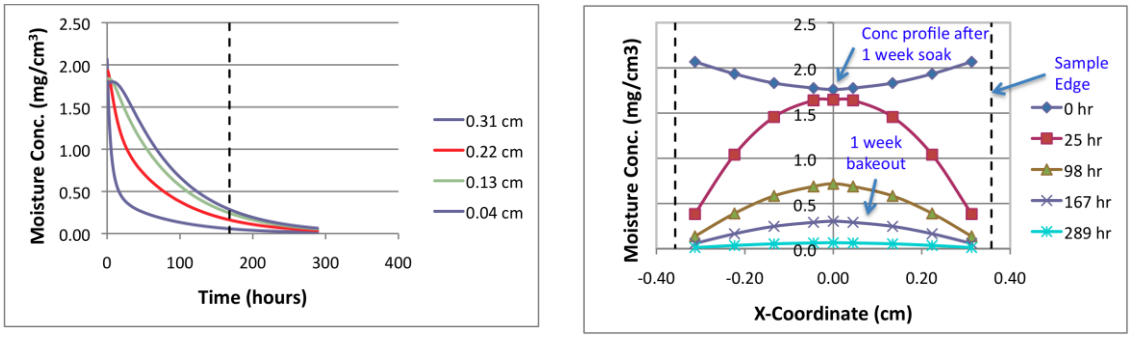

Figure 17 Calculated values of concentration at the capacitor nodes of the stripline sample versus time (LEFT) and versus x-coordinate in the sample (RIGHT) during the bakeout process.

The graph on the right in Figure 17 demonstrates the evolution of the concentration profile after the sample is placed in the bakeout oven, with an initial profile equal to the one after 1 week in soak conditions. As would be expected, the moisture will exit the sample from the edges. The concentration at the edges quickly decreases, while that at the stripline location decreases much more slowly. After 1 week in the bakeout oven, the concentration near the sample edges is only 1% of the saturated value, whereas it is 14% at the stripline location. The left hand graph indicates that nearly 300 hours of bakeout are needed to thoroughly dry the sample.

We have modeled the soak and bake process in this section and correlated it to weight measurements. Using that model, we found that the soak time and bake time used in Section 1.1 was inadequate to fully soak or bake the samples. Thus **we can expect that with full moisture penetration the impact of temperature would be further pronounced as compared to the data shown in Section 1.1.** An important implication of this finding is that **typical organic packages will most likely soak and bake on the order of days, meaning that the impact of moisture penetration on the package's electrical properties is important to characterize and understand.**

3 Method for Material Parameter Extraction

In this part, temperature-dependent, dielectric material properties will be extracted in order to correlate measurements with simulation across both temperature and frequency. With the added dimension of temperature as an input parameter, a temperature-dependent, multi-pole Debye model will be introduced to capture the dependence of the s-parameters on temperature. Specifically, using the attenuation and phase delay extracted from generalized modal s-parameters for the test structures, a library of linear scaling factors will be determined across temperature to be applied to Dk and Df. The final dielectric model will not only depend on frequency, but also on temperature.

The methodology of the fitting algorithm is illustrated in Figure 18. First, the characterization test structures are measured across frequency and temperature. Then the test structure geometry and material properties are entered into a transmission line simulator developed in Matlab™ to correlate with the measurement. The simulator has been correlated to a commercial 2D field-solver. The snowball model is used to capture surface roughness. The multi-pole Debye model is to model the frequency dependence of Dk and Df. Once good correlation is obtained at room temperature, frequency dependent Dk and Df are scaled by factors c1 and c2, respectively, for the temperature effects.

Attenuation and phase delay are used as criteria for fitting of simulation to measurement. From two different length structures, generalized s-parameters are derived to eliminate the termination reflection of the test structures. Then the complex propagation constant is obtained by post-processing the generalized S parameter. Finally, attenuation constant (α) and phase delay (phase constant β / angular frequency ω) across frequency are used as the two fitting criteria. The fitting criteria minimize both the average error of propagation constant and phase delay. In simulation, copper conductivity's temperature dependency is included. At each temperature point, a two objective optimization with two design parameters (c1, c2) is carried out until both fitting criteria are satisfied. After fitting all the temperature points, temperature dependent scaling factors, c1(T) and c2(T), are obtained at each temperature point. The material properties can then be recalculated at any temperature, T_2, using these scaling factors:

$$Dk_2(T_2, f) = Dk_{room\text{-}temperture}(f) * c1(T_2)$$
$$Df_2(T_2, f) = Df_{room\text{-}temperature}(f) * c2(T_2)$$

Ultimately the fitting process provides a set of linear scaling factors of Dk and Df, one for each temperature point. This provides engineers with a simple way to account for temperature effects in their simulation environment.

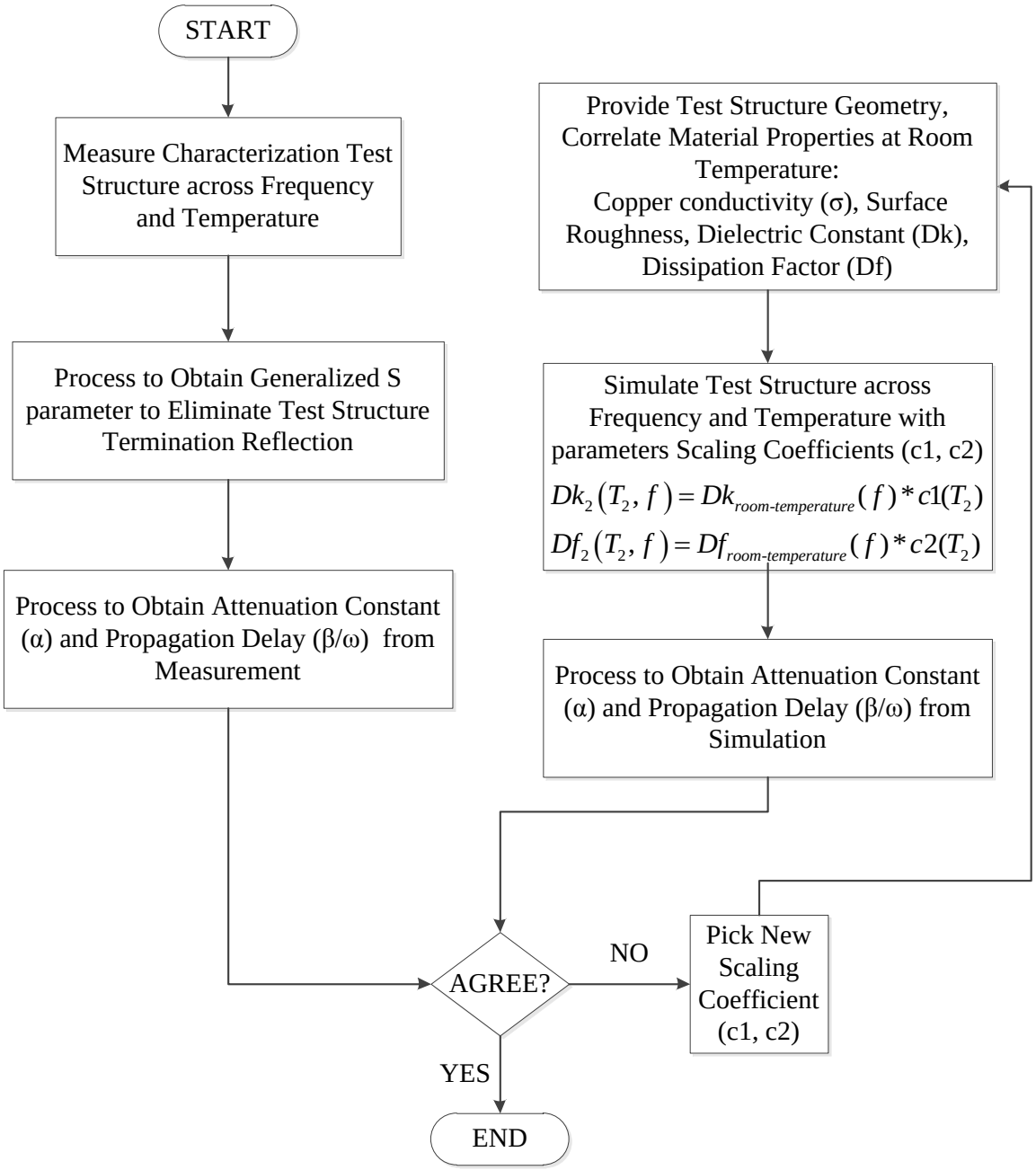

Figure 18 Flow Chart illustrating the fitting algorithm to obtain temperature dependent material properties scaling factors

In the following figures, we show the methodology shown in Figure 18 applied to the materials measured in Section 1, including Material A and Material B. Figure 19 shows the temperature dependent scaling factors for Dk and Df and the average and peak fitting errors for both attenuation constant and phase delay for Material B. The nominal Dk and Df values at 1 GHz are 4.063 and 0.005, respectively. The average and peak errors are low and show little variation across temperature.

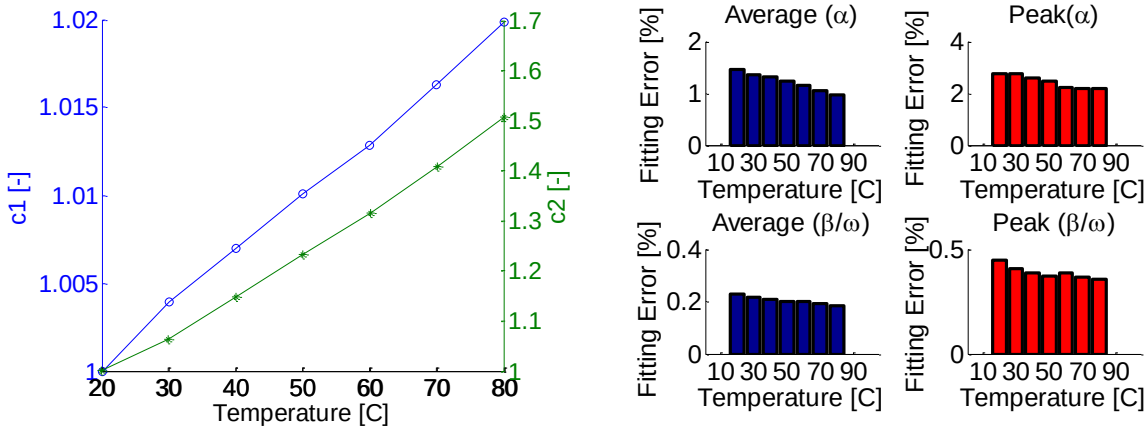

Figure 19 Temperature dependent scaling factors for Dk (c1) and Df (c2) (LEFT) and fitting errors of attenuation constant and phase delay (RIGHT) for Material B. Note that the average error is the average point-by-point deviation between the measured and simulated data. Peak error is maximum error at any point between the measured and simulated data.

For the packaging Material A, Figure 20 shows the temperature dependent scaling factor for both baked and soaked case. Figure 21 shows the fitting errors for both cases. The nominal Dk and Df values at 1 GHz are 3.614 and 0.016 for baked case and 3.640 and 0.0196 for soaked case, respectively. The fitting errors are small.

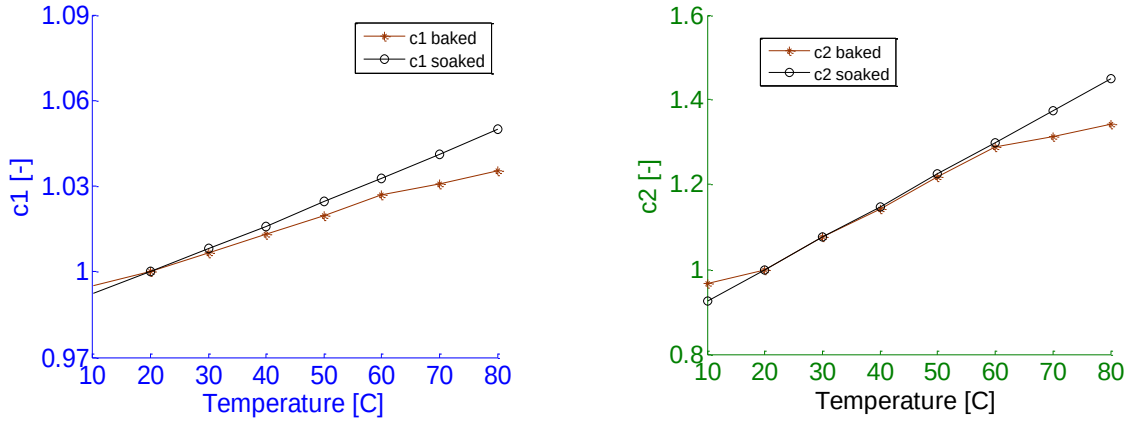

Figure 20 Temperature dependent scaling factors for Dk (c1) (LEFT) and Df (c2) (RIGHT) for Material A baked and soaked case.

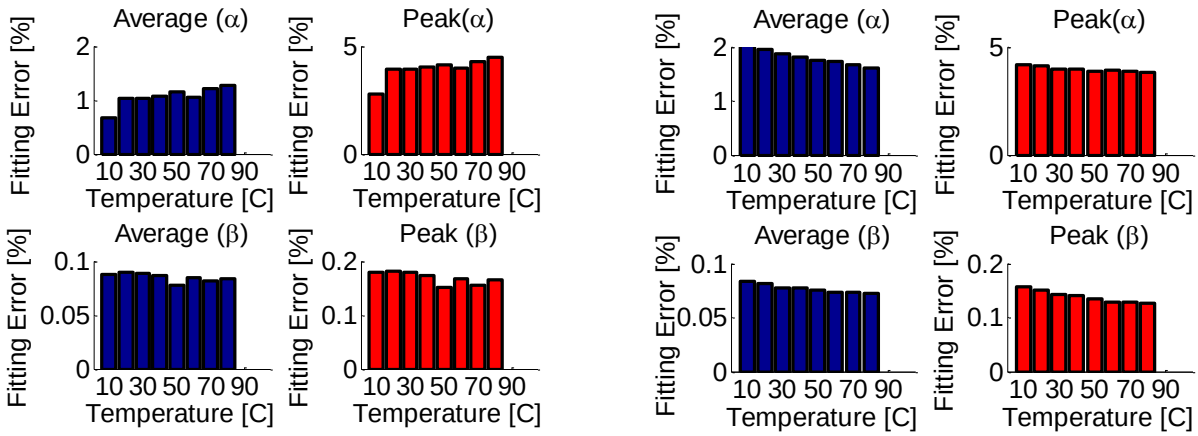

Figure 21 Fitting errors of the attenuation constant and phase delay for Material A baked (LEFT) and soaked (RIGHT) case.

Figure 22 shows an example of the fitting that is achieved across temperature. Specifically, the fitted attenuation constant and phase delay from both measurement and simulation are compared at low and high temperature for the Material A soaked case. Similar quality fits were achieved across temperature.

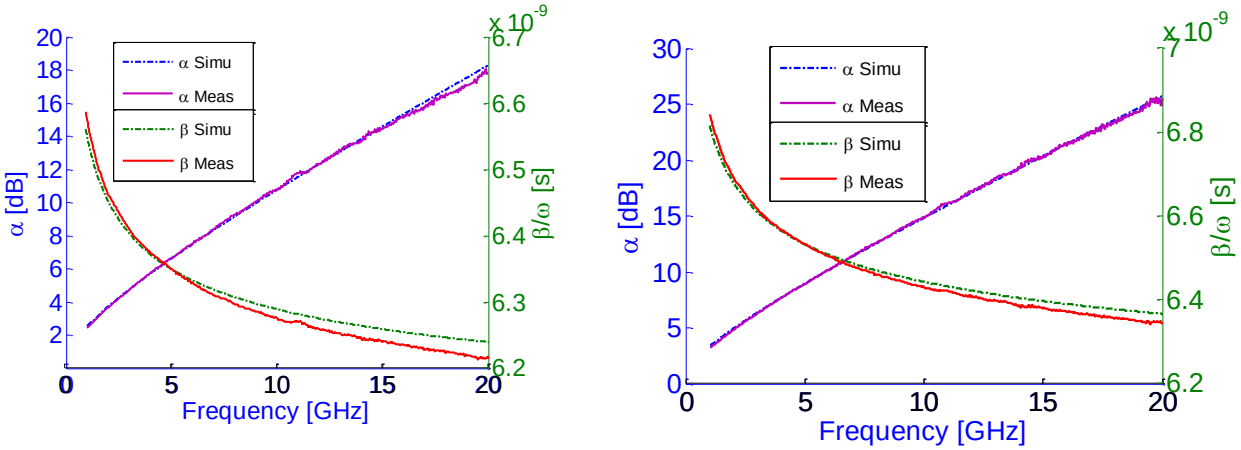

Figure 22 Attenuation and phase delay fit between measurement and simulation at low temperature of 5 ˚C (LEFT) and high temperature of 100 ˚C (RIGHT) for Material A soaked case.

The Matlab™ transmission line simulator includes the effects of copper loss dependency on temperature. In Figure 23, the insertion loss is plotted at 20 ˚C and 100 ˚C with and without considering the temperature dependent copper losses. We see that the temperature dependent copper losses are insignificant compared to the temperature dependent dielectric losses at 100 ˚C but still contribute to the overall losses at 20 ˚C. **Thus, only capturing the change in copper conductivity across temperature is inadequate to accurately capture temperature dependent effects in this material.**

Note that we assume here that although copper conductivity changes with temperature, surface roughness does not.

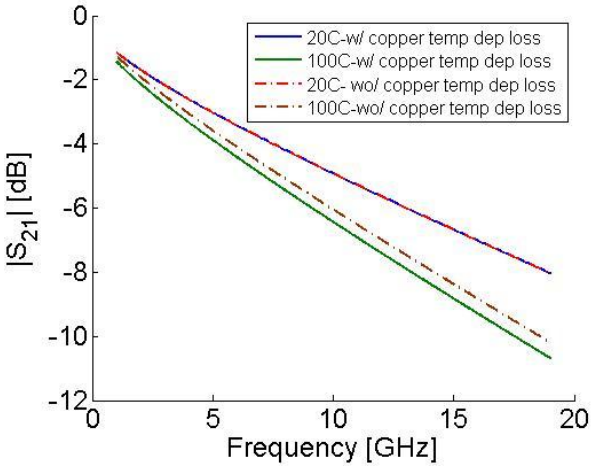

Figure 23 Simulated insertion losses with and without considering temperature dependent conductive loss at 20 ˚C and 100 ˚C for the Material A soaked case.

4 New Method for Capturing Temperature Dependent Effects in Solved S-parameters

Quite often solved package s-parameter files are provided from vendors at a given extraction temperature, usually room temperature. If we wish to include the effects of temperature into our channel simulations we typically aren't able to resimulate the package with new material parameters because we don't have access to the original simulation project. In this section **we present a new method for including the effects of temperature directly without resolving for the s-parameters.**

We do require some limited information to proceed. We assume that we have access to the length of the packaging trace ($\boldsymbol{\ell}$), the nominal trace and stackup dimensions, an estimate of the dielectric constant and loss at the original simulation temperature (T_1) (typically room temperature) and the new temperature point (T_2) and the copper conductivity at the new temperature point (σ_2). Note that one quick way to estimate Dk_2 and Df_2 at the new temperature point is to linearly scale them based on the equations shown in Section 3 for your particular material or a similar material.

At a high level, the method works as follows: we perform a field-solver analysis of a uniform transmission line of length $\boldsymbol{\ell}$ using Dk_1, Df_1 and σ_1 that has the same nominal cross section and stackup as the package. We then perform a second field-solver analysis of a uniform transmission line of length $\boldsymbol{\ell}$ using Dk_2, Df_2 and σ_2 (the material properties at the new temperature point). From this information we are able to scale the supplied s-

parameter file from the baseline temperature, T_1, to the new temperature point, T_2, and account for temperature effects.

This method is an approximation. It assumes that the characteristic impedance of the line does not change much with temperature (which is consistent with what we see in Figure 6). It also assumes that any discontinuities in the signal path are minor.

The derivation for this approximation is as follows. Let A be the ABCD matrix of this nominal transmission line and S the s-parameter matrix.

The ABCD matrix of a lossy transmission line is defined as:

$$\mathrm{A}(\omega,\ell,T)=\begin{bmatrix}\cosh(\gamma(\omega,\mathrm{T})\cdot\ell) & \sinh(\gamma(\omega,\mathrm{T})\cdot\ell)\cdot\mathrm{Z}(\omega,T)\\ \sinh(\gamma(\omega,\mathrm{T})\cdot\ell)/\mathrm{Z}(\omega,T) & \cosh(\gamma(\omega,\mathrm{T})\cdot\ell)\end{bmatrix} \quad (1)$$

where $\mathrm{Z}(\omega,T)$ is the characteristic impedance and $\gamma(\omega,\mathrm{T})$ is the propagation coefficient.

At temperature T_1:

$$\mathrm{A}^{\mathrm{calib}}(\omega,T_1)=\mathrm{s2abcd}(\mathrm{S}^{\mathrm{calib}}(\omega,T_1))$$

$$\gamma(\omega,T_1)=\frac{\operatorname{acosh}\left(\sqrt{\mathrm{A}_{1,1}^{\mathrm{calib}}(\omega,T_1)*\mathrm{A}_{2,2}^{\mathrm{calib}}(\omega,T_1)}\right)}{\ell_{calib}} \quad (2)$$

$$Z(\omega,T_1)=\sqrt{\frac{\mathrm{A}_{1,2}^{\mathrm{calib}}(\omega,T_1)}{\mathrm{A}_{2,1}^{\mathrm{calib}}(\omega,T_1)}} \quad (3)$$

where s2abcd is the conversion between s-parameters and the ABCD matrix. At T_2, the new temperature point, we do the same calculations:

$$\mathrm{A}^{\mathrm{calib}}(\omega,T_2)=\mathrm{s2abcd}(\mathrm{S}^{\mathrm{calib}}(\omega,T_2))$$

$$\gamma(\omega,T_2)=\frac{\operatorname{acosh}\left(\sqrt{\mathrm{A}_{1,1}^{\mathrm{calib}}(\omega,T_2)*\mathrm{A}_{2,2}^{\mathrm{calib}}(\omega,T_2)}\right)}{\ell_{calib}} \quad (4)$$

$$Z(\omega,T_2)=\sqrt{\frac{\mathrm{A}_{1,2}^{\mathrm{calib}}(\omega,T_2)}{\mathrm{A}_{2,1}^{\mathrm{calib}}(\omega,T_2)}} \quad (5)$$

To compute an approximation for the s-parameters for any line with the same pitch including discontinuities at temperature T_2, we use the trace length $\ell^{measured}$ and compute:

$$\mathrm{A}^{\mathrm{measured}}(\omega,T_1)=\mathrm{s2abcd}(\mathrm{S}^{\mathrm{measured}}(\omega,T_1))$$

$$A^{approx}(\omega,T_2)=A(\omega,\ell^{measured},T_2)\cdot A(\omega,\ell^{measured},T_1)^{-1}A^{measured}(\omega,T_1)$$

$$S^{approx}(\omega, T_2) = \text{abcd2s}(A^{approx}(\omega, T_2))$$

where $A(\omega, \ell^{measured}, T_2)$ and $A(\omega, \ell^{measured}, T_1)$ are computed using Equation 1 with $\gamma(\omega, T)$ from Equations 2 and 4; $Z(\omega, T)$ from Equations 3 and 5.

Note that the approximation is guaranteed to be passive as long as the measured parameters are passive because the determinant of the ABCD matrix defined in Equation 1 is algebraically identical to 1.

As a test of this method we solved for the s-parameters for a uniform transmission line at 20 ˚C and at 100 ˚C. The stripline length of both models is 50 mm. Dk_2 and Df_2 at 100 ˚C were approximated based on the coefficients extracted in Section 3 for Material A. We then assume that the s-parameter file we wish to scale to a new temperature consists of a 25-mm trace, a core packaging via and another 25-mm trace. The core via is 0.8 mm in height, typical of a build up organic package. In this test case, we have the ability to simulate all four cases to examine how the s-parameters change across temperature. Namely, Figure 24 (LEFT) shows the uniform stripline at both 20 ˚C and 100 ˚C and (RIGHT) shows the non-uniform stripline at both 20 ˚C and 100 ˚C.

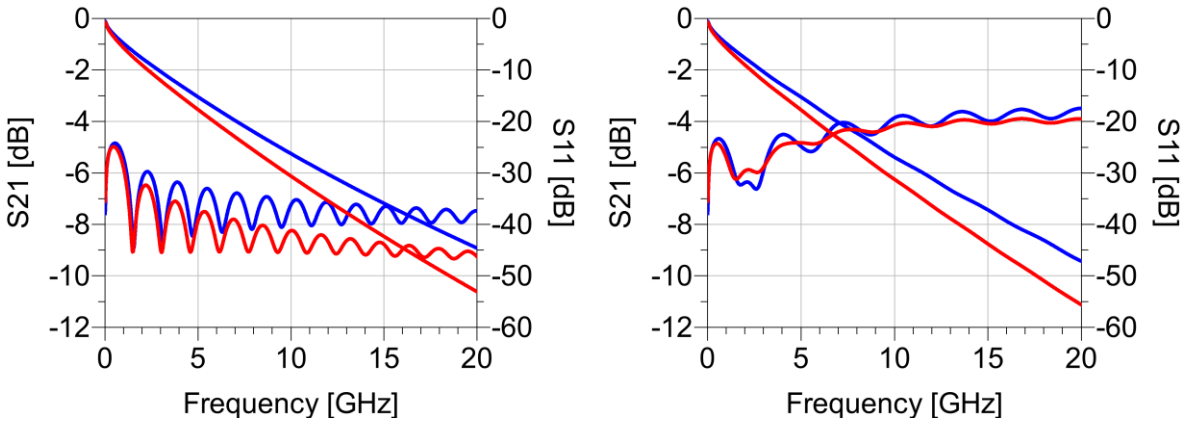

Figure 24 (LEFT) plots the uniform stripline simulation at both 20 ˚C (blue) and 100 ˚C (red) and (RIGHT) plots the non-uniform stripline simulation at both 20 ˚C (blue) and 100 ˚C (red).

Next, the test methodology consists of scaling the 20 ˚C non-uniform s-parameters to 100 C based on the change in γ of the uniform stripline between 20 ˚C and 100 ˚C. All three touchstone files are fed into a Matlab™ script which applies the above equations. Figure 25 plots the results (LEFT) in black compared to a simulation of the 100 ˚C non-uniform stripline. We see that the scaling methodology comes introduces some inaccuracies but overall does an excellent job of capturing the temperature dependent losses.

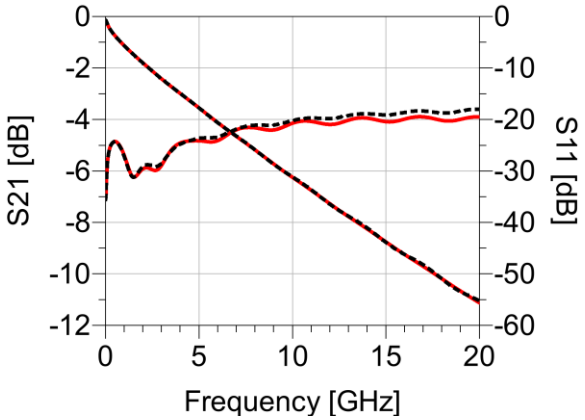

Figure 25 Non-uniform stripline simulation at 100 C, simulated (red) and scaled (black dotted).

5 Impact of Temperature on Signaling Performance

At the end of the day, engineers want to understand the impact of temperature and humidity on signaling performance (i.e. with drivers, receivers and realistic channels). **Package models are typically extracted and modeled at room temperature 20 C and yet packages are typically used in a much hotter environment. As we have seen copper conductivity decreases and dielectric loss increases significantly at higher temperatures.** In this section we quantify the impact of temperature on signaling performance using channel simulations at 2.5Gb/s, 5.0Gb/s and 8.0Gb/s. Channel simulations were performed using the measured package s-parameters from Section 1 at the driver and receiver with two different PCB channel lengths: a short channel (2-inches) and a long channel (20-inches). The channel was standard FR-4 material and was kept at room temperature. Constant throughout these simulations is -3.5 dB of de-emphasis at the transmitter and a CTLE at the receiver. All simulations were performed using a commercial channel simulator.

Figure 26 shows the eye diagrams for a 2.5Gb/s transmitter with a 2-inch channel (LEFT) and 20-inch channel (RIGHT). There are two eye diagrams plotted; the blue eye diagram is with both the driver and receiver package at 20 ˚C and the red is at 100 ˚C. At 2.5Gb/s we observe a slight closure of the eye height (10-15%) when accounting for the higher package temperatures.

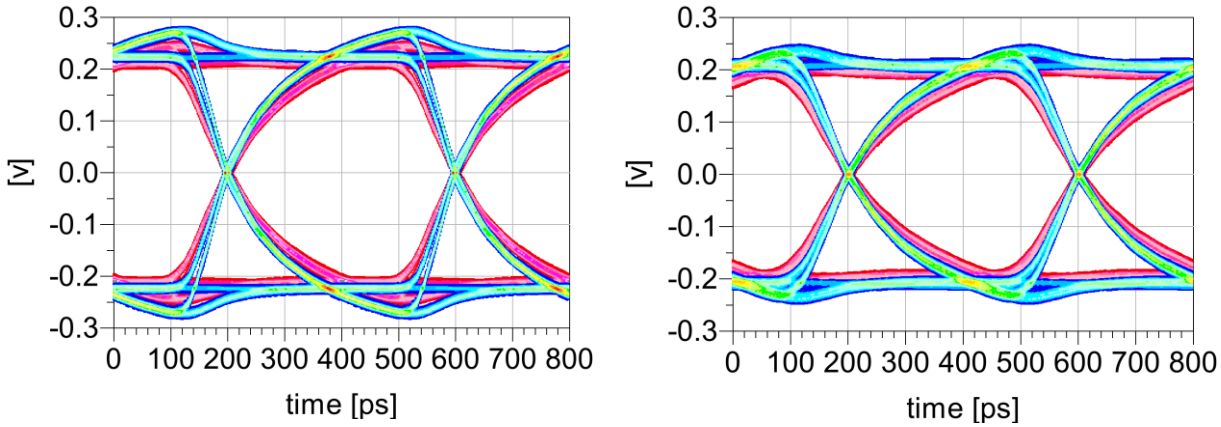

Figure 26 Eye diagrams for 2.5 Gb/s transmitter with a 2-inch FR-4 channel (LEFT) and a 20-inch FR-4 channel (RIGHT). The 50-mm transmitter and receiver package model are at 20 ˚C (BLUE) and 100 ˚C (RED).

Figure 27 shows the eye diagrams for a 5.0Gb/s transmitter with the same channel length at the previous case. Again, the blue eye diagram is with both the driver and receiver package at 20 ˚C and the red is at 100 ˚C. With the increase in data rate we are seeing a growing difference between the 20 ˚C and 100 ˚C eye diagrams. Using the 100 ˚C package models, the eye height is about 20-25% smaller than the 20 ˚C case and we are beginning to see some eye-width closure as well.

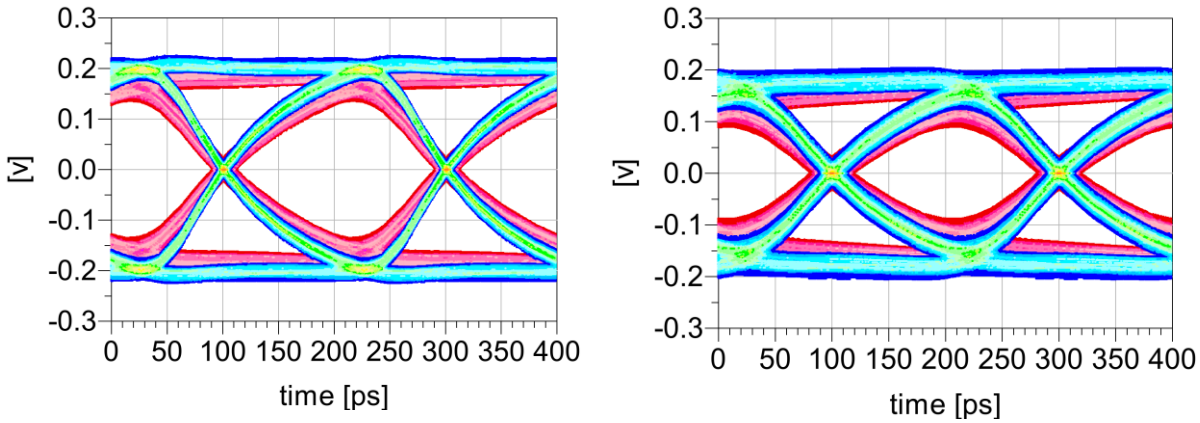

Figure 27 Eye diagrams for 5.0 Gb/s transmitter with a 2-inch FR-4 channel (LEFT) and a 20-inch FR-4 channel (RIGHT). The 50-mm transmitter and receiver package model are at 20 ˚C (BLUE) and 100 ˚C (RED).

Finally, Figure 28 shows the eye diagrams for a 8.0Gb/s channel. At this data rate there is a substantial impact on the eye width and height due to the 100 C package models. The percentage degradation in eye height and width is shown in Figure 29 and Figure 30, respectively. Although there is little degradation in eye width, there is significant impact on the loss which increases with increasing data rates. This is consistent with the findings in Figure 4 which showed that the relative loss due to temperature effects increases with increasing frequency. Figure 31 show the mixed mode s-parameters for the short and long

channels with the 20 ˚C and 100 ˚C package models. From this we can see that jitter due to impedance mismatch and eye width closure is minimized because return loss is not significantly impacted by temperature. This is also consistent with the data provided in Figure 6.

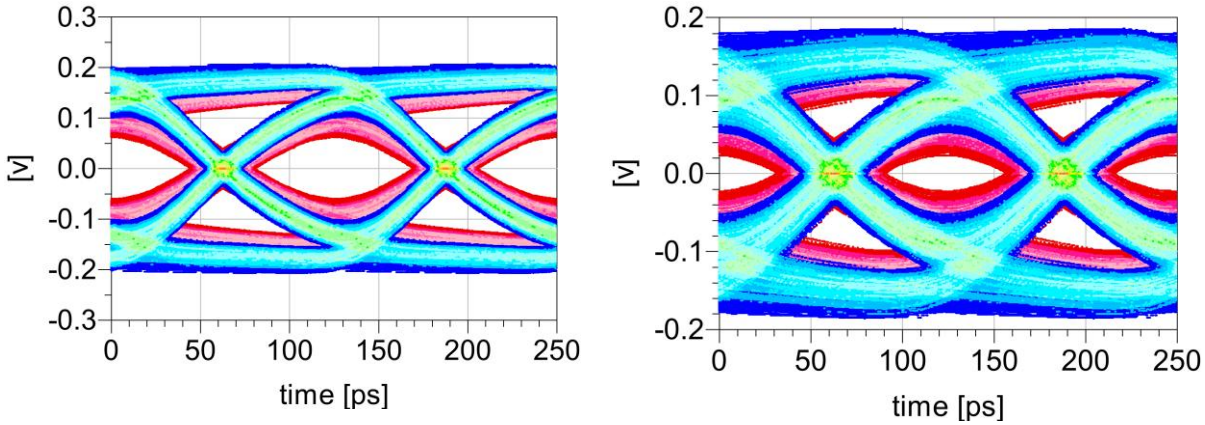

Figure 28 Eye diagrams for 8.0 Gb/s transmitter with a 2-inch FR-4 channel (LEFT) and a 20-inch FR-4 channel (RIGHT). The 50-mm transmitter and receiver package model are at 20 ˚C (BLUE) and 100 ˚C (RED).

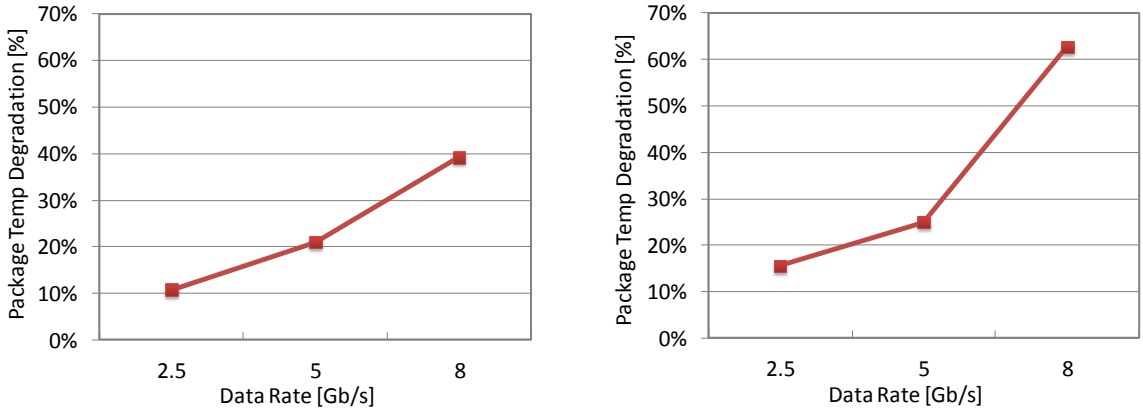

Figure 29 Degradation in eye height due to temperature-dependent losses in the package shown for 2.5, 5.0 and 8.0 Gb/s channel simulations with a 2-inch FR-4 channel (LEFT) and a 20-inch FR-4 channel (RIGHT).

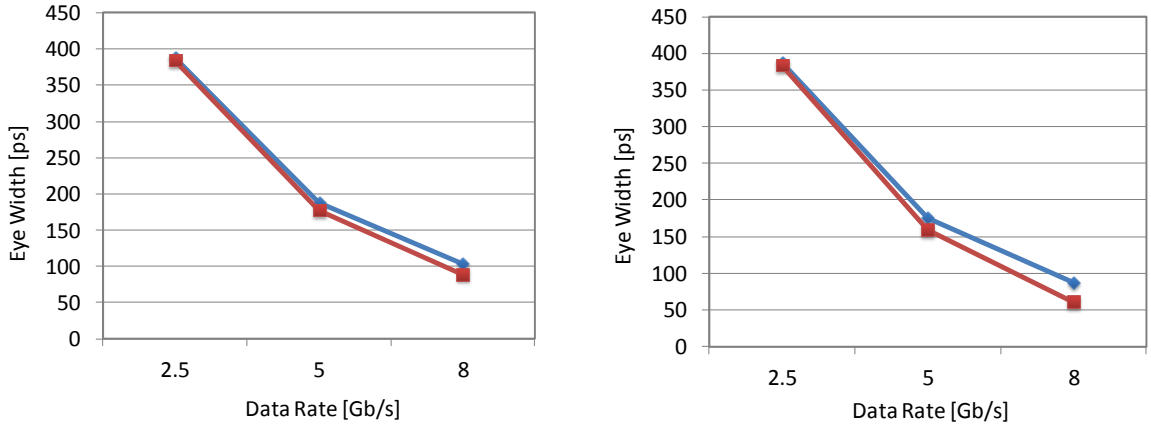

Figure 30 Degradation in eye width due to temperature-dependent losses in the package shown for 2.5, 5.0 and 8.0 Gb/s channel simulations with a 2-inch FR-4 channel (LEFT) and a 20-inch FR-4 channel (RIGHT).

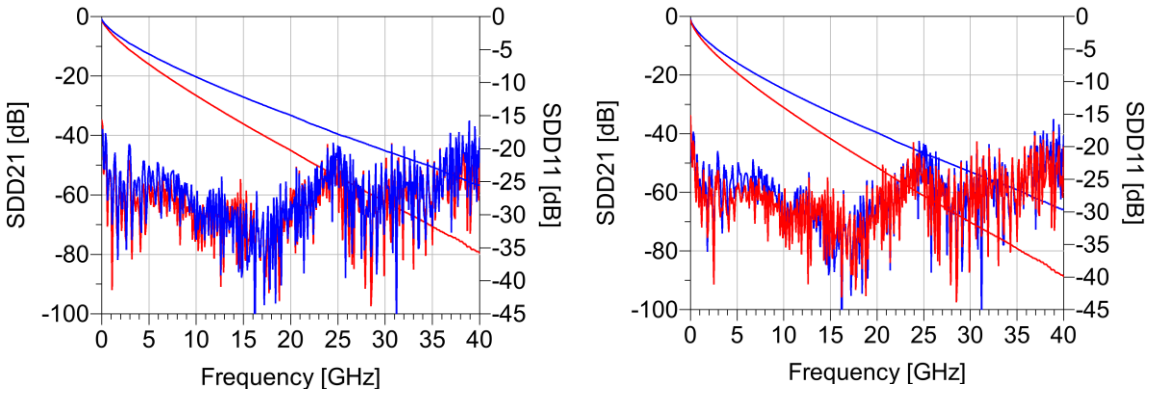

Figure 31 Mixed-mode s-parameters for a 2-inch FR-4 channel (LEFT) and 20-inch FR-4 channel (RIGHT). The 50-mm transmitter and receiver package models are at 20 ˚C (BLUE) and 100 ˚C (RED).

Finally, Figure 32 shows the eye height relative to the PCI express specification for Gen 1, Gen 2 and Gen 3 for the 2 inch channel (LEFT) and the 20-inch channel (RIGHT). The increasing losses due to temperature effects consistently degrade the overall margin. More worrisome is that **as data rates increase, the losses due to temperature increase on a percentage basis while simultaneously operating margins decrease. This stresses the importance of including temperature dependent effects in channel simulations for 8Gb/s and beyond.**

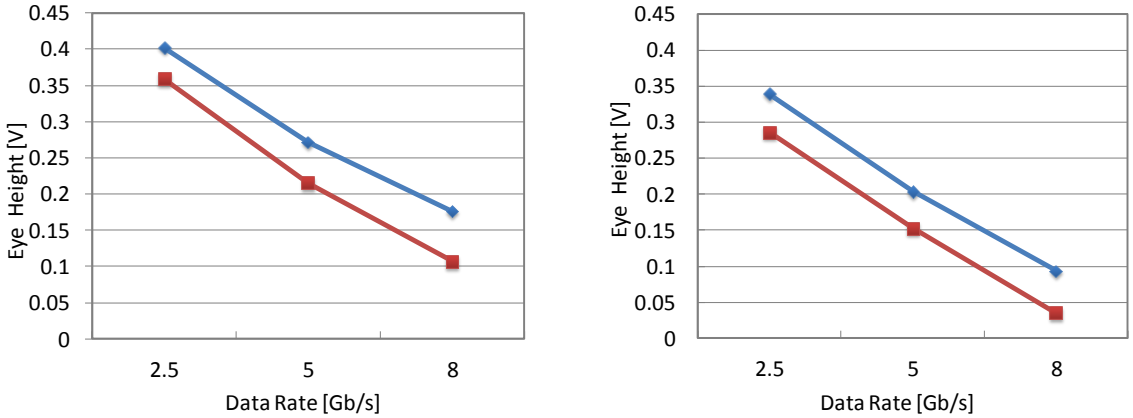

Figure 32 Eye height for 2.5, 5.0 and 8.0 Gb/s channel simulations with a 2-inch FR-4 channel (LEFT) and a 20-inch FR-4 channel (RIGHT). The 50-mm transmitter and receiver package model are at 20 ˚C (BLUE) and 100 ˚C (RED).

Summary

This paper has examined the impact of temperature and humidity on typical organic packaging and PCB materials. The findings and key take-home points of this paper are summarized below, grouped by section.

Measurement data

- The dielectric loss was found to be a fairly strong function of temperature for the packaging material. By comparison, the dielectric loss of low-loss PCB material showed less sensitivity to temperature.
- The variation of the dielectric constant over temperature is relatively moderate for all the packaging and PCB materials characterized.
- In all cases, the presence of moisture accentuates the temperature dependence of the complex permittivity.
- As frequency increases, the loss variation across temperature increases. For the packaging material, we see at 16 GHz, there is about a 25% increase in loss at 100 ˚C.

Temperature-moisture modeling

- A new model was developed for moisture penetration into organic packages that correlates nicely to measurements.
- Typical organic packages will most likely soak and bake on the order of days, meaning that the impact of moisture penetration on the package's electrical properties is important to characterize and understand.

Electrical modeling

- A fitting algorithm was presented which provides a set of linear scaling factors for Dk and Df, one for each temperature point. This provides engineers with a simple way to account for temperature effects in their simulation environment.
- Package models are typically extracted and modeled at room temperature 20 C although packages are typically used in a much hotter environment. Copper conductivity decreases and dielectric loss increases significantly at higher temperatures.
- A novel method for including the effects of temperature directly on solved s-parameters was provided.
- Simply adjusting the copper conductivity across temperature is not adequate to accurately capture temperature dependent effects for the packaging structures.

System simulations

- As data rates increase, the losses due to temperature effects increase while simultaneously operating margins decrease. This stresses the importance of including temperature dependent effects in channel simulations for 8Gb/s and beyond.

Acknowledgements

The authors would like to thank Ivor Barber, Farshad Ghahghahi and Dan Gerlach of LSI for supporting this work, Greg Lee for making the sample weight gain/loss measurements and Jeff Klemovage for laying out the test structures. The authors would also like to thank Theresa Sze of Oracle and Keith Newman of Hewlett-Packard for their support.

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