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Determining PCB Trace Impedance by TDR: Challenges and Possible Solutions

Istvan Novak, Oracle Corp.
Ying Li, Oracle Corp.
Eben Kunz, Oracle Corp.
Sarah Paydavosi, Oracle Corp.
Laura Kocubinski, Oracle Corp.
Kevin Hinckley, Oracle Corp.
Alexander Nosovitski, Oracle Corp.
Nathaniel Shannon, Oracle Corp.
Jason Miller, Oracle Corp.
Gustavo Blando, Oracle Corp.

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Abstract

It is common practice for board fabricators to perform TDR measurements on test coupons or on system traces to see how the impedance specs are met. This information is later provided in a first-article-inspection report to customers for final approval. Since this measurement is done on the production flow, it needs to be simple and robust. With the widespread use of gigabit interconnects, we now have a better understanding of the transmission-line details and complex frequency-dependent losses. So, we have to wonder: How important or useful are TDR measurements now? How is the impedance really measured, and how is the single impedance number extracted? Do all vendors use the same setup and process? Do we introduce systematic errors just because of the way the measurement is done and the data is post-processed? This paper attempts to answer these questions, and to provide a practical way to post-process the TDR measurement data to make it more relevant for today's applications.

Author(s) Biography

Istvan Novak is a Senior Principle Engineer at Oracle. Besides signal integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is a Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies.

Eben Kunz graduated from MIT in 2012 with a BS and Master's in EE. His thesis project was the design and construction of analog processing components for a low frequency radio telescope. He joined Oracle in May 2012, and has been working on simulation and modeling of high-speed interconnects.

Sarah Paydavosi is a hardware engineer at Oracle Corp. Her current work focuses on signal integrity modeling, analysis, and validation in Oracle's MicroElectronics ASIC and SoC IP group. She received her PhD in electrical engineering from Massachusetts Institute of Technology.

Laura J. Kocubinski is a hardware engineer at Oracle Corp. She currently works on signal integrity within Oracle's SPARC T-Series server division. She recently received her BSEE, with a technical concentration in signal processing, from Rensselaer Polytechnic Institute.

Ying Li is a Hardware Engineer at Oracle Corporation where she works on signal and power integrity of ASIC packaging interconnects simulation and measurement validation. In previous graduate studies, her research work focused on computational electromagnetics, sensitivity analysis and optimization. She received her Masters degree in electrical engineering from McMaster University. She is pursuing her Ph.D. degree at University of Washington.

Kevin Hinckley is a Principal Signal Integrity Engineer at Oracle with more than 15 years in the industry. Kevin has spent the last 12 years at Oracle in various product design groups and is currently responsible for all aspects of signal integrity modeling, analysis and validation for Oracle's x86 based servers. Before Oracle, Kevin worked in the Defense Industry with a focus on semiconductor device modeling, simulation and measurement. He received a BSEE from Rensselaer Polytechnic Institute.

Alexander Nosovitski is a Principal Signal Integrity Engineer at Oracle Corporation with more than 12 years in the industry. Alex has spent the last 8 years at Oracle and is currently responsible for signal integrity modeling, analysis and validation for Oracle's x86 based servers. He received a BSEE from Northeastern University and MSSE from Brandeis University.

Nathaniel Shannon is a Signal Integrity Hardware Engineer at Oracle Corporation. He is responsible for the development of signal integrity modeling and simulations of high speed serial and parallel buses as well as simulations of power distribution networks. He received his M.S. from Northeastern University.

Jason R. Miller is a Principle Hardware Engineer at Oracle Corporation where he works on ASIC development, ASIC packaging, interconnect modeling and characterization, and system simulation. He has published over 40 technical articles on the topics such as high-speed modeling and simulation and co-authored the book "Frequency-Domain Characterization of Power Distribution Networks" published by Artech House. He received his Ph.D. in electrical engineering from Columbia University.

Gustavo J. Blando is a Principle Hardware Engineer with over ten years of experience in the industry. Currently at Oracle Corporation, he is responsible for the development of new processes and methodologies in the areas of broadband measurement, high speed modeling and system simulations. He received his M.S. from Northeastern University.

I. Introduction and background

In high-speed signaling it is critical to maintain the impedance of the passive channel within predefined limits throughout its entire length. In the design phase this is usually achieved in the frequency domain, by making sure that each component meets its Reflection Loss (RL) specifications. While for the linear and time invariant printed-circuit board (PCB) traces the frequency or time-domain design and validation approaches can be used inter-changeably, on the PCB production floor, for reasons of simplicity and robustness, the most widely used impedance test method is Time Domain Reflectometry (TDR).

For a single stretch of uniform and low-loss interconnect the voltage reflection coefficient of the TDR response can be converted directly to impedance. This approach has been in use for decades and still today it is the most widely used production-floor test method for printed circuit boards [1]. The actual trace impedance on a real production board, however, will never be completely uniform, and losses today may be high enough that it may make the simple evaluation of the TDR result confusing and/or challenging.

First, it is well known that the characteristic impedance of a lossy interconnect (even if it is uniform) is a complex function of frequency. In calculations, the frequency-dependent characteristic impedance can be obtained from the per-unit-length interconnect parameters; in testing, the Generalized Modal S-Parameter method (GMS) uses the frequency dependent characteristic impedance [2]. With finite dielectric and conductive losses, the magnitude of the characteristic impedance has a shallow minimum at medium frequencies and rises both at lower and higher frequencies. The same losses in the time domain may create a similar signature: after an initial down-slope there is a minimum, followed by a monotonic rise until the end of the round-trip delay, beyond which point the response depends on how the far end is terminated. With finite losses involved, we already face a major question: regardless of whether we use frequency or time domain data, which value(s) do we use in test and validation to compare against our allowed impedance limits?

Second, on a real PCB there are several factors making the impedance of the fabricated traces different from the target value and vary from location to location along the trace and vary also from board to board: etching imperfections and non-uniformities, variations in dielectric thickness and dielectric constant of laminate materials, glass-weave effect, etc. Vias connecting traces on inner layers to the surface create additional discontinuities and furthermore material variations near traces will have an impact on their electrical characteristics. For instance, the presence of closely spaced vias, pads, floating metal shapes, or in the contrary, voids in the reference planes will change the characteristic impedance locally. Some of these disturbances may occur uniformly in a given portion of the trace, creating gradual or step-like changes in the impedance profile. When the actual trace becomes a cascaded series of lumped discontinuities and trace segments with different impedances, peeling algorithms can be applied to back-calculate the impedance of each segment [3]. In the general case, unfortunately, when the impedance and loss characteristics of the cascaded

segments are all unknown, we don't have enough data points to get a unique solution just from TDR and Time Domain Transmission (TDT) measurements at the end points. When discontinuities and losses are present, the bandwidth (rise time) of the TDR stimulus also becomes important.

While time-domain TDR profile and frequency-domain RL response are basically the same data, just presented in different forms, people find the TDR profile more helpful in identifying potential design flaws [4] and locating manufacturing defects; whereas the frequency-domain RL data is usually more convenient to compare against masks and target functions, but may be harder to use it for debugging purposes. In recent years several new IPC standards emerged (SPP, RIE, EBW), targeting the characterization of PCB traces [5]. SET2DIL aims to characterize differential traces with a combined TDR-TDT approach [6].

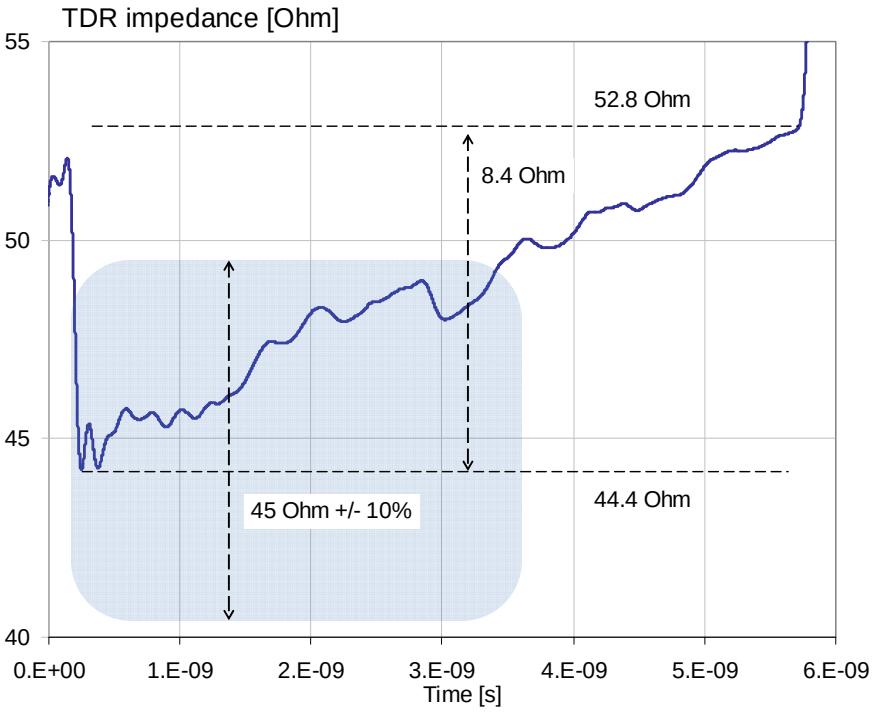

Figure 1: *Measured TDR response of a long trace with nominal 45-ohm impedance target, +-10% tolerance.*

Take for instance the TDR plot shown in Figure 1. The TDR response starts a little below 45 ohms, and reaches up to 52.8 ohms at the end. The total variation is 8.4 ohms, and the TDR response exceeds the 45 ohms +10% limit in its second half. Is this trace acceptable; is it within the specification limits?

This paper will look at current test methodologies and the range of PCB trace parameters we typically use today. Interactions of conductive and dielectric losses, non-uniformities, discontinuities and measurement rise time will be summarized. The data presented in this paper is

for PCB traces, but the concepts, challenges and potential solutions are equally applicable to packages and cables. Finally simple correction algorithms will be explored, which may allow the reduction of TDR-response tilt due to losses, thus allowing for a more direct comparison against impedance specifications.

II. Performance of uniform transmission lines

Uniform and loss-less transmission lines can be described by their per-unit-length capacitance and inductance: C_u and L_u, or by their full-length capacitance and inductance, C and L. With these two parameters we can calculate the two most widely used metrics for transmission lines: characteristic impedance (Z_o) and the per-unit-length propagation delay (t_{pd_u}):

$$Z_o = \sqrt{\frac{L_u}{C_u}} = \sqrt{\frac{L}{C}};\ \ t_{pd\_u} = \sqrt{L_u C_u};\ t_{pd} = \sqrt{LC} \tag{1}$$

With no losses, Z_o and t_{pd} are frequency independent and real numbers. When we have a single stretch of uniform transmission line with Z_o and t_{pd} parameters, connected to a TDR instrument, we will measure the incident wave superimposed with the reflected waves, where the ratio of the reflected and incident waves is called the Voltage Reflection Coefficient, commonly denoted by Γ. For a single reflection, it can be calculated as:

$$\Gamma = \frac{Z_0 - Z_{ref}}{Z_0 + Z_{ref}} \tag{2}$$

Where Z_0 is from (1) and it is the impedance of the transmission line to be measured by the TDR instrument. Z_{ref} is the reference impedance of the instrument, commonly 50 Ohms. When we read the Γ value from a TDR instrument, we can rearrange (2) to give us the Z_0 impedance of the transmission line.

$$Z_0 = \frac{1+\Gamma}{1-\Gamma} \tag{3}$$

We have to keep in mind that in this simple form (3) works only if the Device Under Test (DUT) we measure with the TDR instrument has a frequency independent, constant impedance. When the DUT is a board or package trace, or cable, this means it would need to have negligibly low loss.

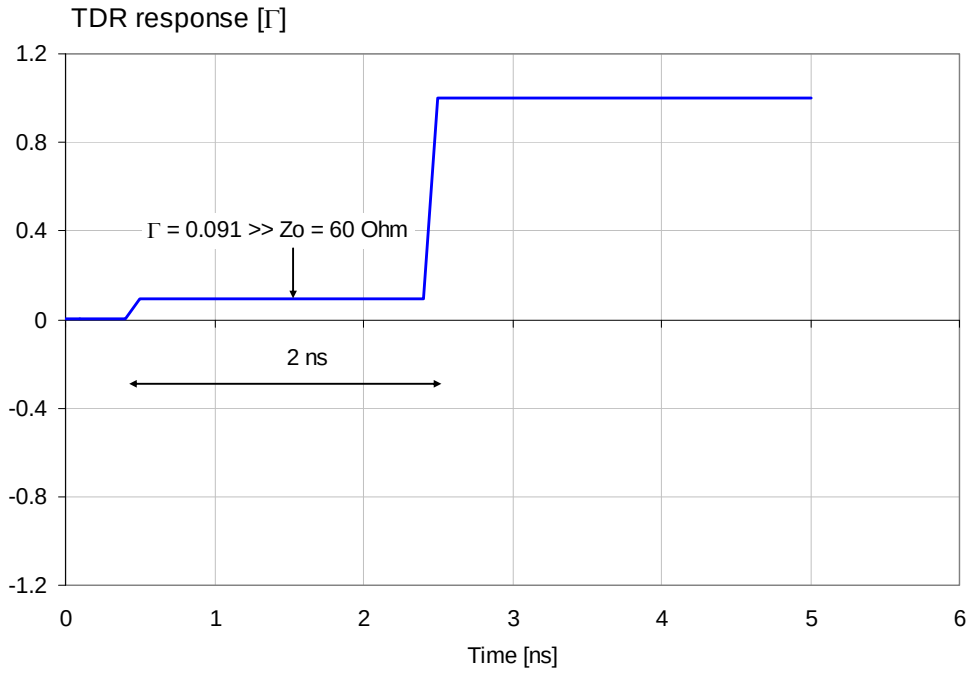

Figure 2: *TDR response of a 60-ohm ideal loss-less transmission line with 1-ns t_{pd}, measured with a Z_{ref} = 50-ohm reference impedance.*

Figure 2 shows a simple example, when the direct inversion of (2) works. It assumes a single uniform transmission line with 60-ohm characteristic impedance, open far-end termination, 1-ns propagation delay, and negligible loss. Since the TDR instrument shows the waveform at the input, the reflection plateau is twice the length of the propagation delay.

When losses cannot be neglected, the transmission line, even if it is uniform over its full length, will have a frequency dependent characteristic impedance and time-dependent TDR response. Instead of inductance, we deal with inductance and series (conductive) resistance. Instead of capacitance, we deal with capacitance and parallel (dielectric) conductance. Instead of only L and C, we now have four parameters: R, L, G and C. Finally, in most practical cases, all four parameters will be frequency dependent. Expressions in (1) will be replaced by:

$$Z_0 = \sqrt{\frac{R(f) + j\omega L(f)}{G(f) + j\omega C(f)}}; \quad \gamma(f) = \sqrt{(R(f) + j\omega L(f))(G(f) + j\omega C(f))} = \alpha(f) + j\beta(f) = \alpha + j\omega t_{pd} \quad (4)$$

Where $\gamma(f)$ is the complex propagation constant; its real part, $\alpha(f)$, describes the attenuation of the waves, its imaginary part, $\beta(f)$ describes the wave propagation. For instance, if we consider a nominally 50-ohm transmission line with approximately 1 ns delay, and assume a medium-loss dielectric with a dielectric loss tangent D(f) = 1% at 1GHz, adherence to the wide-band Debye model for the frequency dependence of capacitance and dielectric loss [7], and an approximately 1-ohm total DC resistance with 10 MHz skin corner frequency, we get the frequency dependent L and C as well as R and G parameters shown in Figure 3. The one nanosecond delay corresponds to an approximately six inch trace in a typical PCB material.

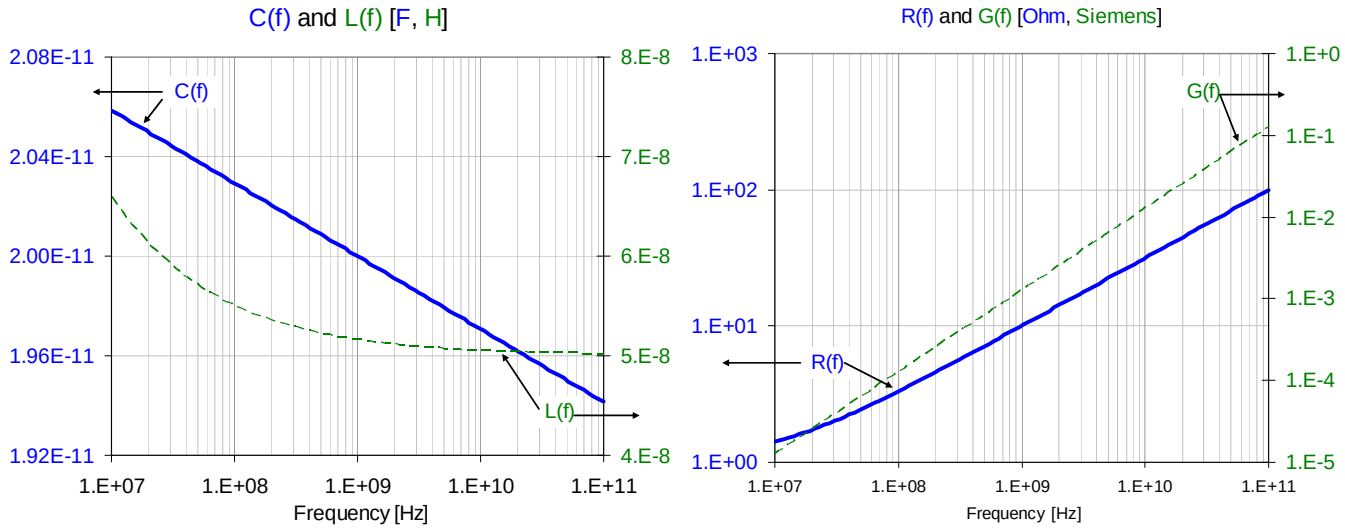

Figure 3: *Frequency-dependent RLGC parameters for a six-inch long medium-loss PCB trace.*

The same trace will exhibit the frequency-dependent characteristic impedance and delay shown in Figure 4.

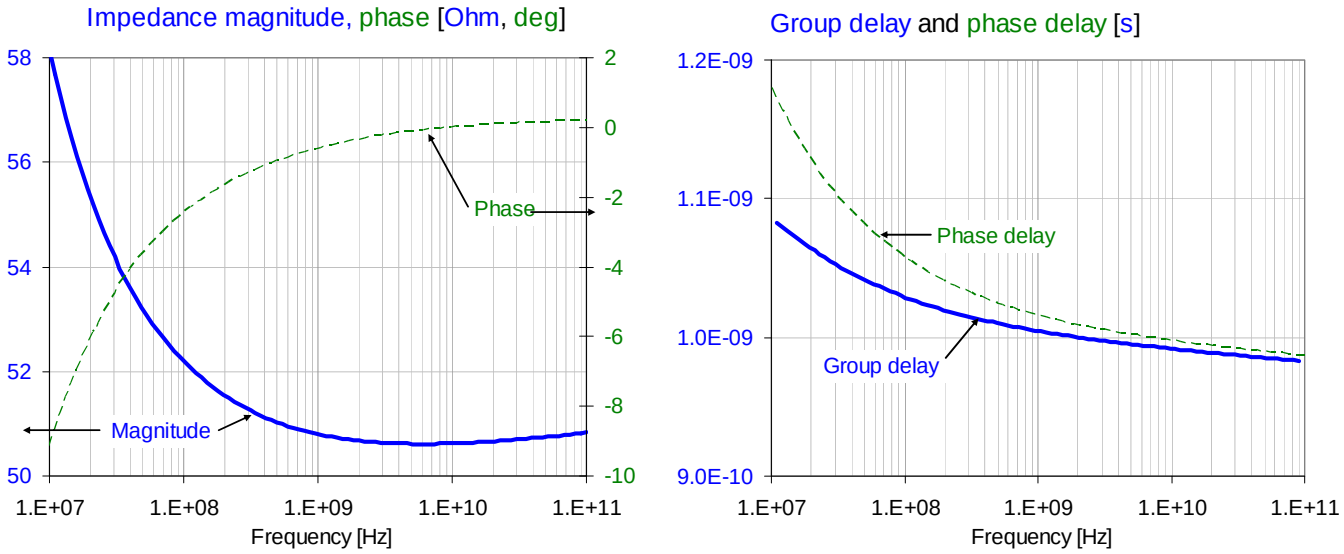

Figure 4: *$Z_0(f)$ (on the left) and delay versus frequency (on the right) for a typical six-inch long medium-loss PCB trace.*

The two main loss categories, conductive and dielectric losses, both will distort the flat TDR response we had for a lossless transmission line. Conductive losses are in the series leg of the equivalent circuit and they will create a positive tilt and deviation; dielectric losses are in the shunt path and they will result in a negative tilt and deviation [8], [9].

To show and illustrate the impact of various parameters on the distortion of TDR response, it is convenient to use SPICE simulations with an RLGC W Element model. The causal W Element RLGC model assumes a square-root of frequency dependence of AC conductive losses and frequency dependent capacitance and dielectric loss [10].

Figure 5 shows the TDR response of transmission lines with DC resistance sweeping over two decades of values above and below a 0.2-ohm/inch center value that we may find in a typical dense board today, for instance on a 5-mil wide ½ ounce copper trace. The RLGC model represents a 20-inch PCB trace terminated in 50-ohm, a fixed R_{dc}/R_s ratio of 10,000, for lossless as well as medium-loss PCB material with Df(1GHz) = 1%. Higher DC resistance may come from a narrower trace and/or lower conductivity. We get lower resistance from wider and thicker conductors, and as we will see later, also from smoother copper.

The DC resistance per inch steps from 0.02 Ohm/inch to 2 Ohm/inch. The response lines rise monotonically, but not linearly, until a peak is reached after a round-trip delay. Afterwards the response decays and monotonically approaches the DC resistance value plus the reference impedance.

The impact of the skin effect and surface roughness, which are captured in the RLGC W Element model by the Rs constant and by adjusting the inductance accordingly, is shown in Figure 6.

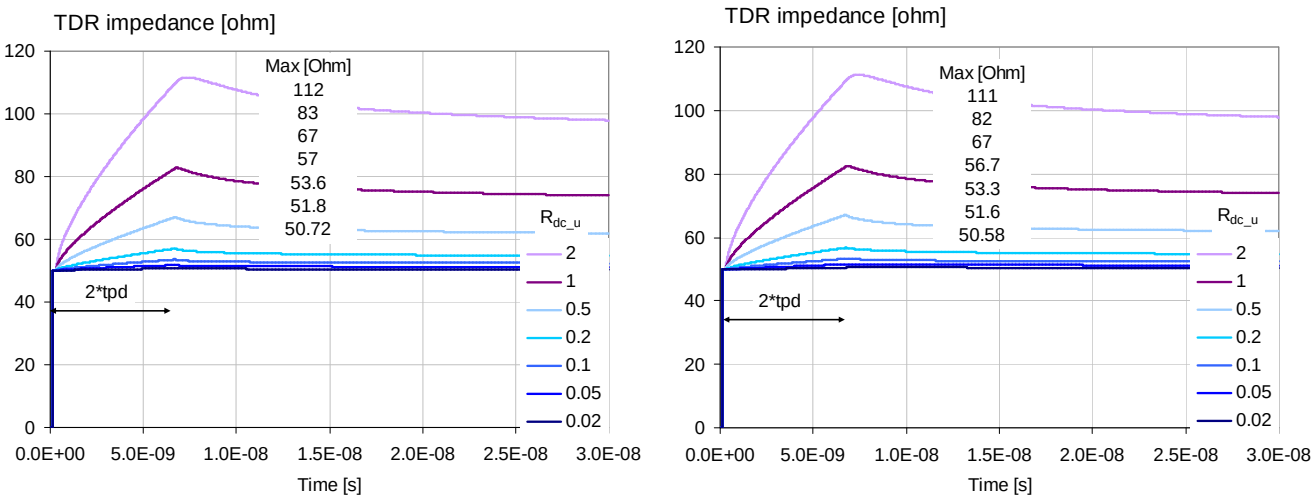

Figure 5: *TDR impedance of a 20-inch trace as a function of DC resistance with ideal dielectric (on the left) and medium-loss dielectric (on the right). The order of legend labels correspond to the order of traces on the plots: upper-most traces have the highest resistance. The table insert lists the corresponding maximum value of each trace, reached at the end of the 2*tpd round-trip delay.*

The TDR traces in Figure 5 eventually all settle at an asymptotic value of the termination impedance plus the total DC resistance. For instance, the top-most line settles at 50 + 20 * 2 = 90 Ohms, but due to the long time constant, the response reaches its steady state long beyond the right axis of the graph. The peak value for this trace is 112 Ohms, or 62 Ohms above the termination impedance.

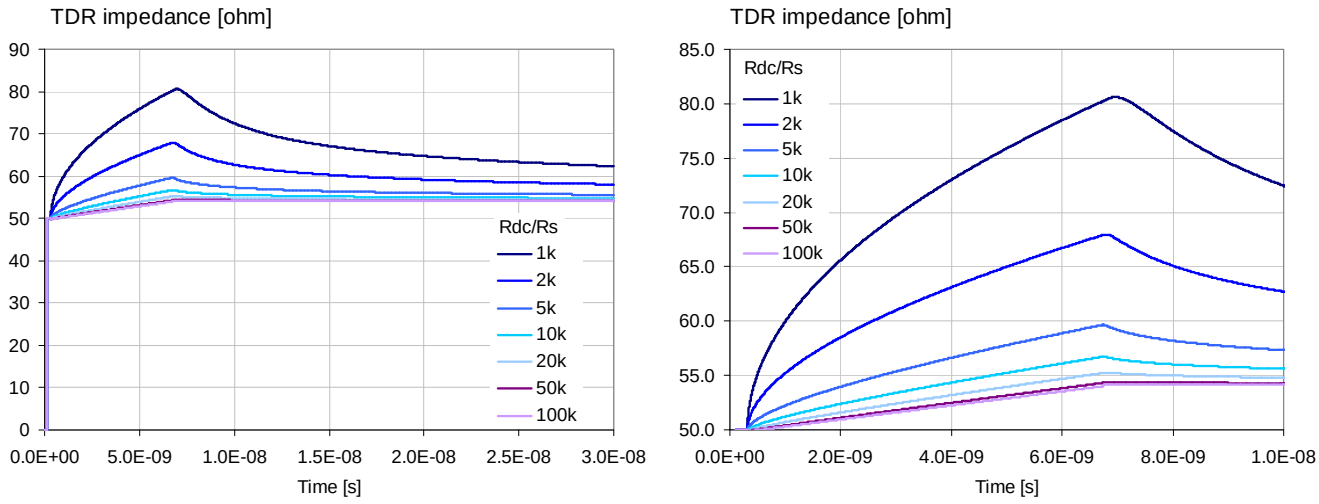

Figure 6: *Impact of AC resistance on the TDR response. Full vertical scale on the left, zoomed vertical scale on the right. The order of legend labels correspond to the order of traces on the plots: upper-most traces have the lowest Rdc/Rs ratio.*

The ratio of the peak deviation (62 ohms for the top trace) and the total DC resistance (40 ohms for the top trace) is a little above 1.5 in this case. We need to note, however, that this ratio is not constant. The ratio depends on the parameters of interconnects and it can be as low as 1.00 for transmission lines with only DC resistance and no AC resistance. This case can be approximated with thin-film conductors.

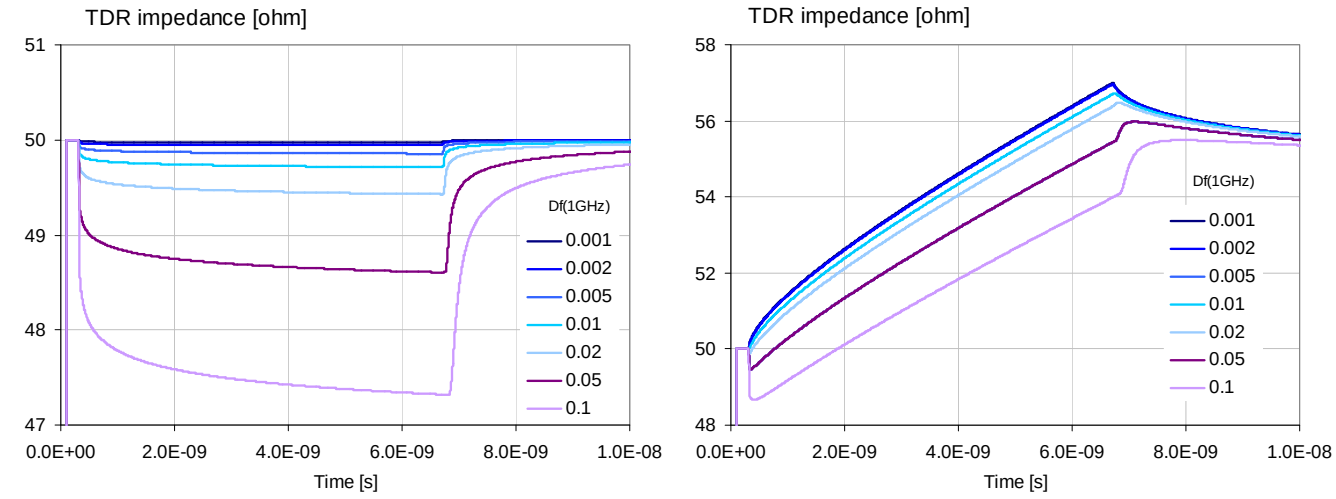

Figure 7: *TDR impedance of a 20-inch trace with ideal (on the left) and typical (on the right) copper loss. The order of legend labels correspond to the order of traces on the plots: upper-most traces have the lowest dielectric loss.*

The plot on the right of Figure 7 and the plot on the left of Figure 4 show the V shapes of the TDR plots and Zo(f) curves, respectively. At high frequencies the magnitude of the characteristic impedance rises due to the dielectric losses, which lowers the available capacitance. This translates to an initial negative tilt of the TDR plot. At medium and low frequencies the magnitude of the characteristic impedance also rises as frequency goes down; this creates the positive tilt and slow rising tail of the TDR plots.

On the following figures we will look at how measurement bandwidth and interconnect length impact the TDR plots. Figure 8 assumes our typical interconnect with R_{dc} = 0.2 Ohm/inch, a fixed R_{dc}/R_s ratio of 10,000 and medium-loss PCB material with D_f(1GHz) = 1%. The excitation step bandwidth was adjusted with a multi-pole Bessel filter logarithmically from 0.5 GHz to 50 GHz in 1, 2, and 5 steps. A 20-inch and a 0.5-inch long uniform trace were simulated.

The lower bandwidth results in a slower excitation edge, longer rise time. The 0.5 GHz BW produces an approximately 250 ps 10%-90% stimulus risetime, which is close to the bandwidth used in some of the widely used PCB test equipment [11]. This gets convolved with the TDR response with ideal bandwidth. Note that for a long uniform trace with no additional discontinuities, the major signature of the TDR profile is impacted very little by the BW change. We see a slight added delay for lower bandwidth, which comes mostly from the delay of the wave-shaping filter at the input. The impact is much more visible in case of a short line, where in addition to the slower rise and fall times, the response plateau value gets shifted as well and this shift eventually distorts the measurement of the line impedance and its delay.

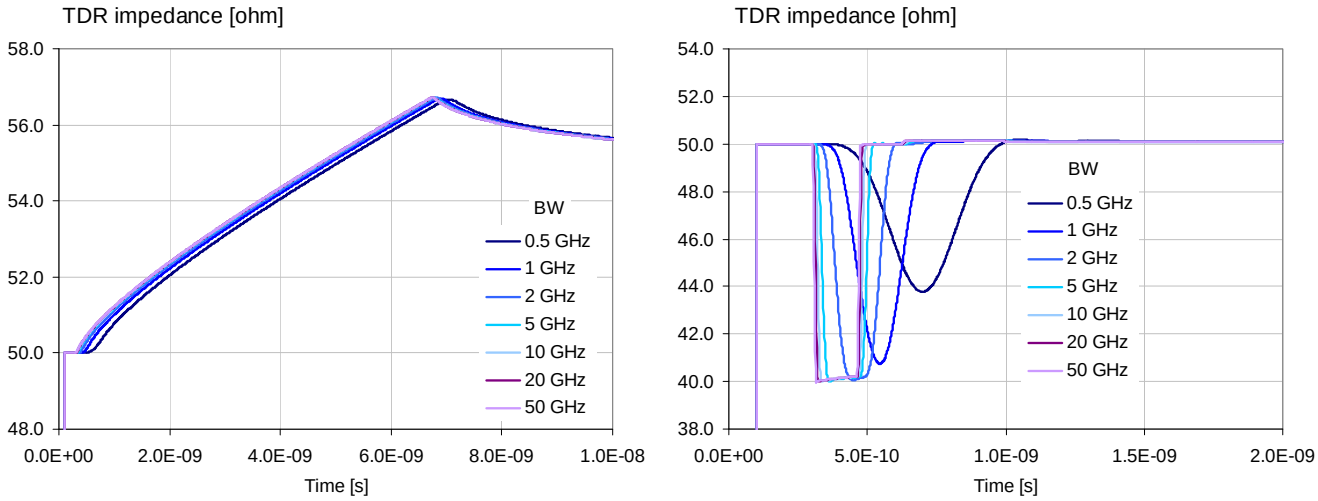

Figure 8: *Impact of BW on TDR response: 50-ohm 20-inch line on the left, 40-ohm 0.5" line on the right.*

Losses in uniform matched interconnects will create a monotonically increasing attenuation at higher frequencies. This will eventually limit the bandwidth of the excitation pulse as it moves through the DUT, limiting our capability to distinguish neighboring features in the TDR plot. Discontinuities

themselves will also limit the bandwidth of the excitation pulse, eventually masking discontinuities downstream. This effect is widely covered in the literature and therefore not included in this study.

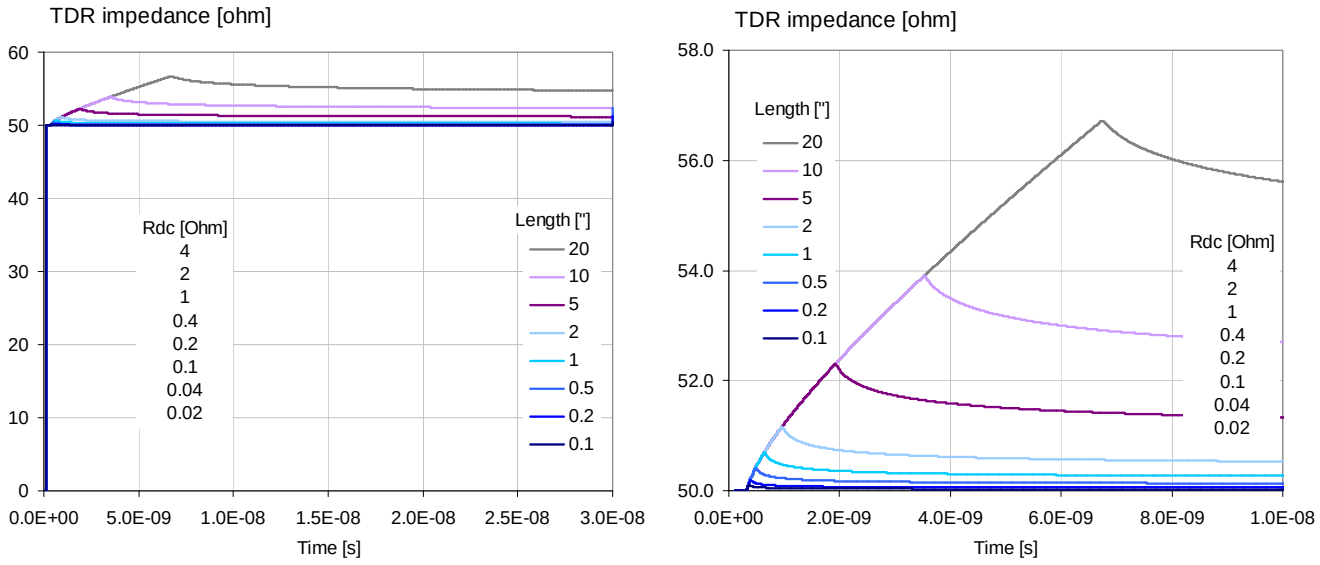

Figure 9: *Impact of interconnect length on TDR profile: zoomed-out scale on the left, zoomed-in scale on the right. The order of legend labels correspond to the order of traces on the plots: upper-most traces have the largest length.*

The next figure illustrates the effect of the interconnect length. Figure 9 shows the effect with a typical 50-ohm trace, R_{dc} = 0.2 Ohm/inch, a fixed R_{dc}/R_s ratio of 10,000 and medium-loss PCB material with D_f(1GHz) = 1%. The total length is swept from 0.1" to 20", which represents the range of trace lengths we may consider TDR-ing. Though we may have longer traces under some circumstances, this 200:1 range already illustrates the facts that a) the TDR response varies non-linearly with length and b) up to the round-trip delay point all response lines follow the same contour and therefore we can 'scale' or estimate the TDR response if we know the response of the longest possible trace we want to model with the same per-unit-length parameters. Note that in this study we are not concerned about the response after $2t_{pd}$. In these plots all responses eventually settle to the reference termination impedance plus the total DC resistance, because the simulation used a matching termination at the far end. In case of open far-end termination the TDR response will jump up to infinite after $2t_{pd}$.

Finally we look at the impact of the characteristic impedance. Figure 10 illustrates the impact with a 20-inch long trace , R_{dc} = 0.2 Ohm/inch, a fixed R_{dc}/R_s ratio of 10,000 and medium-loss PCB material with D_f(1GHz) = 1%. The characteristic impedance varies in 2.5-ohm increments between 42.5 and 57.5 Ohms, the reference impedance is 50 Ohms. This figure shows the obvious: as long as the per-unit-length loss parameters are the same, the characteristic impedance of the uniform interconnect does not change the shape or slope of the TDR response, it merely shifts it up or down.

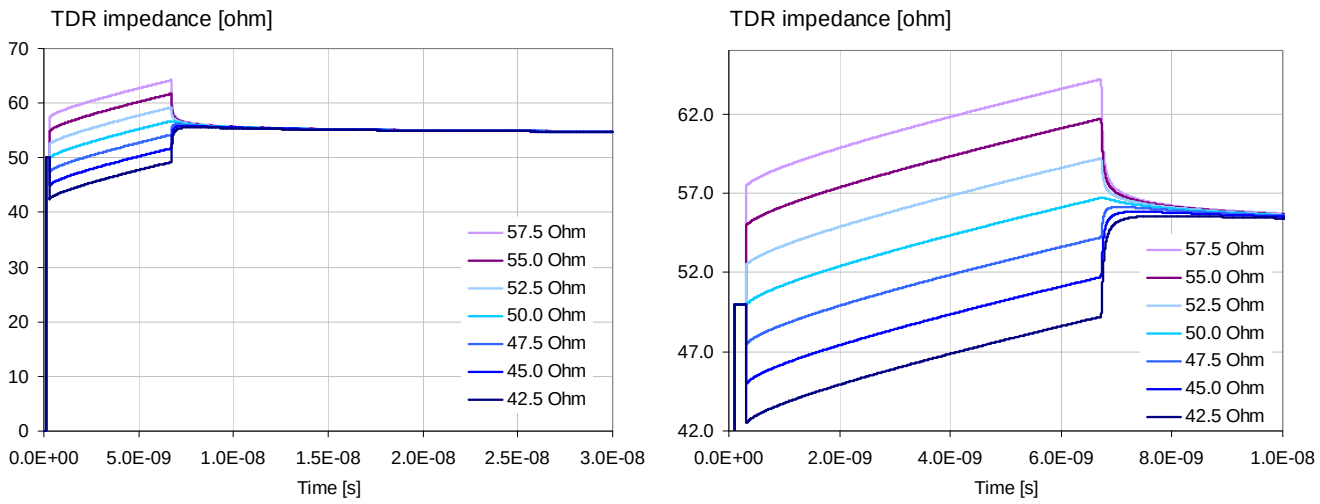

Figure 10: *Impact of interconnect impedance on the TDR response. Zoomed-out scale on the left, zoomed-in scale on the right.*

III. Manufacturing variability

In Section II we looked at the TDR performance of uniform, stand-alone interconnects. In practical interconnects, especially in traces in today's high-density packages and PCBs, there are a multitude of additional practical factors to consider. In this section we will look at some of the most important practical factors, illustrated on measured data from actual PCBs. We will look at the non-uniformity of traces due to etching variations, dielectric height variations, glass-weave effects, copper roughness and conductivity of copper.

We will look at a measured TDR response of a nominally 85-ohm differential pair. The end-to-end length is 17 inches, the nominal trace width is 4.5 mils with 5.5 mils air gap. The differential pair was on the fifth layer of a twenty-layer board in a nominally symmetrical stripline construction, with approximately 3.5-mil thick medium-loss dielectric layer using flat glass and ½ ounce RTF copper. There are backdrilled vias going to the top side at each end. There are no transitional vias along these traces. The vias connecting to the trace ends had ground vias at a 1-mm distance. Any residual surface features beyond the via pads were removed, and measurements were done between the signal via and ground via 1mm away. Very short sections of the differential pair were routed through pinfields, where it was necessary to change the trace width and spacing to fit the pair through. The density and proximity of neighboring traces did vary along the path. The TDR profile was measured on six boards from two different board vendors, Vendor A and Vendor B. The measurements were done with different instruments, different probes and different calibration techniques; some variants were used only for reference or calibration purposes. One set of measurements were done with an 18-GHz TDR head [13] with its matching mainframe and home-made semi-rigid probes with 1-mm pin pitch; see the left and middle photos in Figure 12. The TDR module was first calibrated to its front-panel connector, followed by a normalization including the cable up to the tips of the probe. Data collected from these measurements was single ended, un-terminated, but we made reference measurements with all ports terminated to prove that the features we are after did not noticeably change with terminating the other leg. This is because even with a

few percent of coupling the power leaking to the other leg is very small and the resulting voltage variation on the main path is negligible.

Figure 11: *Footprint of the DUT differential pair.*

Another set of measurements were done by a 43-GHz VNA [14] and 500 μm G-S S-G wafer probes, see the right photo in Figure 12. In this second case all ports were terminated, though here, too, reference measurements were made with the other ports un-terminated to make sure the difference in the important signatures was negligible.

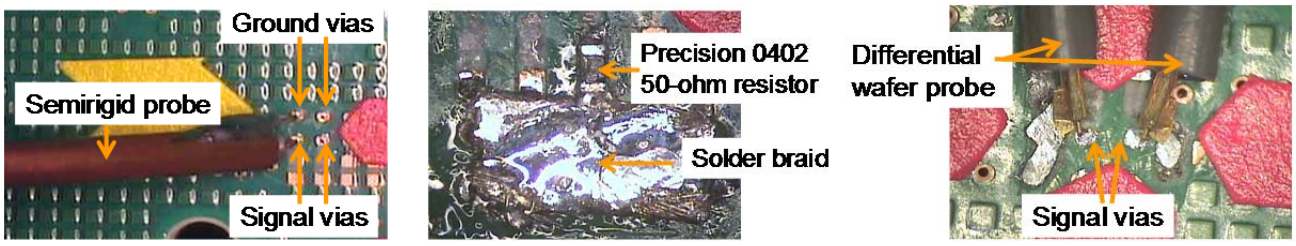

Figure 12: *Measurement connections: semi-rigid probe for TDR and DUT vias on the left, calibration pieces for TDR in the middle, wafer-probe connection on the right.*

With all probes and instruments, reference calibration pieces were measured and repeatability tests were performed. Figure 13 shows a typical result from a repeatability test. The same trace on the same board was measured from the left end and from the right end multiple times, with the same calibration and also with calibration redone. The measurement results shown here were taken with the hand-held semi-rigid probe. In each plot, the blue and red lines represent data measured on

different days with their own calibration. Within one-to-two days, the agreement was very similar using the same calibration.

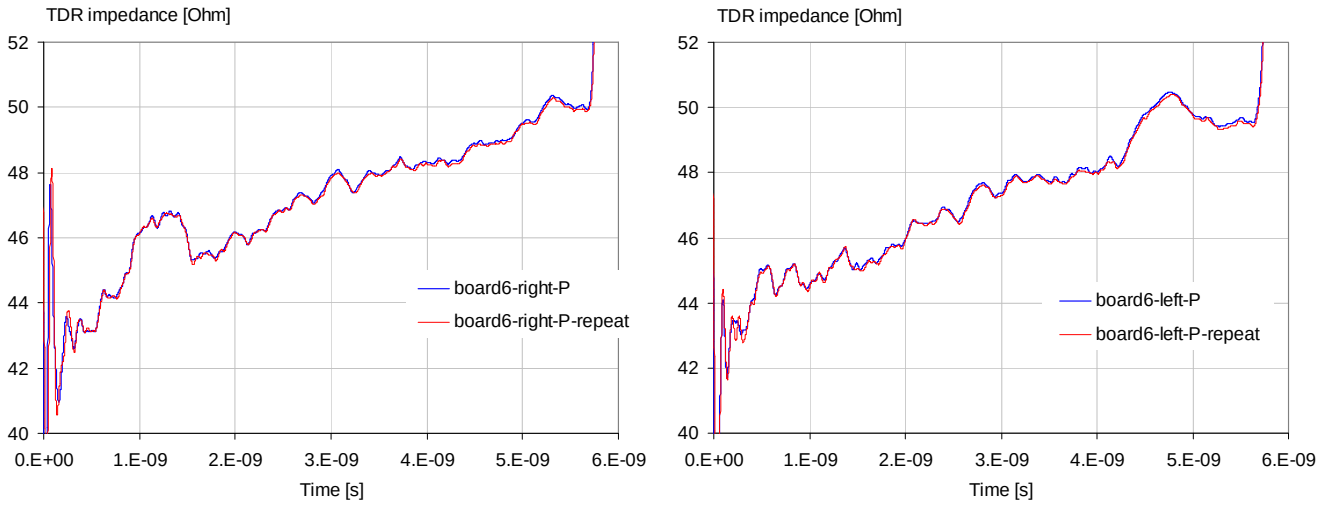

Figure 13: *Repeatability test result.*

Figure 14 shows cumulative plots from all six boards. These are single-ended TDR plots, with a nominal differential impedance of 85 Ohms. With uncoupled traces each trace nominally should have 42.5 Ohms impedance. When light coupling is included, we need to increase the stand-alone trace impedance to compensate for the drop of odd-mode impedance.

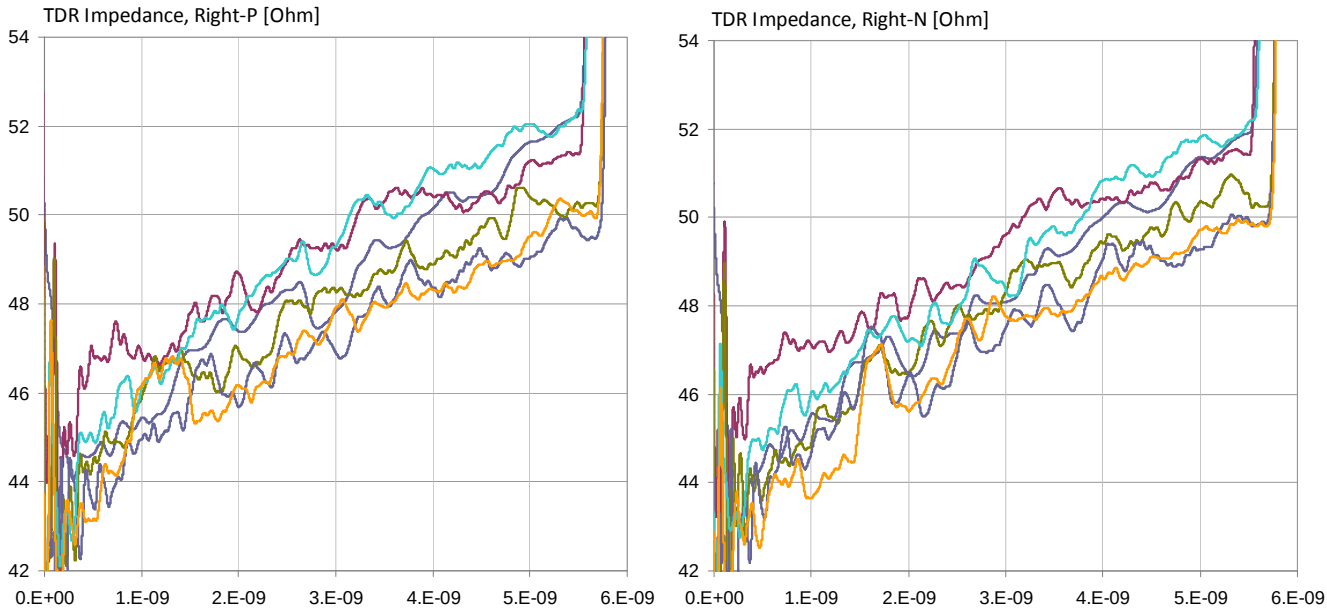

Figure 14.a: *Cumulative plot of the DUT trace impedance for the P (left) and N (right) leg of the differential pair, measured from the right end of the trace.*

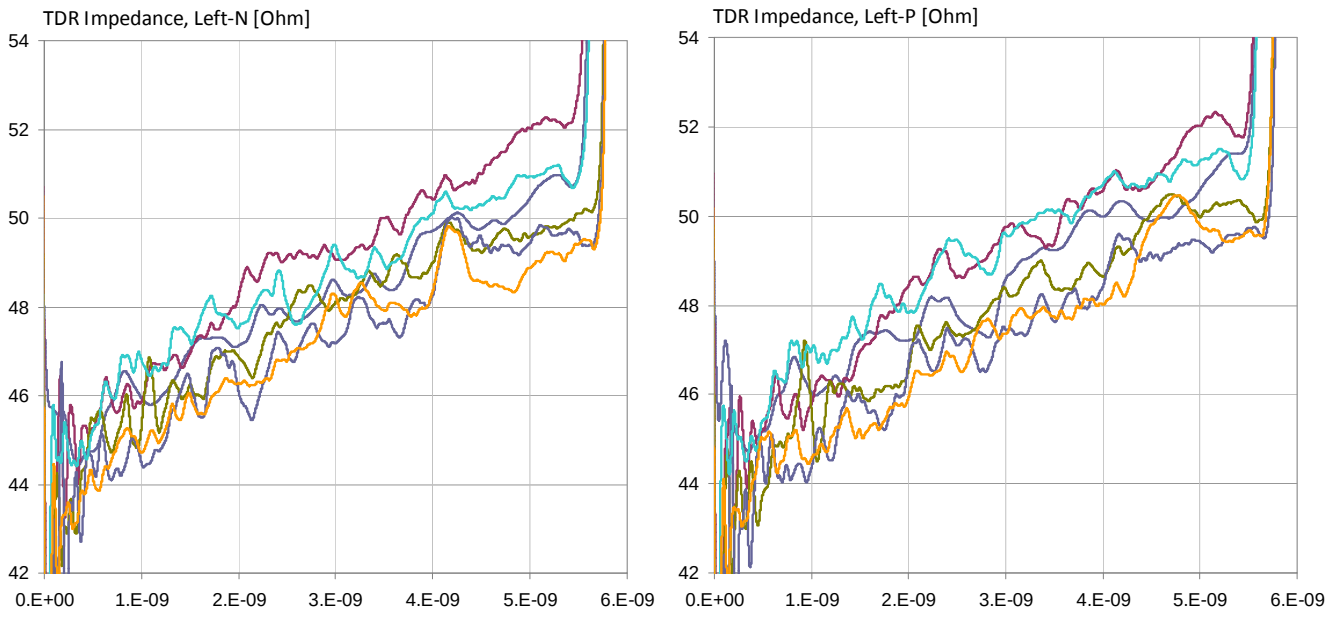

Figure 14.b: *Cumulative plot of the DUT trace impedance for the P (left) and N (right) leg of the differential pair, measured from the left end of the trace.*

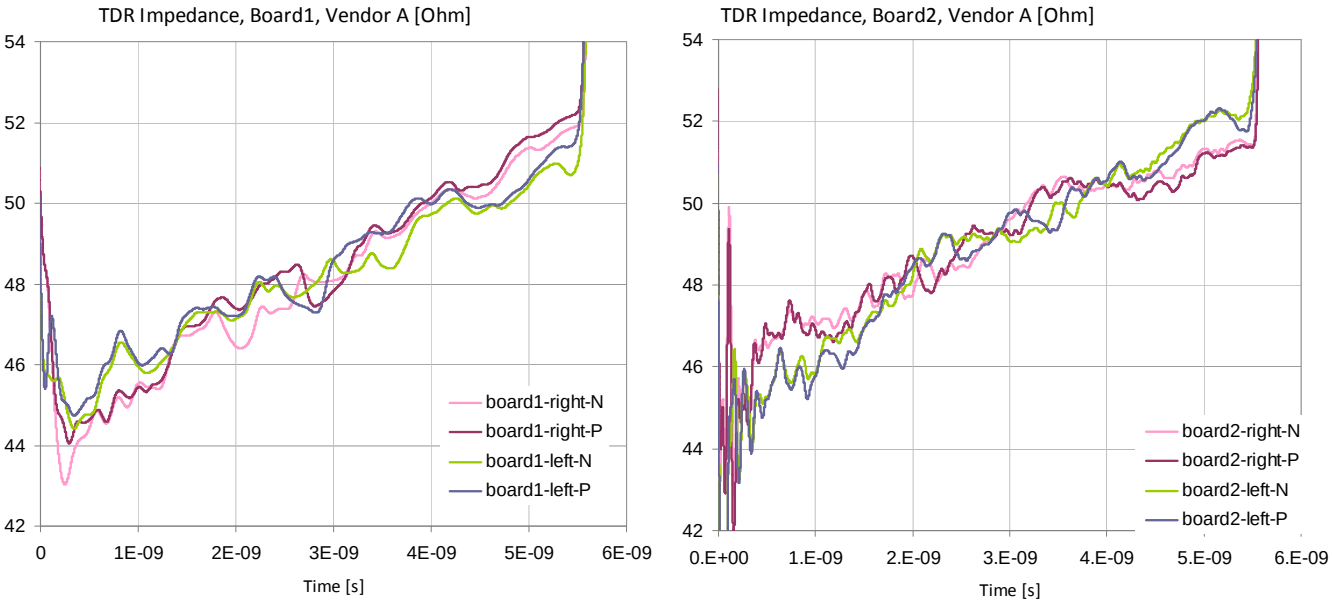

Figure 15.a: *Single-ended TDR responses from Board1 and Board2.*

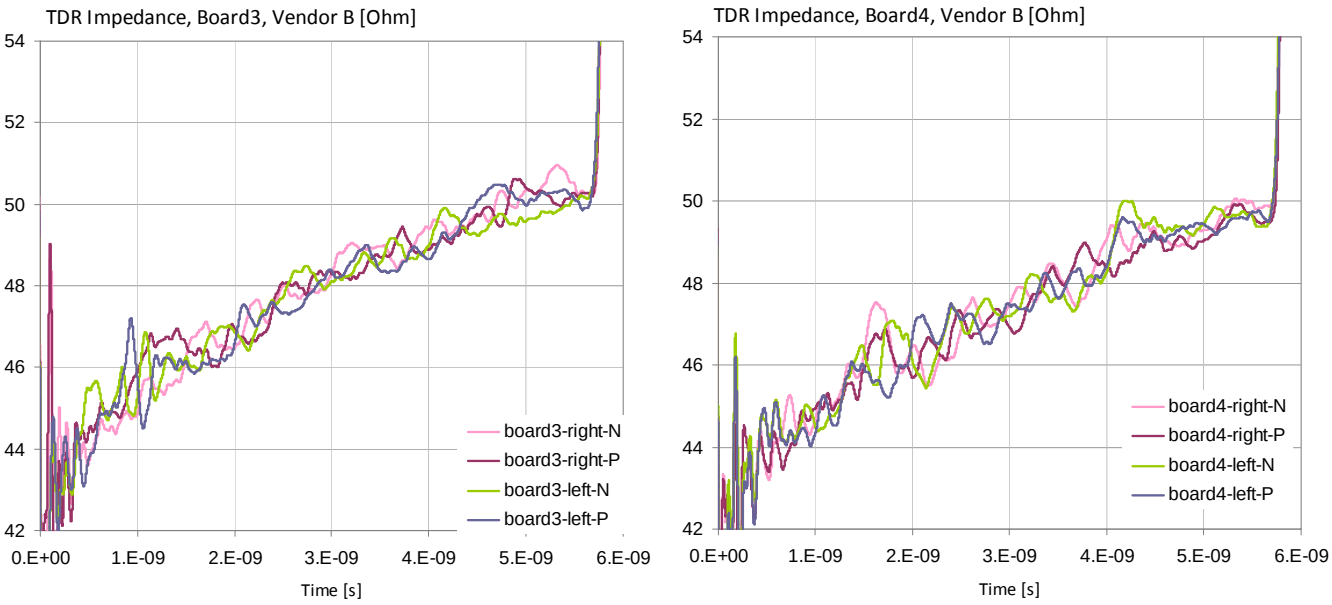

Figure 15.b: *Single-ended TDR responses from Board3 and Board4.*

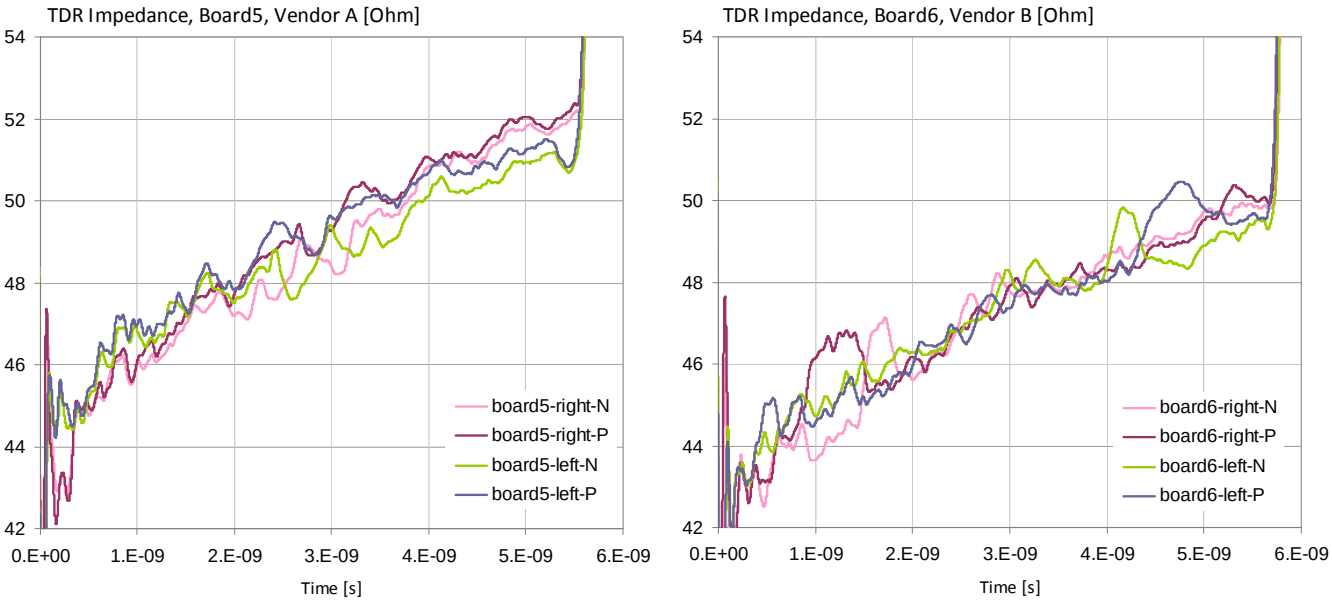

Figure 15.c: *Single-ended TDR responses from Board5 and Board6.*

With the given geometry of the DUT traces, we need approximately 44 – 45 Ohms single-ended trace impedance to get differentially 85 Ohms. We see a band of about three ohms riding over a slanted curvature, starting around 44 Ohms, which resembles very much the TDR signature of AC conductive losses, illustrated in Figure 6. This suggests that the impedance plot we showed in Figure 1, may be acceptable and the trace may meet its specifications. How sure can we be in this assessment, will be explored next.

To better understand the details, we now look at the impedances from the six boards, one by one, comparing the four TDR traces: P-leg from left side, P-leg from right side, N-leg from left side and N-leg from right side. Figure 15 shows the result. If we had a uniform, symmetrical differential pair, all four TDR lines would completely overlap.

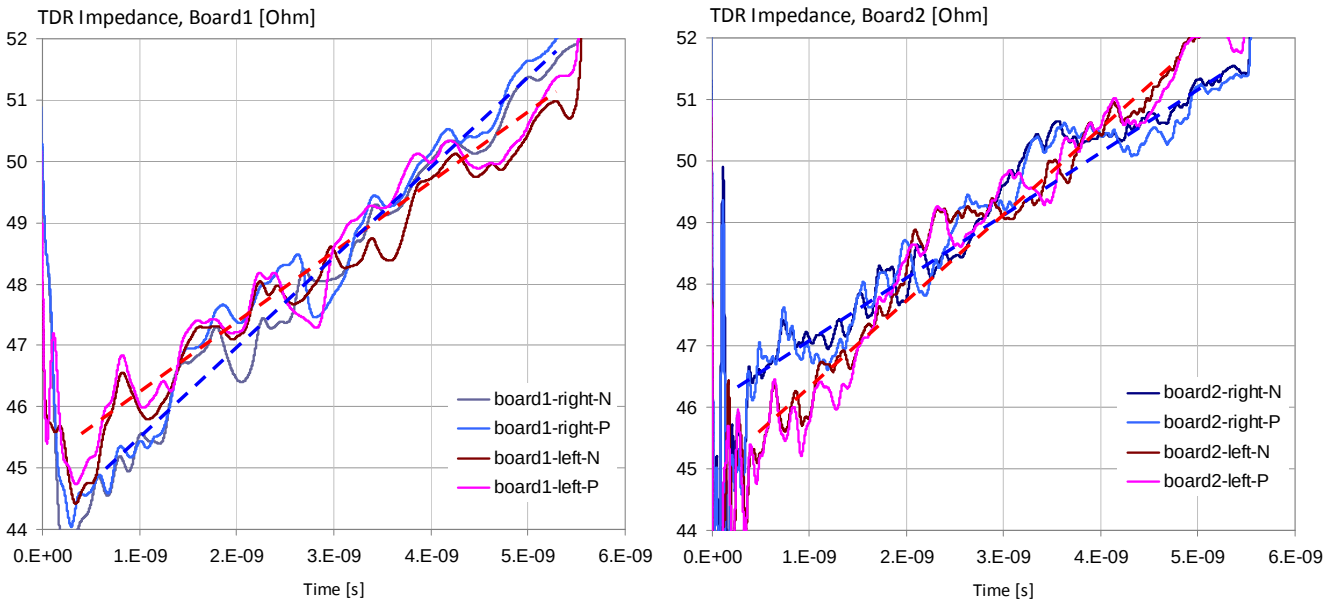

Figure 16: *Board-to-board and left-vs.-right differences across two boards.*

In Figure 16, not only are there up to two ohms of differences among the four TDR responses, but the responses don't seem to be the same measured from the left side versus measured from the right side. This means that the traces are not symmetrical. Some asymmetry is explainable due to differences of the local environment along the differential pair, but nominally those should result in a much smaller variation. The fact that the left *vs.* right difference is not the same board to board also indicates that the asymmetry is most likely due to statistical manufacturing tolerances. Figure 16 illustrates this point with data from Board1 and Board2, both from Vendor A.

Figure 17: *Port assignment for VNA measurements.*

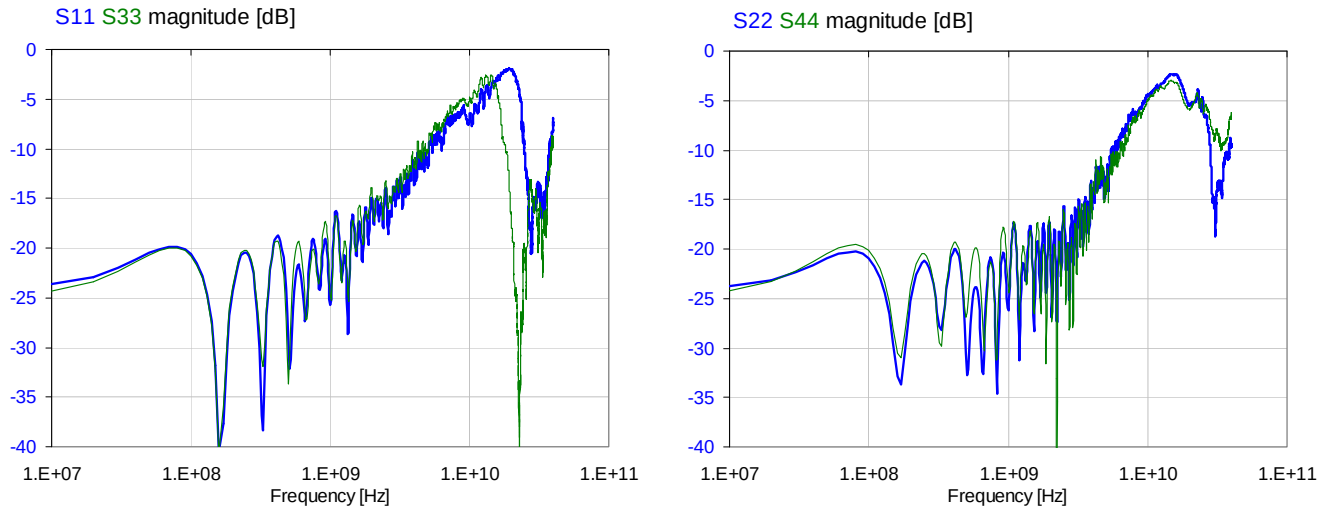

Figure 18.a: *The four single-ended reflection parameters according to Figure 17's port assignment.*

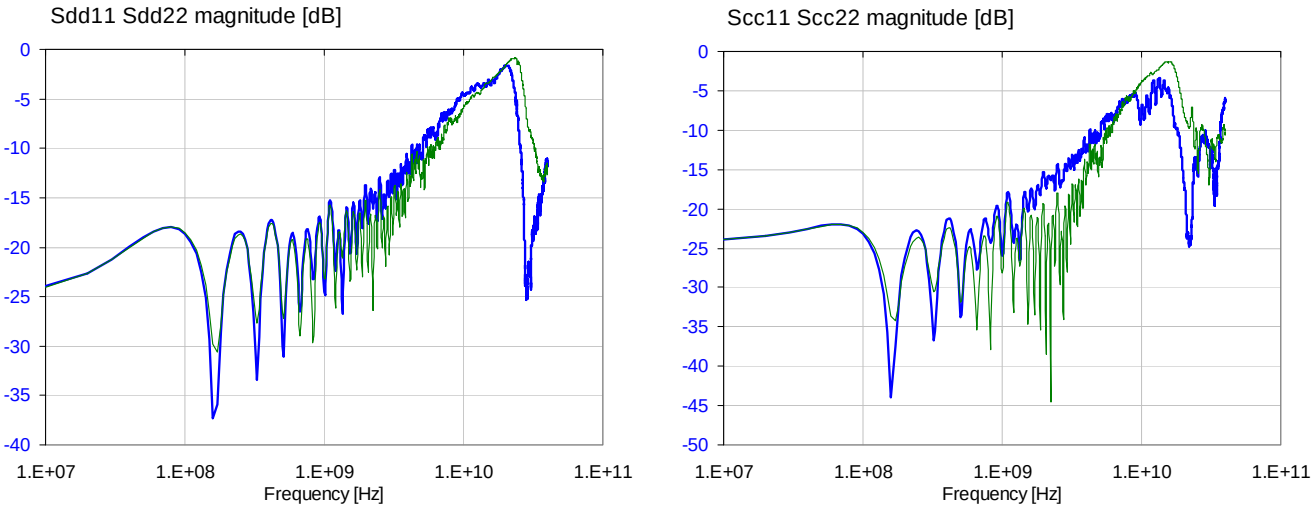

Figure 18.b: *Mixed-mode reflection parameters: differential on the left, common-mode on the right.*

The dashed lines with matching colors approximate the average change of impedance along the TDR responses. Note that in Board1 the TDR response experiences more average upslope measured from the right side. In Board2 it is the opposite. The same asymmetry can be seen in the measured S parameters as well. Figure 17 shows the port assignment, Figure 18 shows the single-ended and differential reflections, all normalized to 50 Ohms single-ended and 100 Ohms mixed-mode impedance. Figure 19.a shows the differential and common-mode forward transfer and the mode conversions. Figure 19.b shows the delay and the asymmetry between the N and P legs of the same differential pair.

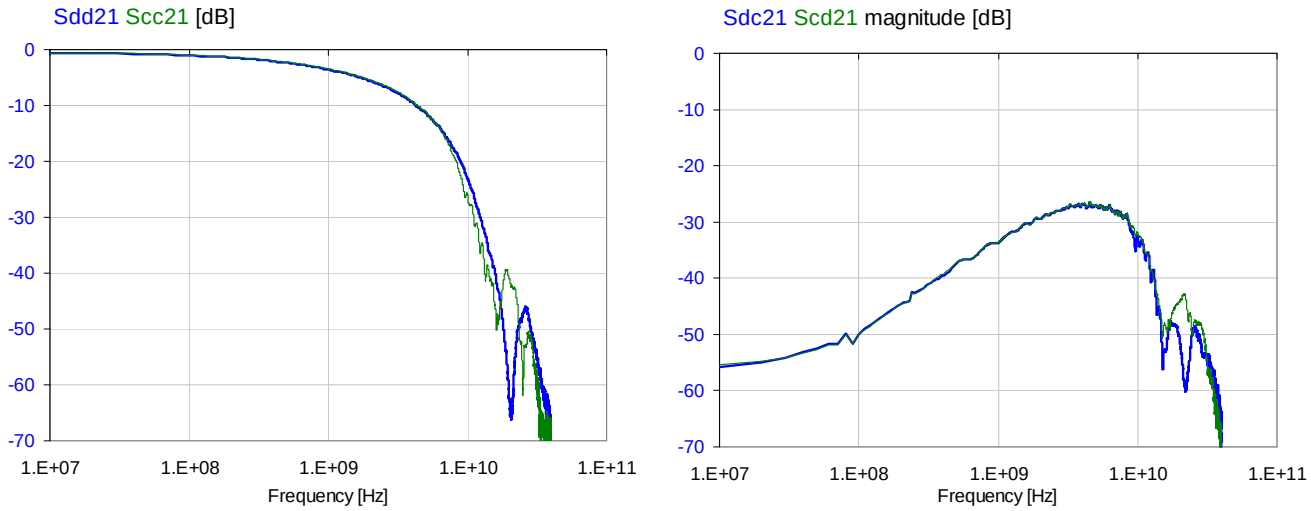

Figure 19.a: *Differential (blue line) and common-mode (green line) transfer on the left, mode conversions on the right.*

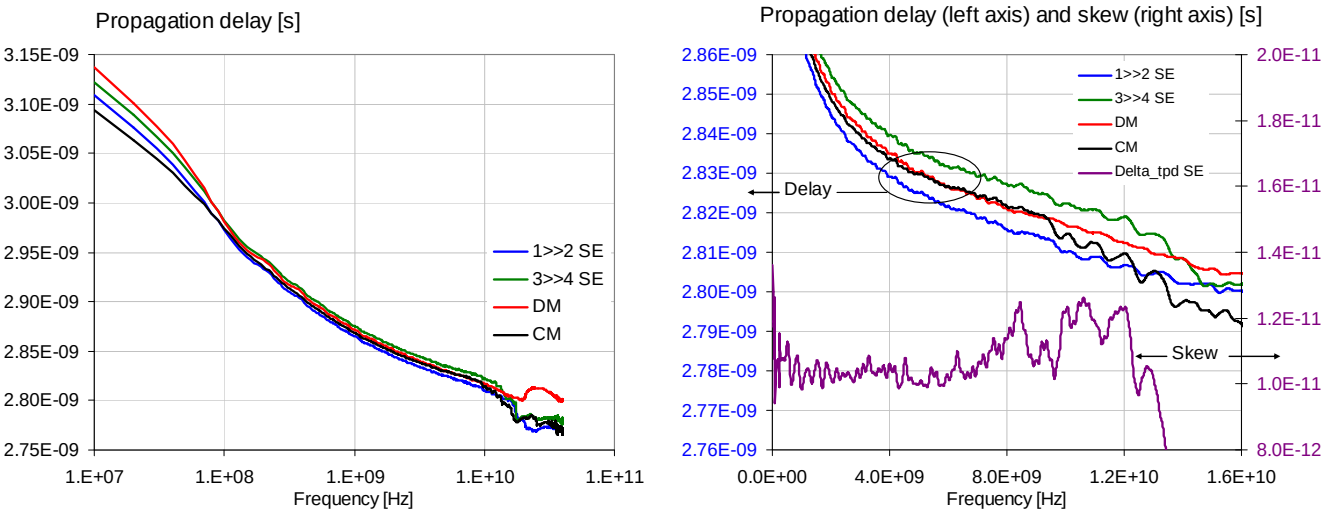

Figure 19.b: *Single-ended and differential delays on full scale on the left, delays and in-pair skew on a zoomed scale on the right.*

The DC resistance of each leg of the differential pair was also measured on all six boards. The end of the trace was shorted to ground and the resistance from the other end was measured. Reference measurements were also made with two different four-wire multi-meters from beginning to end of the traces, without the return plane included. The data measured from left and from right agreed within 1% on the boards. Figure 20 shows a representative TDR plot with the end of the trace shorted. From board to board across the six samples there was a 4.9 – 5.8 Ohm range of single-ended DC trace resistance. Assuming nominal trace width, 0.6-mil etching factor and text-book copper conductivity of 5.8E7 S/m, the calculated DC resistance would be 4.7 Ohms.

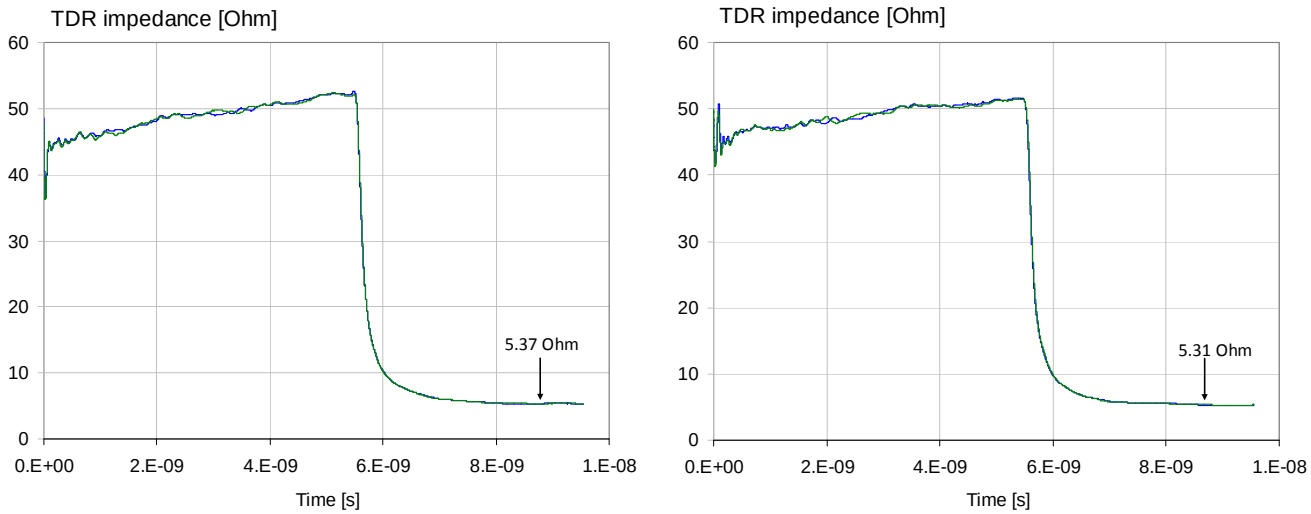

Figure 20: *Representative DC resistance measurement result with TDR, measured from the left (left plot) and measured from the right (right plot). Blue traces: N leg, green traces: P leg.*

To see how the measured DC resistance and the TDR impedance plots can be correlated to estimated values, boards were cross sectioned at ten locations along the differential pair. The percentage deviation measured on one of the boards is shown in Figure 21. Parameters *a*, *e* and *h* are left out from the table as those do not have a strong impact on impedance.

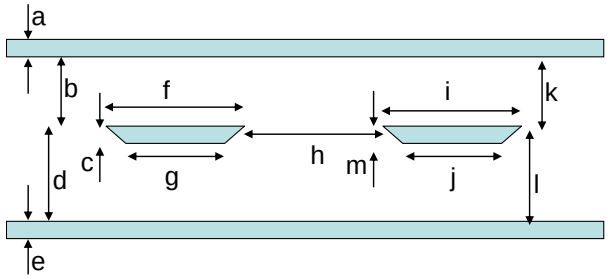

Figure 21.a: *Definition of cross-section measurements.*

Location:	b	d	c	f	g	k	l	m	i	j
1	2.43	5.45	-2.10	2.07	-1.17	3.10	4.00	-0.89	0.86	0.00
2	2.43	1.93	-2.10	-0.46	2.74	-0.18	2.13	-0.89	0.86	0.79
3	-0.83	-4.42	8.41	-0.46	-2.22	-0.18	-5.82	3.56	-0.06	-1.05
4	2.43	0.99	-2.10	1.15	1.69	3.10	0.49	-0.89	-0.06	0.79
5	-0.83	-2.54	-2.10	-2.30	-2.22	-2.56	-2.31	-0.89	-0.75	0.00
6	-2.01	-2.54	8.41	2.07	1.69	-1.37	-3.01	3.56	4.32	0.79
7	-4.38	-1.83	-2.10	-2.30	-3.26	-2.56	-1.38	-0.89	-2.59	-2.11
8	-2.01	-2.54	-2.10	0.23	2.74	-0.18	-0.44	-0.89	-2.59	0.79
9	2.43	0.05	-2.10	-1.13	-1.35	-0.18	1.43	-0.89	-4.89	-1.16
10	0.36	5.45	-2.10	1.13	1.35	1.01	4.93	-0.89	4.89	1.16

Figure 21.b: *Percentage deviation from the mean.*

The laminate material was not specifically analyzed, but at each cross section location we checked the position of the glass bundles with respect to the traces to get a qualitative sense of how it locally may impact trace impedance. Figure 22 shows two cross section photos taken on the same board. Note the glass bundle on the right directly below the two traces, creating locally stronger coupling.

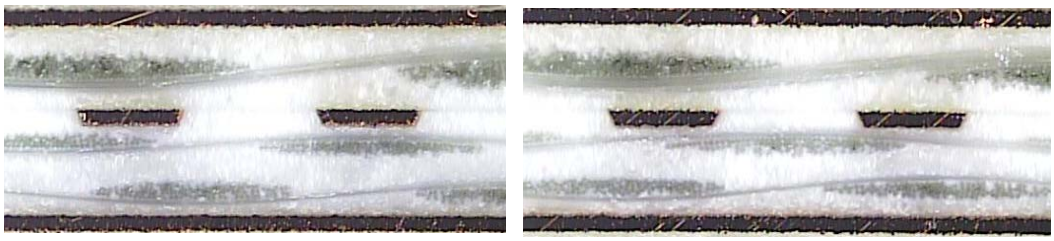

Figure 22: *Cross section photos at two locations along the same differential pair. Black areas are copper, grey areas are glass and bright areas are resin.*

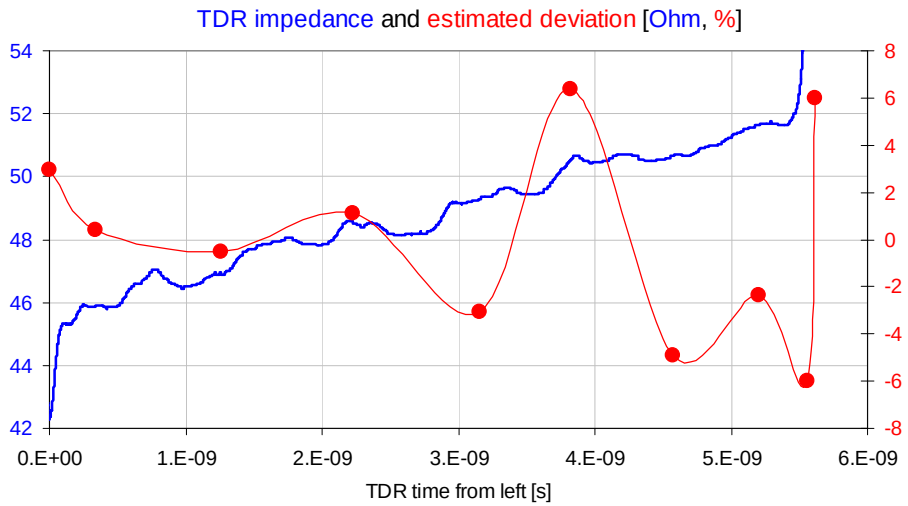

Figure 23: *Measured TDR impedance (blue) and qualitative estimated deviation from nominal (red).*

With the cross-section data, we can create a qualitative estimate by how much we would expect the trace impedance deviate from its expected nominal value. We know that increasing the trace width or the dielectric constant (glass-resin ratio) will decrease the impedance, whereas increasing dielectric height will increase impedance. We can sum up all measured deviations with their proper sign applied, and we get a qualitative estimated deviation value at each cross section location, as shown by the red dots in Figure 23. The blue line in Figure 23 is the measured TDR impedance. Both the estimates and the measured TDR impedance is plotted as the average of the P and N leg values. While we can see some correlation between the two, the strong tilt on the measured data masks out smaller details. We can now return to the difference we see between the estimated and measured DC resistance.

The average trace thickness in the cross section report was 0.67 mils, ranging between 0.61 and 0.687 mils across the two legs and ten locations. The challenge is that in the case of half-ounce copper, we want to establish the thickness of a copper sheet with a nominal thickness of 18 μm. Even with relatively smooth copper, the peaks and valleys of the surface roughness could be an appreciable fraction of the total thickness and therefore it matters how the marker lines are positioned over the tooth structure. Upon closer inspection of the cross section report, it was realized that the marker lines were likely placed over the average of the tooth structure. However, for DC resistance purposes, we need the minimum copper thickness [16]. If we place the marker lines over the minimum points (Figure 24), the measured copper thickness becomes 0.51 mils, and with that estimate we get a better agreement with measured resistance.

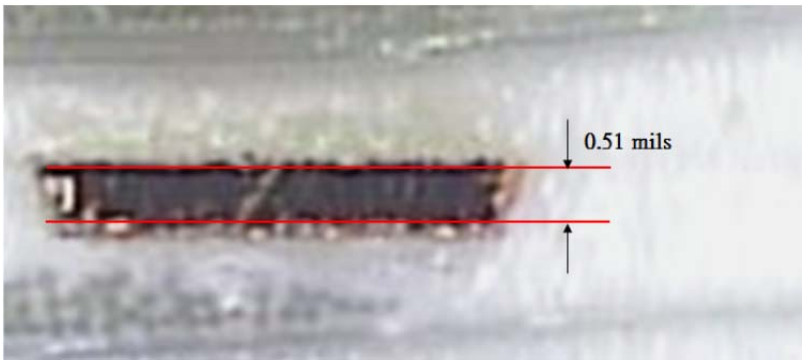

Figure 24: *For DC resistance calculation, we need the minimum copper thickness, by placing the markers over the minimum points of the roughness profile.*

We already see that the actual TDR response can deviate from an ideal flat line for several reasons: losses and local non-uniformities as well as local discontinuities, such as vias are the main reasons. For our measured case there were only back-drilled end vias, so if we exclude the end points, the deviation from a horizontal line will be caused by losses and local non-uniformities. Figures 21 – 23 showed an example of measured non-uniformities sampled at a few locations. The following figures illustrate some simplified simulated cases of non-uniformity. Figure 25 shows the simulated TDR response of a 20-inch lossy trace, split into two 10-inch sections, each having different impedance. When we have 50-Ohm impedance on both sections, the response is a smooth line matching the response of a twenty-inch long uniform trace. When the impedances are different, each section follows its own slope, eventually creating the same bounds that we would get with uniform traces with the extreme impedances all the way.

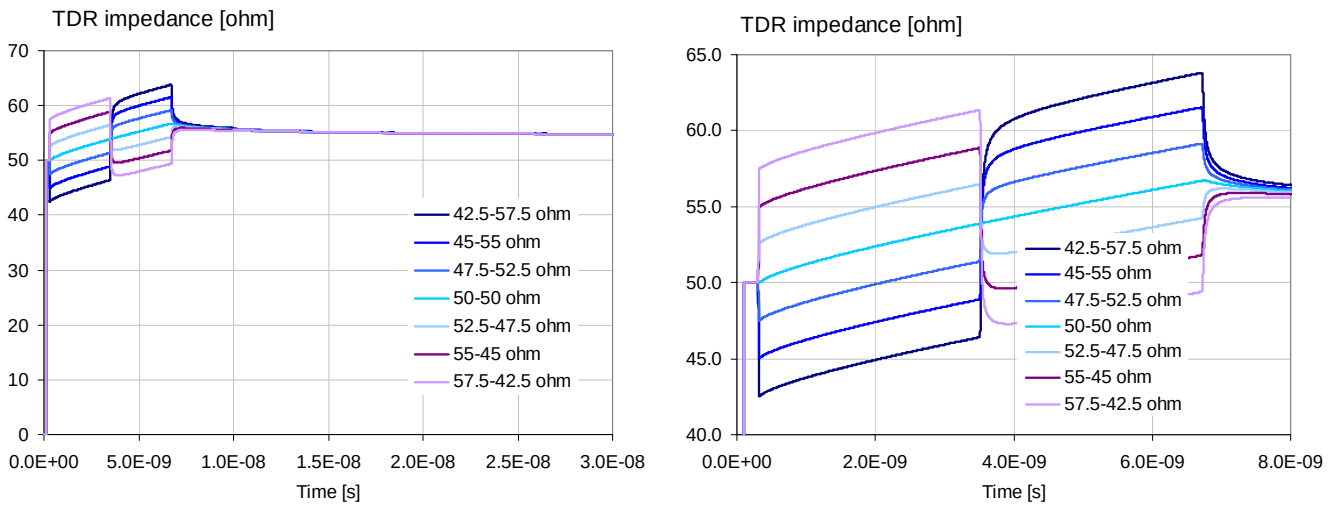

Figure 25: *TDR profile of two cascaded 10" transmission lines with different impedances.*

More interesting could be the case when we assume that there are multiple changes of the trace impedance along its length. One typical scenario with glass-reinforced laminates is the periodical variation of dielectric constant due to changing glass-resin ratio or the periodical change of impedance due to a regular array of disturbances (for instance antipads) in the return path. The periodical change of impedance, similar to periodical discontinuities, creates a low-pass filtering transfer function [15].

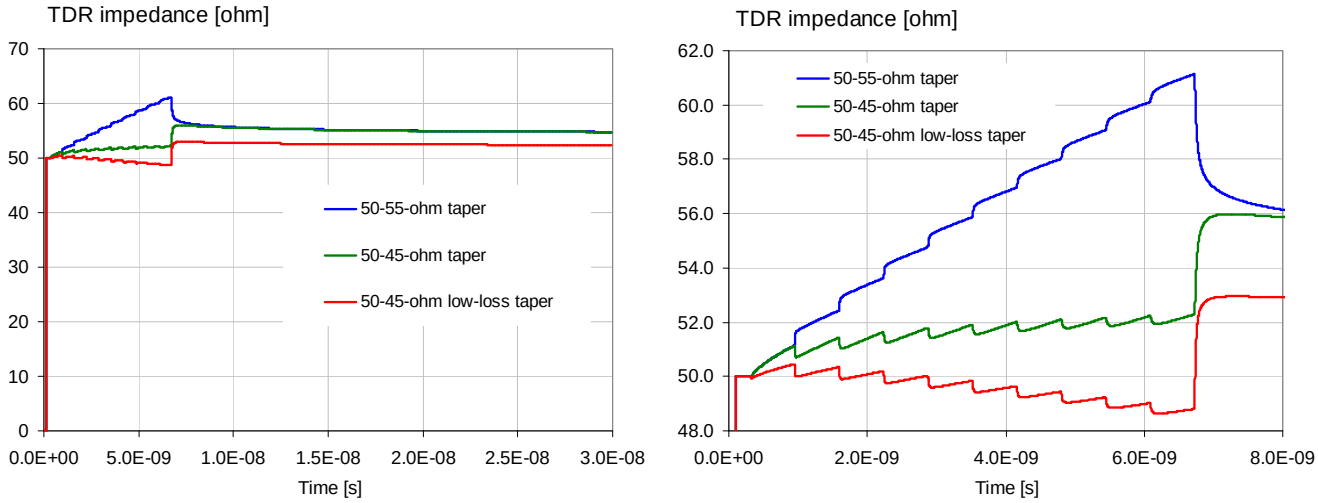

Figure 26: *TDR profile of ten cascaded 2" transmission lines with varying impedances: full scale on the left, zoomed scale on the right.*

Figure 26 shows the TDR response of ten pieces of 2-inch long cascaded transmission lines, where the characteristic impedance changes in 0.5-ohm increments step-wise going up or going down from 50-Ohm at the observation point. The lines represent the typical properties we assumed for the

earlier examples: Rdc = 0.2 Ohm/inch, a fixed Rdc/Rs ratio of 10,000 and medium-loss PCB material with Df(1GHz) = 1%. The blue line shows the response of line impedances changing from 0% to +10% with respect to 50 Ohms. The green line shows the response of line impedances changing from 0% to -10% with respect to 50 Ohms. If measured from one end only, and assuming that at the observation point the impedance deviation is zero, the blue and green lines bound the area where the actual trace response can be with a linear change of impedance. Whenever characteristic impedance changes, losses may also change. If the characteristic impedance increases due to narrower traces, it will also increase the resistive loss, further opening up the envelope. The red line in Figure 26 shows a more hypothetical case, when we assume that the DC resistance of each segment is lowered by a factor of two: Rdc = 0.1 Ohm/inch The factor of two range can be considered as the worst-case bound from all of the contributors that affect DC resistance: variation of trace width (usually specified as +-10%), variation of copper thickness (for instance, 0.5-mil to 0.7-mil for 0.5 oz copper, [16]) and also variations in conductivity and etching factor.

IV. Modeling and potential compensation

In this section we look at a couple of options how we could model the TDR response, as well as looking into the possibility of removing the loss-dependent tilt from the TDR results.

From Section II we can conclude that for nominally uniform PCB or package traces the main factor that we might want to model is the impact of resistive losses on the TDR profile. As we showed, dielectric losses for typical medium and low-loss materials create less deviation from nominal impedance and most of the time-dependent change is concentrated around sudden changes, which on a nominally uniform trace can happen around the end points, where via discontinuities will have a tendency to mask it. Resistive losses, on the other hand, induce a long rise of the impedance plot. The longer and more resistive the trace, the more deviation we get from the nominal impedance value [9]. (5) uses a first-order Taylor-series approximation to obtain the Z_c characteristic impedance:

$$Z_c(\omega) = \sqrt{\frac{L}{C}}\left(1 + \frac{1}{2}\frac{R_{DC}}{1 + j\omega L}\right) \tag{5}$$

This translates to linearly time-dependent characteristic impedance in the time domain:

$$Z_c(t) = \sqrt{\frac{L}{C}}\left(1 + \frac{t}{\tau}\right), \qquad \tau = \frac{2L}{R_{DC}} \tag{6}$$

If we apply (6) to the measured and simulated data set in our illustration, we get a time constant of 72 ns and the estimated curve shown by the green line in the left plot of Figure 27. Since the first-order Taylor series does not capture the frequency-dependent AC impedance, the impedance rise is just partially captured by (6). We could still get a better estimate with a linear function, if we apply it directly to the simulated data. The result is shown on the right plot of Figure 27.

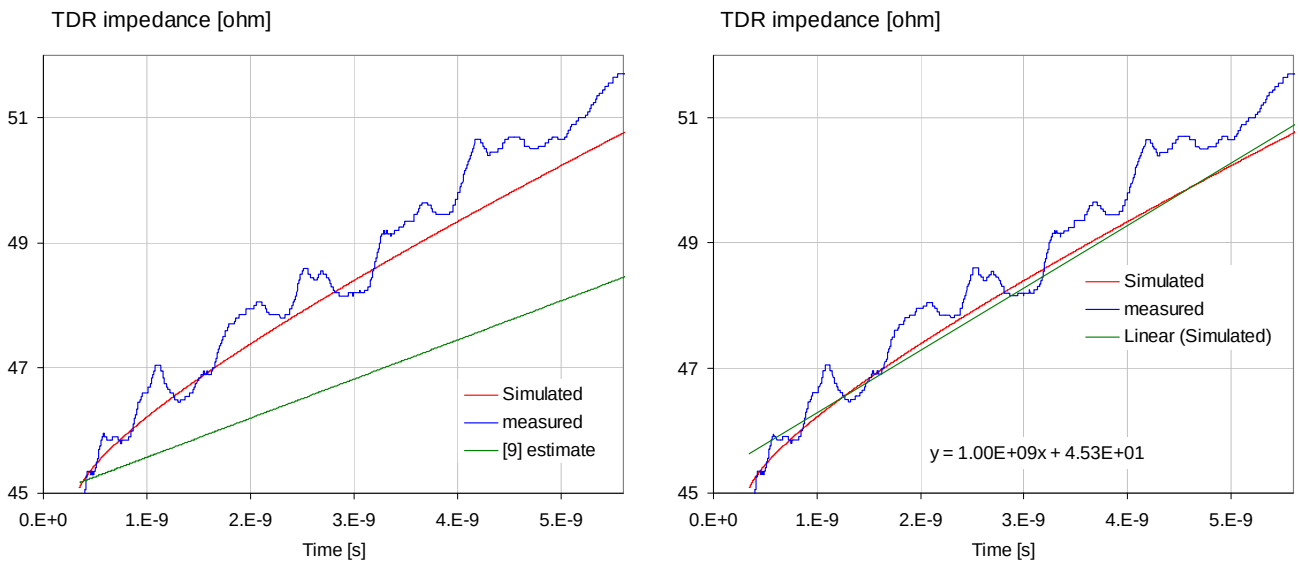

Figure 27: Measured, simulated and estimated impedance profile of the 17" trace from Section III. Linear estimate based on (6) on the left, linear approximation of the simulated impedance curve on the right.

After the first nanosecond, the linear approximation of the simulated impedance is within +-0.5 ohms, but there is a sharply increasing difference as we move closer to the origin on the time scale. A higher order polynomial can capture the frequency and time-dependent variations more accurately. The left plot of Figure 28 shows a sixth-order polynomial fit of the simulated data.

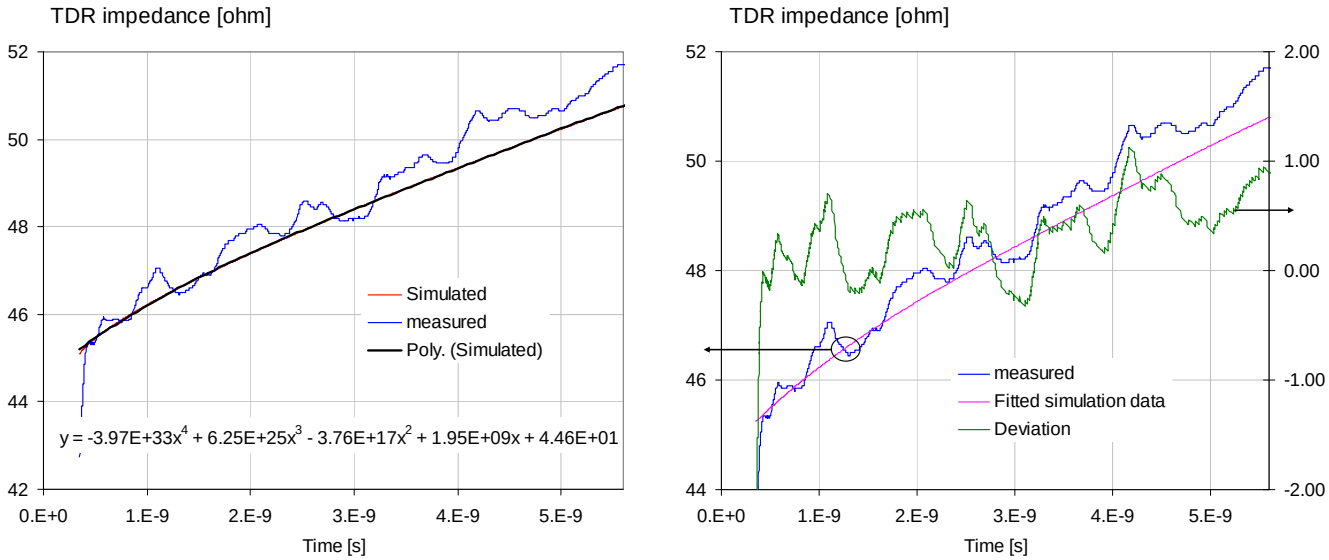

Figure 28: *Measured, simulated and estimated impedance profile of the 17" trace from Section III. Sixth-order polynomial estimate on the left plot, measured, simulated data and deviation between them on the right plot.*

The green trace on the right plot of Figure 28 shows the difference between the measured trace TDR profile and simulated TDR profile based on nominal parameters. We can see that the deviation is well within +- 1.5 ohms, which is better than +- 5%. Unfortunately as it was pointed out in connection with Figure 26, this is still not a full guarantee that the trace impedance is within spec throughout its entire length.

In PCB manufacturing it is customary to have test coupons on the panel for various purposes, among others to check the characteristic impedance of traces on different layers with given trace width. [1] suggests the impedance reading to be taken as the 30-70% average of the TDR response. Let us assume a 6" long test coupon, which may be typical on larger PCB panels. We can take the simulated trace data from Figure 28 and average the values between 30 and 70% of delay corresponding to a 6" long trace. The value we get is 1.61 ohm above the nominal. Note that this is due to the way how the TDR plot is interpreted; because otherwise the frequency-dependent characteristic impedance varies much less in the frequency range of interest (see Figure 4). Note also that this offset depends on the trace geometry and conductor conductivity. In some package applications, where pure copper cannot be used for the conductors, the lower conductivity and the usually narrower thinner traces will create more offset.

Conclusions

Testing PCB and package traces for impedance compliance commonly uses TDR instruments. The TDR response can be converted into impedance, but the conversion is unique and yields a single characteristic impedance only if the DUT trace has zero loss, is uniform throughout its length, and discontinuities are negligibly small. Losses create frequency dependent characteristic impedance and time dependent TDR response. Dielectric losses reduce the impedance by a small amount sharply after the excitation step and it is followed by a small negative tilt of the response. The average drop of impedance due to dielectric losses is approximately half a percent for each percent of dielectric loss tangent. Because most of the drop occurs within a short time at the beginning of the TDR response, the later impedance response does not depend strongly on the interconnect length.

Resistive losses create an upward tilt of the TDR response. DC resistance of conductors creates a linear rise of the response, which creates an increase of impedance by the end of the round-trip delay equal to the full DC resistance. AC conductor losses, such as skin, proximity and surface-roughness losses, create further positive tilt of the TDR response. The gradient of the extra impedance rise is highest at the beginning of the response, where the bandwidth of the stimulus is the highest, gradually approaching zero gradient on very long lossy interconnect as the stimulus bandwidth gets lower. Because the upward tilt due to the DC conductor resistance is always present, the deviation from the nominal impedance keeps rising as we measure longer and/or more resistive traces. For typical long PCB traces in high-density large-size PCBs, the positive deviation of the TDR response can reach more than 10%. To get the DC resistance of traces for measured cross section data, the copper thickness has to be measured across the minima of the tooth structure.

Even on a nominally uniform trace, manufacturing tolerances create different trace width and dielectric height at different locations. Moreover, the relative position with respect to glass-weave bundles will create location-dependent dielectric constant around the traces. As a result, the characteristic impedance varies along the trace. By taking the TDR response we want to identify local anomalies along the DUT, but the distortion of the TDR response due to dielectric and

conductive losses may mask out smaller local changes. The bulk of the TDR response distortion on long and/or resistive traces can be modeled and captured by a six-order polynomial. The predicted nominal TDR response can be extracted from the actual TDR response to better reveal local anomalies.

Test coupons on large panels with narrow traces may have up to a couple of ohms positive offset in the TDR response of the coupon trace. This offset is dependent on the trace cross section and material conductivity and has to be established separately for each combination of parameters.

Acknowledgement

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