DesignCon® 2013

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SANTA CLARA CONVENTION CENTER

Determining PCB Trace Impedance by TDR: Challenges and Possible Solutions

Session 6-TA4

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UBM Tech

Acknowledgement, Credit

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Outline

- Introduction and Background
- Performance of Uniform Transmission Lines
- Manufacturing Variability
- Modeling and Potential Compensation
- Conclusions

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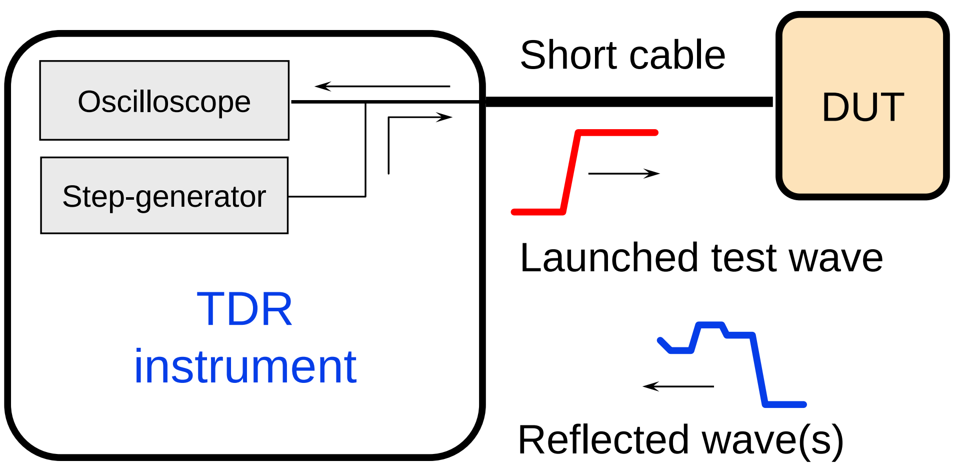
Time Domain Reflectometry (TDR)

- High-speed interconnects must be designed for specified impedances
- Validation requires measuring the impedance
- Popular option to measure impedance is TDR



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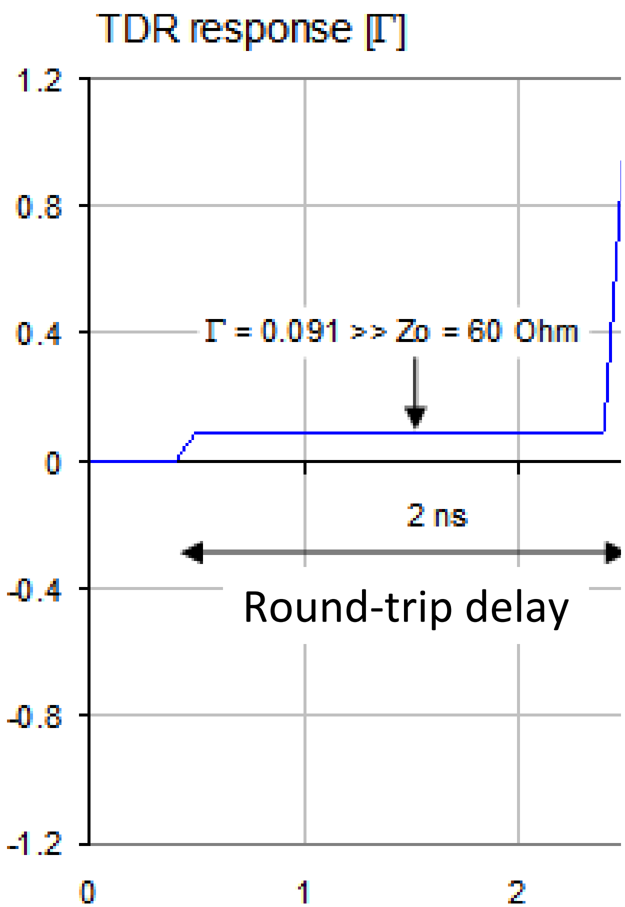
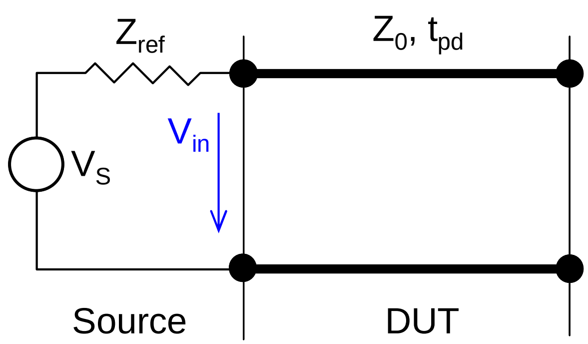
TDR Response of Uniform Loss-less Line

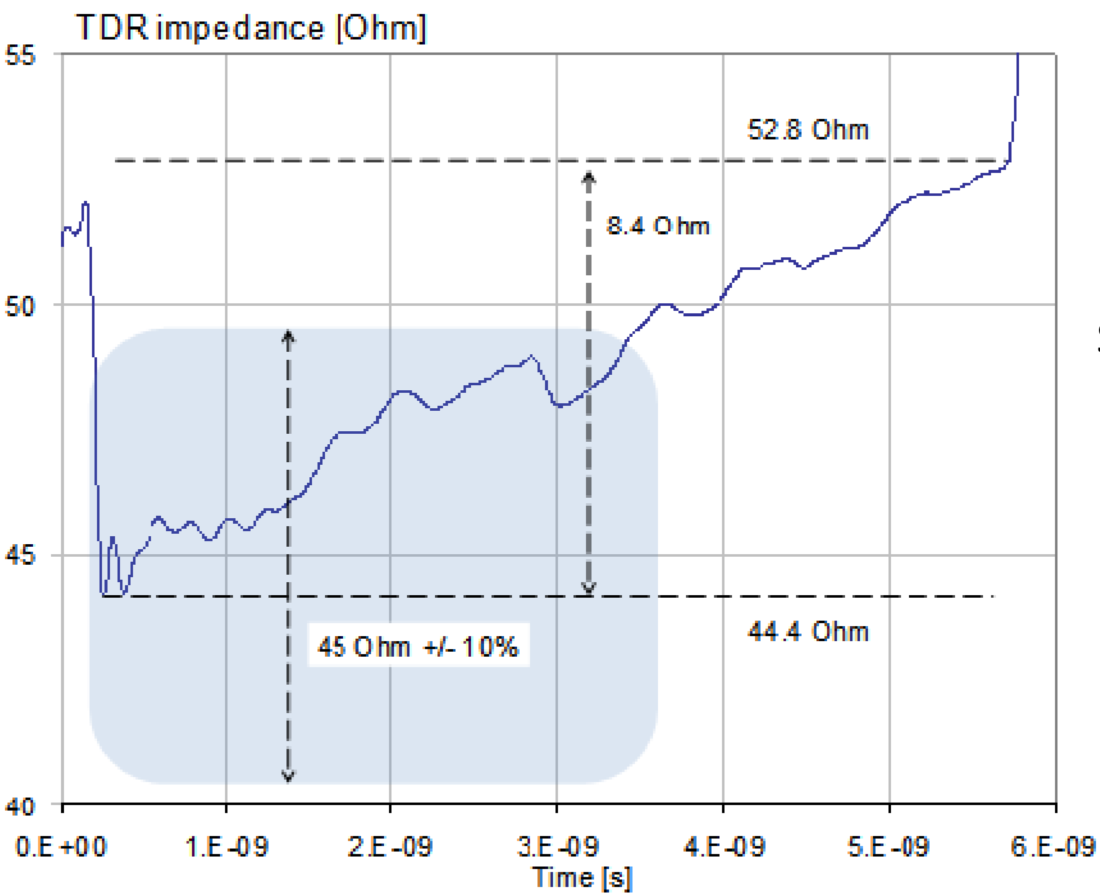




$$\Gamma = \frac{Z_0 - Z_{ref}}{Z_0 + Z_{ref}}$$

$$Z_o = \sqrt{\frac{L_u}{C_u}} = \sqrt{\frac{L}{C}};\ \ t_{pd\_u} = \sqrt{L_u C_u};\ \ t_{pd} = \sqrt{LC}$$

PCB Trace Validation



Specification: 45 ohms +/- 10%

Is this trace OK?

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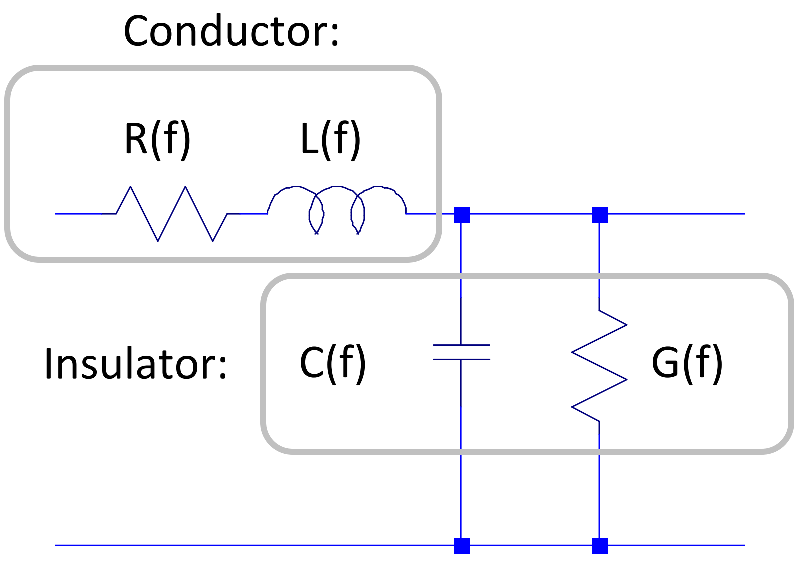
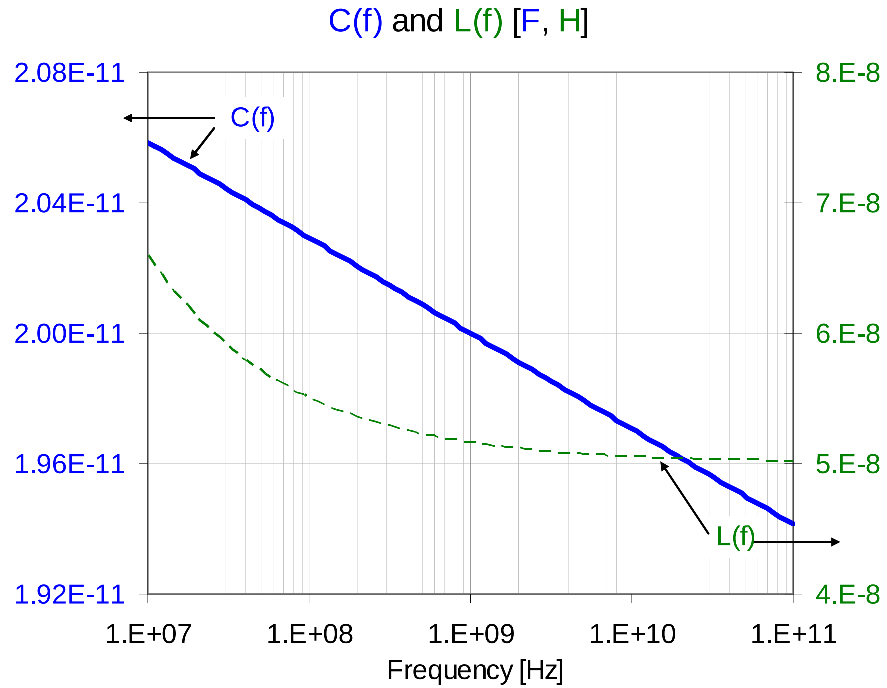
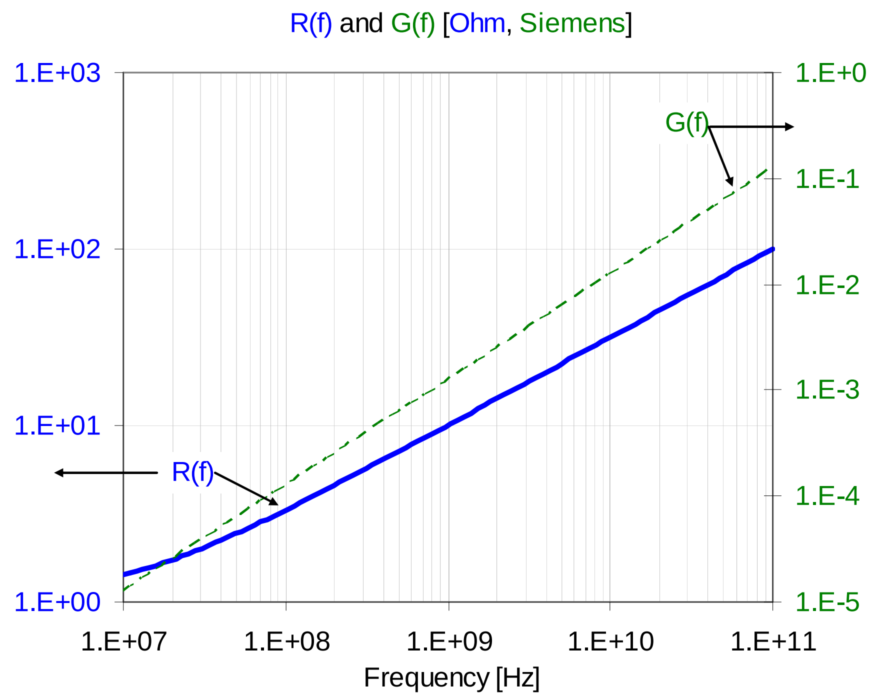
Uniform Lossy Line



$$Z_0 = \sqrt{\frac{R(f) + j\omega L(f)}{G(f) + j\omega C(f)}}; \quad \gamma(f) = \sqrt{(R(f) + j\omega L(f))(G(f) + j\omega C(f))} = \alpha(f) + j\beta(f) = \alpha + j\omega t_{pd}$$

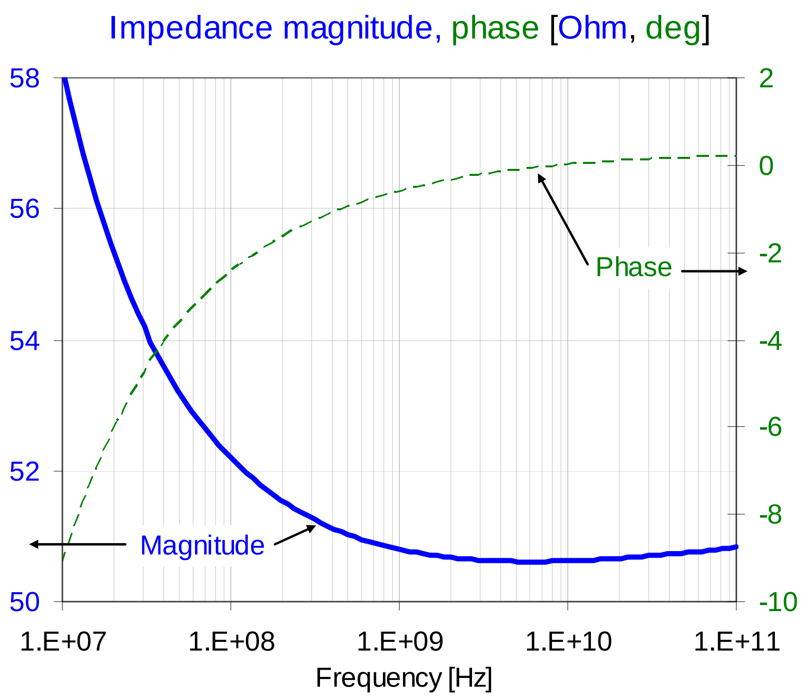
RLGC Parameters of Uniform Lossy Line

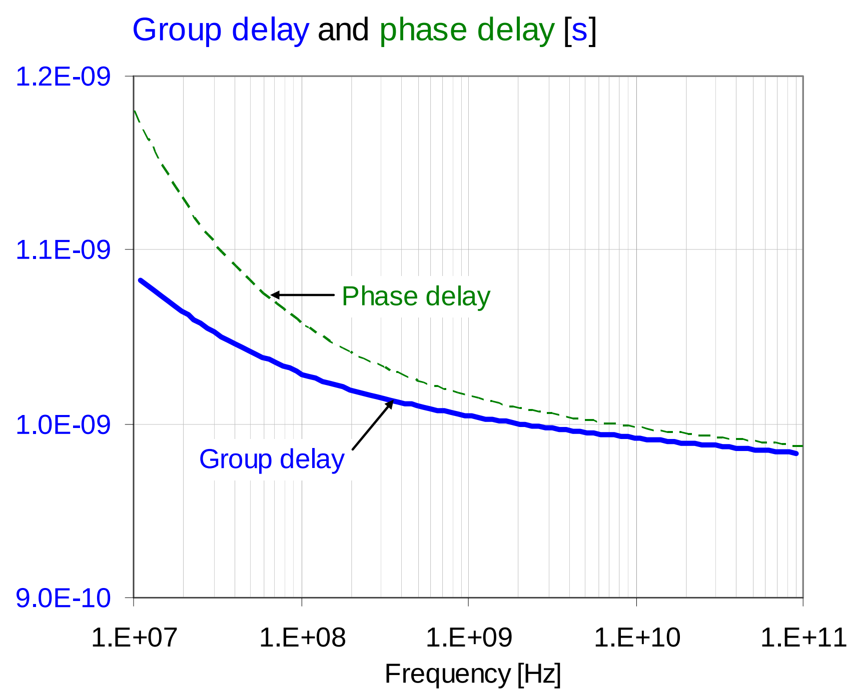




- Wide-band DeBye model used
- With increasing frequency:
  - Capacitance and inductance drop
  - Resistance and conductance grow

Impedance and Delay of Uniform Lossy Line





- Wide-band DeBye model used
- As a function of frequency Z_0 has a shallow bath-tub shape
- With increasing frequency delay drops

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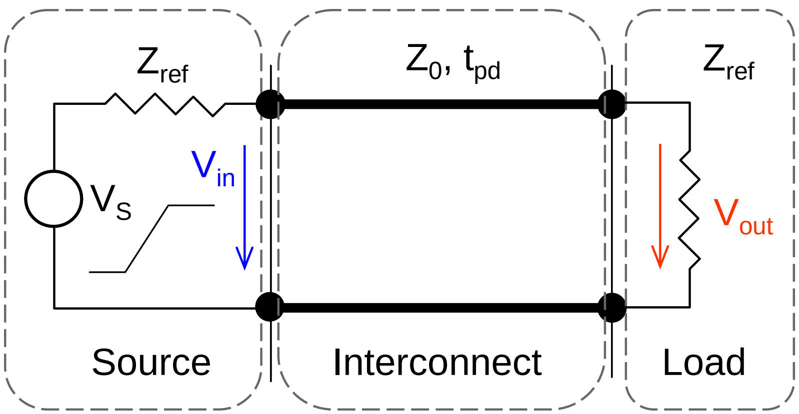
Simulating a Uniform Lossy Line

W Element RLGC Model

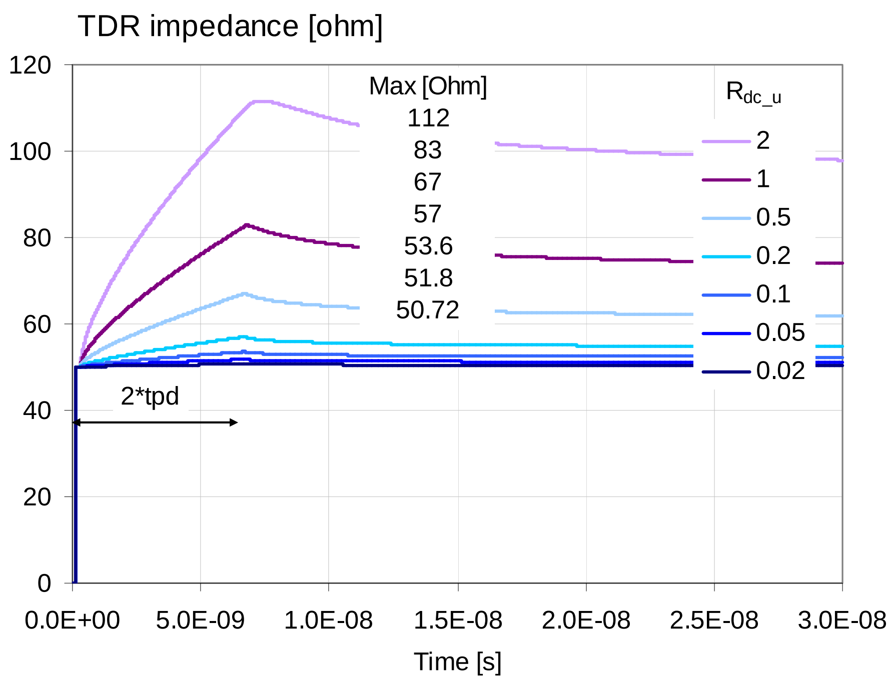


All TDR responses should settle at $Z_{ref} + R_{DC}$

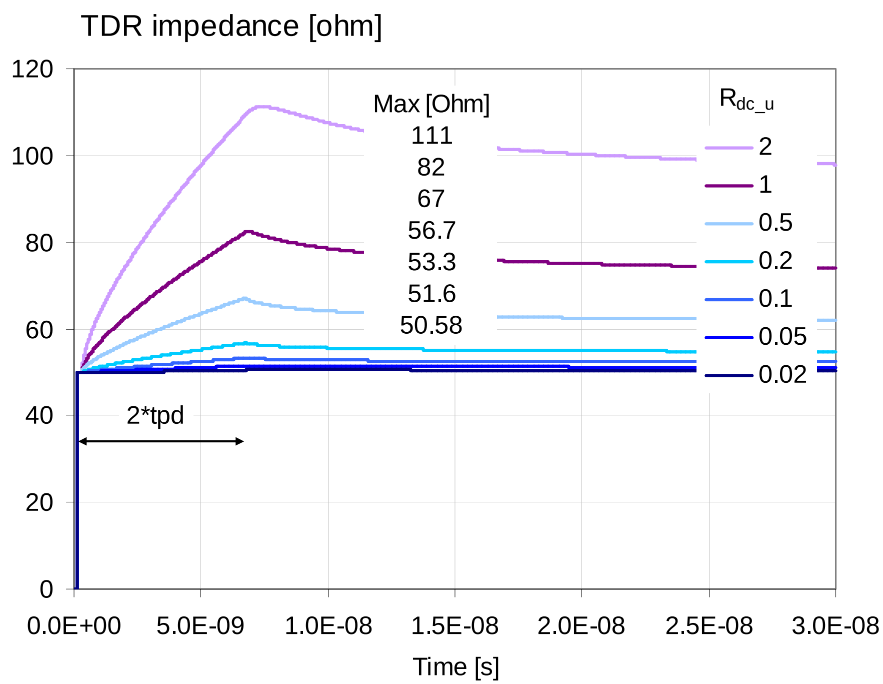
```
Wtest1  in2 0  out22  0  N=1  RLGCMODEL=W1  L=20
+ INCLUDEGDIMAG=YES
+ INCLUDERSIMAG=YES
* W-line model, values are per inch
.param Charimp1=50
.param Delayperinch1=160p
.param Lunit1='Delayperinch1*Charimp1'
.param Cunit1='Delayperinch1/Charimp1'
.param Rdcunit1=0.2
.param tandelta1=0.01
.MODEL W1  W  MODELTYPE=RLGC,  N=1
+ Lo = Lunit1
+ Co = Cunit1
+ Ro = Rdcunit1
+ Go = 0
+ Rs = 'Rdcunit1/10000'
+ Gd = 'Cunit1*tandelta1'
```

Uniform Lossy Line, Resistance Sweep

20-inch 50-ohm line
Ideal dielectric, Df = 0



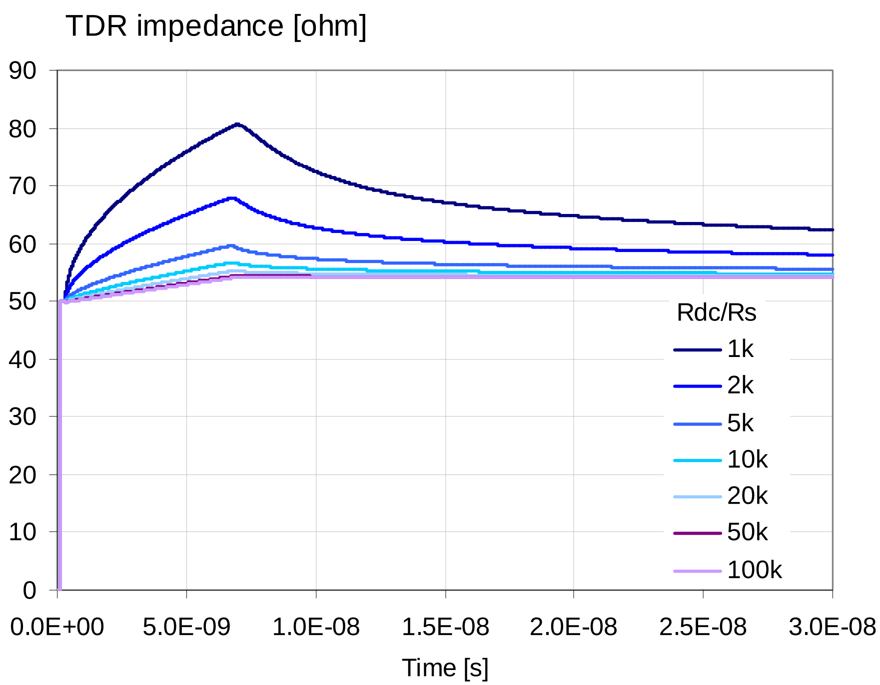
20-inch 50-ohm line
Medium dielectric loss, Df = 1%

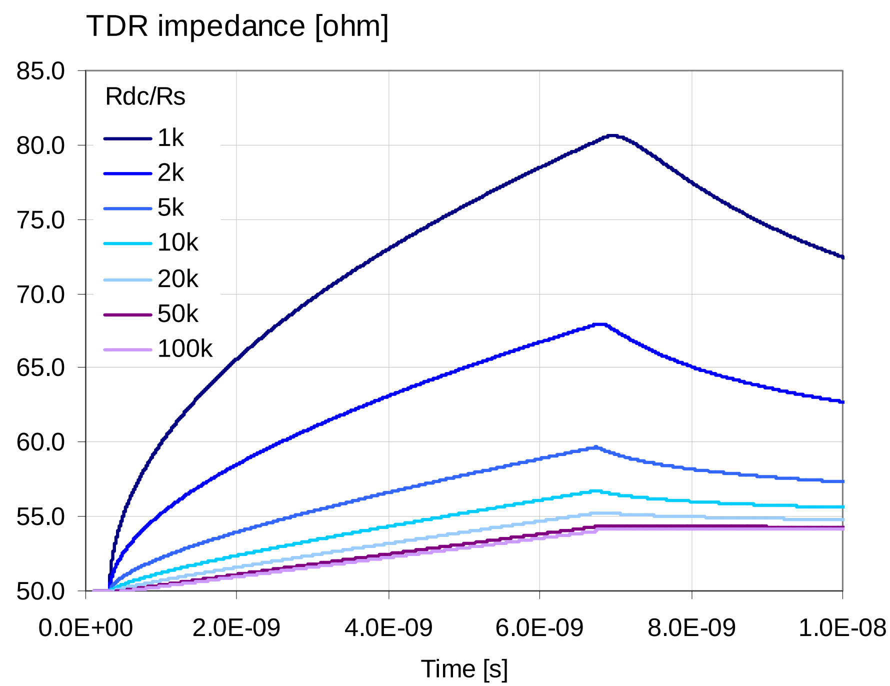


Resistance creates upslope.
AC resistance produces overshoot.
Dielectric loss reduces impedance!

Uniform Lossy Line, DC/AC Resistance

20-inch 50-ohm line
Medium dielectric loss
Df = 1%

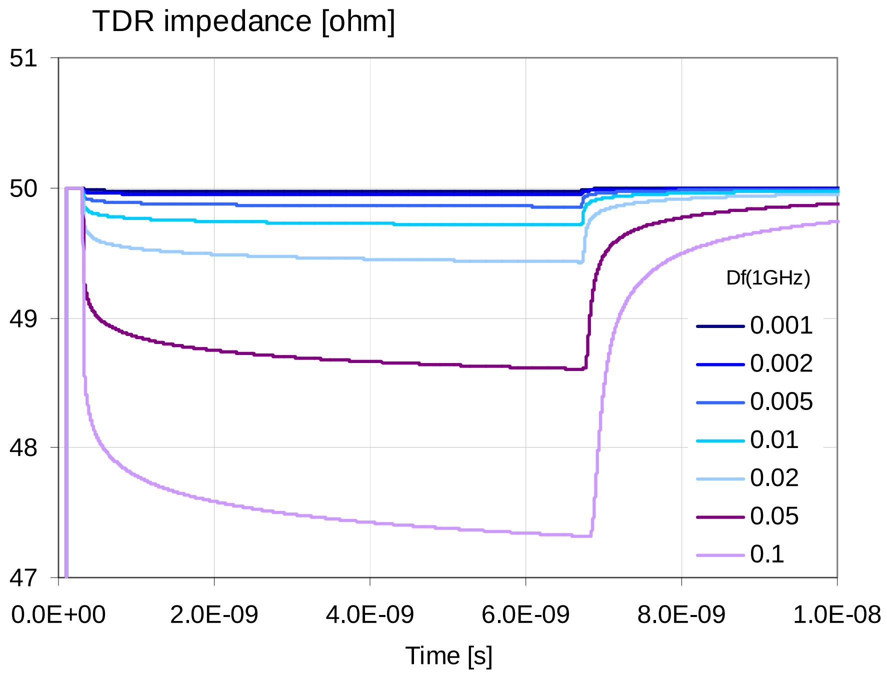




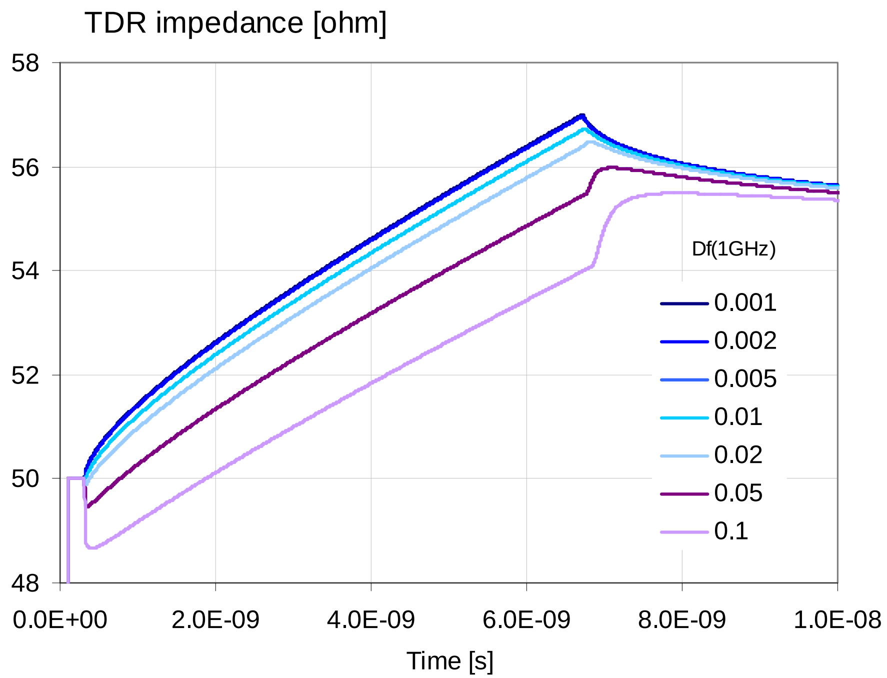
AC resistance increases apparent impedance and creates a changing slope.
With no AC resistance, TDR response climbs linearly to $Z_{ref} + R_{DC}$

Uniform Lossy Line, Dielectric Loss

20-inch 50-ohm line
Ideal conductor



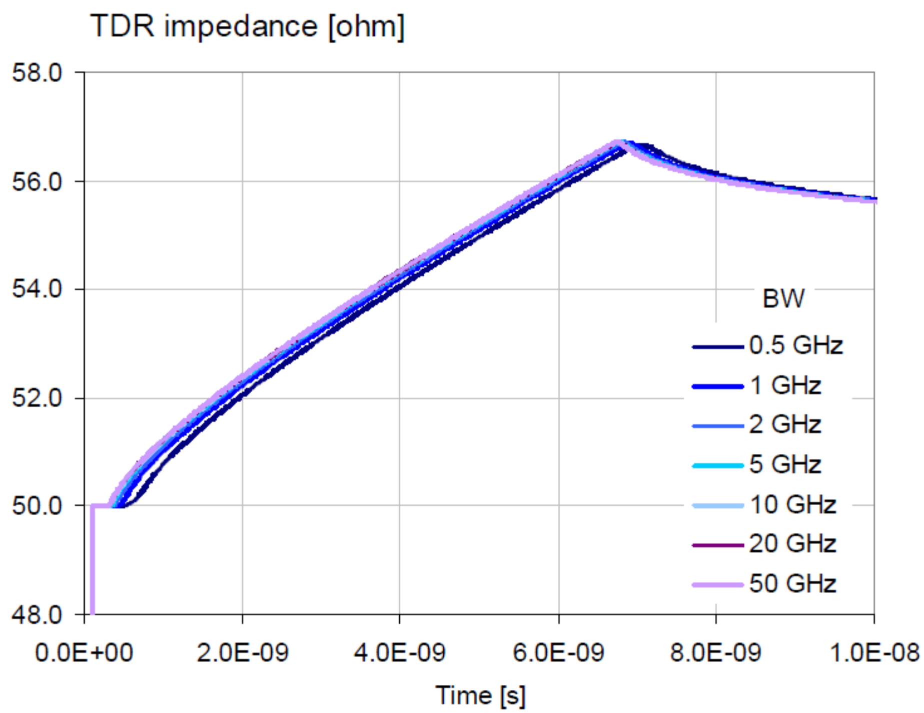
20-inch 50-ohm line
Rdc = 0.2 ohm/inch



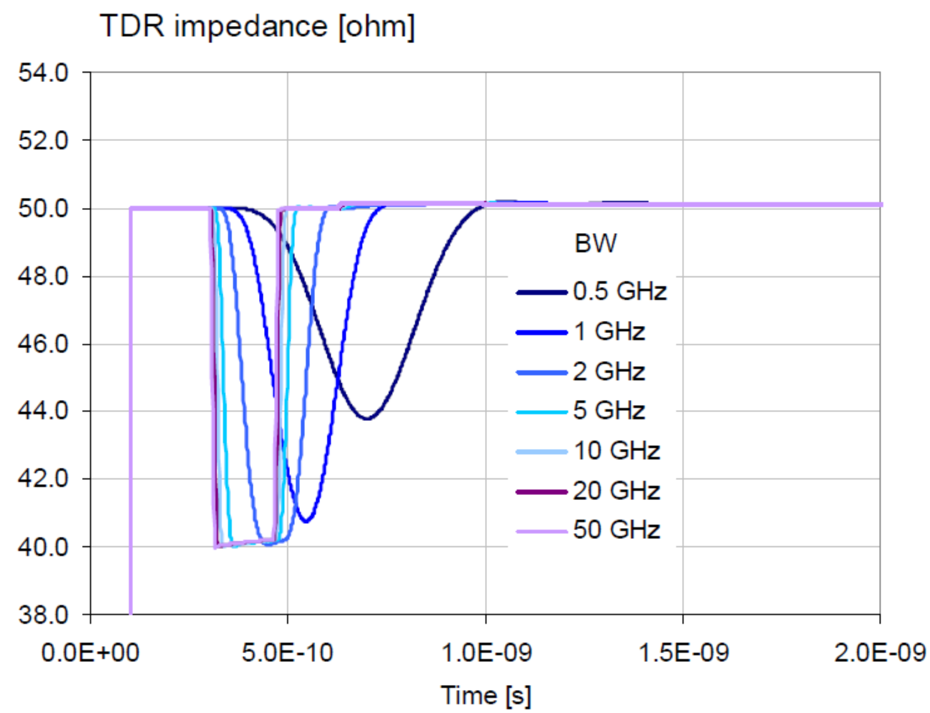
Dielectric loss lowers apparent impedance.
After a fast initial drop, impedance drops slowly.

Uniform Lossy Line, Bandwidth

20-inch 50-ohm line
Typical parameters



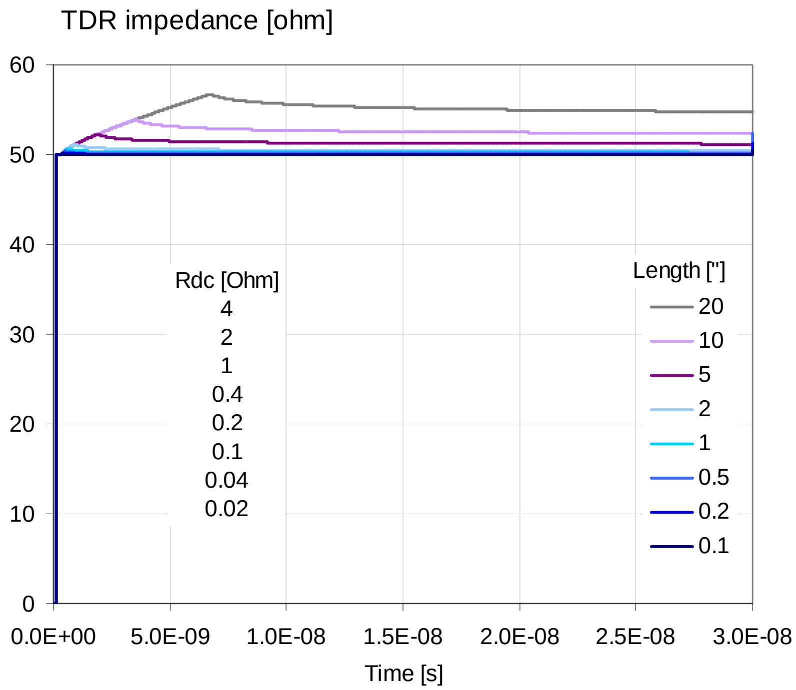
0.5-inch ***40***-ohm line
Typical parameters

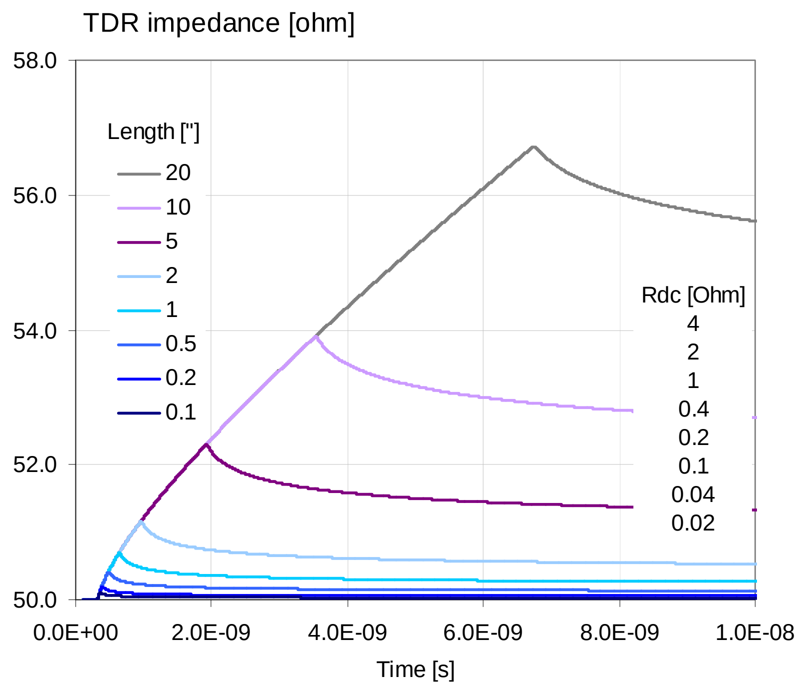


Lower bandwidth reduces horizontal resolution and slows response edge.

Uniform Lossy Line, Length Sweep

50-ohm line
Typical parameters

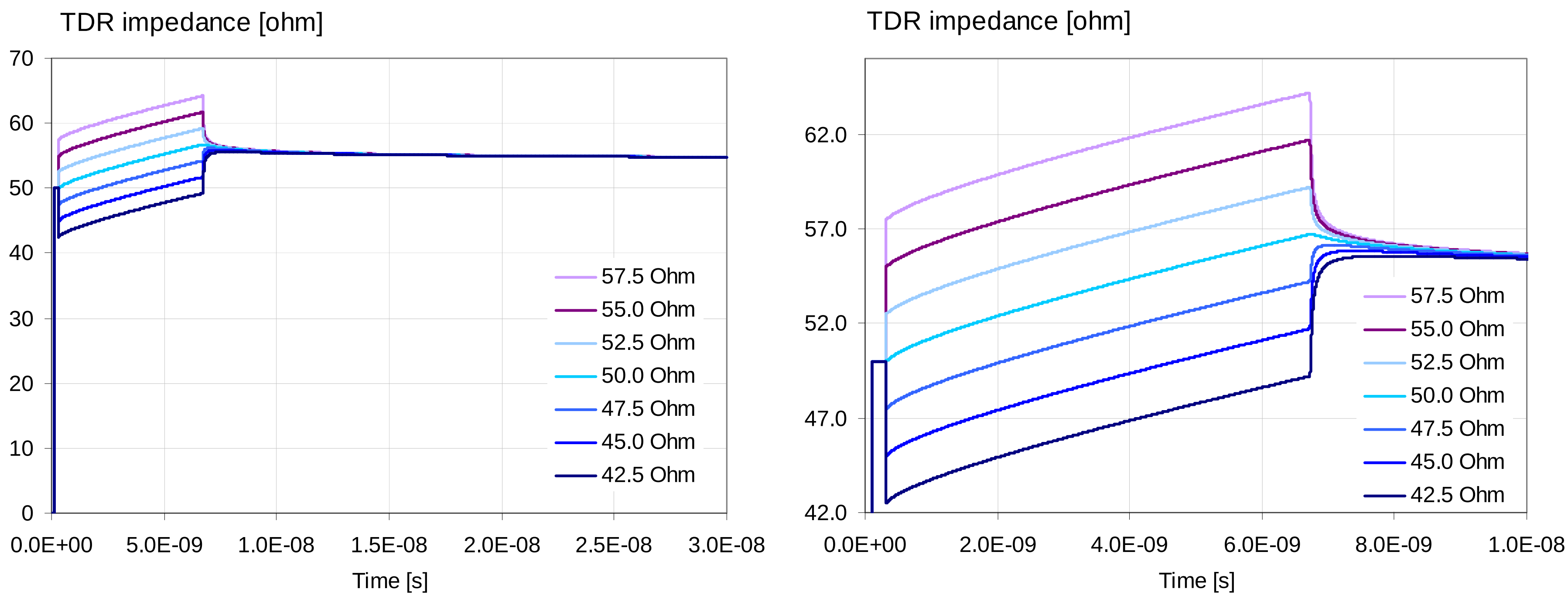




Envelope response can be used for any length of DUT

Uniform Lossy Line, Impedance

20-inch line
Typical parameters



Response shape is independent of DUT characteristic impedance as long as loss parameters stay the same

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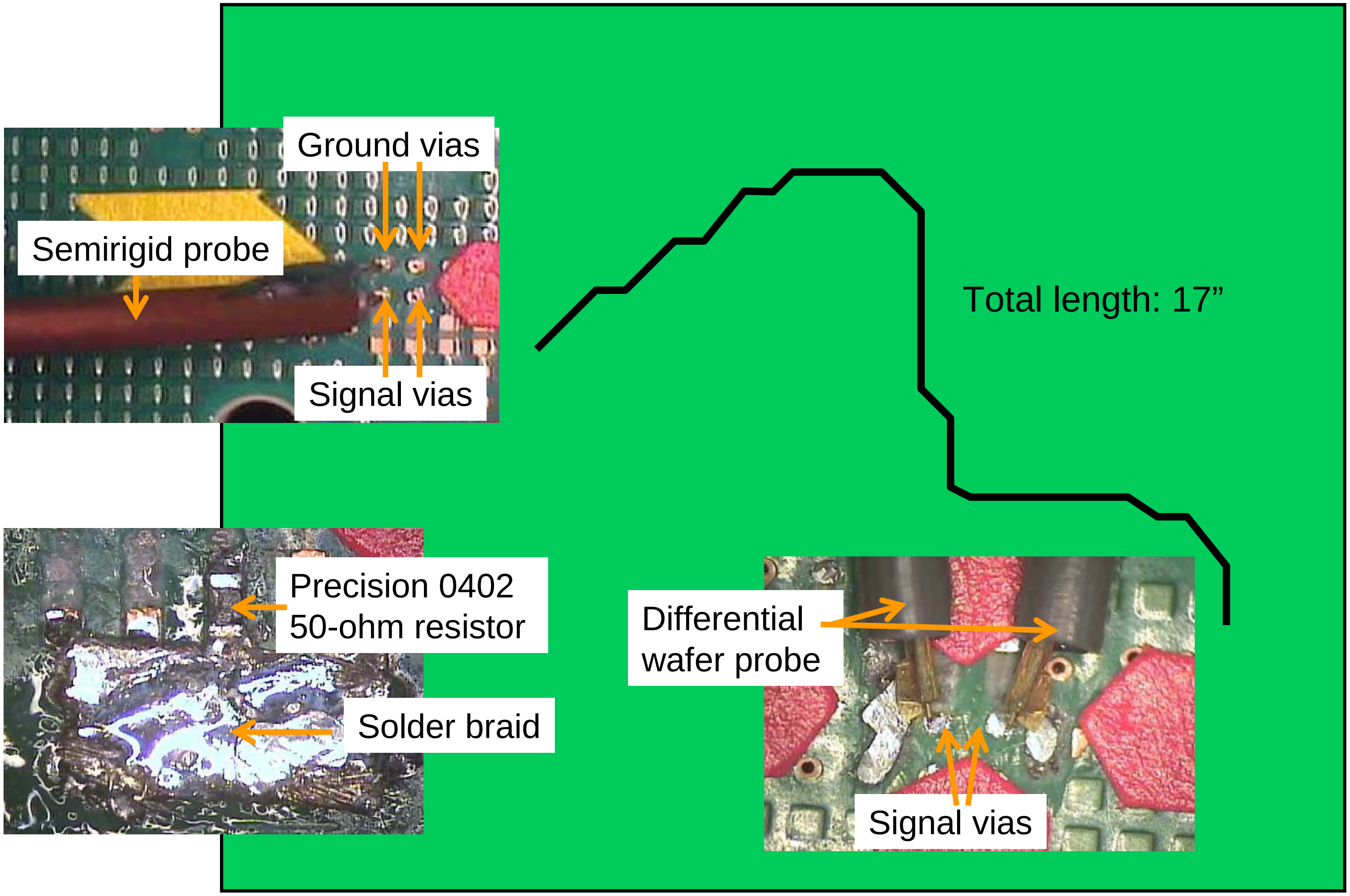
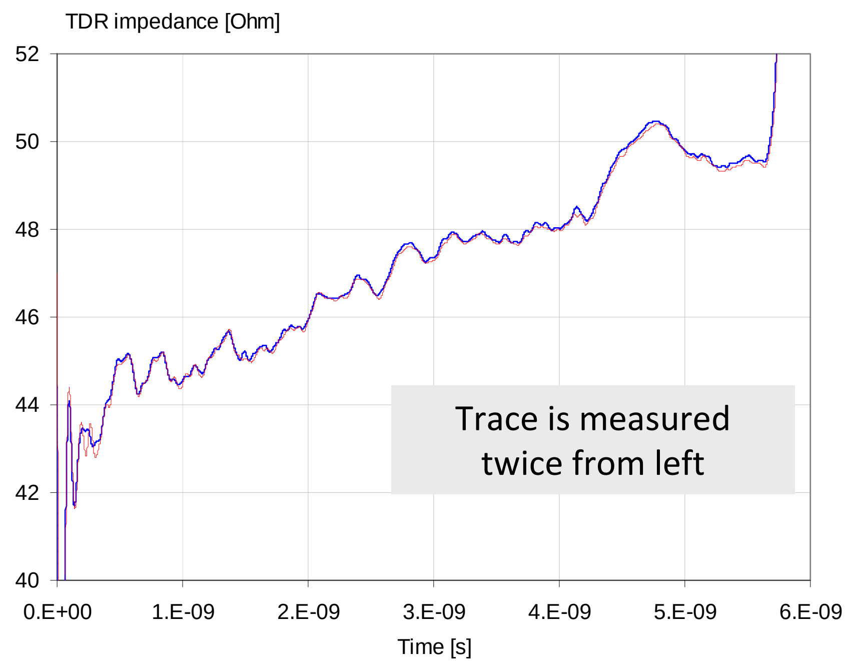
Device Under Test, Connections

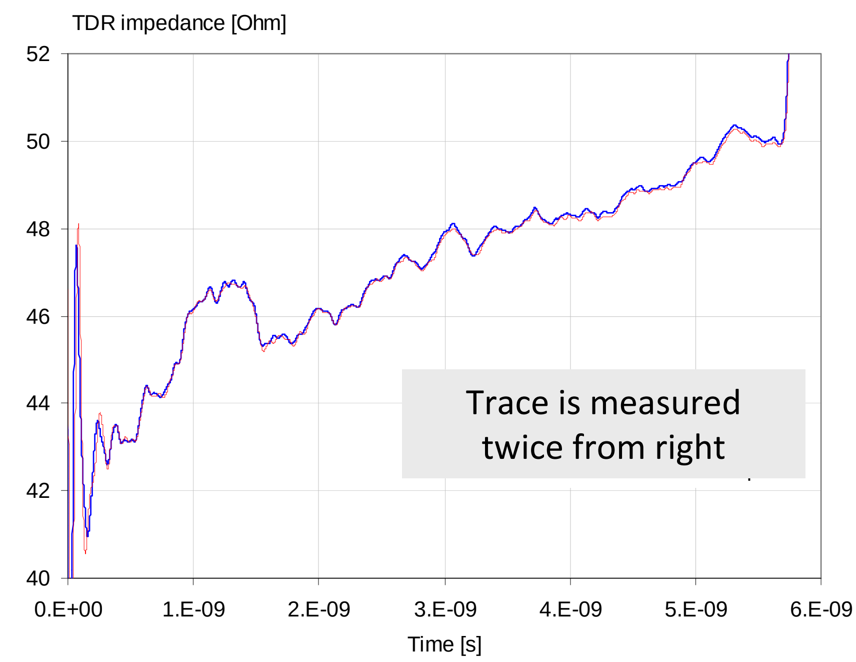


Repeatability

Same board, same trace measured multiple times.
- Same day with same calibration.
- Next day with old calibration.
- Next day with new calibration.

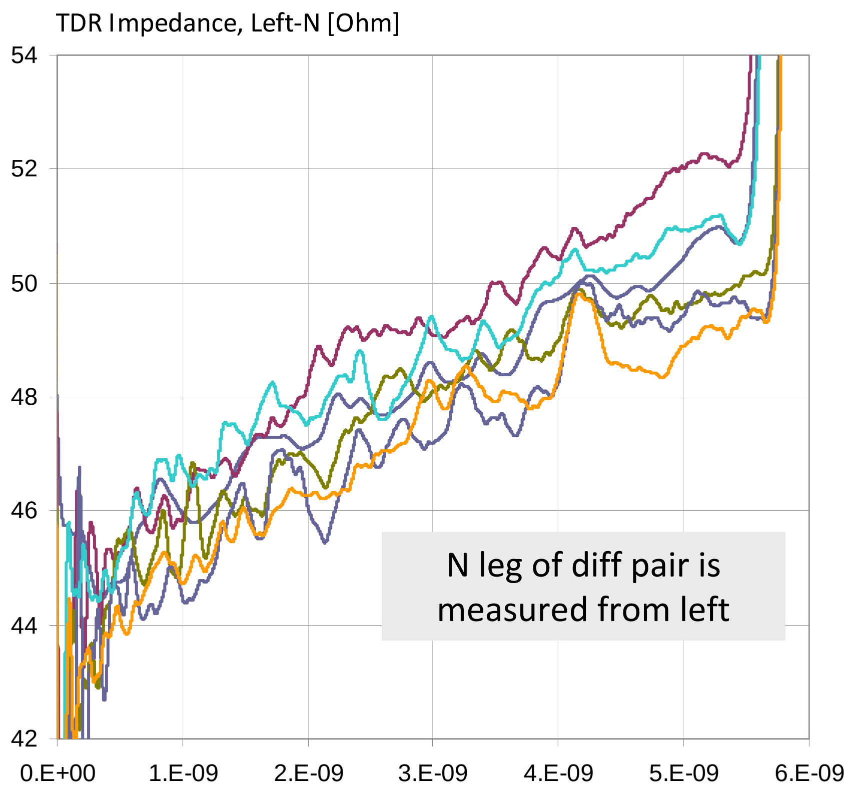
Very little variation was seen.

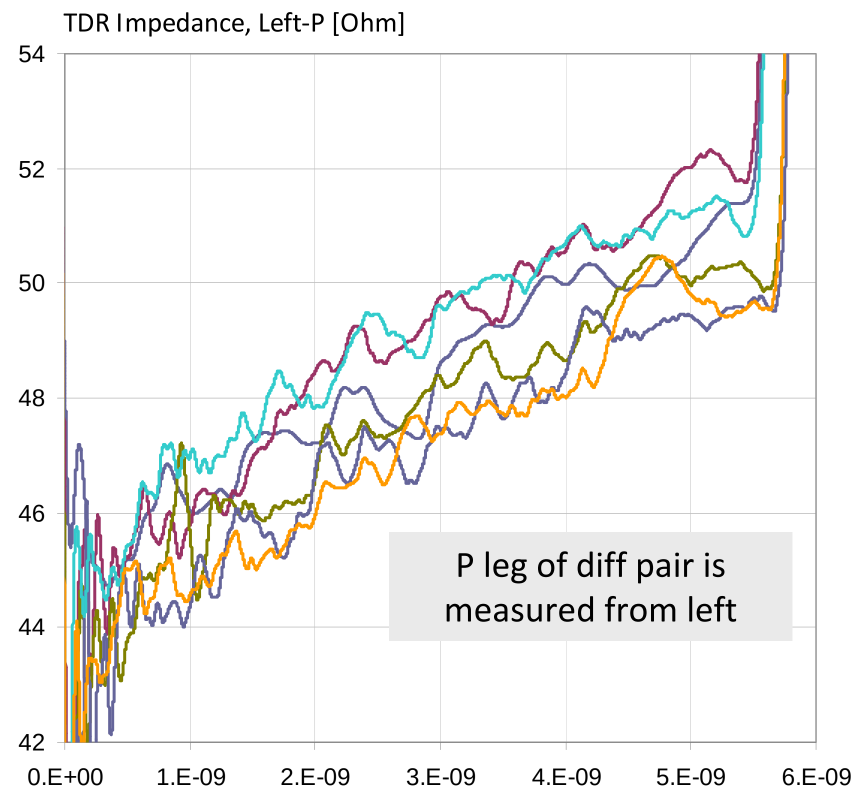




Board-to-Board Variation

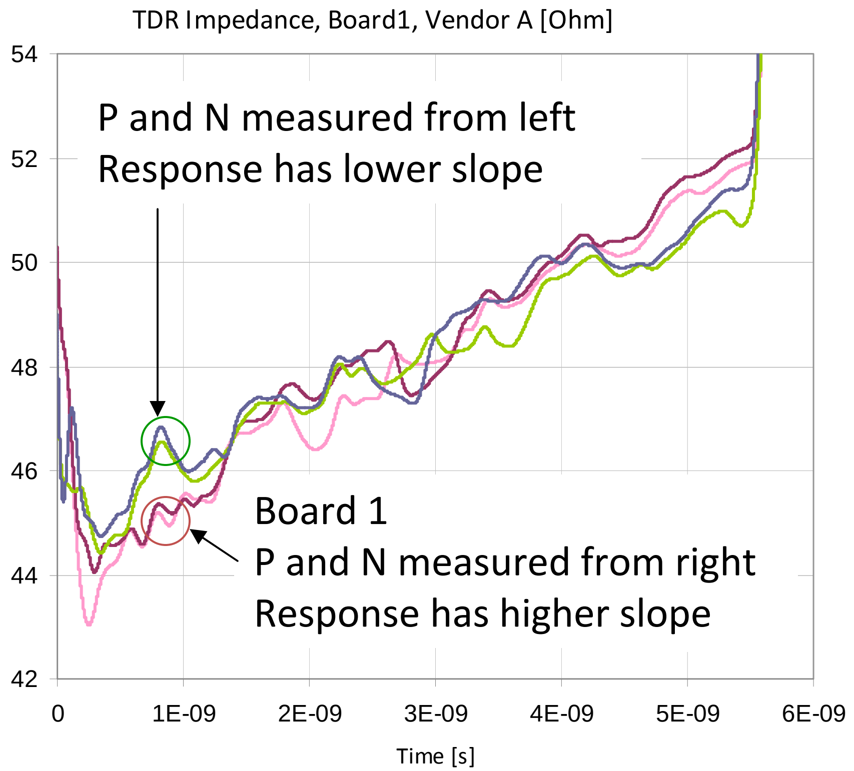
Six boards from two vendors
The same trace pair is measured
Same calibration, same probe
All traces follow the simulated signatures

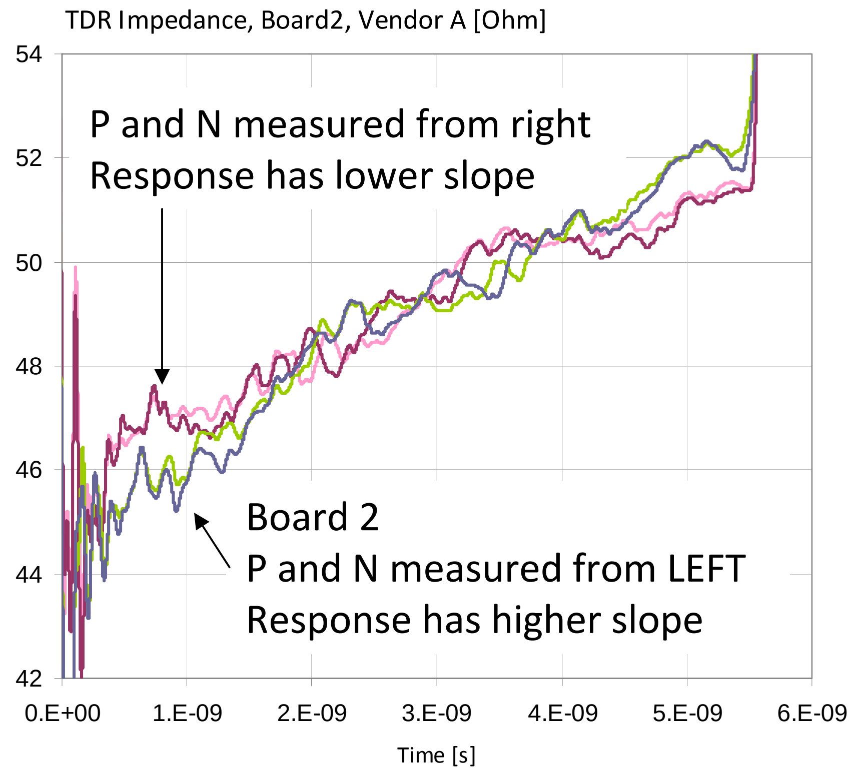




P-N, Left-Right Variation

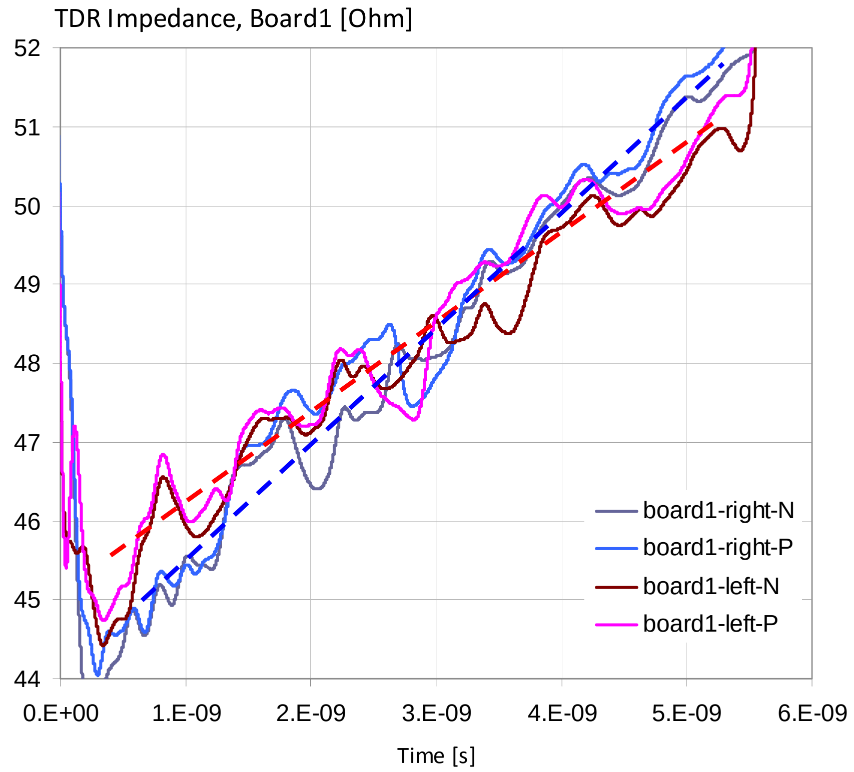
Two boards from the same vendor

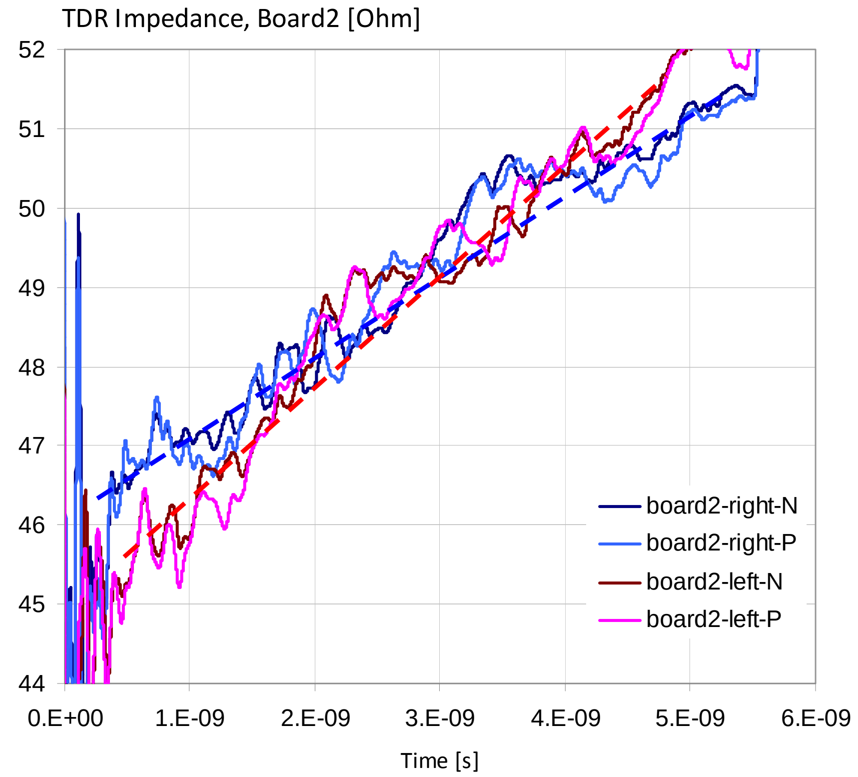




P-N, Left-Right Trends

Two boards from the same vendor
Different slopes from left-to-right vs. right-to-left!!!





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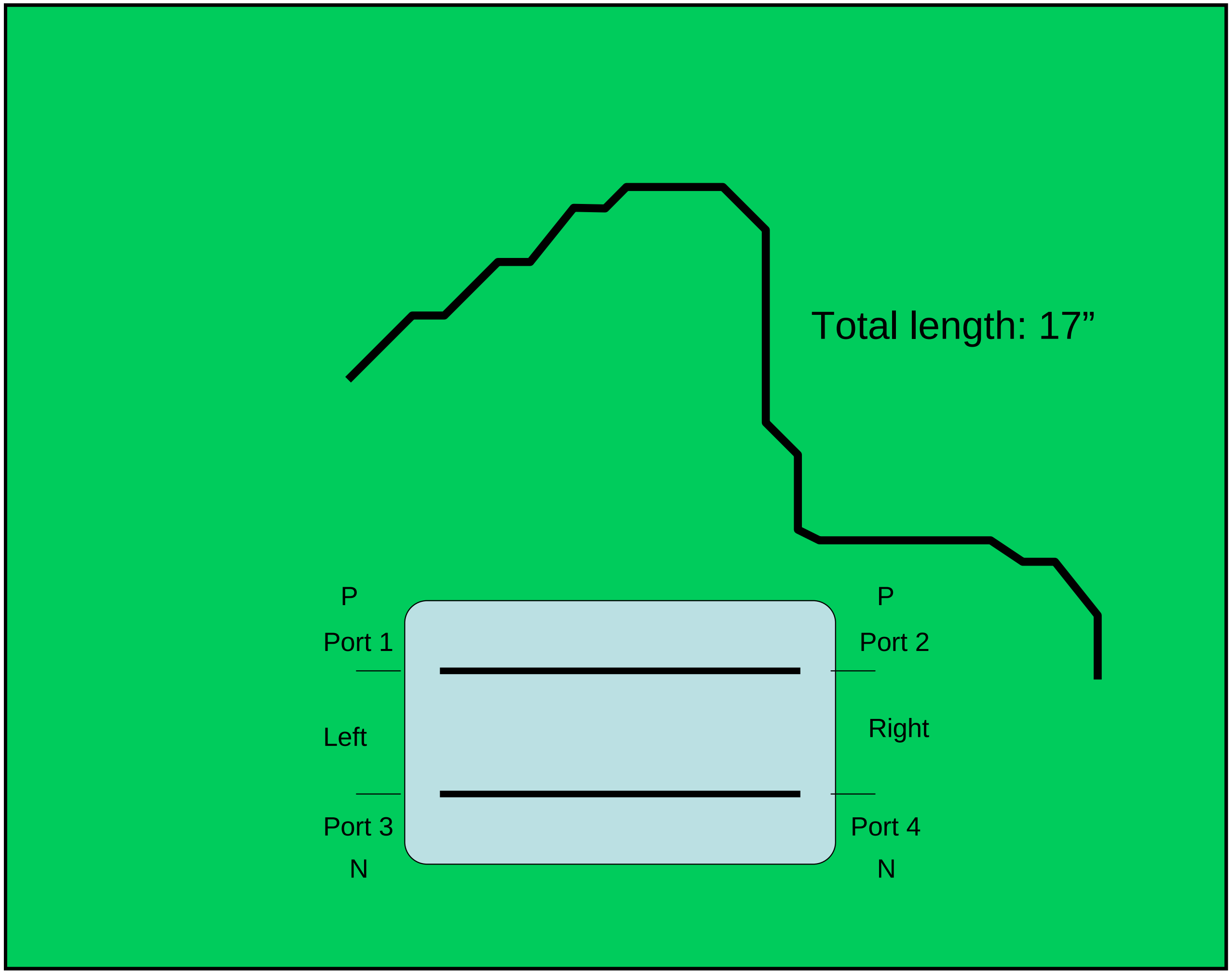
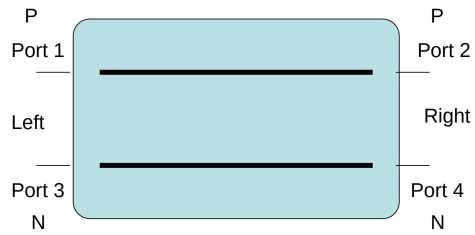
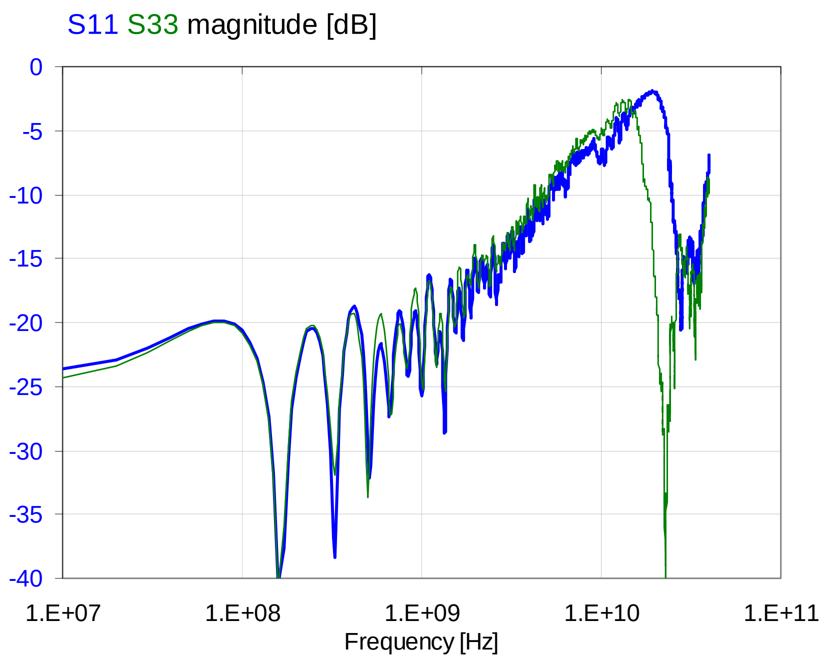
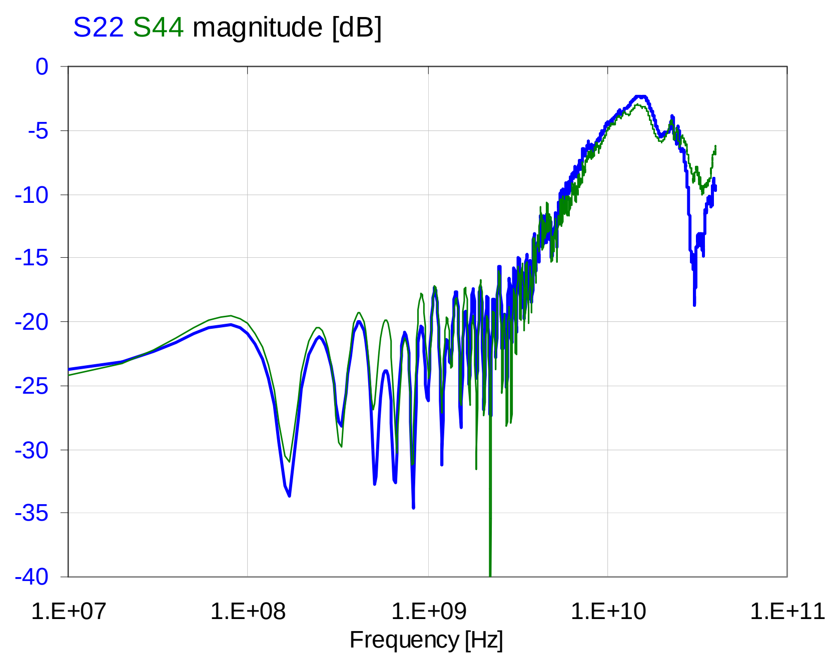
VNA Measurements, Ports



Single Ended Reflections

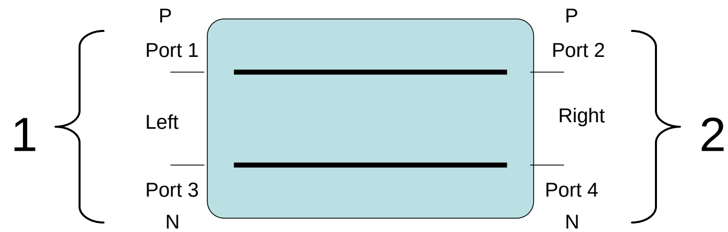


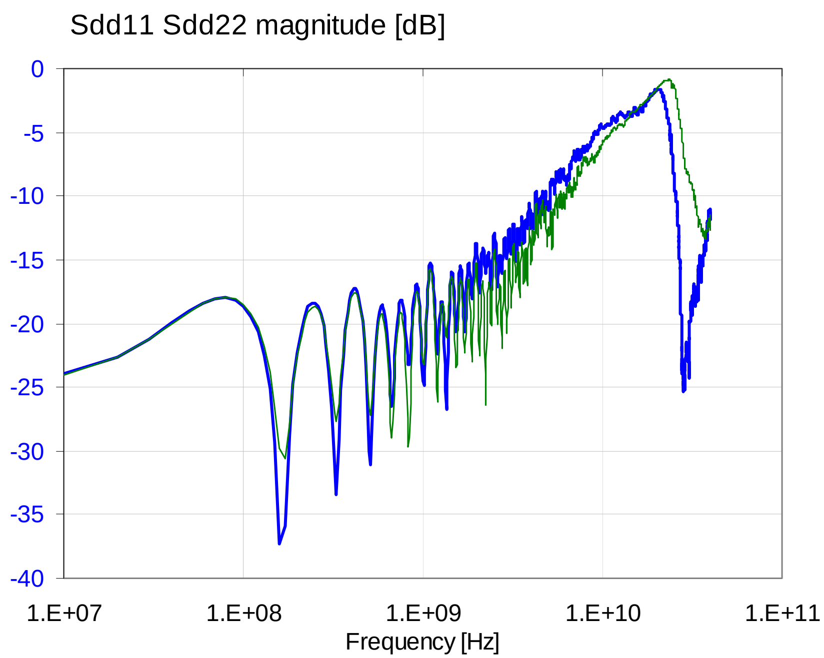


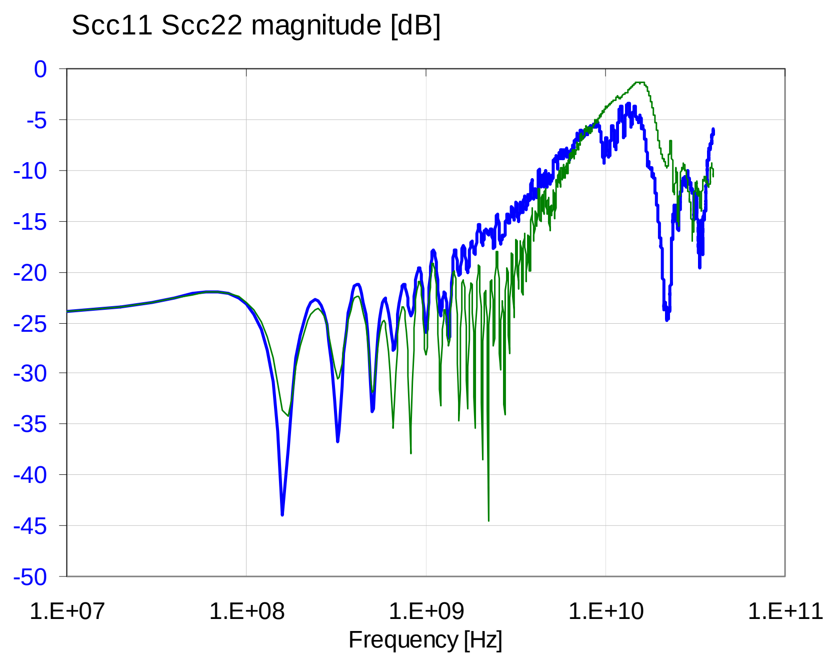


Up to 10 GHz only small differences

Differential Reflections

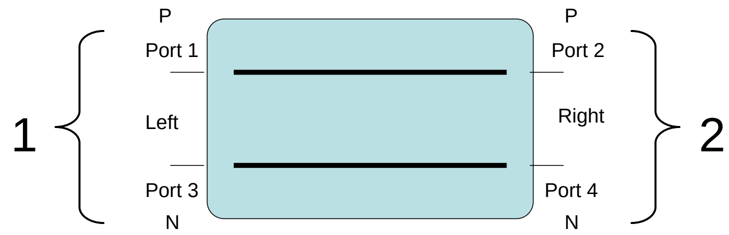


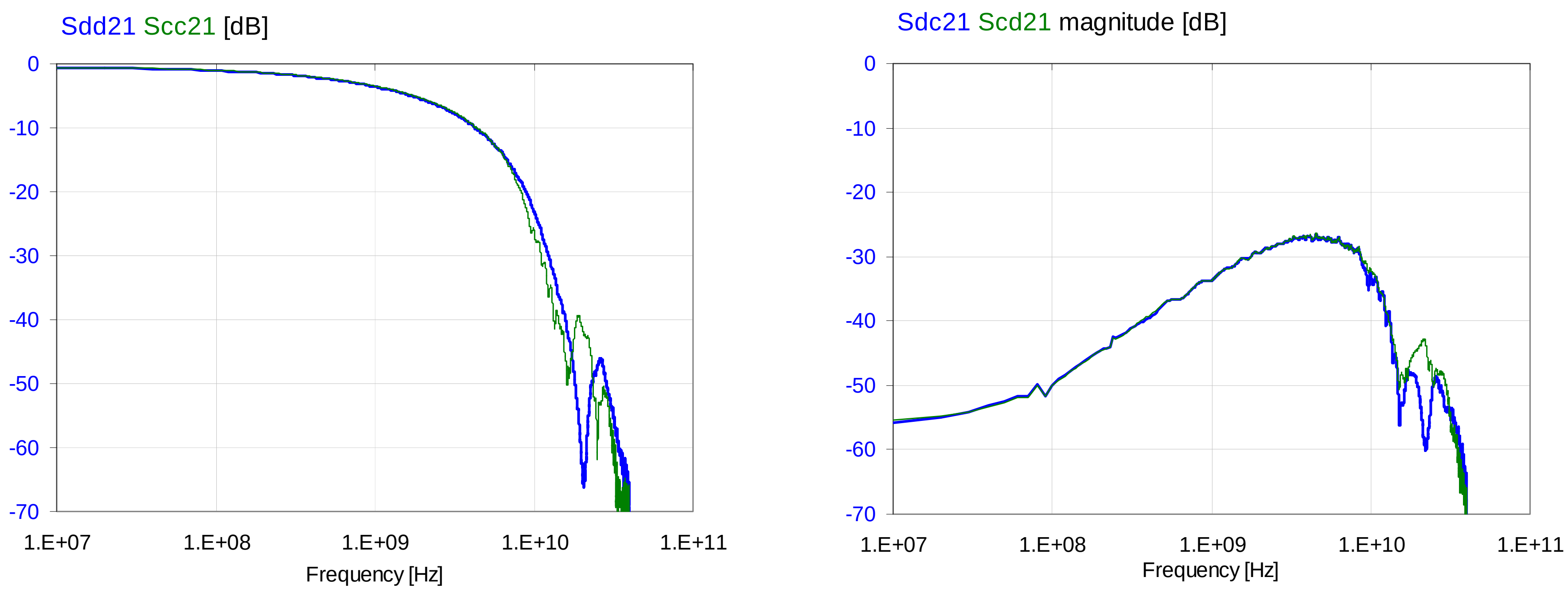




5-10dB difference in the 1-10 GHz range

Transfer, Mode Conversion





Up to 10 GHz only small differences

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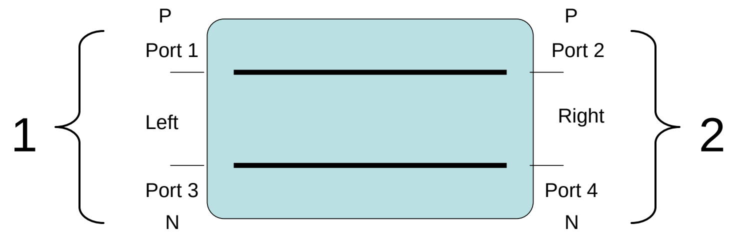
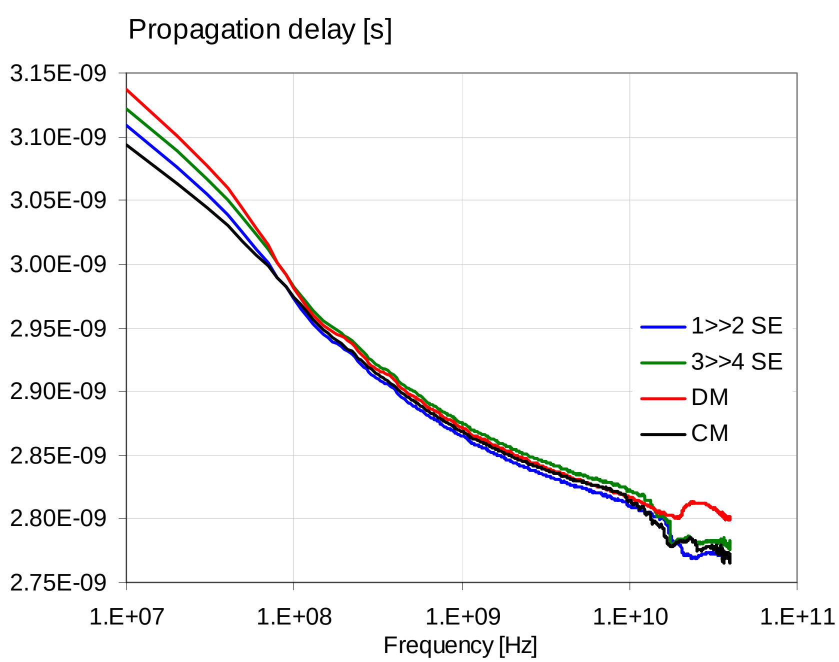
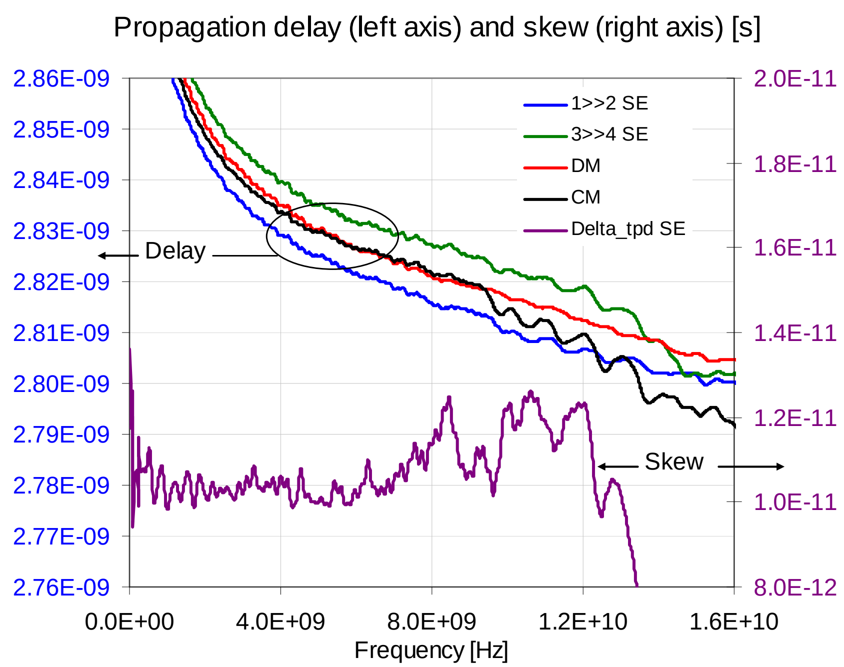
Delay, Skew







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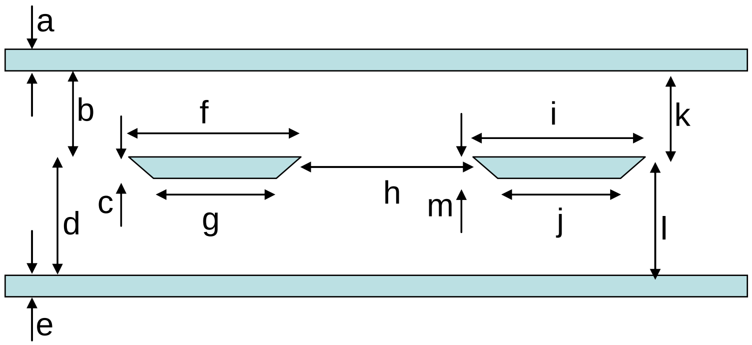
Cross Sections, Dimensions

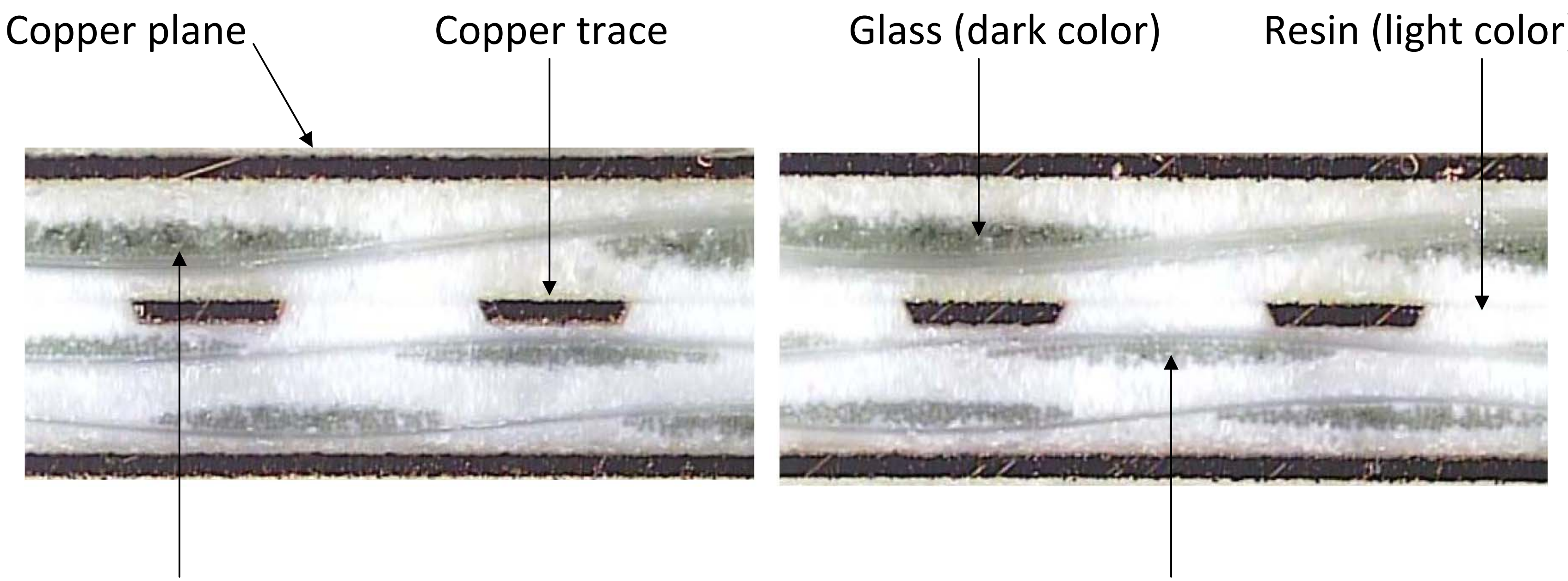


Percent deviation from average:

Location:	b	d	c	f	g	k	l	m	i	j
1	2.43	5.45	-2.10	2.07	-1.17	3.10	4.00	-0.89	0.86	0.00
2	2.43	1.93	-2.10	-0.46	2.74	-0.18	2.13	-0.89	0.86	0.79
3	-0.83	-4.42	8.41	-0.46	-2.22	-0.18	-5.82	3.56	-0.06	-1.05
4	2.43	0.99	-2.10	1.15	1.69	3.10	0.49	-0.89	-0.06	0.79
5	-0.83	-2.54	-2.10	-2.30	-2.22	-2.56	-2.31	-0.89	-0.75	0.00
6	-2.01	-2.54	8.41	2.07	1.69	-1.37	-3.01	3.56	4.32	0.79
7	-4.38	-1.83	-2.10	-2.30	-3.26	-2.56	-1.38	-0.89	-2.59	-2.11
8	-2.01	-2.54	-2.10	0.23	2.74	-0.18	-0.44	-0.89	-2.59	0.79
9	2.43	0.05	-2.10	-1.13	-1.35	-0.18	1.43	-0.89	-4.89	-1.16
10	0.36	5.45	-2.10	1.13	1.35	1.01	4.93	-0.89	4.89	1.16

Random!

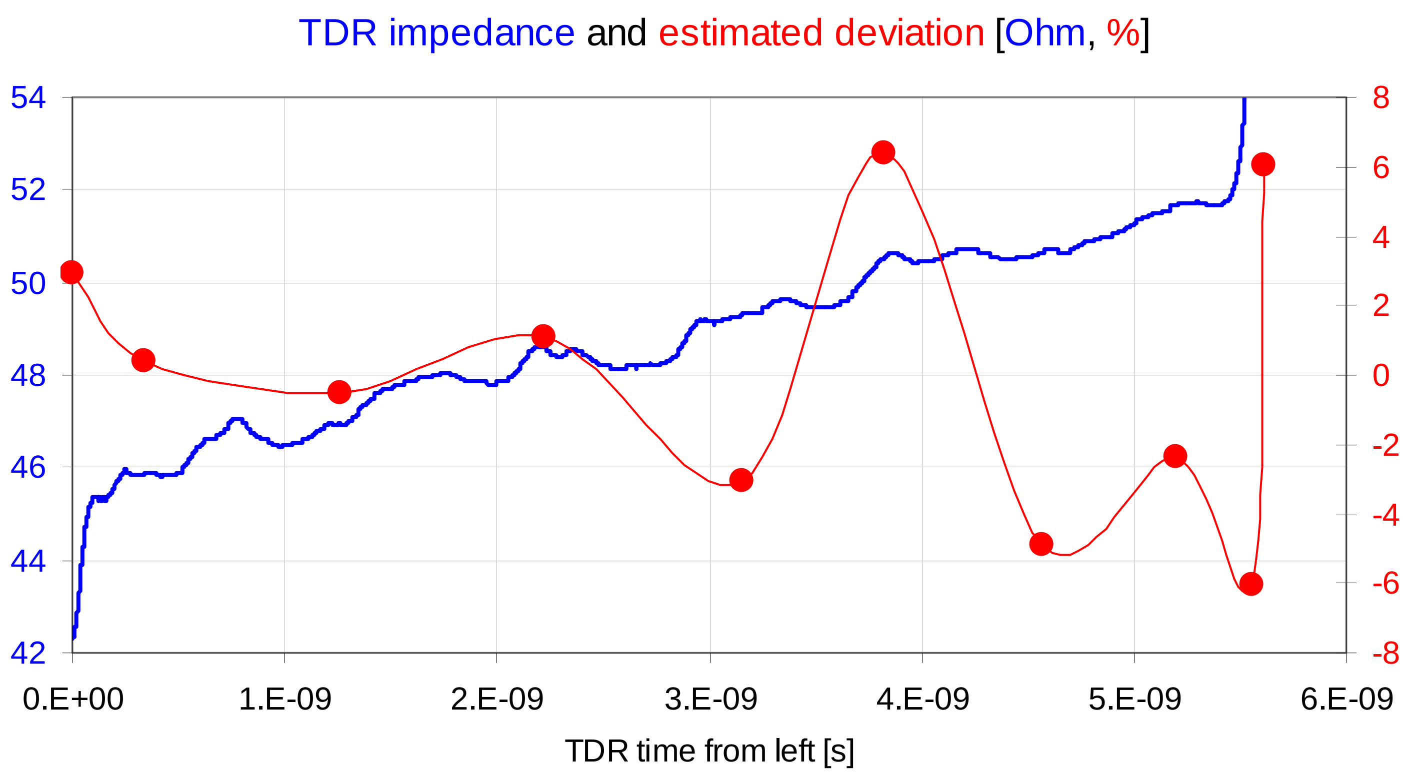
Cross Sections, Glass Weave



Higher capacitance due to glass bundle.   More coupling due to glass bundle.

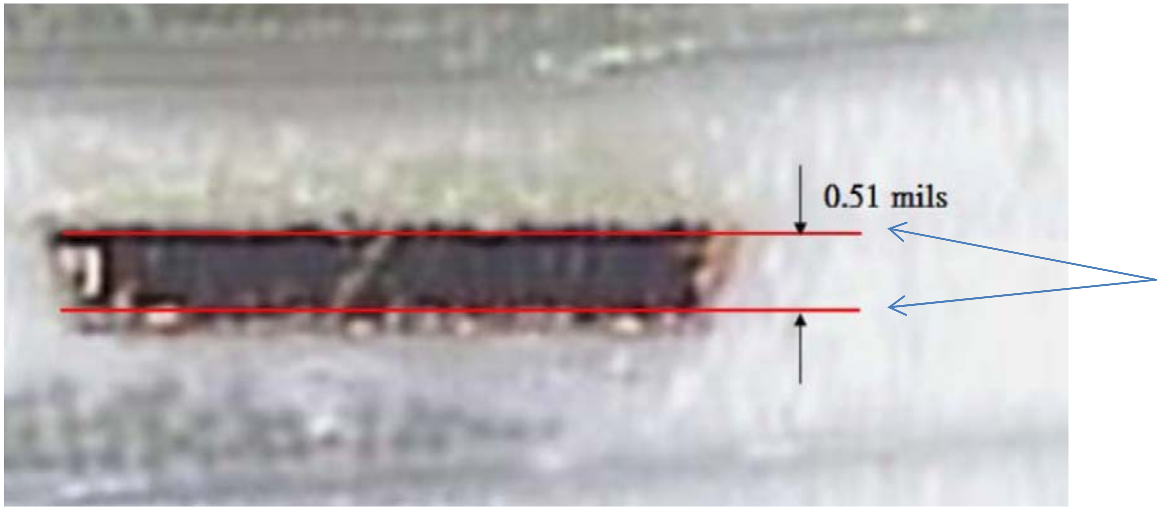
Same differential pair at two different locations.
Glass-weave effect changes local Dk.

Estimated Deviation



Little correlation!

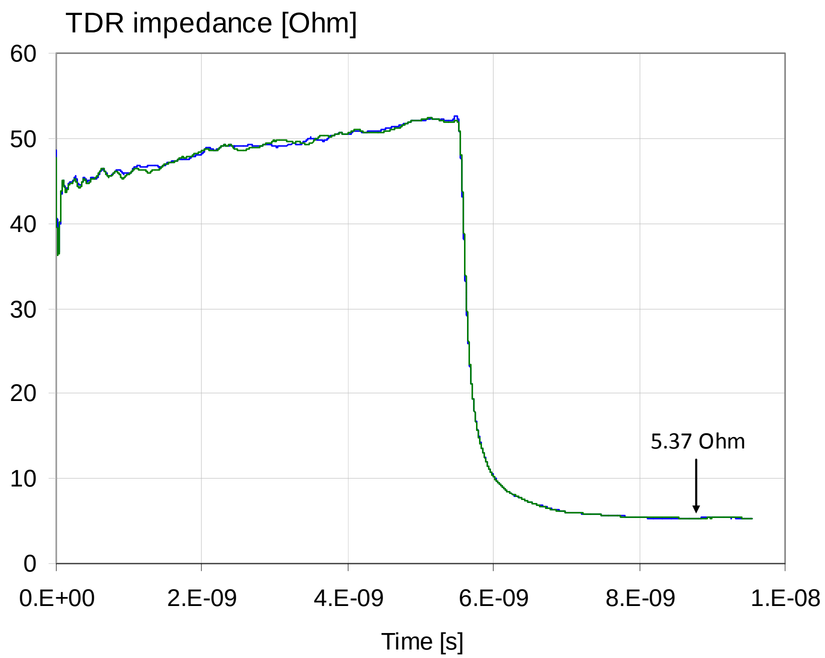
Recalculate DC Resistance

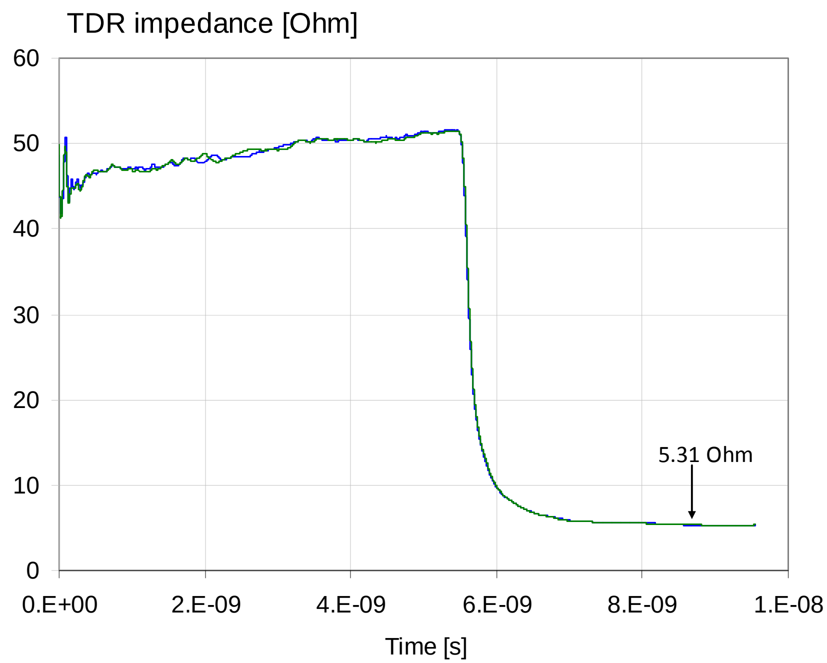


Measurement lines must be placed across minima.

Even at DC, surface roughness matters.
Current will not (fully) penetrate the peaks.
For DC resistance purposes, copper thickness must be measured between lines across minima.

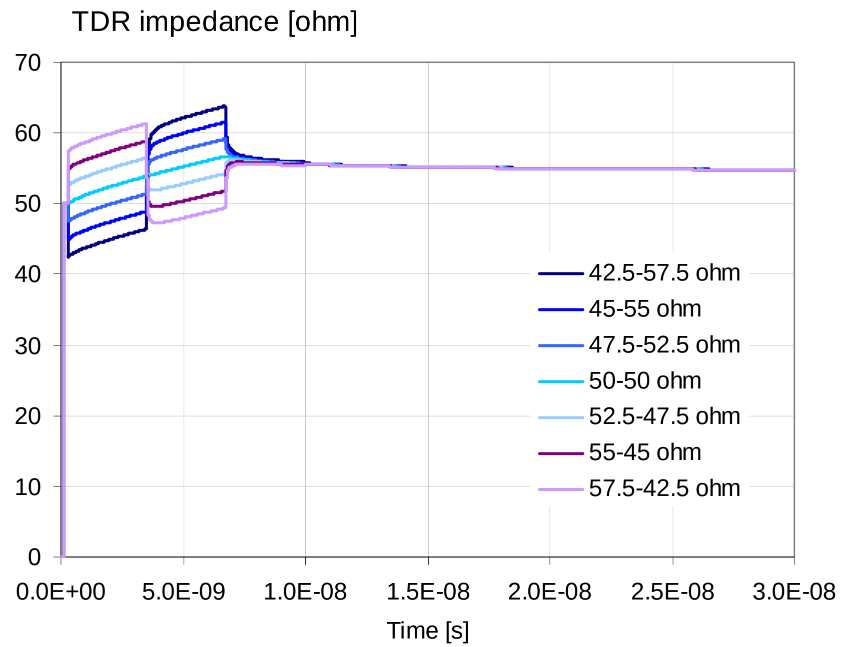
DC Resistance Measurements

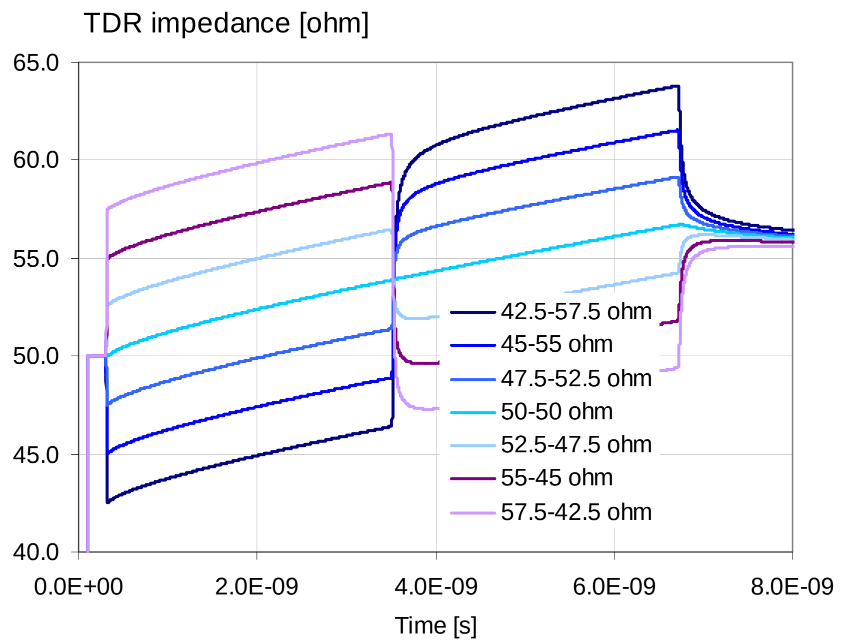




Reasonable correlation is achieved only with copper thickness measured between lines across minima.

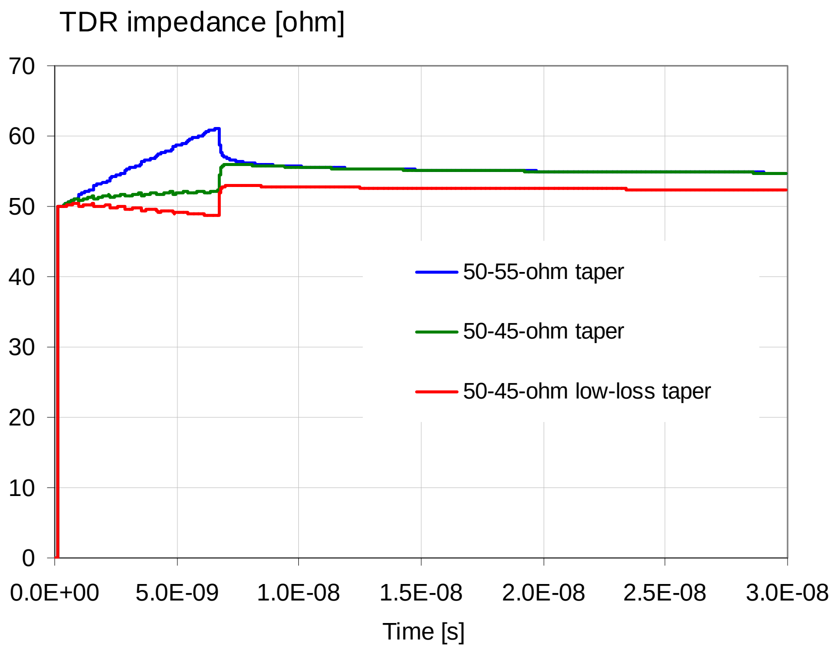
Cascaded Lines

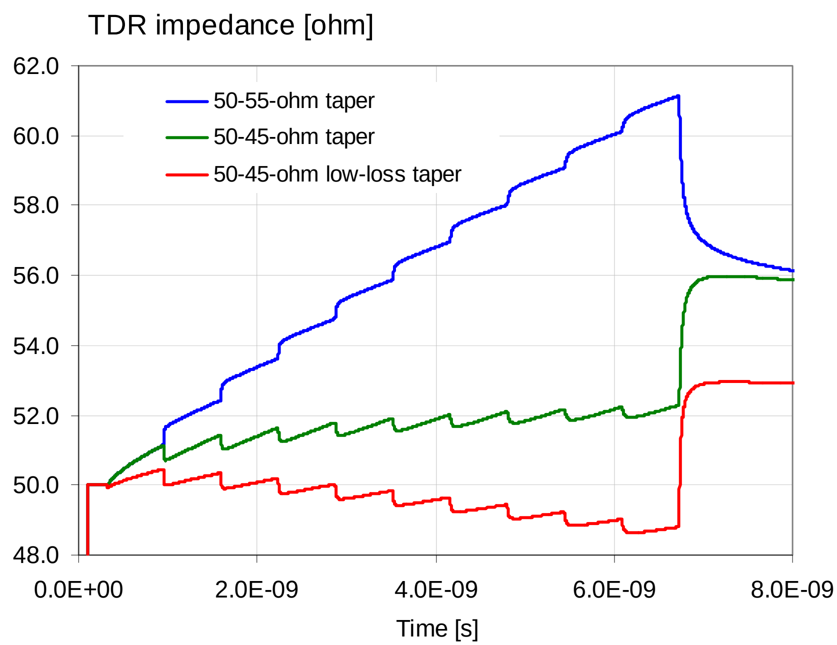




Each cascaded section follows its own trend.
The only interaction among sections is due to edge slow-down.

Tapered Lines





Even if specified as a uniform trace, its characteristic impedance could change or vary within the specified limits.
Simulations with ten cascaded uniform lines.
The characteristic impedance values step up or step down.

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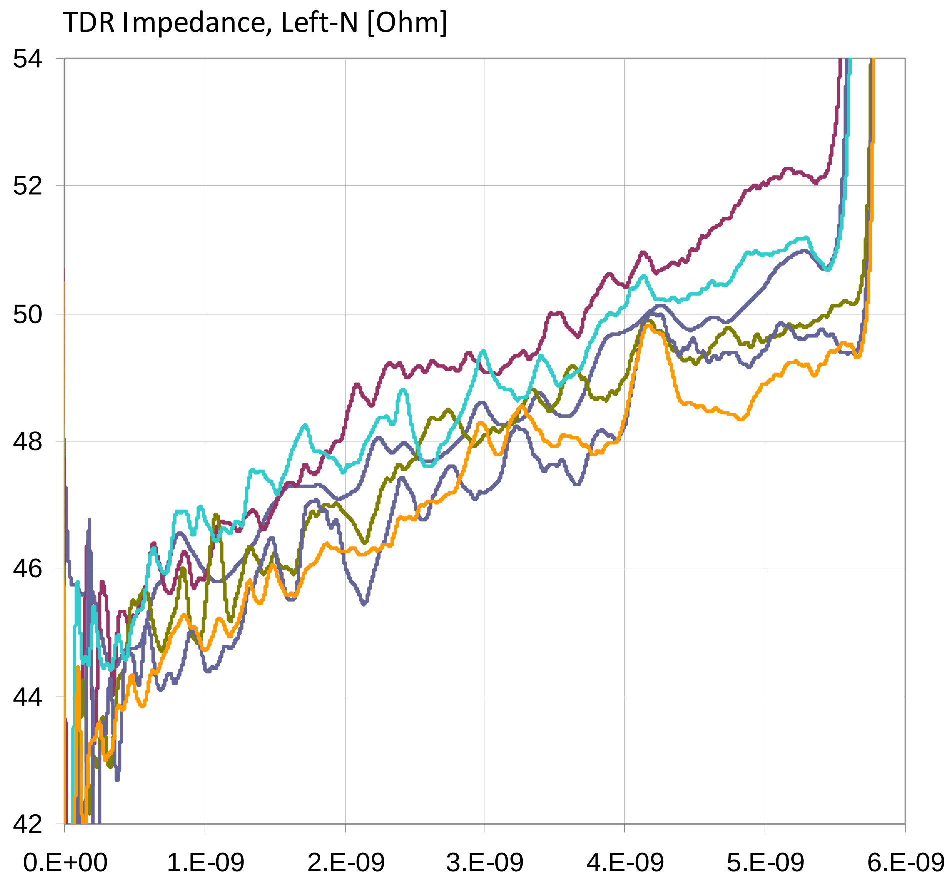
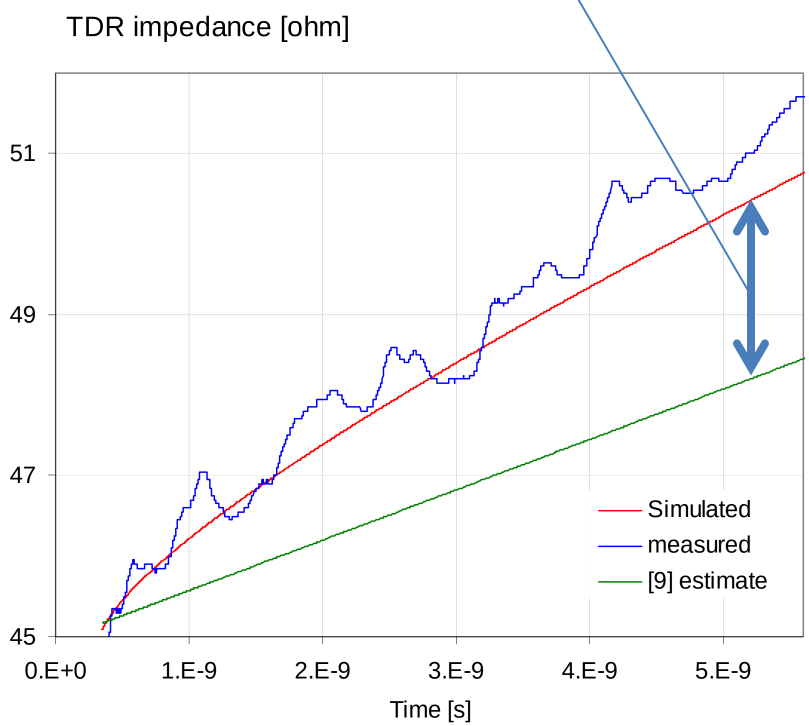
Approximating the Slope



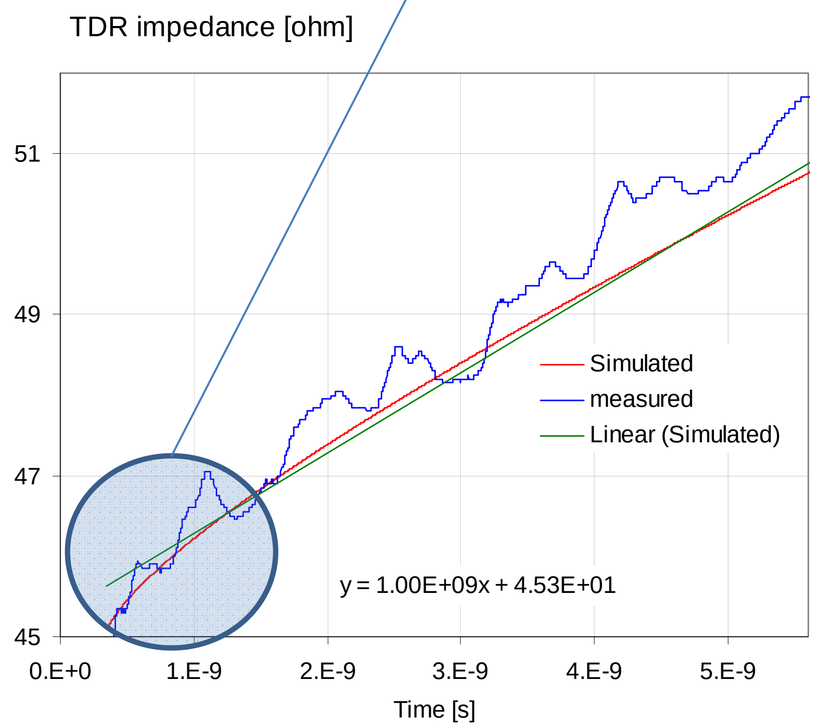
- If the interconnect is uniform and its parameters are known, we know the TDR response.
- In long resistive traces the response has a positive tilt.
- The positive tilt can be approximated and subtracted from the measured response.

Linear Approximations

A linear estimate ignores the impedance increase due to AC resistance.

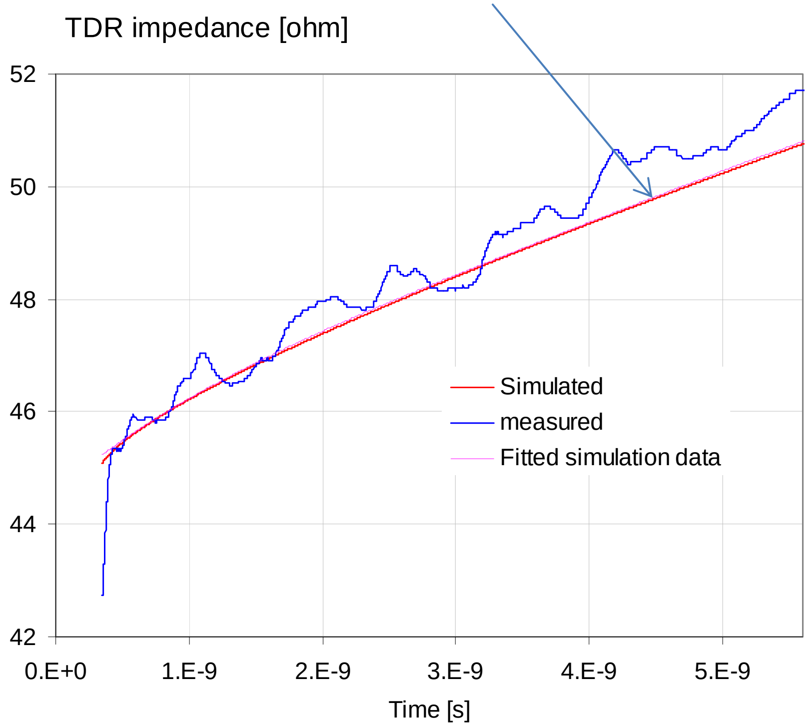


A linear estimate of the actual response still has large errors close to the excitation edge.

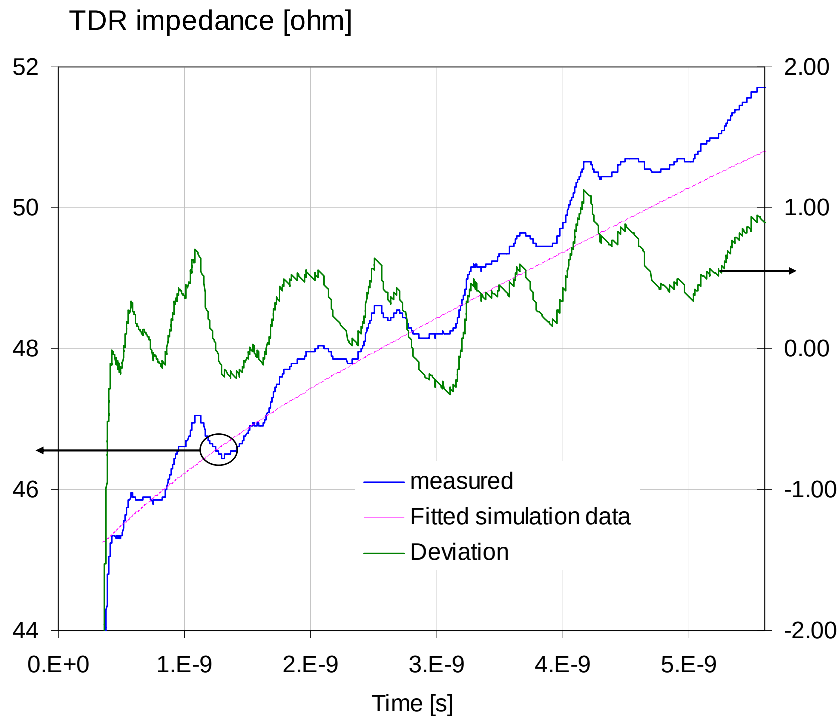


Polynomial Approximations

A sixth-order polynomial captures the time-dependent impedance with sufficient accuracy.
Lines are undistinguishable.



Subtracting the estimated response from the measured TDR curve.
Trace is within +1.5 -0.5% of nominal.

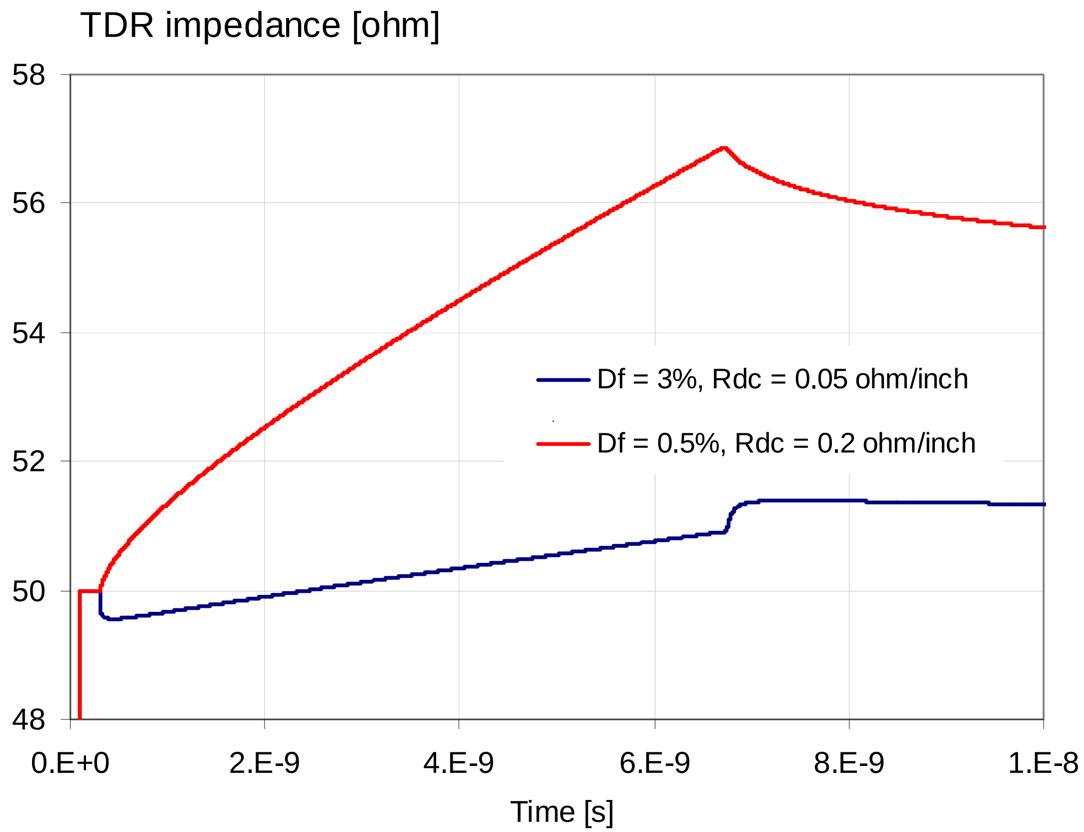


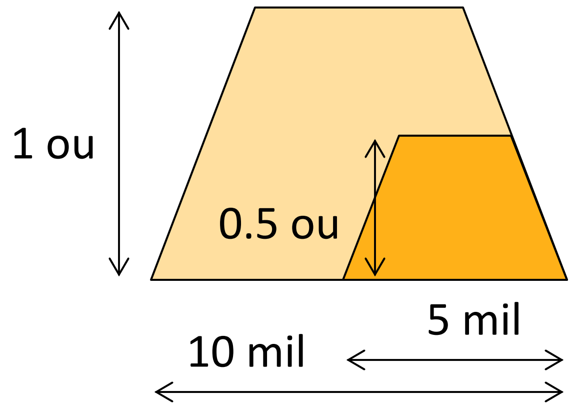
Conclusions

- Long and/or resistive traces have significant difference between actual and apparent impedance.
- Apparent impedance is increased with increasing DC and AC resistances.
- AC resistance creates overshoot beyond the DC resistance value.
- Apparent impedance is decreased by dielectric loss.
- DC resistance is increased by surface roughness.
- Thin 20-40" traces may have apparent impedances go outside the tolerance window.
- In PCB manufacturing, resistive panel coupons need compensation.
- In full-board validations, TDR results need compensation.
- A sixth-order polynomial is suggested to compensate for losses.

Closing Remarks

- TDR has been used for decades to check trace impedance.
- Why was this not a problem earlier?





Because we used lossier dielectrics, wider and heavier traces and maybe shorter etches…

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THANK YOU!

Any Questions?