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Panel 11-WE7: System-Level Power Integrity: Tools Providers and Tool Users Engage

Bruce Archambeault, IBM
Brad Brim, Cadence (panel organizer)
Patric Carrier, Mentor Graphics
Istvan Novak, Oracle (panel moderator)
Steven Pytel, Ansys
Stephen Scearce, Cisco Systems

Abstract

On this panel, EDA tool providers join OEMs responsible for system design and validation. Tool providers discuss their vision for Power Integrity in the design implementation and analysis flow. System Integrators will share their view of what is working well today and where EDA needs to go to meet future needs.

Author(s) Biography

Dr. Bruce Archambeault is an IBM Distinguished Engineer in Research Triangle Park, North Carolina. He received his BSEE degree from the University of New Hampshire in 1977 and his MSEE degree from Northeastern University in 1981. He received his PhD from the University of New Hampshire in 1997. His doctoral research was in the area of computational electromagnetics applied to real-world EMC problems. Dr. Archambeault has authored or co-authored a number of papers in computational electromagnetics, mostly applied to real-world EMC applications. He is a member of the Board of Directors for the IEEE EMC Society and a past Board of Directors member for the Applied Computational Electromagnetics Society (ACES). He currently serves as the chair for the Technical Activities Committee and Vice President for conferences of the EMC Society. He has served as a past IEEE/EMCS Distinguished Lecturer and Associate Editor for the IEEE Transactions on Electromagnetic Compatibility. He is the author of PCB Design for Real-World EMI Control and the lead author of EMI/EMC Computational Modeling Handbook.

Brad Brim is a Product Engineer at Cadence Design Systems with over 20 years of experience in EDA tools for code/algorithm development, marketing, applications engineering, and product management. His present responsibilities are with package and board SI/PI extraction tools and chip/package/board system-level applications. His past experiences were in the area of RF/microwave/antenna modeling for components, circuits and systems with EM and circuit analyses.

Patrick Carrier has over 12 years of experience in the fields of signal integrity, power integrity, thermal analysis and EMI/EMC for PCB designs. He is currently a Product Marketing Manager at Mentor Graphics for the Hyperlynx analysis tools.

Istvan Novak is a Senior Principle Engineer at Oracle. Besides signal integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models and develops measurement techniques for power distribution. Istvan has over 20 years of experience with high-speed digital, RF, and analog circuit and system design. He is a Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies.

Dr. Steven Pytel is Signal Integrity Product Manager for ANSYS. He received a Master's and PhD in Signal Integrity from the University of South Carolina and a BS from Northern Illinois University. Steve worked at Intel as Senior Signal Integrity and Hardware Design Engineer designing Blade, Telecom, and Enterprise servers. His research addressed transmission line frequency dependent dielectric losses and copper surface roughness. He has over 20 publications plus invited papers and presentations. He has written an invited chapter on signal integrity simulation entitled "Maxwell's Equations: The Foundations of Signal Integrity", by Paul G. Huray.

Stephen Scearce is the manager of the Systems and Silicon Engineering High Speed Design team at Cisco Systems Inc. Stephen has worked for Cisco for more than 10 years in the Signal integrity and EMC field. Prior to working at Cisco, Stephen worked for NASA LaRC as a research engineer in the Electromagnetic Research Branch HIRF team. Stephen has 3 US patents and 2 pending patents. He received his BSET and MSEE from Old Dominion University, Norfolk VA.

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We live in the Time Domain so Why Analyze in the Frequency Domain?

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Bruce Archambeault, PhD
IEEE Fellow, MST Adjunct Professor
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- Most PDN analysis is performed with frequency domain impedance analysis
  - Magnitude only – only half the story!
- Frequency domain analysis
  - Steady state!
    - Charge can take hours/days/weeks to arrive!
    - Unrealistic

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- Time Domain Analysis
  - IC needs charge when it needs it! --- not later!
  - Too slow charge delivery increases SI jitter, slows rise time, increases PDN noise
- Charge arrives from local storage
  - Very rarely does change travel directly from capacitors to IC – takes too much time
  - Similar to fish ladders in rivers
    - IC draws from package caps, which draw from planes, which draw from local discrete capacitors, etc

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- Must include inductance
  - More than ESL → connection inductance between discrete capacitors and planes dominate
  - Distance from discrete capacitors to IC local planes area is another 'inductance'
  - Connection inductance between IC and planes

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- Summary
  - Frequency domain analysis is easy…and wrong
  - Time domain analysis is harder, but right!
  - Inductance dominates charge delivery time!

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Power Integrity Challenges and Solutions

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Brad Brim, Cadence Design Systems

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Power Integrity is a Team Effort

More than just an expert PI/SI analyst contributes to the Power Integrity of an electronic product.

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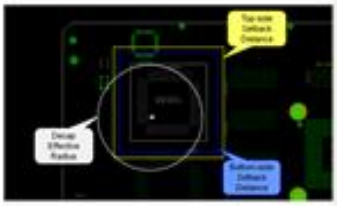
Roles and Responsibilities

- Design Engineer
  - Performs cost, form factor and performance studies for feasibility of the design
  - Applies vendor guidelines to define design intent and system schematic
- Layout Designer
  - Physically implements design intent
  - Controls placement, routing and ECO process
  - Driven by design constraints and intuitively actionable information
- Analysis Expert
  - Provides guidance and design rules
  - Provides analysis support from pre-layout through post-layout
  - Performs sign-off analysis post-layout for PI/SI/EMC
- EMC Consultant
  - Provides guidance and design review
  - Performs sign-off measurement, may perform EMC analysis

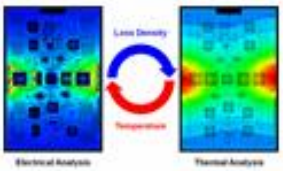
OEM Needs

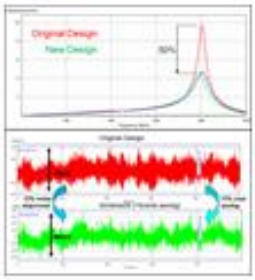
- Analysis
  - breadth of accuracy, efficient and high capacity, accessibility, easy setup and re-use
  - frequency *and* time domain circuit/system simulation
- Analysis results available when most actionable
- PI constraints for components
  - DC, AC and thermal for both VRM and switching devices
  - frequency and time domain guidance/specs
- Power-aware analysis models
  - CPM models for chips
  - operating conditions to enable time domain analysis
- Guidance for decap physical implementation
  - dynamic placement guidance (constraints/DRC)
- Efficient communication amongst team members
  - information defined by one team member accessible by all
  - common and re-usable analysis models/libraries
  - ECO process automation



EDA Solutions

- Many stand-alone analysis tools are available
  - spreadsheet based decap selection
  - DC IR drop and current constraint analysis
  - thermal simulation and electro-thermal cosimulation
  - AC "hybrid", 2.5D and 3D solvers
  - on-die PDN extraction and macromodel generation
  - FD and TD circuit/system simulation
  - decap "optimization"
  - EMC capable solvers
  - physical DRCs
- Layout tools
  - more PI constraints and analysis results are becoming available
  - physical DRCs
- Integrated solutions are becoming available to serve the entire PI design team
  - enables from schematic to post-production ECO, not just analysis





Questions to Seed Discussion

- What are the bottlenecks for general PI design?
- Are there specific roadblocks to system-level PI design?
- Which PI team members are most/least served today?
- What more is needed from vendors to define design intent?
- Are adequate component models available to support PI analyses?
- What are the perceived analysis shortcomings?
- Would more approximate analysis (e.g. "checking") for PI be helpful?
- Is EMC a PI concern?
- Is cost of PI-driven design content a concern?
- To how many PI teams is thermal a concern?
- Are component tolerances important to PI?
- Are multi-sourced components a PI concern?
- Are manufacturing tolerances a PI concern?
- Is PI revisited or set aside once SI is pursued?

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PDN Simulations: Goals and Requirements

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Patrick Carrier, Mentor Graphics

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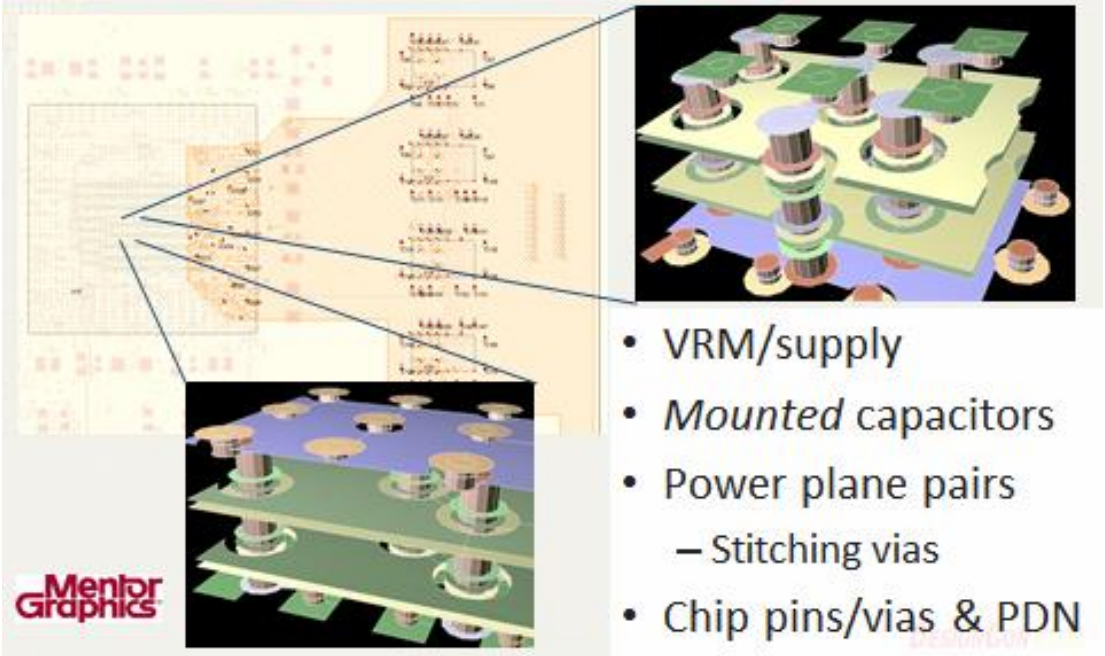
PCB PDN at a glance



- VRM/supply
- *Mounted* capacitors
- Power plane pairs
  - Stitching vias
- Chip pins/vias & PDN

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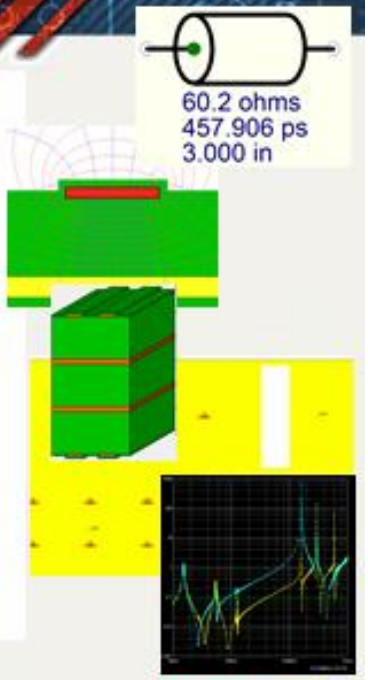
First steps

- In SI analysis, we first calculate the trace characteristic impedance
  - Use trace dimensions, dielectric properties, and reference planes to determine
- In PI analysis, we first calculate the PDN impedance
  - Must include mounted parasitics of capacitors
  - Connection to pins through plane pairs/stitching vias
  - Varies at different board locations



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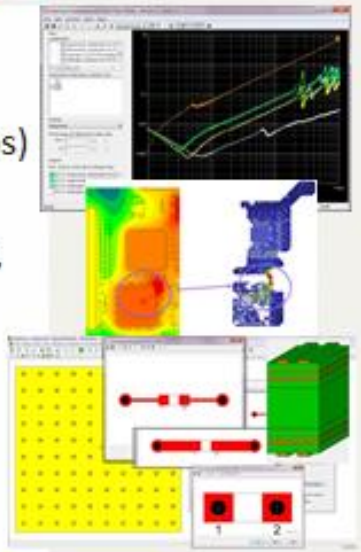
How do we use the info?

- Predict performance
  - PDN impedance often sufficient
  - May need to apply stimuli (more steps)
- Make design tradeoffs
  - Determine value, number, placement, mounting of caps
  - Adjust stackup, plane shapes
  - Analyze PI-specific technology
    - Cplanes, X2Y, reverse geometry, etc.
  - Add more metal (don't forget DC!)
    - Wider/thicker planes, more stitching



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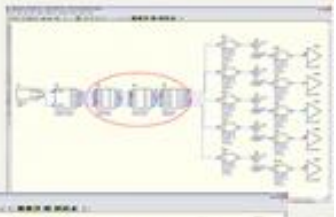
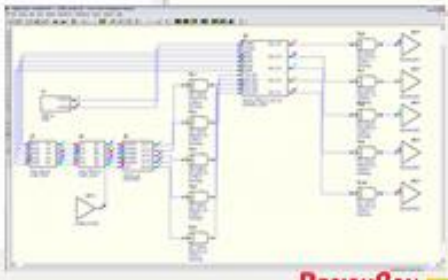
Next steps

- Apply stimuli
  - In SI, usually a pulse train and a buffer model (IBIS, SPICE, AMS)
  - In PI, could be a number of items
    - SPICE model(s)
    - IBIS model(s) with ISSO and/or Composite Current keywords
    - Triangle pulse, ramp, PWL function
- Look at voltages
  - Signal and power
  - Coupled noise voltage
    - Through PDN (planes, vias)
  - Voltage droop (from SSN)





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Why PDN Simulations Are So Difficult

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Istvan Novak, Oracle

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Why PDN Design is *so* Difficult?

- PDN is a system-wide network, present everywhere
- PDN has multiple, intertwined roles
- Signal integrity is a 1D problem
- Signal integrity deals with known excitation (signals)
- Power integrity is a 2D (or 2.5D) problem
- PDN deals with less known excitation (noise)
- Metric may be tricky to define

What is the Metric Anyway?

Set of requirements:

- Worst-case peak-to-peak transient noise, or RMS noise
- Resonance-free construction
- Low sensitivity
- Uniform stress distribution
- Portability
- Competitive cost
- Size (area, component height)

Peak-to-Peak *vs.* RMS Noise

Instantaneous peak-to-peak transient noise should be the metric if the load can not recover from a glitch

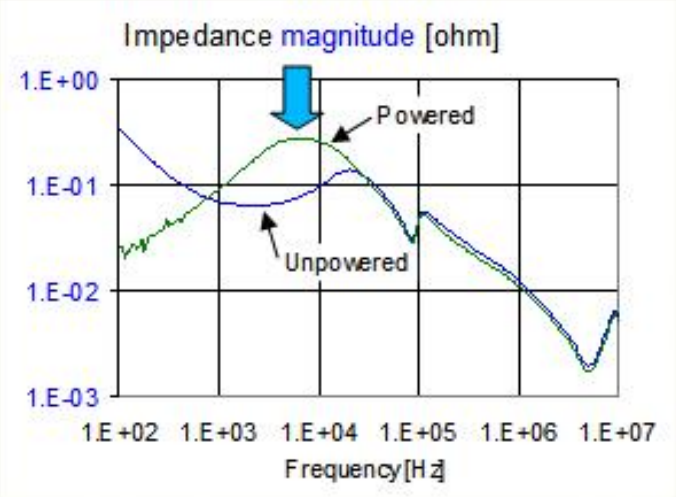
- CPU core, FPGA core, ASIC core
- any logic in a critical path

RMS noise is a better metric for narrow-band noise receiver

- Narrow-band analog subsystem
- Oscillator circuits
- PLL circuits

Active-Passive Component Interaction

DC-DC converter active loop simulation is necessary



PDN Trends

- Increasing number of independent supply rails (less room for planes and PDN components)
- Increasing system density (noise sources and sensitive circuits are closer). Note: scaling.
- Higher efficiency (lower losses create more high-frequency noise)
- Size and cost constraints (resonances may not be sufficiently suppressed)

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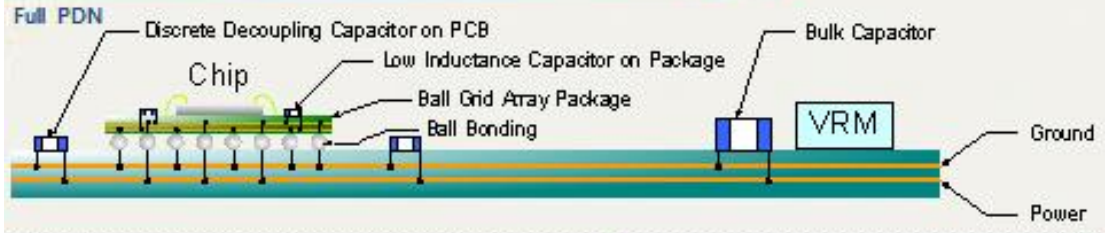
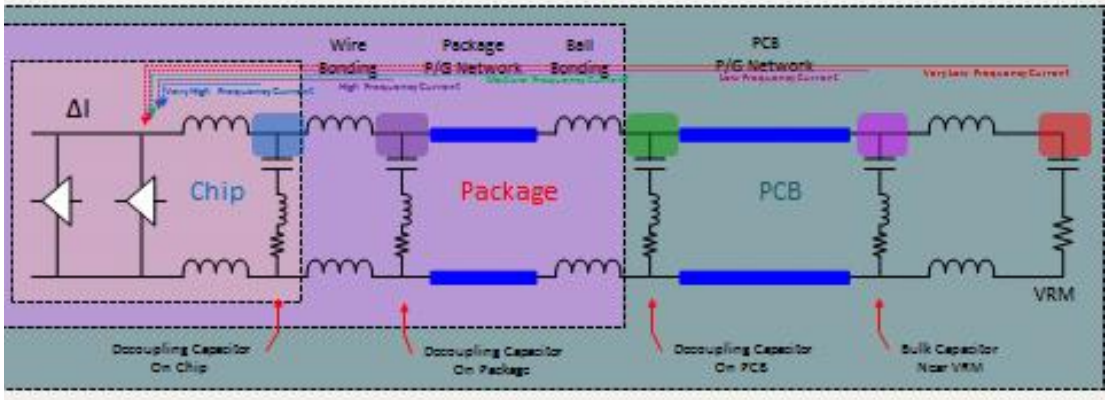
Components of PDN



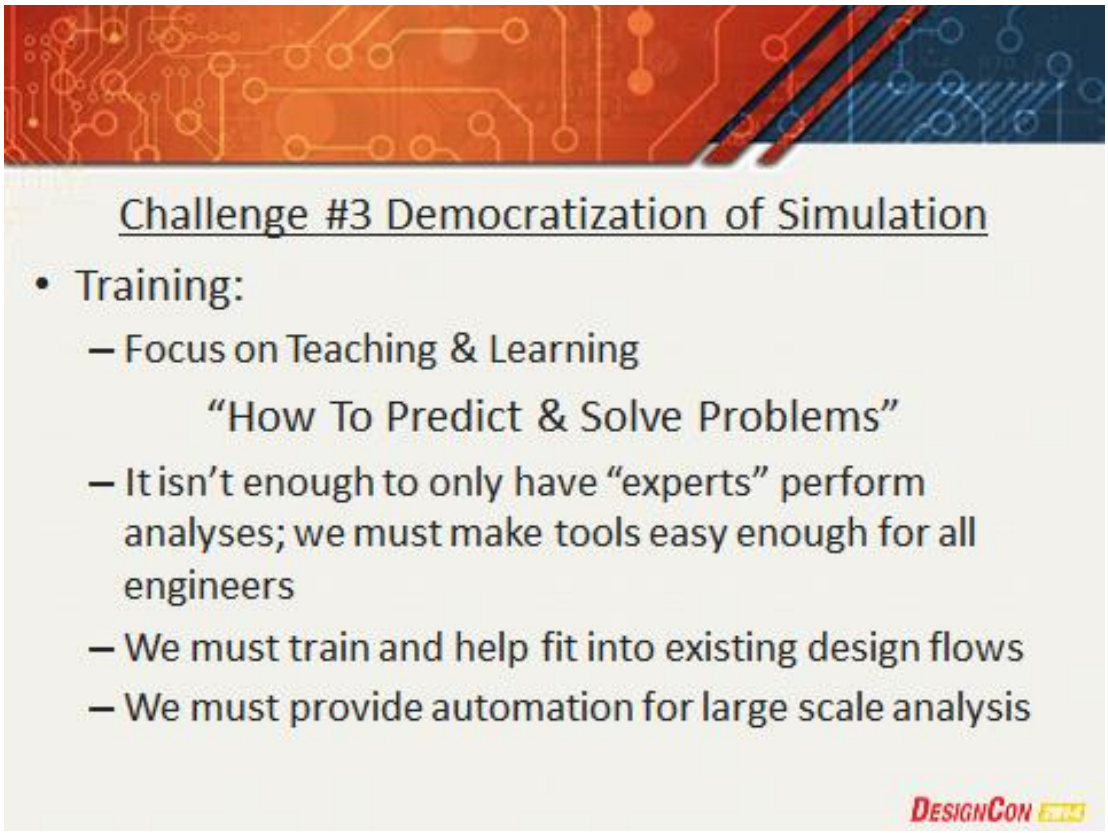


Challenges

1. System level "Charge"
   - Is it good enough to only solve VRM and PCB?
   - Must we include PKG + PCB?
   - Or must we include Chip + PKG + PCB + Connector + …
     - System Level Solutions
   - 3DIC and Interposer Design
     - GIT 2013
2. Frequency Domain vs. Time Domain
   - Memory simulations and capacity
3. Democratization of Simulation
   - How to use the tools

Challenge #1: How much Charge and Where does it Go?
Challenge#2: Frequency Domain or Time Domain?

- Key area for Electronic Design
  - Inclusion of Chip PDN into PKG and PCB
    - Apache CPM with Dynamic vs. Static
- Simulation Technologies:
  - PI Product Offerings:
    - DC Power Product
    - PI Focused Product (AC, DC, Optimization, & Cavity Resonance)
  - Technologies that enable 3D FEM PI Studies
    - Meshing Technologies
      - Much greater robustness
      - Require speed up
      - Require capacity improvements
  - Accurate Capacitor models
    - Causality, Passivity, BW, Temperature, DC Biasing, and easy inclusion into simulation
  - Combined Thermal offerings: AC and DC
    - 3DIC and Interposers
  - Mechanical stress and warranty (reliability issues)
    - Warpage & delamination
  - Capacity into Time Domain for Memory Solutions
    - 16 ports or 256: DQ, DQS, CMD/ADD, CLK, …


Challenge #3 Democratization of Simulation
• Training:
– Focus on Teaching & Learning
"How To Predict & Solve Problems"
– It isn't enough to only have "experts" perform analyses; we must make tools easy enough for all engineers
– We must train and help fit into existing design flows
– We must provide automation for large scale analysis
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Challenges for Power Integrity

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Stephen Scearce, Cisco Systems Inc.

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Cisco ENG PE High Speed Design Team
28 – Engineers/Contractors

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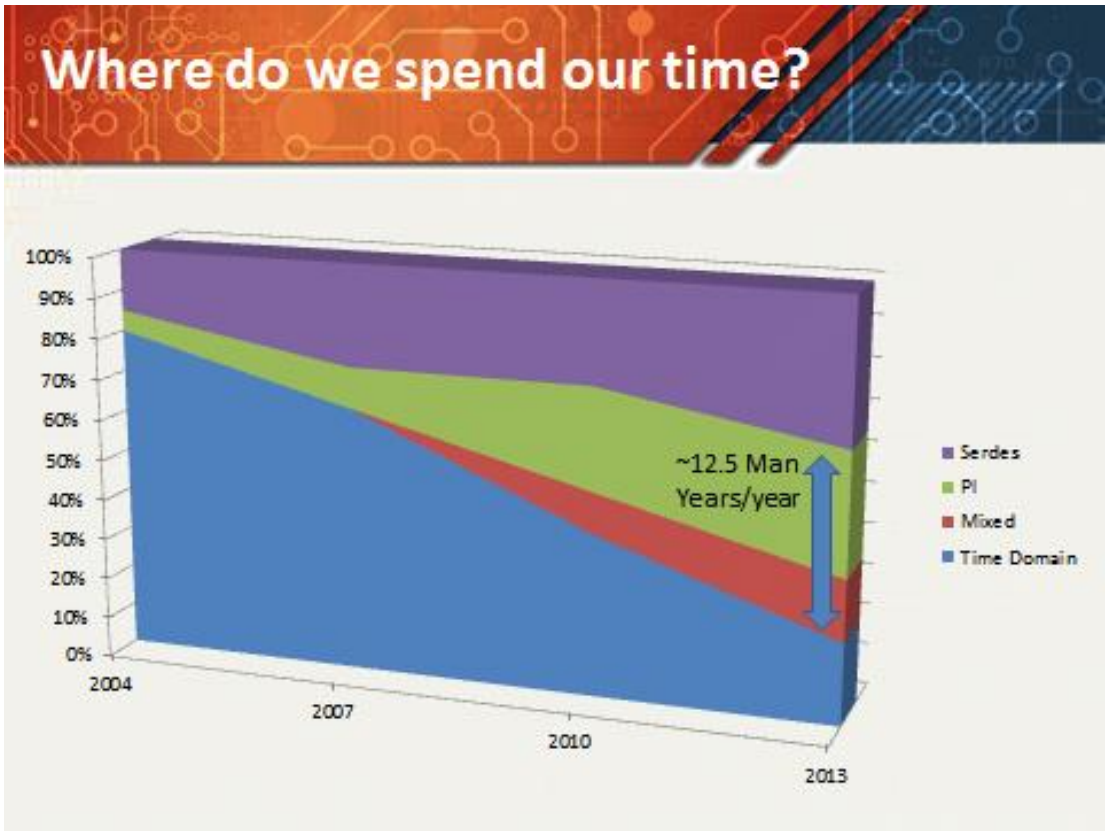
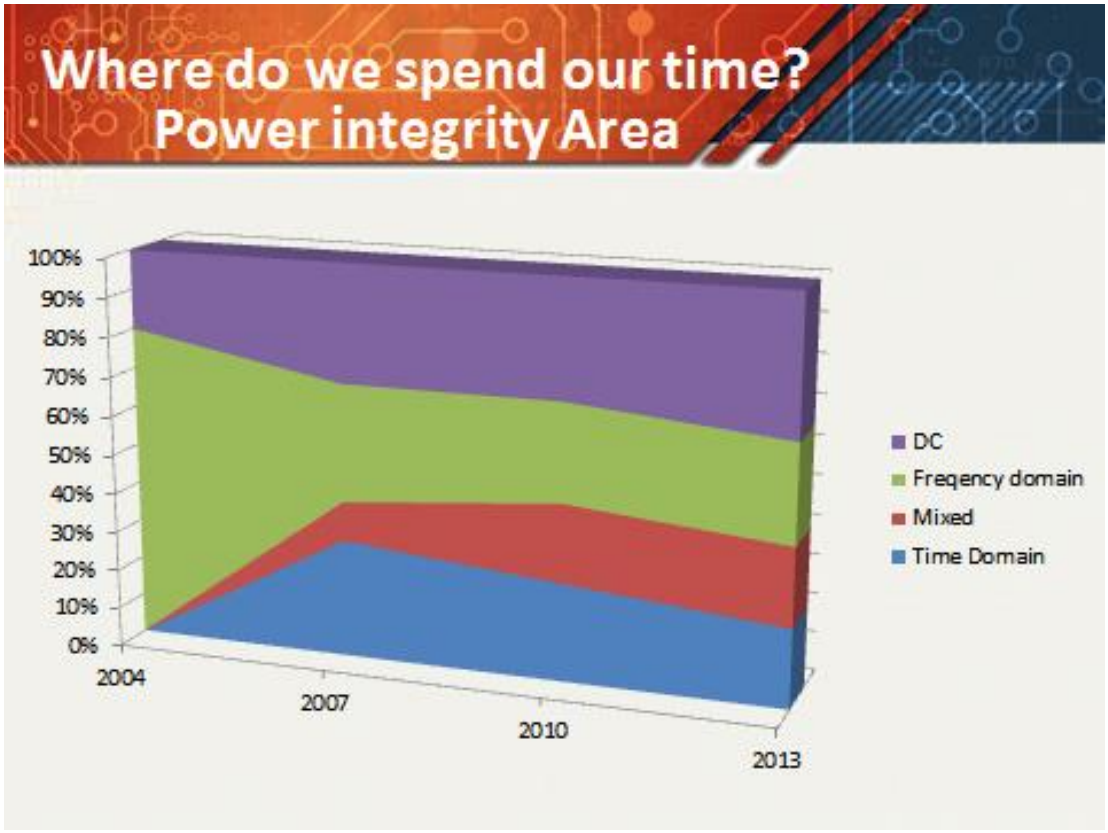

Where do we spend our time?
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%
2004
2007
2010
2013
~12.5 Man Years/year
Serdes
PI
Mixed
Time Domain


Where do we spend our time?
Power integrity Area
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%
2004
2007
2010
2013
DC
Freqency domain
Mixed
Time Domain

Challenges for Power Integrity

- DC/IR/Thermal Simulation
  - Solution speed for larger designs
  - Thermal integration significantly slower
  - Improved thermal tool integration
  - Re-analysis for verification
  - System level setup challenges Connectors, Multi-board
  - 80-100 Amps with 0.9V or less(Copper weight required?)
  - Finer Pitch BGAs (0.7mm,0.65mm, 0.5mm…)
  - 10+ power domains

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Challenges for Power Integrity

- AC/Frequency Domain
  - Complex models needed to relate more complete broadband behavior vs RLC
  - Voltage/Temp dependence
  - Inter power domain coupling
  - PCB cutoff 10-20 MHz
- Time Domain (Dips/sags/droop)
  - Speed/ Convergence issues with S-parameters
  - Current stimulus vector basic PWL or CPM
  - Multiple loads on the same rail
  - Behavioral DC-DC convertor model generation

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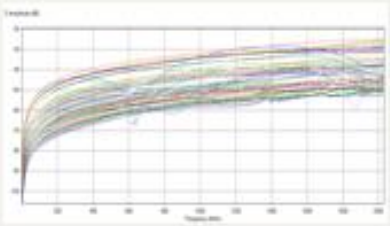
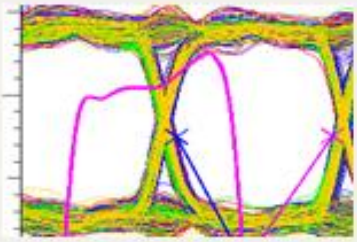
Challenges for Power Integrity





- Mixed analysis/Time Domain
  - Very large S-parameters
  - Simulation setup
  - Visualization
  - Root cause/Mitigation
  - Model availability (power aware)
  - Ensuring W/C analysis, excitation of system resonance
  - Multiple loads on the same rail

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Wish List future tool upgrades

- Design Constraints for Power Integrity
  - Component aware
  - Position of low/high freq caps WRT loads
  - DC resistance of components/ mounting flagged
- DRC feedback to Cad
- Cad tool integration and cross probing
- Pre/Post Route what if analysis
- Single tool for DC/AC/time/Frequency domain

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