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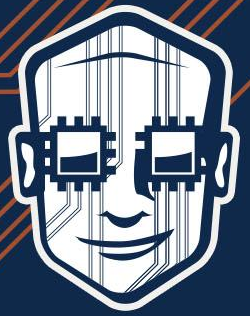

Jae Young Choi and Istvan Novak, Oracle Corporation

Simulating and Measuring Microohms in PDNs

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Speaker

Jae Young Choi

is a Senior Hardware Engineer at Oracle America Inc. He is engaged in the design and characterization of high-speed signal interconnects and power distribution networks for high-performance server systems. He received his Ph.D. in Electrical and Computer Engineering from the Georgia Institute of Technology.

Istvan Novak

is a Senior Principal Engineer at Oracle. Besides signal integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is a Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies.

Agenda

- Introduction
- DUT, Simulation & Measurement Setup
- DC Simulations/Measurements
- AC Simulations/Measurements
  - DUT-VRM & DUT-CAP: Shorts at DC-DC converters & capacitor pads
  - DUT with capacitors
- Conclusions

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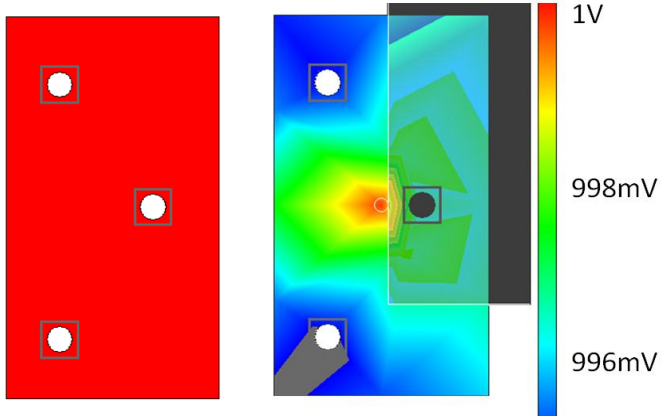
Introduction

- PDN designs get more challenging
  - Dropping supply voltages
  - More interactions between power supply rails
  - Stringent target impedance
  - PDN impedance requirement can be in the sub-milliohm range
- Low-frequency simulations pose resource and setup challenges
- Measurement of extremely low impedance is vulnerable to multiple factors
  - Ground loop error
  - Noise floor
  - Measurement discontinuities

Potential Issues with DC Drop Simulation

- Large pads for high-current devices
- Attached device may force equipotential surface
- In extreme case, if simulation does not enforce equipotential surface, voltage drop can be as high as 5mV across a typical DC-DC converter pad
- Assuming equipotential pad will result in slightly optimistic impedance

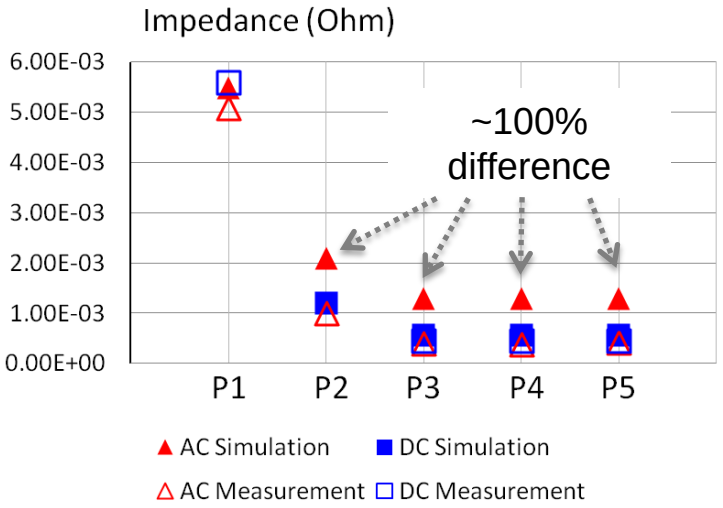
- Hundreds of sources/loads with equipotential device assumption may lead up to 50% miscalculation of DC drop in large dense memory arrays



Simulated current distribution with (left) and without (right) equipotential pad option

Potential Issue with AC Simulation

- Simulating at low frequencies
  - Inter-plane coupling effect (skin-depth)
  - Full-wave solutions are challenged at low frequencies
- AC simulations may show poor correlation for very low impedances
- Can be improved by fitting to DC simulation result

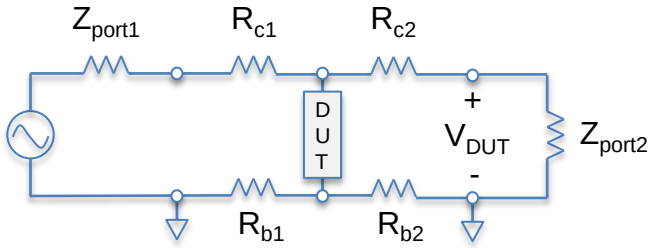


AC data are at 100 Hz
(DUT impedance is flat from DC up to 10 kHz)

Potential Issues with Measurement

- Measurement method
  - Network analyzer
- 1-port vs. 2-port measurement
  - Error: $Z_{connection}/Z_{DUT} >> Z_{connection}/Z_{VNA}$
  - Receive-only port provides much lower noise floor
- Ground loop error caused by test cable shield resistance
  - Finite resistance of the cable shield creates a common-mode error

- Solutions:
  - Increase shield inductance with large toroid core
  - Differential amplifier



$$R_{error}=R_{b1}\|R_{b2}$$

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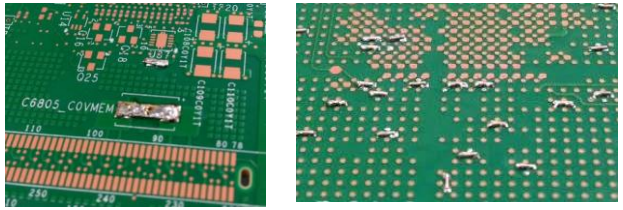
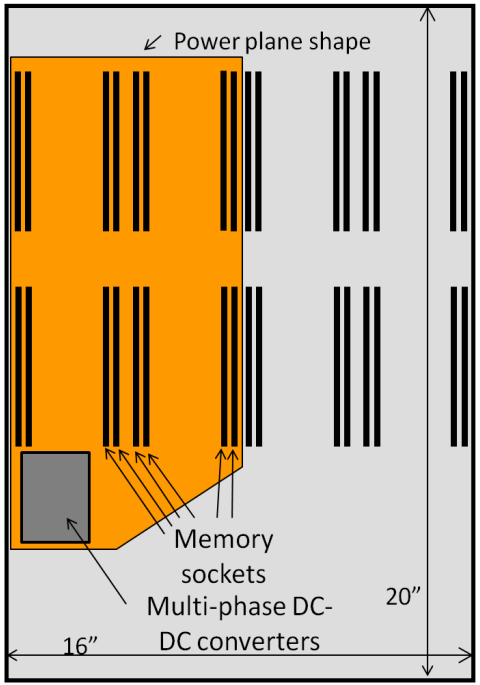
DUT with Low Impedance

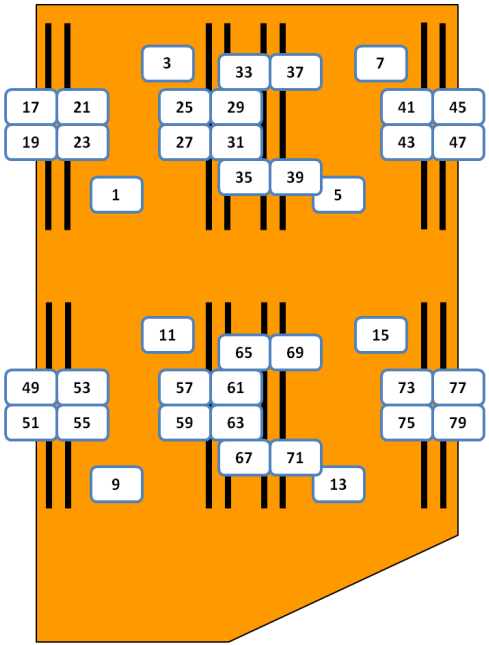
- Large bare PCB with 4 power layers
- 80 ports on 8 memory controllers and 16 DIMM sockets
- Port(N) and Port(N+1) are in close proximity
  - Hence, Z(N,N+1)≈Z(N,N)≈ Z(N+1,N+1)
- DUT-CAP: shorted all capacitor pads (DC-DC converter pads open)
- DUT-VRM: shorted DC-DC converter pads (capacitor pads open)



Shorted capacitor pads



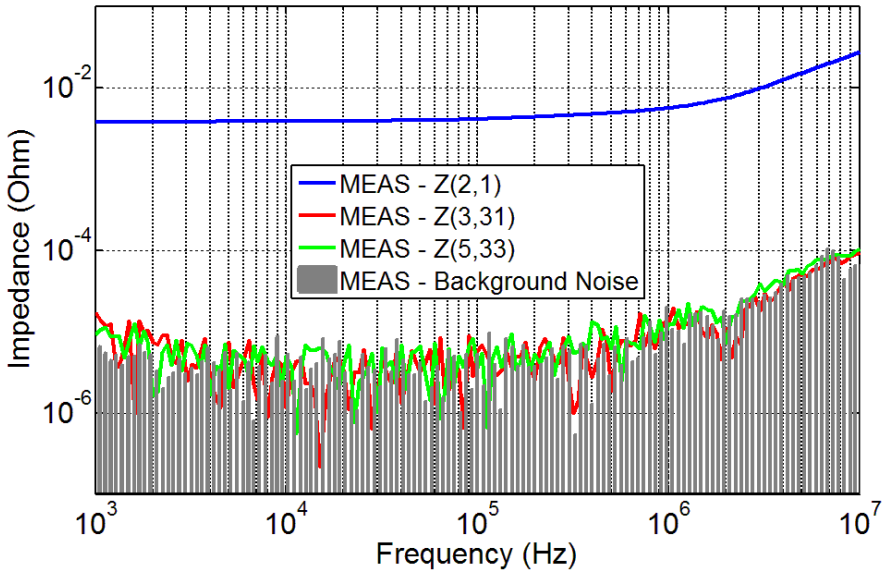
Approximate dimensions and placements of memory controllers and DIMM sockets



Port numbering definition

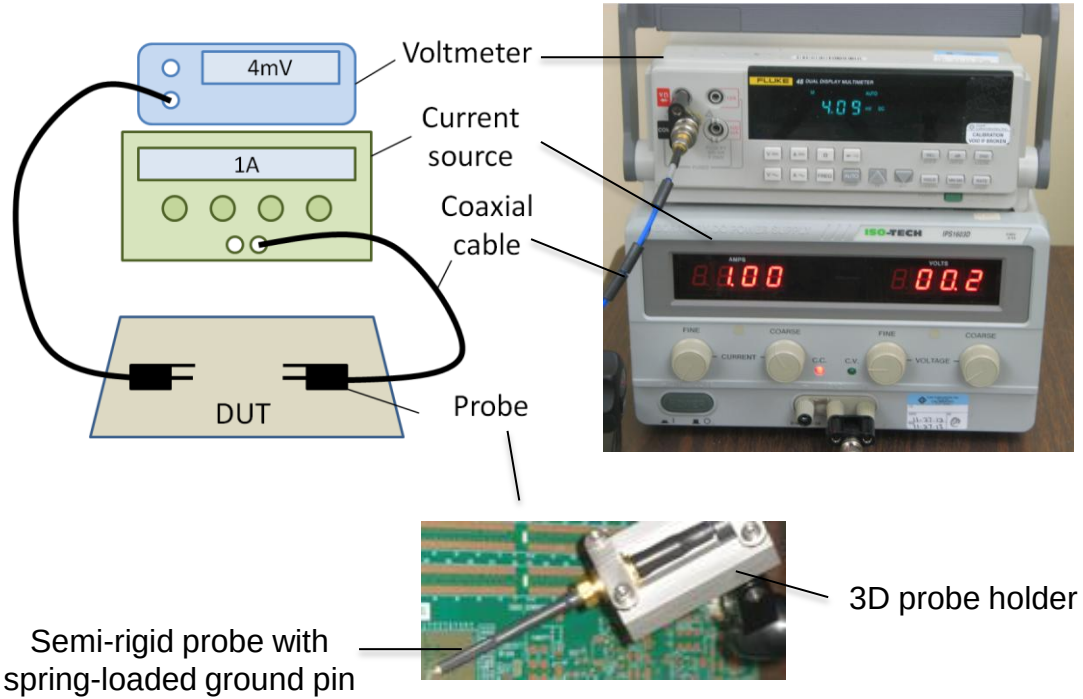
Measurement Noise Floor

- Noise floor is obtained by measuring on the opposite sides of a solid metal sheet using the same measurement setup, cables, and probes
- Some very low measured transfer impedances are masked by the measurement noise floor
- With the given setup, below 1 MHz, the noise floor is around 10 microohms.



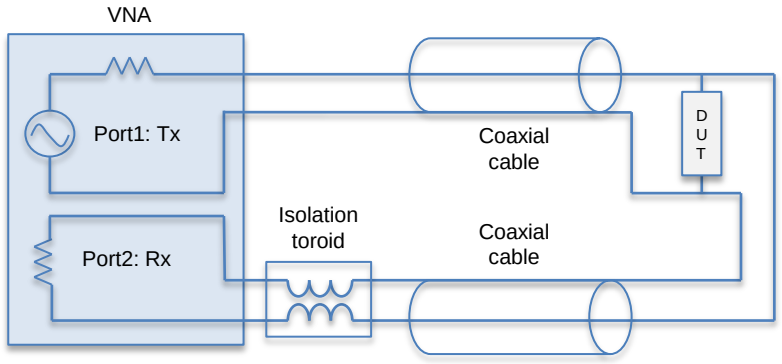
Measurement Setup - DC

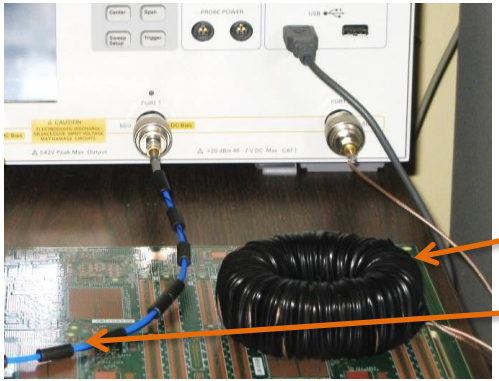
- Voltmeter (resolution=10 uV)
- Current source (1A)
- Coaxial cable (d=0.084”)
- 3D probe holder
- Semirigid probe with spring-loaded ground pin
- Measure voltage
- R=V/I



Measurement Setup - AC

- VNA (100Hz ~ 100MHz)
- Two-port shunt thru setup
- 0 dBm power
- Isolation toroid
- Ferrite-bead capped coaxial cables
- 3D probe holder
- Semi-rigid probe with spring-loaded ground pin
- SOLT calibration
- Cable with ferrite-beads & isolation transformer to reduce cable-braid error





Simulation Setup

- Commercial hybrid solver
- Extracts frequency-dependent network parameters (S-parameter)
- Import layout file
- Define port locations
- Frequency setup
  - 100Hz-100MHz, logarithmic step
- Modeling of shorts
  - Series R-L (R=1mOhm, L=1nH)

- Detailed Setup Matters
  - Stack-up (updated with cross-section data)
  - Material properties (metal conductivity, dielectric constant & loss, via conductivity)
  - Extracted via dimensions (diameter, plating thickness)
  - DC solver option (engages DC-dedicated solver to calculate DC and low frequency points)
  - Void size to be neglected in the simulation (<60mil)
  - Natural boundary condition considering radiation
  - Inter-plane coupling (neglected)

Cross-Section Data

- Two DUTs were cross-sectioned after completing measurements
- Actual thickness of each metal/dielectric layer
- Via diameter/plating statistics
- Created three simulation corner cases representing best/typical/worst impedance profiles

❖Via diameter: 11.8 ~ 12.3mil
❖Plating thickness: 1.1 ~ 1.6mil

(Unit: mil)

Layer	Layout	Board 1	Board 2
Power1	1.20	1.24	1.23
	4.24	4.01	4.04
Power2	1.20	1.24	1.24
	1.00	0.97	0.96
Power3	1.20	1.23	1.23
	4.24	4.11	4.13
Power4	1.20	1.23	1.22
	1.00	0.96	0.96

		Best	Typical	Worst
Copper		Thickest	Median	Thinnest
DE		Thinnest	Median	Thickest
Via diameter		Largest	Median	Smallest
Via plating		Thickest	Median	Thinnest
Copper Conductivity		No Derating	Derated 10%	Derated 20%
Short Wire	**ESR**	0	1mOhm	3mOhm
	ESL	0	1n~3nH	3nH

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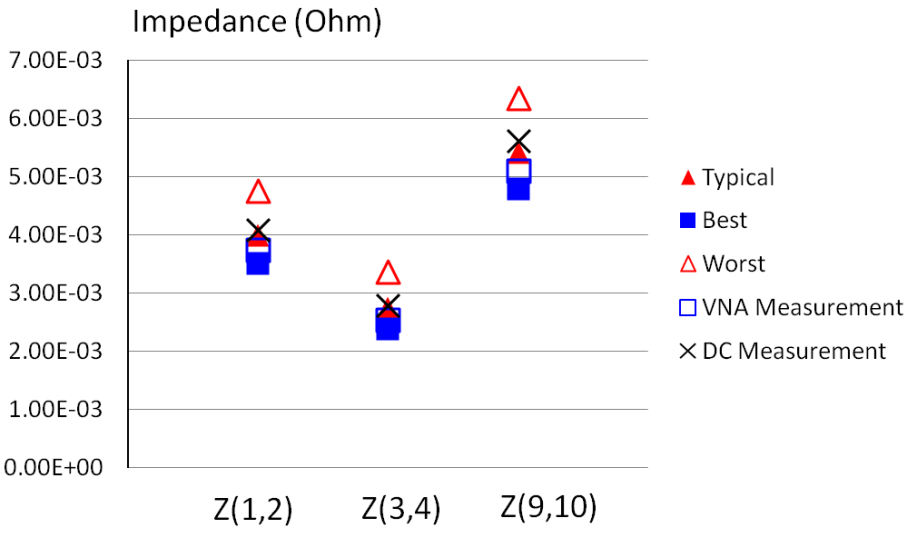
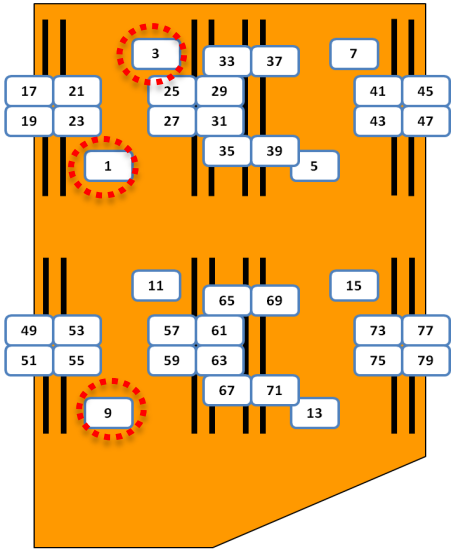
DUT-VRM: DC Correlation

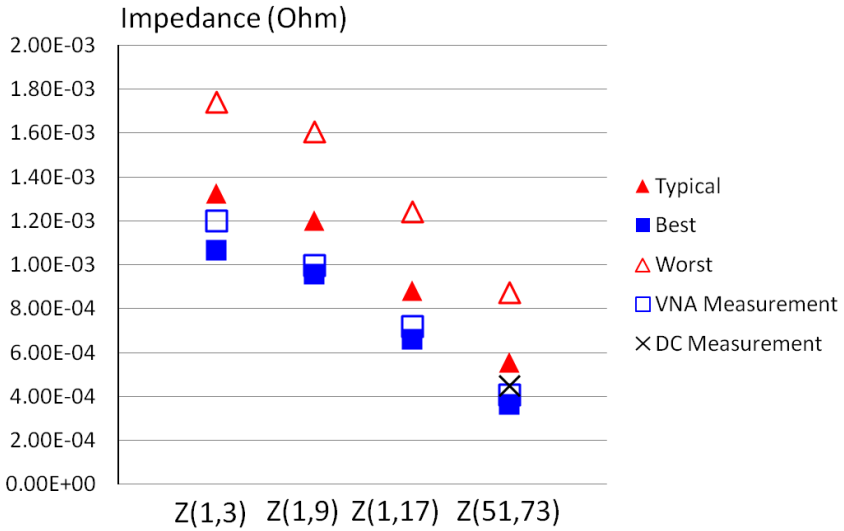
- Self-impedance results
- VNA measurement point is at 100 Hz (impedance is flat from DC to 10 kHz)
- Measurement data are within simulation corner cases

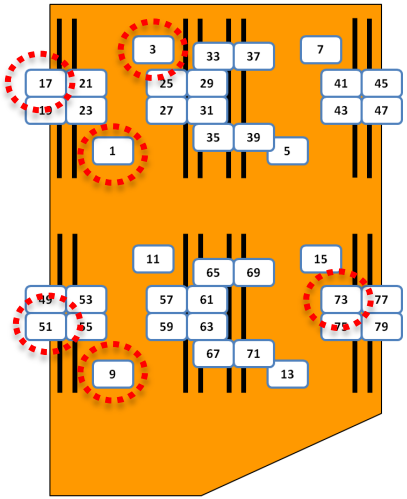




DUT-VRM: DC Correlation

- Transfer-impedance results
- VNA measurement point is at 100 Hz (impedance is flat from DC to 10 kHz)
- Impedance is as low as ~400 microohms
- Measurement data are within simulation corner cases





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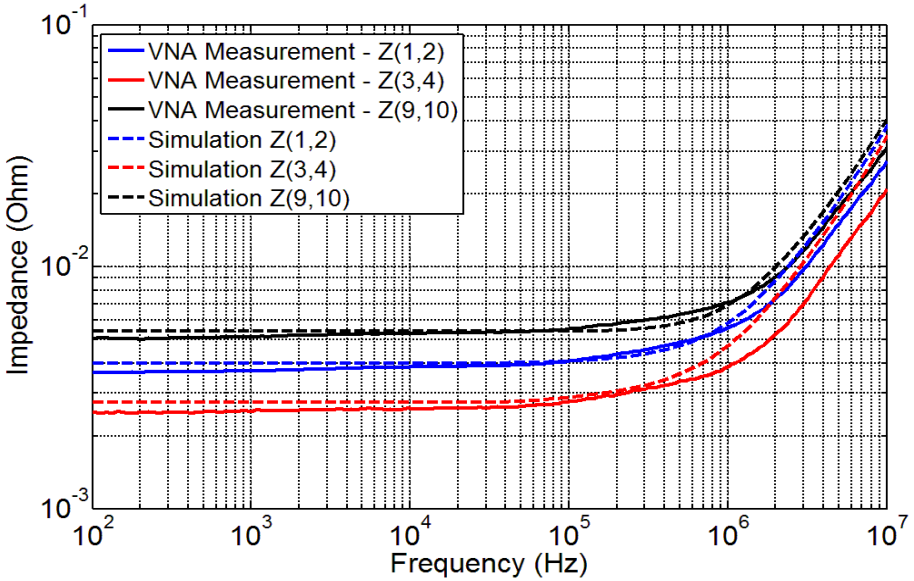
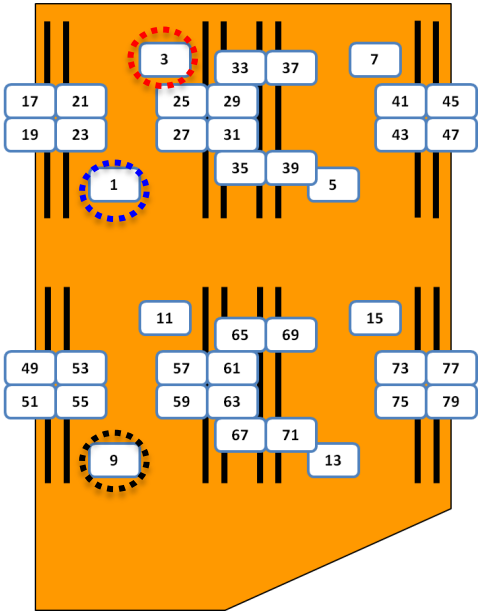
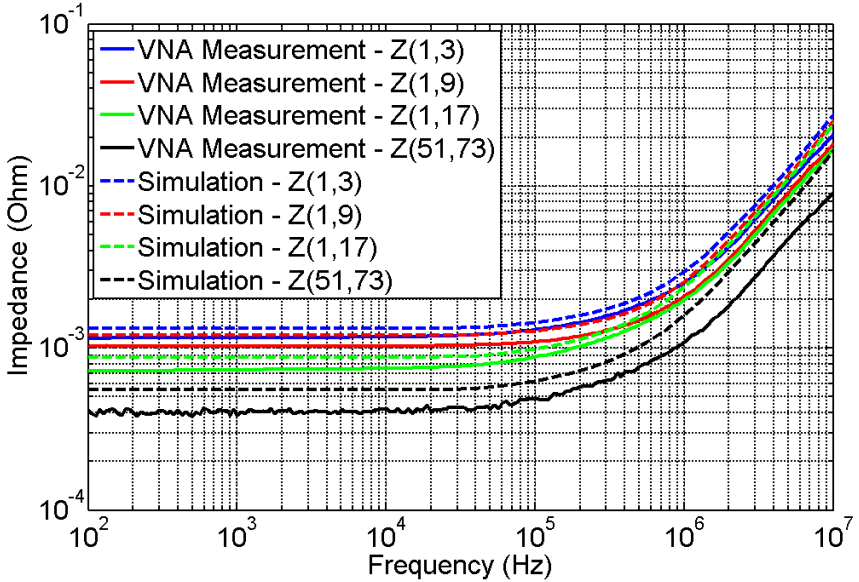
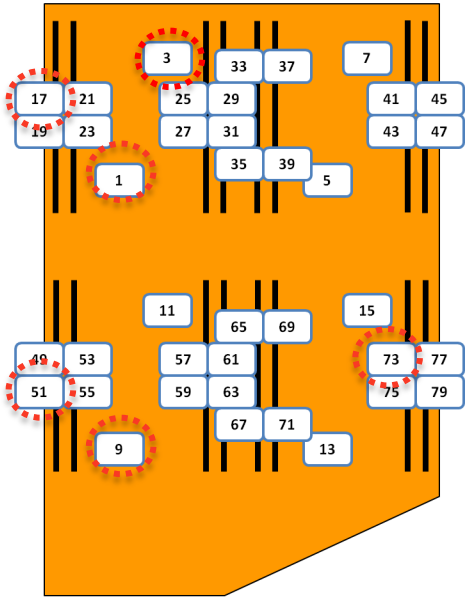


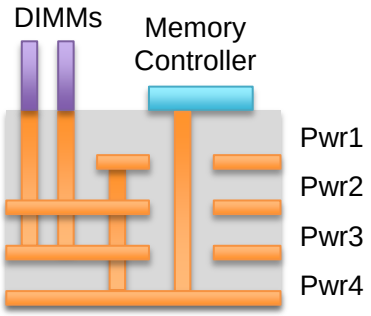


DUT-VRM: AC Correlation

- Transfer-impedance results
- Simulation is based on the typical values of the cross-section data
- Electrical path: Z(51,73) > Z(1,17) > Z(1,9) > Z(1,3)



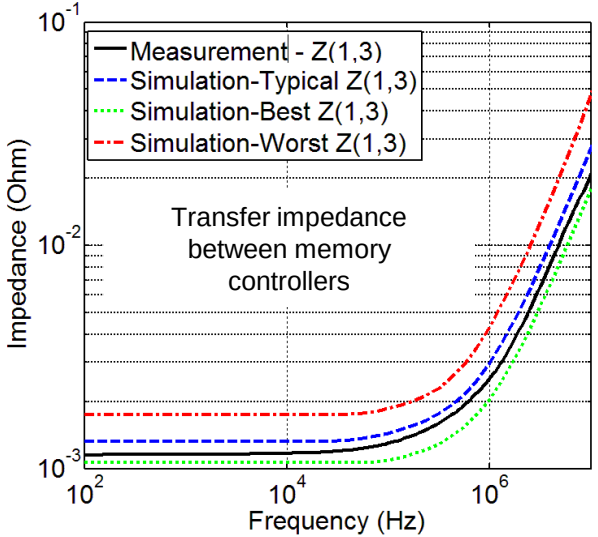


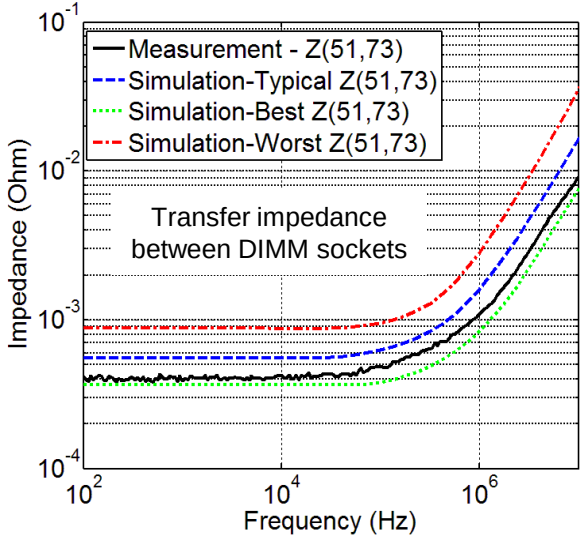


Power plane stack-up and connectivity

DUT-VRM: AC Correlation

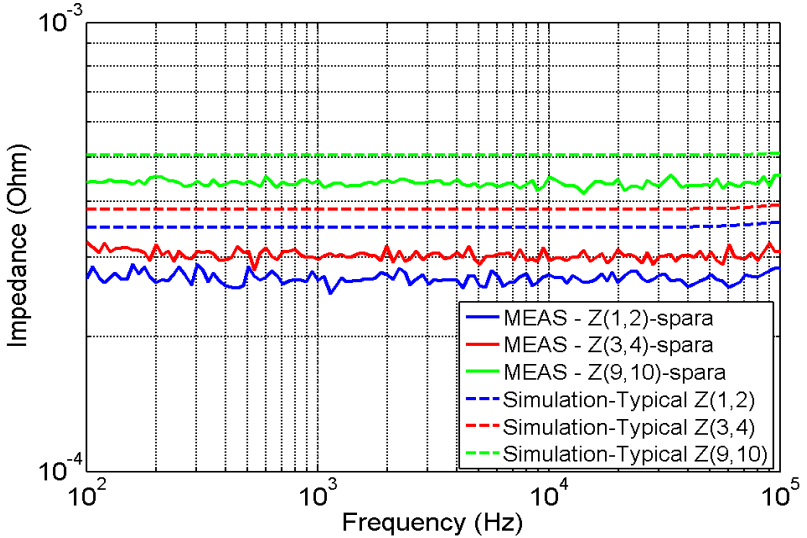
- Best and worst cases define the minimum and maximum impedance boundaries caused by manufacturing variations
- Measurement results stay within the simulation corner cases along the frequency range





DUT-CAP: AC Correlation

- Shorting over five hundred of capacitor pads dramatically lowers the DUT impedance
- Self-impedances are in the microohm range
- Transfer-impedances are below measurement noise floor (<~10^{-5}; not shown)



Self-Impedance at memory controllers

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Capacitor Models

- Measure capacitors
- Measure test fixture with shorted pads
- De-embed test fixture from capacitor

$$Z_{de-embedded}(2,1) = Z_{capacitor}(2,1) - Z_{testfixture}(2,1)$$

- Conversion of S(2,1) to Z(2,1)

$$Z(2,1) = \frac{Z_{VNA}}{2}\frac{S(2,1)}{1-S(2,1)}$$

- Conversion of 2-port to 1-port model

$$S(1,1) = \frac{Z(2,1) - Z_0}{Z(2,1) + Z_0}$$

Test fixture for ceramic capacitor

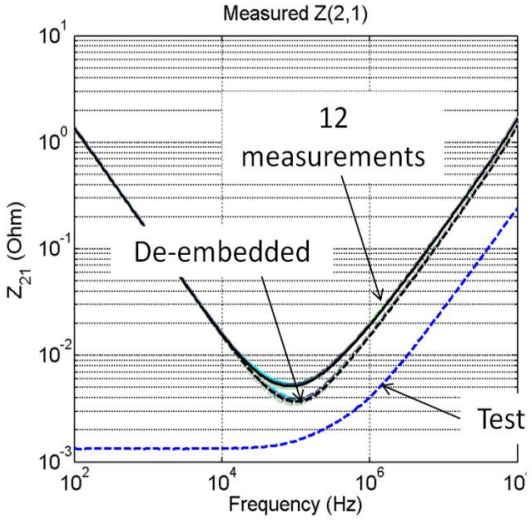
Test fixture for bulk capacitor

Capacitor Models

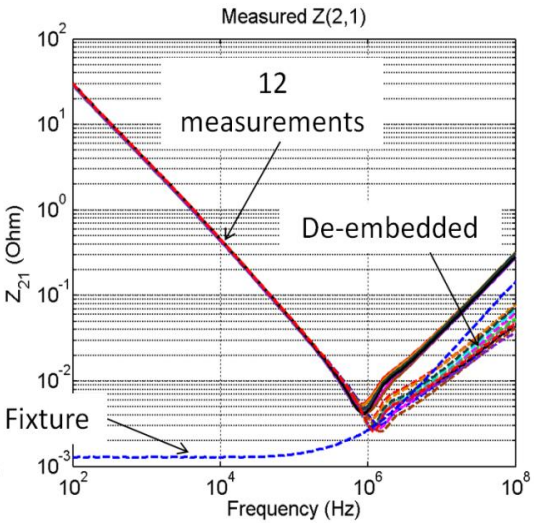
- ❑ Measured samples for each type
- ❑ Capacitance from the measurement

Type	Min	Mean	Max
1000uF	1130uF	1157uF	1194uF
47uF	52uF	54uF	56uF

- ❑Capacitance varies within +/- 4%
- ❑ESR varies within +/- 5%



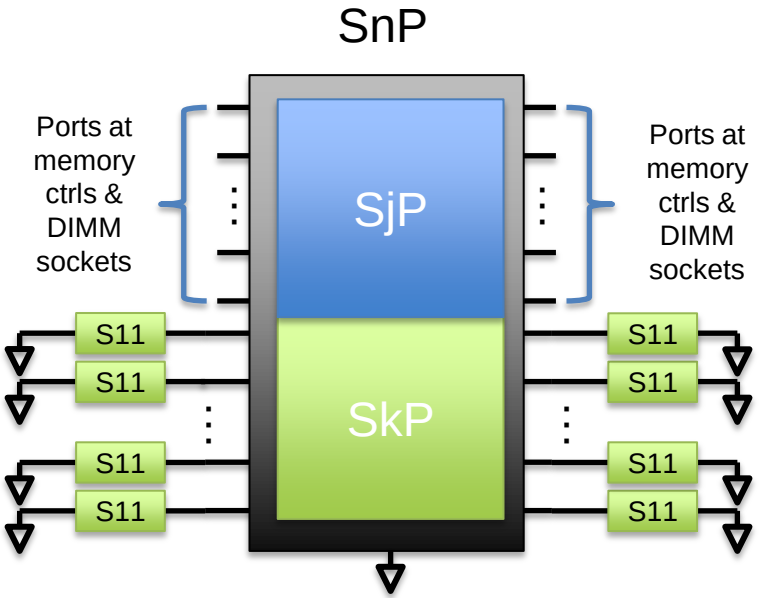
1000uF bulk capacitors



47uF ceramic capacitors

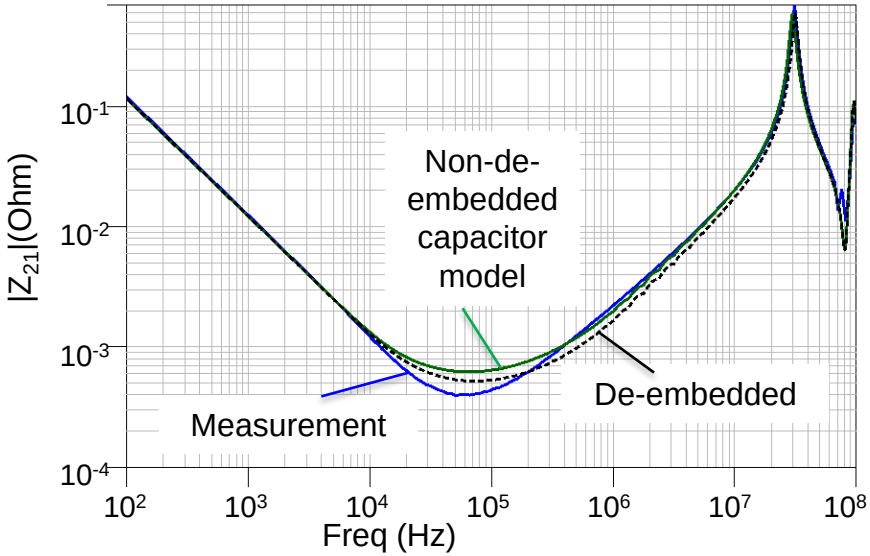
Concatenating Capacitor and PCB Models

- Create PCB model with additional ports for capacitors
  - Added ‘b’ ports at capacitor pads
  - ‘a’ ports are observation ports
  - n=j+k
- Concatenation
  - Commercial tool with a GUI
  - Manual concatenation using ABCD matrices



PCB + 1000uF Capacitors

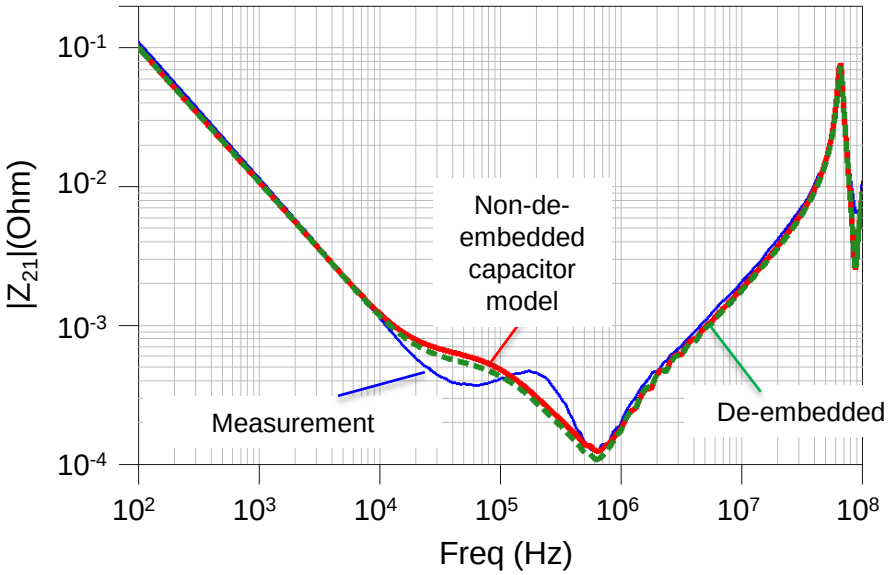
- Each of 12 bulk capacitor model was concatenated at each corresponding location
- De-embedding test fixture subtracts extra components
  - Short wire/braid used for test fixture measurement (extra R, L components)
- Inconsistent soldering quality may also affect



Transfer impedance between memory sockets

PCB + 1000uF + 47uF Capacitors

- Numbered12 bulk capacitor models were concatenated at their corresponding location
- All 40 ceramic capacitors were represented by a single model (thus, model variance neglected)
- Discrepancies may be due to one or many of the following factors
  - Capacitor model variation (measurement, solder, heat)
  - De-embedding method
  - Accuracy of AC simulation at low frequencies



Transfer impedance between memory sockets

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Conclusions

- Correlation of simulations and measurements in the sub-milliohm range
- Different techniques used for AC and DC simulations and measurements
- AC measurements using VNA and two-port shunt-thru concepts
- Low frequency accuracy of AC simulations can be improved by fitting to DC simulation result
- Simulation accuracy can be enhanced by PCB cross-section data

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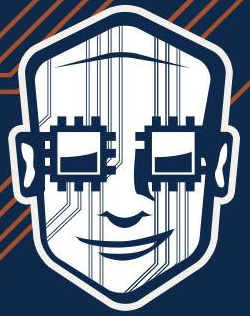

THANK YOU

Q&A

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