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Measurement and Simulation of a High-Speed Electro/Optical Channel

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Abstract

As the bandwidths of multi-gigabit interconnects continually increase, optical components are becoming increasingly necessary for high speed data transmission. Given the cost of system prototypes, simulation of high speed electrical and optical links is a critical tool for architecture considerations. In this paper we look at a high-speed SerDes channel with an optical interconnect. We present the benefits and drawbacks of IBIS-AMI modeling of these components and show correlation between channel measurements and simulations.

Authors Biographies

Shirin Farrahi is a Senior Hardware Engineer at Oracle. She is engaged in the design and characterization of high-speed signal interconnects for high-performance server systems. She received her Ph.D. in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology.

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Jeff Marquart is a Senior Product Development Engineer at TE Connectivity with 15 years of industry experience. He is currently performing high speed electrical design and modeling, as well as characterization and measurement. He received an MS in Electrical Engineering from North Carolina State University, USA.

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Xun Zhang is a Principal Hardware Engineer at Oracle. Her work focuses on high-speed SerDes architecture development, link modeling and circuit design specifications. Before joining Oracle, she had been working at LSI Corporation as a system architect for 8 years, where she was responsible for servo IP development for high density magnetic recording channels. She got her PhD from Carnegie Mellon University in 2006, and master's degree from Shanghai Jiaotong University in 2001, both specializing in communications and signal processing areas.

Gustavo J. Blando is a Principal Hardware Engineer with over twenty years of experience in the industry. Currently at Oracle Corporation, he is leading the SI/PI team and responsible for the development of new processes and methodologies in the areas of broadband measurement, high speed modeling and system simulations. He received his M.S. from Northeastern University.

Istvan Novak is a Senior Principal Engineer at Oracle. Besides signal integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is a Fellow of the IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies.

I. Introduction and Background

Optical signaling has been in use for decades in long distance communications, but as the aggregate bandwidth of individual systems grows to multiples of Terabits per second, we are seeing the need for input/output devices with optical signaling located close to the processor in high-end server systems [1]. Here we look at the use of one such optical device, a mid-board optical module (MBOM). This device is designed to be placed close to a host processor, providing optical input/output capabilities. Given the cost and complexity of these systems, the ability to perform simulations of high speed SerDes links is critical for system design decisions. In this paper we describe the generation of IBIS-AMI models of this device then look at simulations of a SerDes channel at 14 and 25 Gbps with an optical transmit to receive link between the channel's driver and receiver. By comparing measurement and simulation results for this channel, we describe the benefits and pitfalls of IBIS-AMI simulations of complex channels containing both electrical and optical components.

Traditional SerDes modeling involves a linear driver and channel model, allowing non-linearities in the receiver to be studied on their own. However, with optical components in the channel, particularly with no CDR, non-linearities of the optical link complicate the picture. Previous studies have shown the validity of modeling the non-linearities of optical link components using IBIS-AMI [2]. Using a behavioral model of a mid-board optical module, we will study to what extent traditional SerDes techniques such as transmitter FIR can improve performance for a non-linear channel and look at the challenges of tuning links with a non-linear component in its path.

As a first order, channels containing optical components can be treated as two separate SerDes links: one before the optical component and one after. ***However, in cases where the optical component does not have a CDR, how well can a complex end-to-end simulation predict overall link performance?*** In addition, given the temperature dependence and reliability requirements of the optical components that modulate electrical to optical signals, ***how much care must be taken to keep the optical components cool in our systems, and how well does IBIS-AMI modeling account for temperature dependent effects?***

How useful are the IBIS-AMI models in our experience to predict system behavior and FIR settings? How can a methodology be developed to successfully use or correlate the models? We will show answers to these questions using measurement and simulation results of a multi-gigabit SerDes channel.

II. Generation of IBIS-AMI Models

The following section describes the steps used to generate a model of the active and passive components of the MBOM. The following block diagram is used as the basis. Figure 1 shows the layout of an active optical cable or optical transceiver in loopback mode (transmit side looped back into receive side). The dotted lines show the sections at which IBIS-AMI models are created. There are four models, which are combined to create two ReTimer models, a ReTimer consists of a receive portion (input) and transmit portion (output), with a clock and data recovery (CDR) in the middle of the two. For non-CDR models, in the case of operating with the CDR(s) bypassed, the model is a

ReDriver, but is assembled in a similar fashion. This nomenclature and structure are based on the IBIS 5.1 and above interface standard (Input/Output Buffer Interface Standard). The AMI (Algorithmic Model Interface) portion is added in this standard and allows the use of non-linear components to be modeled in most channel simulators.

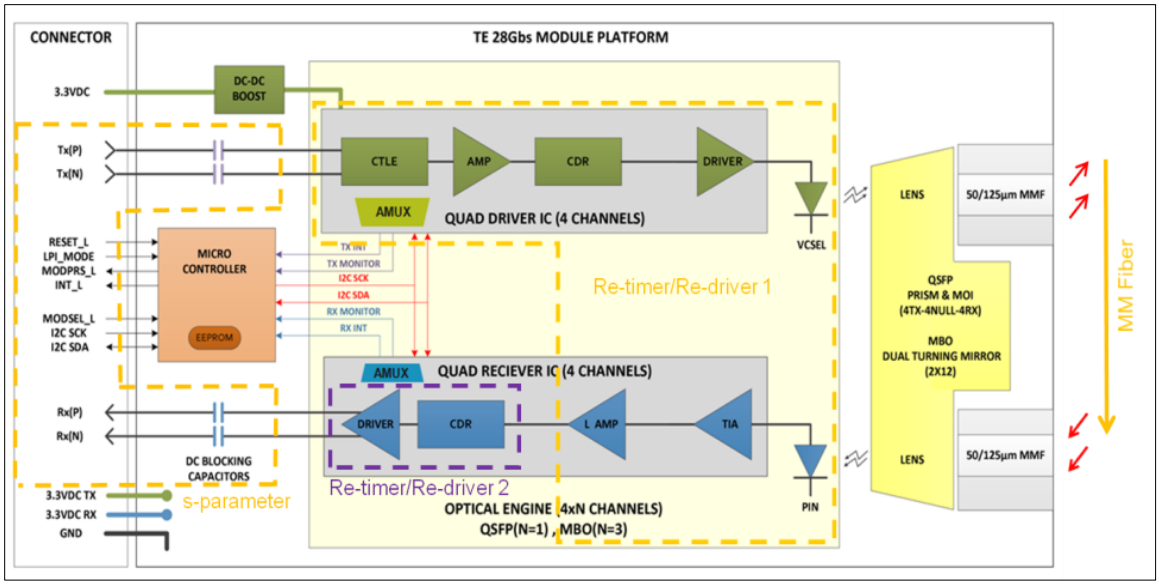

Figure 1 Block diagram of MBOM in optical loopback

The transmit (Tx) side of the module (top part of figure 1) consists of an input equalizer (CTLE: Continuous Time Linear Equalizer), used to remove jitter from frequency dependent losses in the customer channel before the module. The CTLE output is passed into a CDR, when not bypassed. The CDR output feeds a VCSEL (Vertical Cavity Surface Emitting Laser) driver and VCSEL, where the multi-mode light output is coupled to a fiber, whether pigtailed or via a removable connector, through a lensing array system.

The receive (Rx) side of the module takes light in from the fiber and couples it to a photodiode array, where a small electrical current is produced. This current is amplified by a trans-impedance amplifier (TIA) and clipped by a limiting amplifier. The next stage is a receive side CDR, similar to the transmit CDR, which drives the electrical output with adjustable amplitude and pre-emphasis. The pre-emphasis is available to pre-shape the signal to compensate for jitter due to frequency dependent loss going from the module to the host receiver IC.

IBIS-AMI models of the transceiver are then created using SystemVue software from Keysight Technologies. With the software, a schematic representation of the circuit is drawn, using built-in and/or custom components. The SystemVue software uses C++ code, which is the basis for the IBIS-AMI models. The code is then compiled into machine language, where it is transparent to the end user and serves as a black box model. The deliverable IBIS-AMI models protect all intellectual property of the module design, yet closely represent the function of the transceiver module. SystemVue is used to create the assembled models; however, it has limited simulation capabilities, so a channel simulator is used for final bit-by-bit simulation.

The optoelectronic module under simulation is assembled with vertically integrated parts, giving us the advantage of control and in depth knowledge of all electrical and optical components. The next step in the modeling process is to create models of the IC designs where applicable. The input and

output function of the ICs in the module can be derived from the computer-aided engineering tools where the transistor level designs reside. From the transistor level models, a step-response is captured for use in the IBIS-AMI model space. The transistor level models are a significant portion of the IBIS-AMI models and have been experimentally proven to be accurate and to provide reliable response output. Step-responses for the CTLE on the Tx side and output pre-emphasis (PE) on the Rx side are used to create the models at the external interfaces of the transceiver, serving as an accurate electrical bridge into the host system. The internal signal conditioning and O/E-E/O conversions within the transceiver are described in a subsequent section.

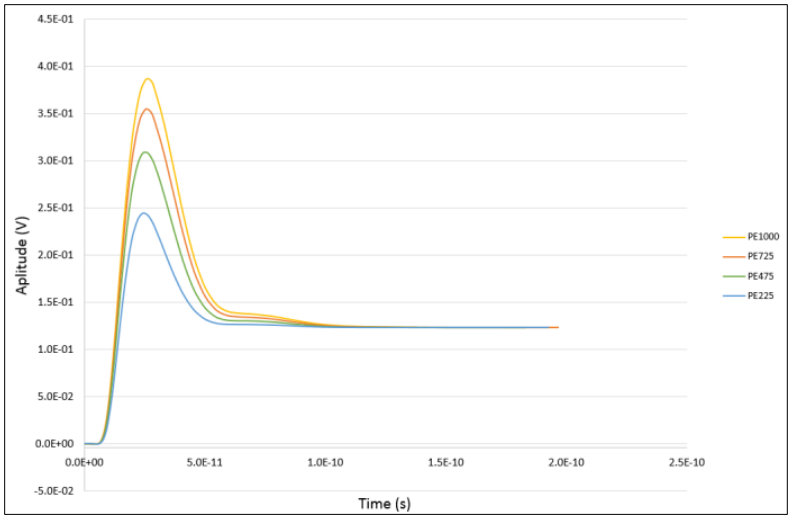

Figure 2 Step responses of MBOM output pre-emphasis settings

Figures 2 and 3 are example step-responses from the Tx CTLE and Rx PE for four hardware settings. The DC level, seen as the steady state condition, relates to the high and low levels of the differential signal, while the peaking provides the compensation for the frequency dependent channel losses.

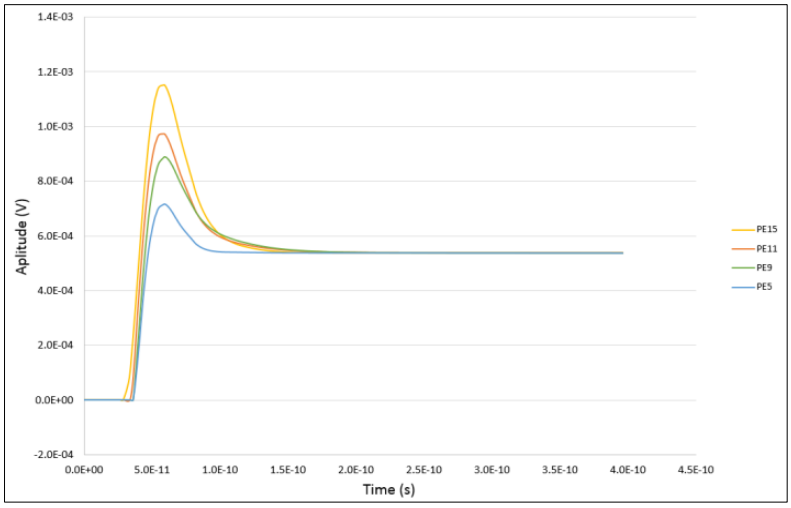

Figure 3 Step responses of MBOM CTLE

The next model is a software based model, namely the CDR model. Since a CDR is a non-linear device and contains many thousands of transistors and complex functionality, it is not practical to model the internal circuitry of the IC directly. In this case, custom program code and SystemVue library parts are used to simulate the behavior of a CDR. When all pieces are assembled in a schematic, fully functional models can be exported.

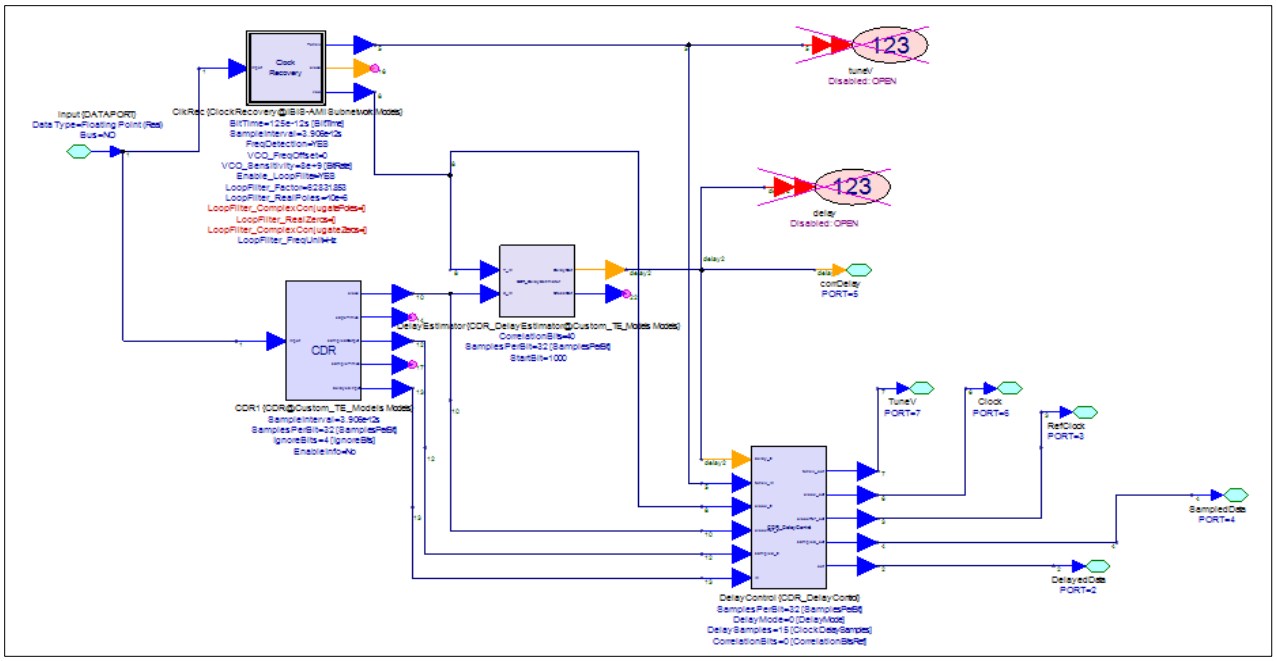

Figure 4 SystemVue CDR schematic

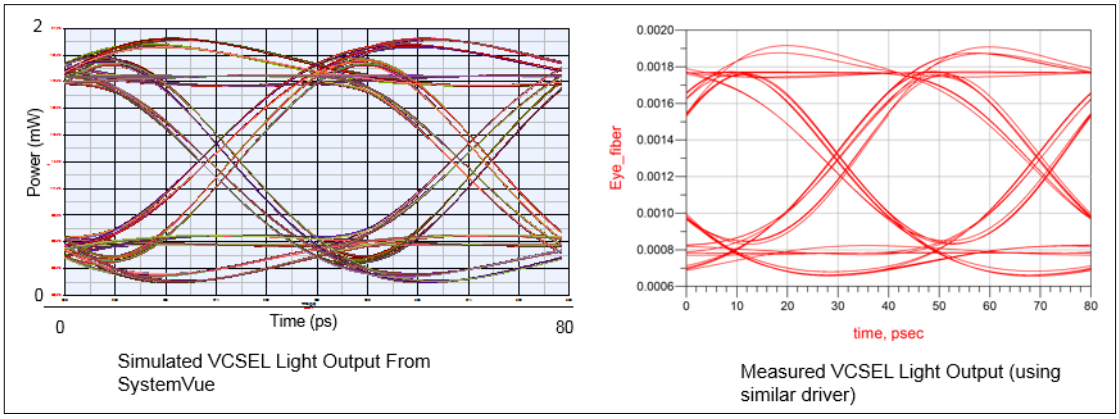

Figure 5 VCSEL output correlation

The CDR circuitry is based on a phase lock loop system with a voltage controlled oscillator created in software, which are the basic building blocks of most clock and data recovery circuits. Note that the Tx CDR and Rx CDR are derived from similar circuitry and are virtually the same. This simplifies the model process to one single CDR model. Figure 4 shows the SystemVue CDR schematic consisting of both built-in and custom components. It accurately locks to the incoming signal and retimes the data, removing all timing jitter. Since no CDR is perfect, known timing jitter

can be added back into the channel simulator at a later time, such as adding measurement based jitter to obtain increased model accuracy.

The VCSEL driver, VCSEL, and the path between the two are represented by one step response which includes the full path parasitics for increased accuracy in this portion of the model. The VCSEL model is derived from a small signal, linearized model based on a non-linear, behavioral model. The non-linear model cannot be used to create a single step-response, but the small signal model is adequate for model use and is shown to closely match the true VCSEL behavior over the intended range of operation. Figure 5 shows eye diagrams of modeled VCSEL light output next to measurement based VCSEL light output. The correct shape of the VCSEL output and jitter is properly captured in the model and will be transmitted along the fiber to the receive PIN diode.

The PIN diode on the receive side of the module is a linear device, making model creation less complicated. The generated PIN diode model is derived from a physical model and its step-response translates nicely into an IBIS-AMI model. The PIN diode model flows into the TIA, which is a built-in SystemVue model, in which electrical parameters can be entered that closely match the hardware properties. The PIN/TIA model combination matches well with measured data. The TIA portion is a high gain, limiting amp, with a fixed rail-to-rail output signal, and allows the jitter from the prior sections and the PIN diode to pass through to the next stage. Similar to the TIA, the fiber model in this loop, connecting the VCSEL output and PIN diode input, is a built in SystemVue model. This model has a similar loss characteristic to multi-mode OM3 fiber. In addition to the fiber itself, fiber coupling losses are implemented using properly set gain blocks in the schematic. The optical path contributes a relatively small amount of loss and impairment over the specified operating range of the optoelectronic link.

Lastly, the electrical interface connector, module PCB traces, optical engine path, and host channels are represented by modeled or measured s-parameters. The s-parameters can then be incorporated into the channel simulation. The exported IBIS-AMI models include s-parameters for all parts of the module and interface. Combining the transceiver IBIS-AMI models and related s-parameters with the relevant host transmitter, receiver, and channel models makes complete end-to-end system simulation possible.

III. Description of test setup

Measurements

To determine how well our simulations matched with the real operation of the MBOM, we performed measurements of the component at two data rates: FDR (14.0625 Gbps), and EDR (25.78125 Gbps). The measurements at the two data rates were done in different configurations. As shown in figure 6, at FDR where the CDR is disabled, we used our own processor as a signal generator. We then connected the optical output of our system to an MBOM evaluation board and measured the electrical signal out of that setup using a real-time oscilloscope [3]. At EDR, we used a pattern generator [4] to drive the MBOM on the evaluation board (figure 7). The pattern generator allowed us to vary the data pattern presented to the MBOM and gave us FIR capabilities.

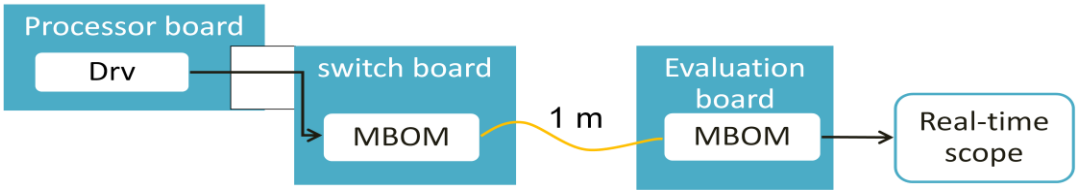

Figure 6 Measurement setup for FDR

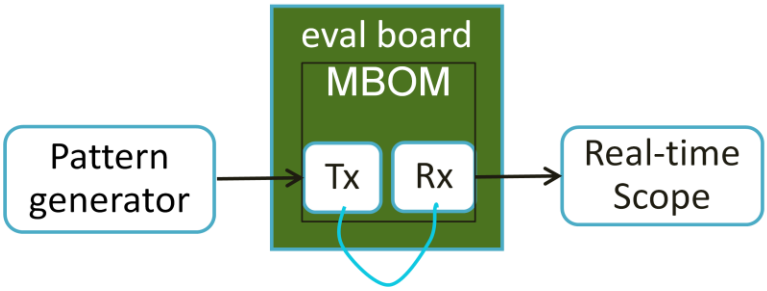

Figure 7 Measurement setup for EDR

We also performed some measurements with a Peltier heating element on the board behind the MBOM to heat the part to its maximum rated operating temperature of 70°C. A thermocouple was attached to the MBOM at the base of one of its heat sink fins to monitor the part's temperature.

To measure the optical signal out of the MBOM, we used an optical breakout cable which gives access to each optical lane as an individual fiber channel (FC) connection. This connection was fed into optical modules that were used with a sampling oscilloscope [5] and a real-time oscilloscope [6]. The output waveforms were measured in mW representing the optical power of the signal.

The MBOM contains a CDR in the optical driving circuitry and in the optical receiving circuitry (figure 1). The CDR is only designed to work at EDR, so it is not used for any of the FDR measurements or simulations, making it particularly important to simulate the entire link at this data rate as opposed to simply the two portions on either side of the MBOM. In the current revision of the hardware, the optical receiver CDR introduces errors even at EDR, so for both the measurements and simulations shown here at this data rate there is only one active CDR in the link.

Simulations

We performed simulations of our test setup using IBIS-AMI models of the MBOM that were generated as described above. We ran our simulations using a Matlab-based IBIS-AMI simulator created in-house. For FDR measurements, we used a custom, linear model of our processor's driver. For EDR measurements, we used an ideal linear driver to model the pattern generator output. We used a third party tool to draw the block diagram shown below [7]. From the diagram, we see that

the MBOM is broken up into two re-driver models. In this case, the CDR is bypassed on both, making this an FDR simulation deck. At EDR, the first stage is a retimer, containing a CDR.

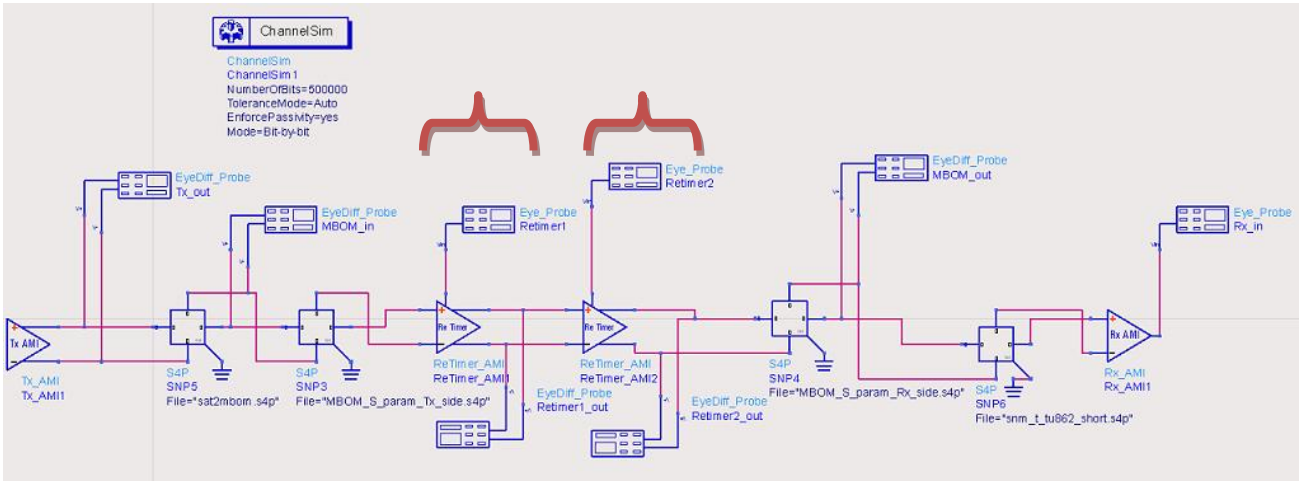

Figure 8 Block diagram showing simulation setup. First and second MBOM stages highlighted with brackets

Some designers would simplify this link as two separate one-stage simulations: one on each side of the MBOM. However, since even at EDR the MBOM optical receiver CDR is not functional, we perform an overall simulation to study the impact of jitter in the optical domain on the final result. Starting from the left, we see models of our driver, package and channel on our motherboard. All these elements, including the driver are fairly linear in nature. Starting at the first stage of the MBOM we believe the model is very non-linear. Because of this, we expect that changes before the MBOM input will not affect the eye quality at its output. This is due to the non-linearities in the CDR and in the MBOM optical receiver's limiting amplifier. At the MBOM output, we have another set of channel and package models. This output is then fed into our receiver model to determine the final eye seen internally in the chip.

IV. Results

Measurement and Simulation Correlation

Before looking at any active component responses, we wanted to determine how well our passive simulation models agree with the real components being measured. To do so, we used time domain reflectometry (TDR) as a quick way of checking correlation. Using s-parameter models of the MBOM socket and the traces and connector on the evaluation board, we computed the TDR response for each of these elements and compared the responses to our single-ended measurements. Figure 9 shows a comparison of the MBOM socket model and measured TDRs. The socket includes pads, vias, and a flex cable connecting the vias to a second series of pads. Our measured TDR has some similar features to the TDR from the model, but we see an impedance difference (~50Ω vs

~62Ω) for a region of the model. We took another version of the MBOM and removed the active element sitting on the top ports. From the location of the high impedance (open) portion of that measurement, we determined that the region of impedance mismatch corresponds to the flex cable portion of the model. It could be that this flexible material is not well represented in the 3D simulation tool. In addition, the slope of the measured TDR increases steadily with time. We considered the possibility that this slope could be due to DC coupling capacitors located inside the integrated circuit (IC) of the MBOM. They cannot be removed in the hardware without removing the IC. We created a model of a discrete capacitor of the correct magnitude and chained it with the package model; however, the TDR of this result still did not correctly predict the upward slope of the measured package TDR. Therefore, this mismatch will exist in our measurements and can explain some of the differences between our measurement and simulation results.

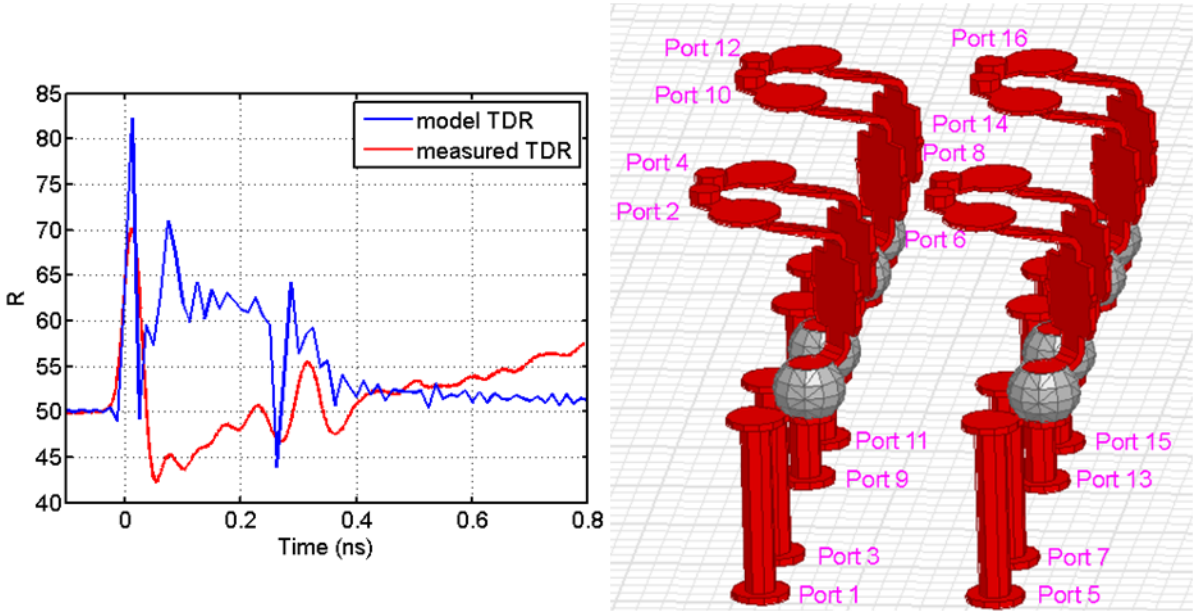

Figure 9 TDR of MBOM socket from measurement and model (left). Diagram showing MBOM socket 3D model (right)

For the evaluation board trace and connector model, the s-parameters were actually obtained by measuring a reference trace on the board with the same length as the trace being used for our measurements. However, the reference trace was connected with a different SMA connector than the one used for the measurements in this paper. As seen in figure 10, the connector used for our measurements seems to have a smaller via depth and better matching with the evaluation board trace compared to the connector used for the reference trace measurement. The mismatches in these two models between measurement and simulation will have an impact on the measurement to simulation correlation shown in the following sections.

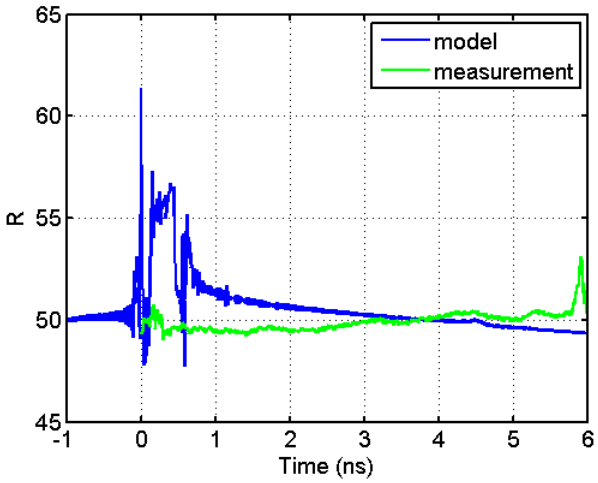

Figure 10 TDR of evaluation board traces and connectors from model and measurement

FDR

Before performing measurements through the MBOM, we compared the signal at the input to the MBOM by attaching a 33 GHz probe to the vias on the board before the MBOM. We compared the responses obtained at this point to simulated waveforms of our driver and channel model. Although there is a significant difference in the detailed shape of our measured and simulated waveforms at this stage, we will see that this difference does not propagate through the MBOM. As will be shown, even fairly large changes in input eye properties have a minimal impact on the output properties of the MBOM due to its non-linearity.

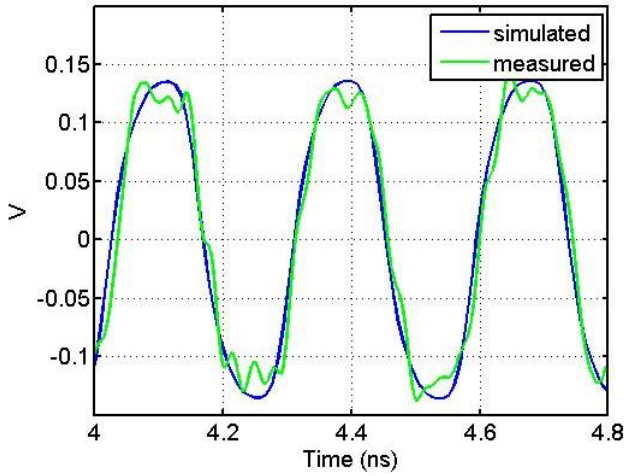

Figure 11 MBOM input electrical signal measurement to simulation correlation

Our initial MBOM measurements at FDR were performed using a PRBS 31 pattern. Comparing the measured and simulated eye diagrams obtained from this measurement, we see similarly shaped eyes

with very different amounts of jitter. The driver used for our simulations was an ideal transmitter with no jitter; whereas, the pattern generator used for measurements had roughly 11 ps of random jitter at its output, causing roughly 0.15 UI in random jitter which corresponds well to the difference in jitter between our simulated and measured eye diagrams.

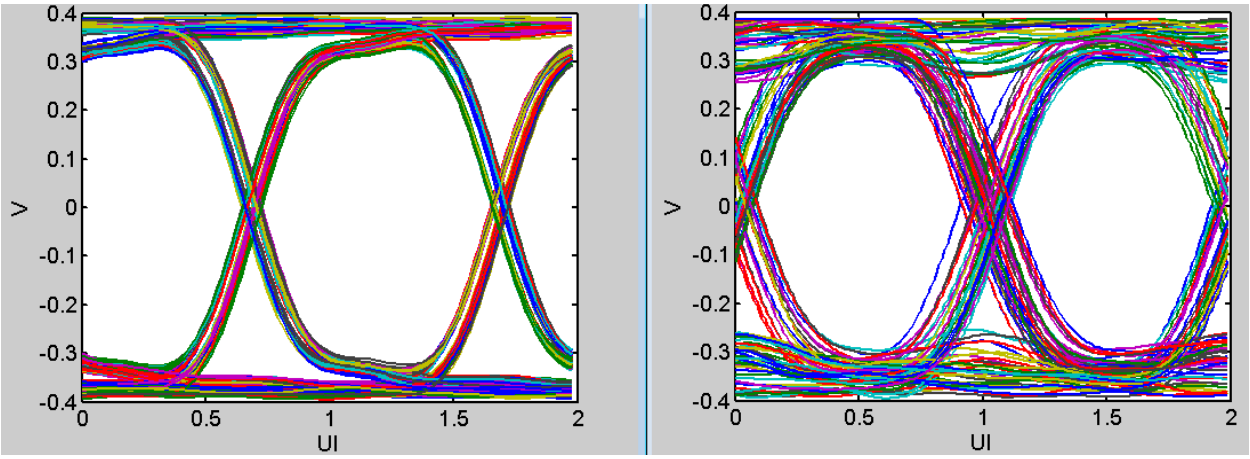

Figure 12 Simulated eye (left) vs measured eye (right) at FDR

To more carefully look at the MBOM output electrical properties, we measured the response using a clock pattern slowed by a factor of four. From this measurement using the minimum output amplitude from the MBOM but maximum pre-emphasis, we see a mismatch in the overall amplitude from the model and measurement but a good match in the shape of the waveform.

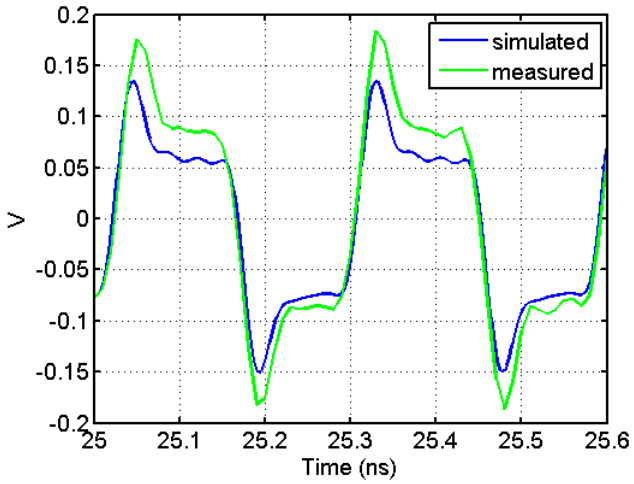

Figure 13 Measured vs simulated waveform of MBOM electrical output at FDR

We have shown that when comparing measurement to simulation results at FDR, the correlation shows the overall trends well but does not produce a perfect match. In this case, the mismatch can be explained partly by the fact that TDR results of each linear element model show differences with our

measured TDR result. Overall we do see, and are able to identify the first order effects. For example we can see that changes in shape of the curve at the input of the MBOM do not result in significant changes at the output due to non-linearities in the device. This suggests that the simulation could be simplified to ignore the driver and channel before the MBOM. However, the MBOM itself should still be simulated in its entirety. We will now look at measurement to simulation correlation at a higher data rate.

EDR

To determine the MBOM's performance at its target data rate (EDR), we performed a series of measurements and simulations at this higher data rate. Initially, we measured the MBOM's response to a clock pattern slowed by a factor of 16 with the minimum output amplitude and pre-emphasis settings from the MBOM. As described in the measurement setup section, the optical receiver CDR was disabled in both measurements and simulations. As shown in figure 14, our measured and simulated responses agree to a first order. The largest difference is in the rise time of the measured response which is significantly longer than that of the simulated response. In addition, as seen in the MBOM input measurement at FDR, the settling behavior of the measured response shows significantly more ringing than the simulated response.

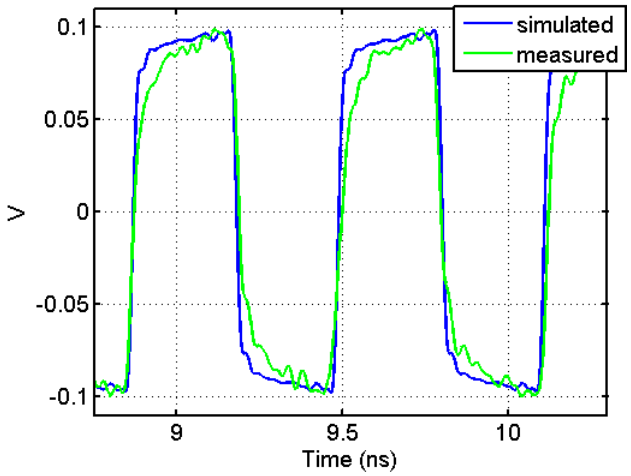

Figure 14 Measurement vs simulation of MBOM electrical output to a clock pattern slowed by a factor of 16. Minimum output amplitude, minimum pre-emphasis, and maximum CTLE settings

Our pattern generator for these measurements had FIR capabilities. We looked at the impact of varying these parameters on our output measurements (figure 15). As expected, even large changes in pre and post on the pattern generator do not have an effect on the MBOM output pattern. This is because of the highly non-linear nature of the MBOM and the fact that there is a CDR in the device. The link is therefore re-timed and reshaped by the MBOM.

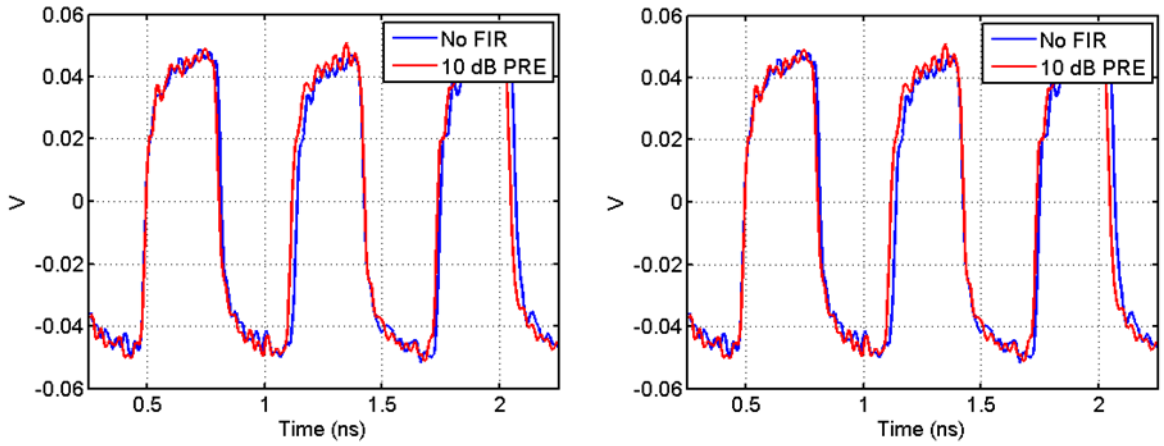

Figure 15 Varying pattern generator FIR settings and observing effect on MBOM electrical output

Although not all of the MBOM settings available in hardware are included in the IBIS-AMI models, we measured waveforms for a subset of the settings available through the IBIS-AMI models to determine the degree of correlation. In figure 16 below, we see the correlation plots for the minimum output amplitude setting with a range of pre-emphasis values at the MBOM optical Rx. Compared to the case with zero pre-emphasis, we now see good correlation in the rise and fall times between measurement and simulation. For the zero pre-emphasis setting (figure 14), it looks like the model assumes the maximum rise time but with no peaking. As shown here, the real hardware doesn't achieve this fast rise time if pre-emphasis is not used. As seen previously, our measurements include significantly more ripples during the high or low settling times. Also, for the three higher pre-emphasis values measured (9, 11, and 15), our simulation results consistently predict a larger peaking amplitude than we are seeing in the measurements. To investigate if the 33 GHz bandwidth of our real-time oscilloscope was causing this difference, we filtered the output signal from our simulations with a 33 GHz low-pass filter. This had little to no impact on the simulation result. Therefore, this appears to be a genuine difference between the IBIS-AMI models and hardware.

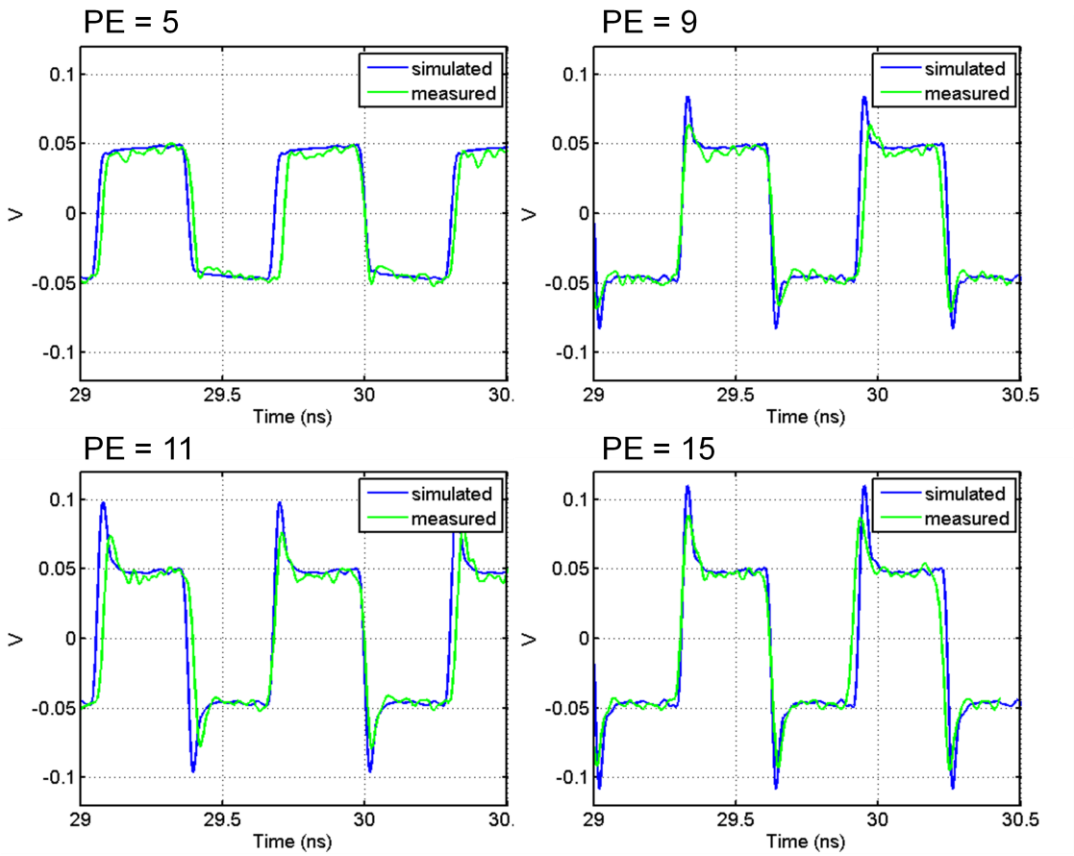

Figure 16 Measurement and simulation correlation for various MBOM pre-emphasis (PE) values

In both the simulation and measurement environments, we have the ability to view the optical signal out of the MBOM. This can be useful for tuning the portion of the link from our transmitter to the MBOM and for ensuring proper optical output power and eye opening. In figure 17 below, we show our optical measurement and simulation results using a clock pattern slowed by a factor of 4. The optical module used for these measurements did not provide a DC output optical power value. As a result, we also centered the simulation result above and below 0 mW. However, as shown in figure 18, the VCSEL light never turns off when the MBOM is operating, so the signal must vary around a constant DC optical output power.

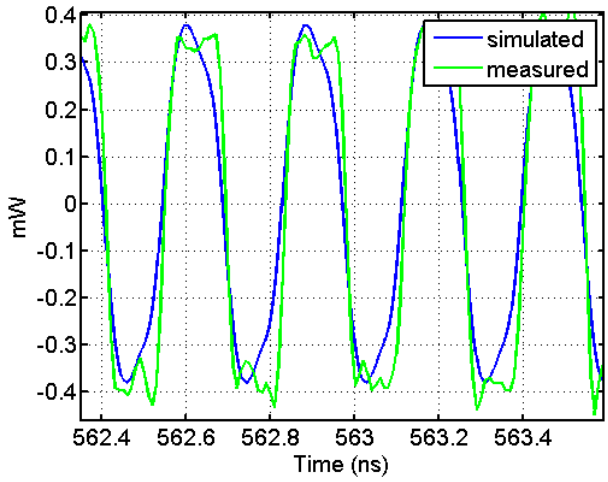

Figure 17 EDR MBOM optical output measurement vs simulation

As we saw in our previous results, in the optical domain at EDR the quality of the correlation is acceptable overall in terms of amplitude but not very good in terms of the details and rise time. If future revisions of the MBOM hardware resolve the issue with the Rx CDR, then some of these differences will be unimportant since they will be recovered and re-sampled. Although we are using an oscilloscope with a fairly low bandwidth for these measurements, we still see higher frequency effects in the measurements than the simulations. At this point we have not investigated where the loss of BW is happening in the model. The fact that we don't see a difference in the overall amplitude is comforting, telling us the optical power of the model and driver are well matched. Therefore, from all our correlation we believe that at a high level the link is likely to provide error free transmission but will still require tuning using the real hardware.

Varying temperature

The component that generates the optical signal in our MBOM is a vertical-cavity surface-emitting laser (VCSEL). These components have a wide range of linear operation; however, the slope of the linear curve decreases with increasing temperature as shown in the cartoon below. The MBOM has the ability to vary the input properties to the VCSEL to accommodate the change in slope, but in our measurements we disabled this compensation mechanism to determine how big an impact the temperature increase might have on the optical performance.

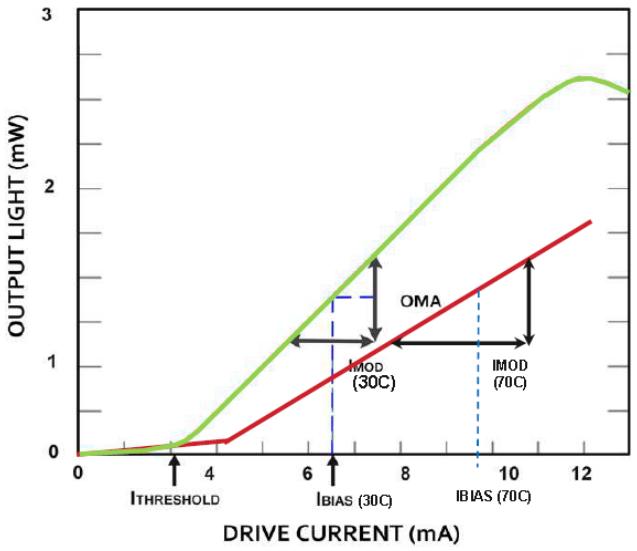

Figure 18 VCSEL input-output curve with varying temperature

Our measurements show little to no change in MBOM output properties when the part goes from room temperature to its maximum recommended operating temperature of 70°C at low data rates, but we observe a significant change in the eye properties as we increase the data rate. As shown in figure 19, we observe more than 10% decrease in eye height and width when increasing temperature at EDR and a similar increase in the RMS jitter.

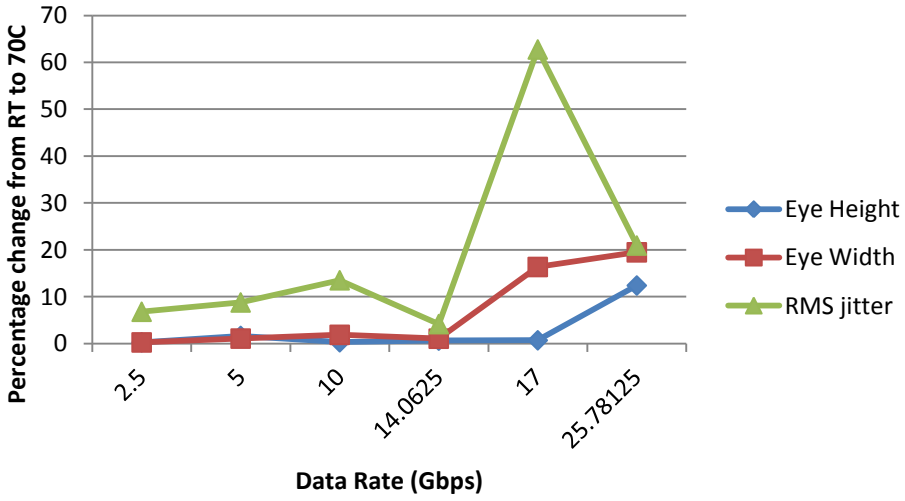

Figure 19 Measurement of MBOM electrical output parameters at room temperature (RT, 25°C) and high temperature (70°C)

Our IBIS-AMI models of the MBOM include a high temperature parameter, simulating operation of the device at 85°C. Performing channel simulations at this high temperature, we found a roughly 14% decrease in eye margins even at lower data rates. The fact that we are not seeing a change in

our high temperature measurements below EDR could be because of the lower temperature (70°C), or it could be that the model is giving a pessimistic view of the MBOM's temperature performance.

Conclusions

In this paper we have shown measurements and simulations of an electro-optical channel operating at data rates above 10 Gbps. Through our investigation, we learned that it is very important to understand how the settings available through the IBIS-AMI models relate to the settings available in the real hardware. If the model does not cover the entire range of settings, it's possible that the link will work much better than simulation results suggest.

We have presented correlation results between our measurements and simulations to look at the use of IBIS-AMI modeling of optical devices at high data rates. Our correlation results show matching responses to a first order. However, we are seeing differences in the detailed responses such as the ripple seen before the signal settles and the amount of peaking. As with all simulations, they are helpful when hardware is not available, but the results cannot be completely trusted without any hardware correlation.

We therefore conclude that we cannot use IBIS-AMI models to predict performance with a high accuracy at a pre-hardware level. We can use these models as another element in our toolset to increase our understanding of the problem. When test hardware or very preliminary spins arrive, we try to correlate and most times "correct" these models, whether they are S-parameters from vendors or IBIS-AMI models, to develop an understanding of the system and to increase the accuracy of the model and confidence in its results. We find that this effort ultimately increases our understanding the bounds of the model. At that point, we can go further with simulation to try to predict performance before final hardware. It's also important to mention that the ultimate determination of settings is obtained by doing in-system BER shmoo tests as an absolute necessary step for proper tuning, implying that even after all the modeling and correlation, the predicted settings by simulations for these complicated channels are almost never the same as the actual optimum BER. We are happy if it at least comes close, letting us know we have captured the first order effects.

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