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Mid-Frequency Noise Coupling between DC-DC Converters and High-Speed Signals

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Abstract

As density increases on printed circuit boards, designers are forced to make trade-off decisions, such as routing multi-gigabit signals close to noisy power rails without adequate shielding. When making these trade-offs, designers must consider noise coupling very carefully. In this paper we will analyze some coupling mechanisms board designers face, particularly coupling from DC-DC converters to nearby high-speed signals. By using a case study, we will demonstrate that some coupling mechanisms may be difficult to detect and prevent. Techniques to avoid these coupling mechanisms will be suggested.

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1. Introduction

As form factor decreases and routing density increases on printed circuit boards (PCBs), designers are forced to make trade-offs, such as routing multi-gigabit signal lines close to noisy rails, sometimes without adequate shielding. A documented source of noise in electronic systems is switching power converters, such as a non-isolated step-down DC-DC converter, also known as a Buck converter or a step-down switching regulator [1-3]. Although switching regulators have higher efficiency compared to linear regulators, they introduce electromagnetic interference (EMI) due to the fast switching of the power devices that may be coupled onto nearby signal traces [4]. When making layout decisions, signal integrity (SI) and power integrity (PI) engineers must consider the noise coupling mechanism of a switching power supply very carefully.

It is relatively easy to understand and contain high-frequency noise where the power is mostly concentrated in a frequency range above the onset of skin effect on the PCB traces and planes. High frequency noise is normally observed with close proximity to the aggressor circuit and may stay localized as it decays rapidly due to skin effect. Reference planes can effectively isolate high-frequency noise from one cavity to the next. The onset of skin effect in a typical printed circuit board with one ounce copper layers is around 10 MHz.

Understanding and containing mid-frequency noise (close to 100 MHz, where the skin-depth related attenuation is not yet high enough) is more difficult. Since the wavelengths associated with mid-frequency noise are larger in size compared to the structures within PCBs, the noise may float around the system with minimal attenuation. Reference plane thickness is comparable to the skin depth, and reference planes will not completely isolate this noise from one cavity to the next. Noise locality cannot be assumed. Mid-frequency noise may even be superimposed on high-frequency signals and may cause a reduced margin or fatal system errors.

Mid-frequency noise coupling associated with a switching regulator in a practical server system will be shown by means of a case study. This work will go through this case study step by step in attempt to emulate the typical debug process to find these types of issues. This approach will aid in the process of understanding and uncovering the mechanism by which the coupling occurs. Through the process it will become clear how difficult the coupling mechanism can be to detect and prevent. Finally, with a solid understanding of this specific failure mechanism, practical guidelines to mitigate this noise coupling will be suggested.

2. Background

2.1 Problem Discovery

The noise coupling issue was initially discovered during routine PCIe Gen3 compliance testing on a motherboard in a multi-processor server system.

During testing, one specific option card, in one specific slot, repeatedly failed on a single transmitting PCIe differential pair, which will be referred to as the victim lane. The eye diagram of the victim lane, juxtaposed with the eye diagram of a compliant lane in an adjacent slot, is shown in *Figure 1*.

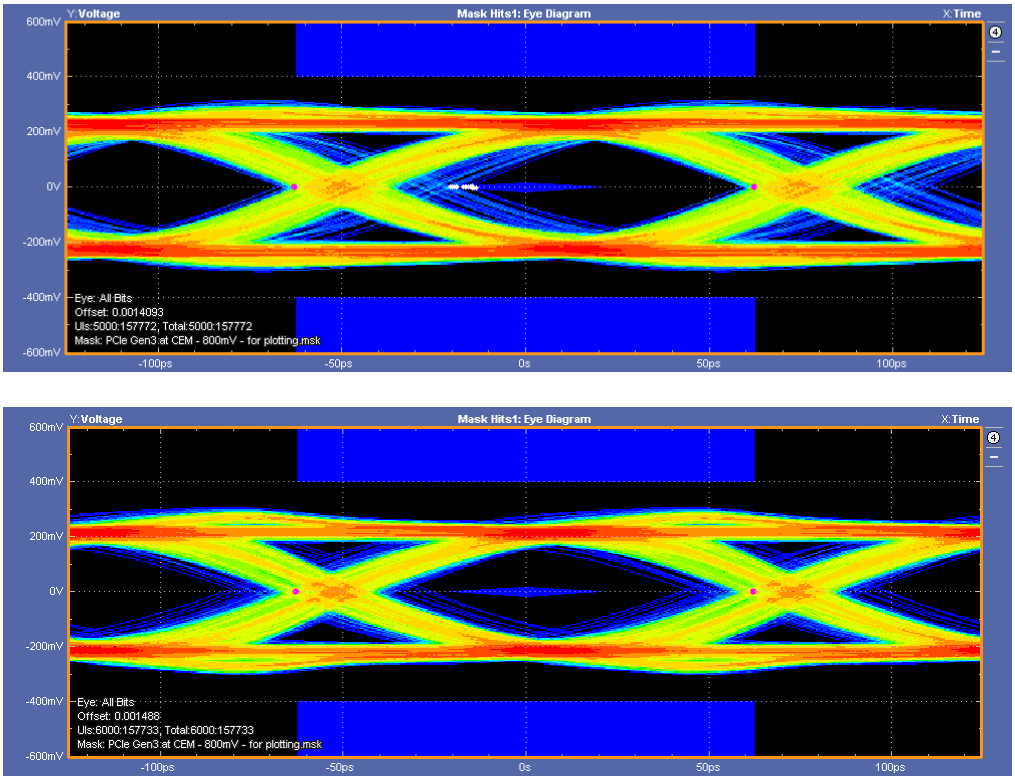

Figure 1: *Measured PCIe Gen3 (preset 5) eye diagram of (top) victim lane and (bottom) same lane in adjacent slot. The eye diagrams are plotted against an eye mask specified by PCI Express Base Specification Revision 3.0 [5].*

The eye diagrams shown in *Figure 1* were measured on a 12.5 GHz real-time oscilloscope using applications Serial Data Analysis (SDLA) and DPOJET. The eye diagram measurements also required a PCIe Compliance Load Board (CLB) inserted into the problematic slot. All lanes were terminated on the CLB with either SMP plug-in terminators or hand-soldered resistors.

The bottom of *Figure 1* displays a better-behaved, compliant eye of the same lane (as the victim lane) in an adjacent slot. As expected, the eye has an opening and some level of jitter, as observed by the distribution of the edges. The top of *Figure 1* shows the non-compliant, failing eye associated with the victim lane. There are 15 mask violations and significant jitter. It appears that most of the distribution is where it should be (the edges are bunched up together), but there seems to be a few edges encroaching the eye, causing mask violations.

A disturbance is happening that is repetitive but not happening all the time (i.e., on only a few edges). From the non-compliant eye diagram, it can be inferred that there might be a mid-frequency event that is distorting the edges.

The next step was to verify the failing lane by means of mapping an internal eye contour on the option card. The option had a UART port which enabled generation of an internal eye contour map of the Rx signal post continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE).

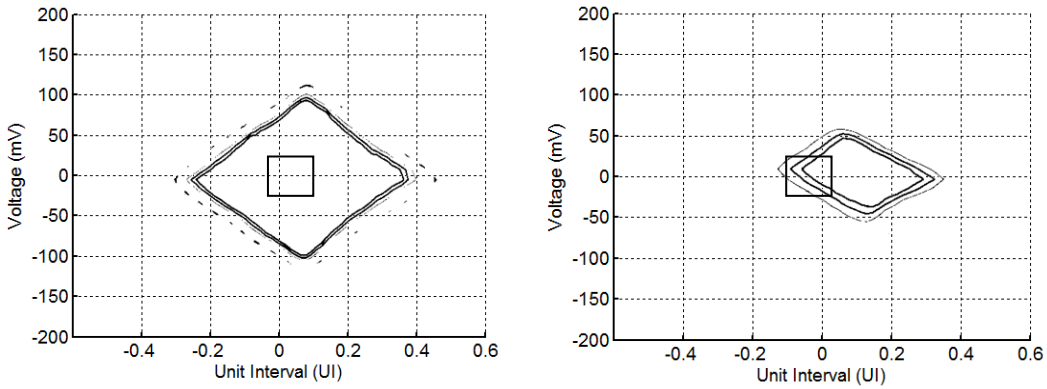

Figure 2: *Option eye contour map of (left) lane close to victim lane and (right) victim lane. Rectangle is Rx mask, and inner contour is BER 1e-8.*

As can be seen in *Figure 2*, the victim lane hits the mask and fails. It has about 40 mV peak-peak vertical opening at 0 UI. A nearby lane's map is significantly open. It has about 150 mV peak-peak vertical opening at 0UI.

A real-time oscilloscope measurement was taken of the victim lane to further understand and quantify the problem. With a real system running, the oscilloscope displayed periodic noise with a frequency of about 110 MHz and an amplitude of 150 mV peak-peak on the victim lane, as can be seen in *Figure 3*.

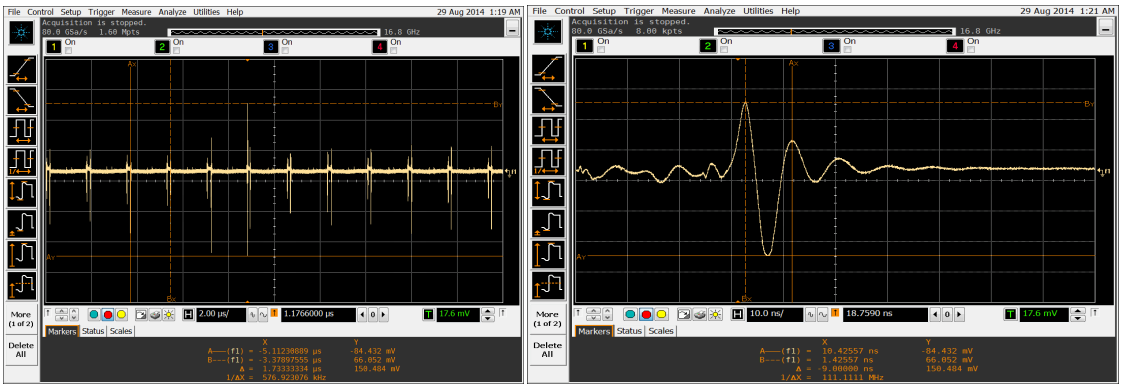

Figure 3: *Noise observed on the victim lane at the CLB.*

It should be noted that the amplitude of the waveform in *Figure 3* is the common-mode signal, the summation of the P leg and the N leg of the differential pair for convenience. It follows that the maximum common-mode voltage noise would then be 75 mV, (P+N)/2.

When measuring the waveform of other compliant PCIe lanes, this common-mode noise was not present. By looking at the eye diagram and observing the signature of the baseband common-mode noise, it was strongly suspected that this noise might be the cause of the lane failure.

The next step was to review the board layout.

2.2 Layout Description

Near the victim net there was a step-down DC-DC switching regulator which delivered a maximum of 17 Amps of current to a nearby load. This can be seen in *Figure 4*. There were several PCIe differential traces, including the victim, running through and next to the 12V main vias feeding the regulator.

The 12V input supply, which powered the power FETs of the converter, was located on the top of the board. All the required decoupling capacitors were connected to the 12V input supply.

The 12V input supply (Vin) was connected to 12V main through an input fuse on the top of the board. The 12V supply had vias stitching the top puddle to an internal 12V layer. The associated PCIe transition vias were placed close to the 12V feed vias.

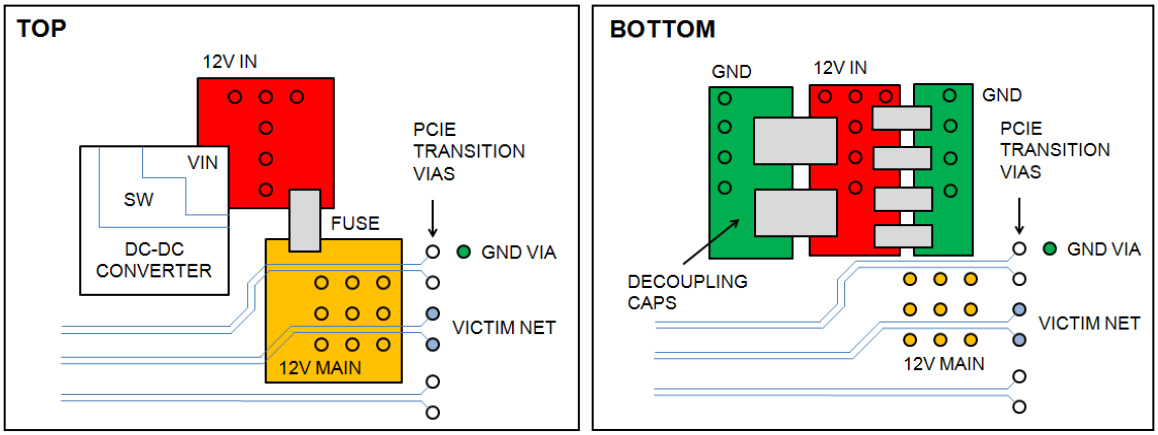

Figure 4: *Layout of problem area as seen from (left) the top of the board and (right) the bottom of the board. The internal signals of the victim and adjacent lanes are also shown.*

The first observation was that the victim net was routed in a noisy 12V main via-field. The initial assumption was that dominant coupling mechanism was trace-to-via coupling and that the noise observed on the victim PCIe differential pair was from routing the victim net through the 12V main feed via-field.

2.3 Identifying the Noise Coupling Aggressor

Before continuing with steps to isolate the 12V main vias from the trace, it was important to correlate the current (aggressor noise) on the 12V main vias to the switching of the converter. To establish that the noise coupling was a result of the current dI/dt and voltage dV/dt transients of the power FET switching, a new set of measurements was taken to isolate the coupling noise from the converter.

In these measurements, the converter was the only active component on the board. As there were no processors installed, no SerDes signals were running on the nearby traces. 12V was delivered to the board by means of an external power supply. In these measurements the converter was not supplying a load. The switching regulator was turned on and controlled by means of a digital interface. Oscilloscope ports were attached to the P and N legs of the victim lane (by means of the CLB), the switch-node of the regulator, and the 12V input. The victim net was terminated with 50 ohms on the other end on each phase to match its characteristic impedance. A view of the measurement setup can be seen in *Figure 5* below.

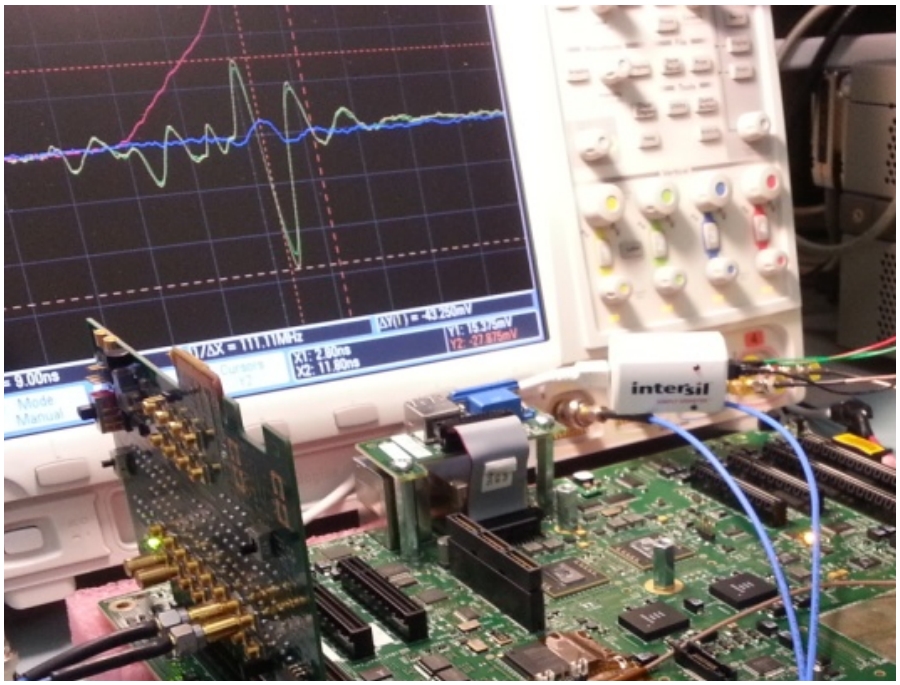

Figure 5: *Measurement setup when isolating switching converter noise.*

The measurement results show that the noise coupling on the victim lane occurs during the switching edges of the switch-node, and the bigger disturbance occurs on the rising edge, when the top-side FET turns on. This can be seen in *Figure 6a*. The frequency of ringing is observed to be 110 MHz.

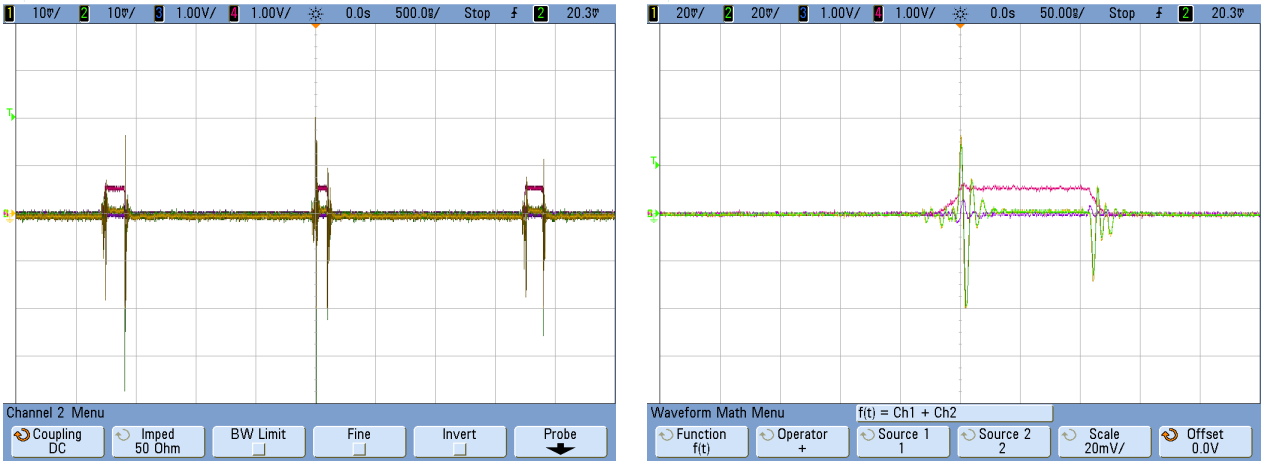

Figure 6a: *Time-domain measurements of victim lane showing both the signal around the rising and falling edges of the converter's switch-node voltage.*

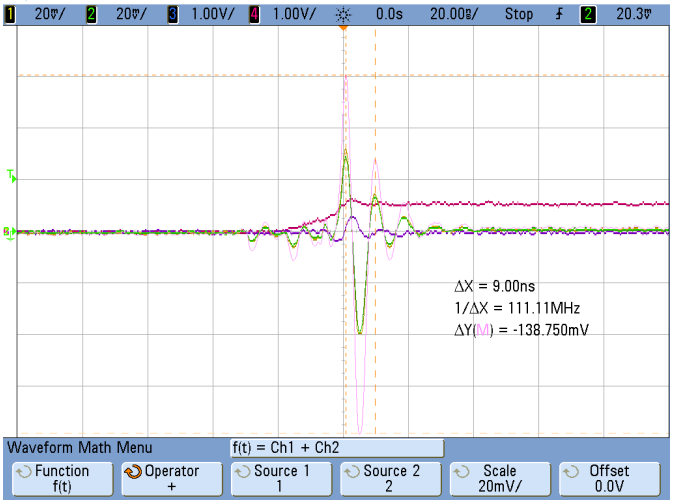

Figure 6b: *Time-domain measurements of victim lane captured on rising edge of converter switching. Channel 1(Yellow) – P, Channel 2 (Green) – N,Channel 3 (Purple) – 12V Filter Input,Channel 4 (Magenta) – Switch-node, Pink – Math – Channel 1 (P) + Channel 2 (N).*

The noise coupling aggressor was now believed to be the current transient in the 12V main vias during the switching of the converter, when the top FET turned on.

3. Debugging a Solution

3.1 Solution and Proposed Fix

Working under the assumption that the coupling mechanism was trace-to-via that occurred during the switching of the converter, several layout re-works were implemented in the lab to reduce the coupling and formulate a solution.

Condition	**Common-Mode Noise (mV)**
No Change	75.0
Isolate 3 Vias (See *Figure 7*)	62.2
Isolate 6 Vias	53.0
Isolate 3 Vias and Add 1 uF Cap on 12V Input	34.84
Isolate 3 Vias and Add 1 uF Cap on 12V Main	40.42
Remove Fuse and Bypass 12V Main Vias	3.07

Table 1*: Layout changes and resulting common-mode peak-peak noise measured on victim lane.*

Table 1 describes the layout re-works applied and the resulting maximum peak-peak common-mode noise measured on the victim differential pair with an oscilloscope.

As described in the *Table 1* above, removing the column of 12V vias closest to the transition vias was attempted. This re-work can be seen in *Figure 7* below.

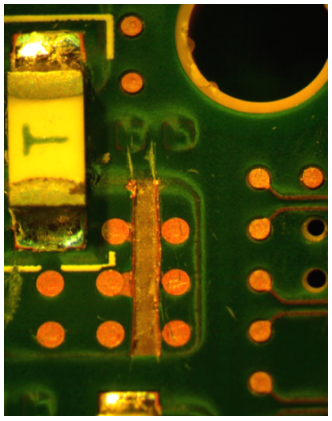

Figure 7: *Disconnecting 3 right-most vias closest to PCIe transition vias.*

As can be seen in *Table 1*, bypassing the 12V main vias eliminated almost all of the noise on the victim lane. In this re-work, the fuse was removed, and 12V to the converter input was connected from a far away 12V source. This avoided current circulation in 12V main vias closest to the PCIe differential trace. This re-work can be visualized in *Figure 8*.

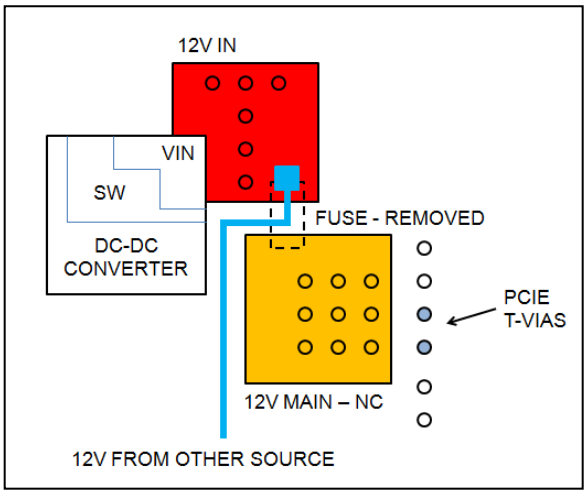

Figure 8: *Re-work block diagram. Fuse is disconnected, and 12V is provided to input of DC-DC converter by means of another far away 12V source. 12V main is not connected and current is not circulated through the 12V main vias.*

The fuse re-work yielded a clean, compliant eye, and no failures on the victim lane. It appeared that problem had been solved, and there was proof that no coupling occurred when current was not circulating in the 12V main vias. In the next spin of the board, this revision was added such that the traces were routed far away from the 12V main vias, and five unnecessary 12V main vias were removed. The re-spin can be seen in *Figure 9*.

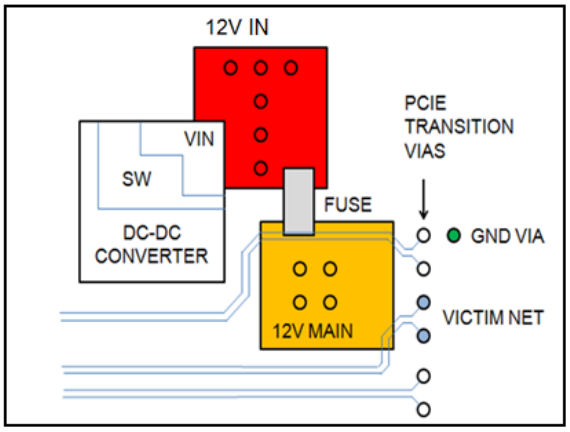

Figure 9: *Re-spin such that PCIe differential signals are routed far away from 12V main vias.*

Even with a proposed solution, some questions remained unanswered. Why was the frequency of ringing 110 MHz? Why had one net and not the neighboring nets been affected? These questions will be analyzed in detail later.

3.2 Crosstalk Measurements

To validate that the re-spin had successfully removed the common-mode crosstalk, ***S***-parameter measurements were taken on the original board and the first revision of the board. These ***S***-parameter measurements were taken in order to quantify the crosstalk improvement resulting from the re-spin of the problem area.

The crosstalk was measured from the input to the regulator to the victim vias. A Vector Network Analyzer (VNA) was used to measure the crosstalk of the passive network in the frequency domain [6]. As shown in *Figure 10*, port 1 of the VNA had a hand-held 50-ohm coaxial probe, and its pins touched down on the power input and ground pins of the DC-DC converter.

The 2 port ***S***-parameter measurements were taken on a bare board. Crosstalk on one leg of the victim differential pair was measured at a time. When one leg was measured, the

other leg was terminated with 50 ohms on both ends. One port was attached to the input pad to the regulator and the other port was attached to the via of the victim lane. *Figure 10* shows the location of the ports for the ***S***-parameter measurements.

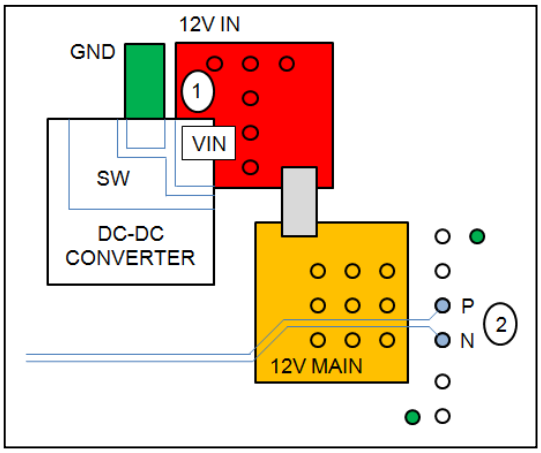

Figure 10: *Port location for **S**-parameter measurements. Port 1 is placed on the top pad of the 12V input to the regulator. Port 2 is placed on the victim PCIe transition via.*

The crosstalk measurement results in *Figure 11* show only a 10% improvement in crosstalk magnitude after the first revision of the board, which implies the coupling mechanism was not completely removed by the applied layout changes.

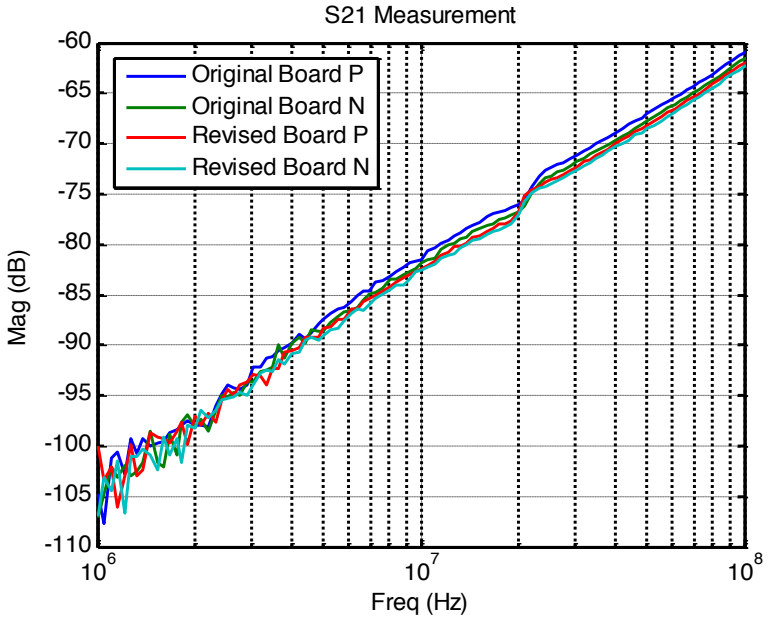

Figure 11a: *Crosstalk measurements taken on the original and the revised board between the 12V input to the regulator and the victim PCIe transition vias. from 1 to100 MHz.*

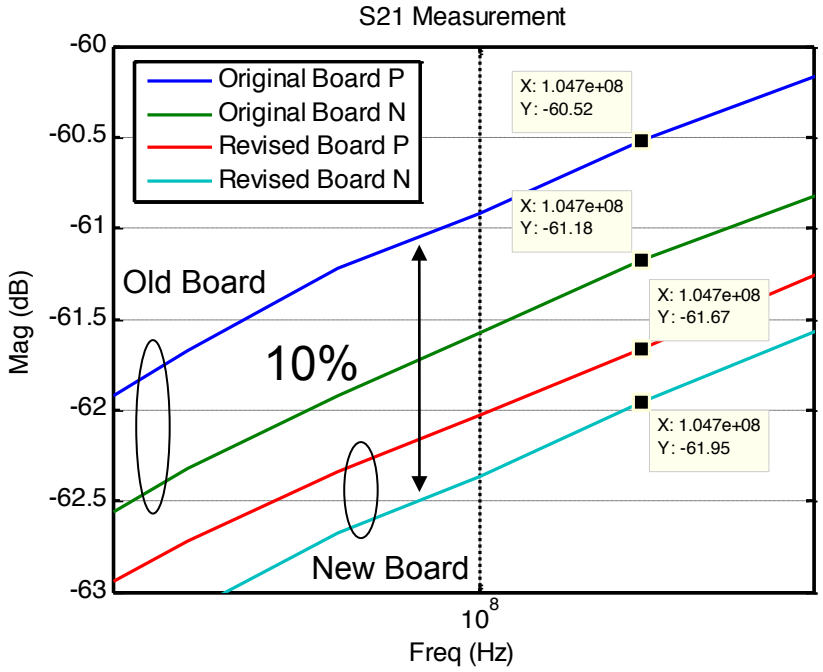

Figure 11b: *Crosstalk measurements taken on the original and the revised board between the 12V input to the regulator and the victim PCIe transition vias. Close-up around 100 MHz.*

At this point, it was necessary to reflect. The lab re-works suggested that the coupling was trace-to-via. The locality of the problem also supported this assumption. When the 12V circuit was bypassed (removing current from the assumed aggressor vias) the problem completely went away.

This illustrates that at mid-frequencies, the fields can easily expand without much attenuation to larger parts of the board, and the real aggressor can be farther away from the victim than was thought.

To try to further understand the issue, several simulations were devised to back up the experimental findings.

3.3 Simulations

A simulation to quantify the magnitude of coupling between the signal traces and the 12V main vias was conducted using a 3D field solver. In the simulation setup, as can be seen in *Figure 12*, differential traces are routed in between vias that are connected on an

internal and external layer. This setup is intended to mimic the differential PCIe traces routed through the 12V field of the actual layout.

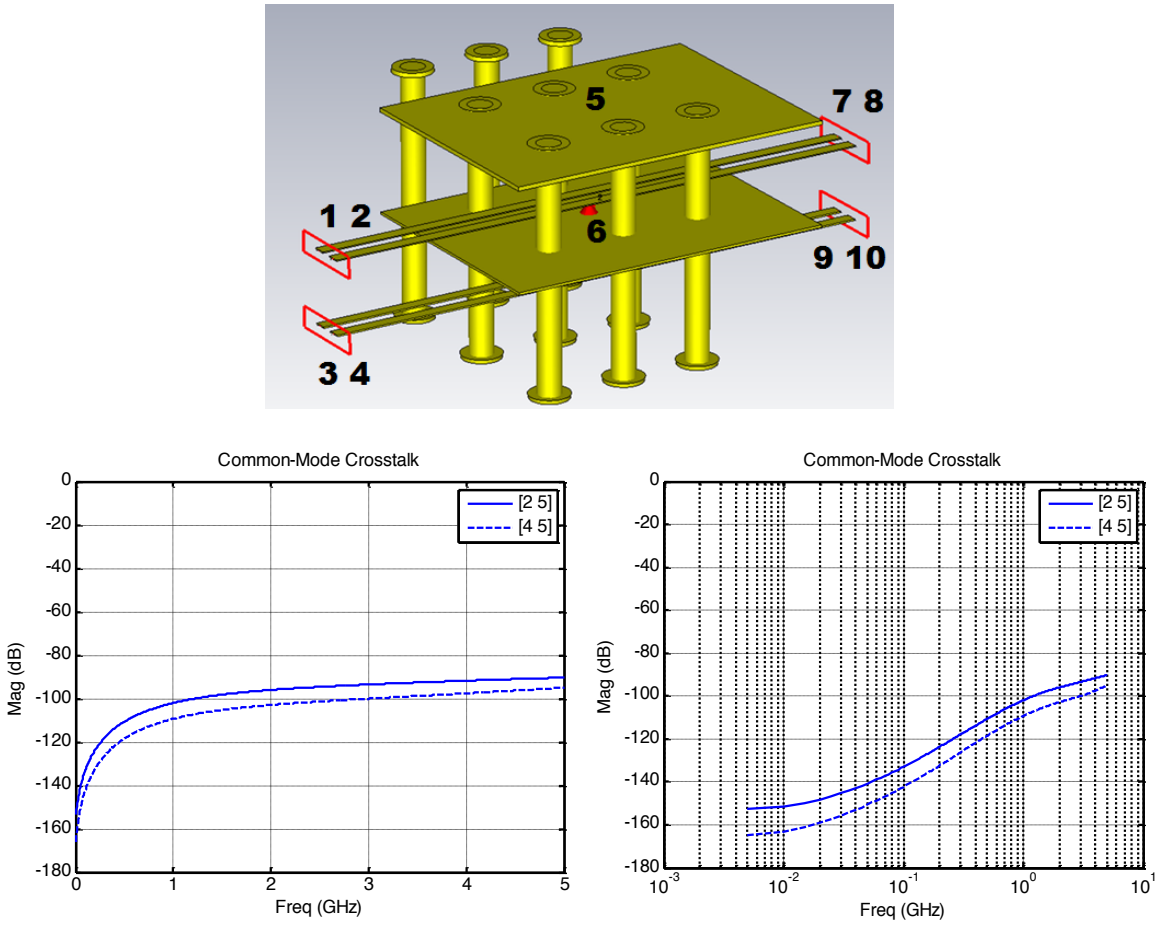

Figure 12: *(Top) View of 3D field solver simulation setup. Port placement and numbering is denoted. (Bottom) Simulated common-mode crosstalk between differential traces and vias connected together by an external plane. (Left) Linear horizontal scale. (Right) Logarithmic horizontal scale.*

Figure 12 shows the simulated trace-to-via common-mode crosstalk from DC to 5 GHz. Contrary to the former assumption, the simulation results show that perpendicular trace-to-via crosstalk is much less than what would cause the level of interference that was measured on the trace, and as such, cannot be the source of coupling. The coupling mechanism is not capacitive (trace-to-via) but must instead be magnetic (via-to-via) associated with mutual inductance.

3.4 Different Types of Coupling

The classic signal integrity crosstalk scenario is two uniform parallel traces in homogeneous (stripline) or nonhomogeneous (microstrip) medium, and the starting point for the discussion usually assumes matched traces. This results in a uniform coupling along the traces simultaneously by the mutual capacitance and mutual inductance. Even in typical nonhomogeneous cases, the relative capacitive and magnetic coupling strengths are close in magnitude. This changes when the structure becomes different and highly mismatched. For instance, when the agressor circuit is very low impedance compared to the impedance of the victim trace, the inductive portion of the coupling will dominate. This is the typical case at mid-frequencies from power structures, which have an impedance much lower than the typical trace impedance. If an inductance is identified in the victim circuit across which the resulting noise voltage is calculated, the classic ground bounce formula applies:

$$\Delta V = L\frac{di}{dt}$$

In contrast, if the source tends to be high impedance, such as an inductive loop at high frequencies or an electrically short monopole stub, the electric field coupling will dominate resulting from the mutual capacitance (c_m) between the agressor and the victim. In the time domain, the crosstalk coupled onto the victim may be simplified to [7]:

$$I_{vic} = c_m \frac{dV_{agr}}{dt}$$

3.5 Larger Plane Simulation (Inductive Coupling)

After understanding that the coupling mechanism must be magnetic, a larger scale simulation, not suitable for a 3D field solver, was set up to simulate the noise coupling. A hybrid field solver, which was able to simulate a large portion of the board, was used to simulate the amount of current coupled to the victim vias (in different layout scenarios) from an AC source set up in the location of the regulator. It should be noted that absolute accuracy was not sought in these simulations; the simulations results, relative to one another, were used to uncover a trend and the main coupling mechanism.

An AC (frequency-domain) current source with constant amplitude (17A) was setup at the 12V input vias of the DC-DC converter to emulate the regulator's current draw. The current induced in the victim vias from the current source was monitored while the simulation frequency was swept from 10 MHz to 500 MHz. The simulation setup can be seen in *Figure 13.*

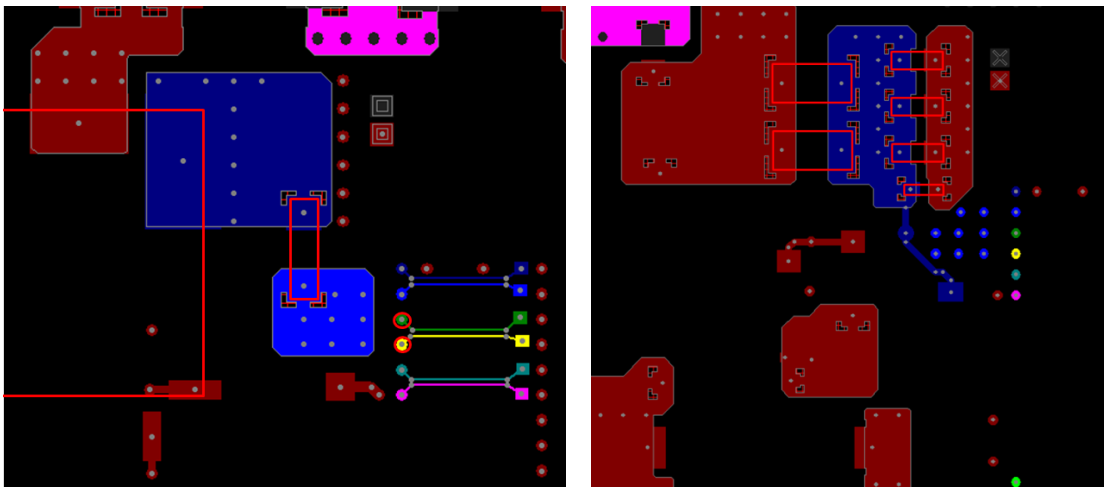

Figure 13: *Simulation setup. (Left) Top layer. Red circles show the victim vias where the current was monitored. (Right) Red rectangles show capacitor placement on bottom layer.*

This simulation was run with a number of layout changes, as can be seen in *Figure 14*.

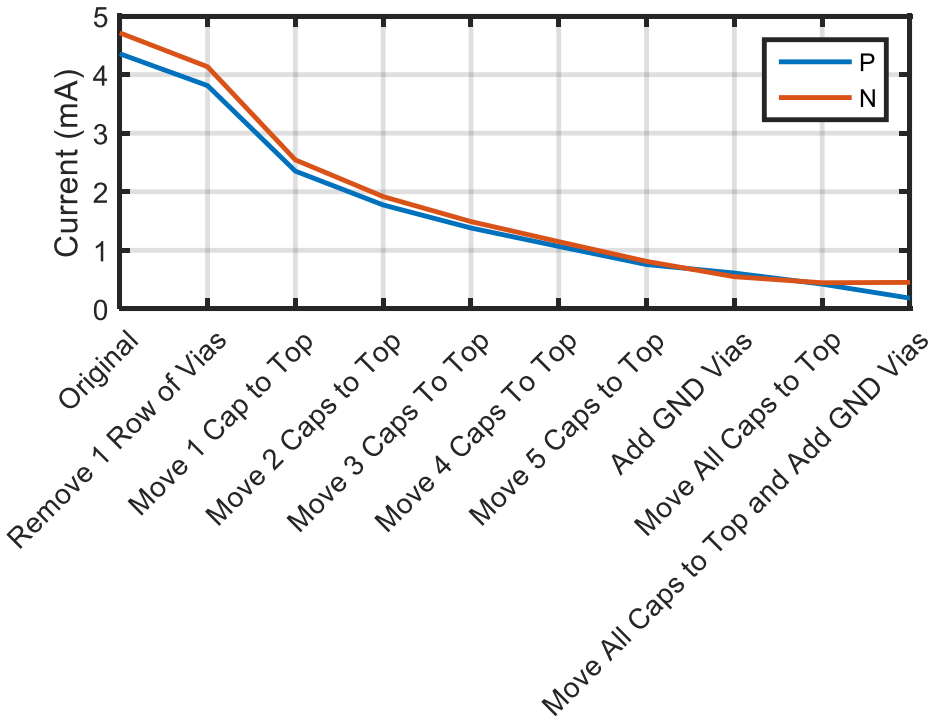

Figure 14: *Current induced in victim vias (P and N legs) in different layout scenarios at resonance frequency of 110 MHz.*

Although the simulation was run from 10 MHz to 500 MHz, *Figure 14* extrapolates the current induced in the victim vias (P and N) at the resonance frequency of 110 MHz.

It can be seen in *Figure 14* that the first data point is the current induced at 110 MHz with the original layout. The next data point shows the reduction in current resulting from removing one column of the 12V vias. This was one of the original lab re-works. This simulation result corroborates previous measurements that show removing only a fraction of the 12V vias does not result in a large change in noise coupled onto the victim vias.

The real reduction in noise coupling happens when the decoupling capacitors across the DC-DC converter input are moved from the bottom of the board to the top of the board. Placing the decoupling capacitors on the bottom of the board creates a physical loop for the high dI/dt input current. This loop is the aggressor noise source, and moving the capacitors to the top of the board effectively eliminates the aggressor noise loop with high dI/dt.

The noise from the magnetic coupling between the aggressor and the victim is determined by four factors: the size of aggressor loop, the size of victim loop, the distance between the loops, and the relative orientation of the loops. This is illustrated in *Figure 15*.

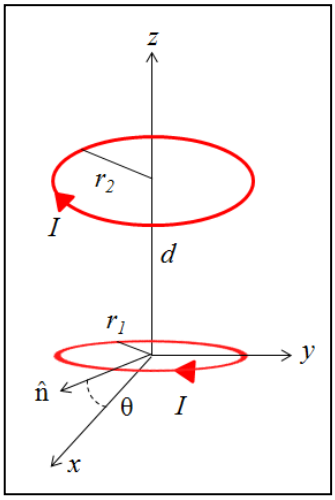

Figure 15: *Visualization of coupling parameters between magnetic loops. Assume the loops are circular for simplification. The four parameters are: size of the aggressor and victim loop (r_1 and r_2), the distance between the two loops (d), and the relative orientation of the loops (θ).*

It is important to note that adding shielding ground vias adjacent to the victim vias also reduces the noise coupled onto the victim vias. The ground vias reduce the size of the victim loop; they may also change the orientation of the victim loop. It is important to

note that this PCB had multiple ground planes to absorb the ground return current from the magnetic coupling. Ground shielding vias in a stackup with a single ground plane may not offer adequate shielding without additional ground planes.

A 3D view of the layout and current loops can be seen in *Figure 16*.

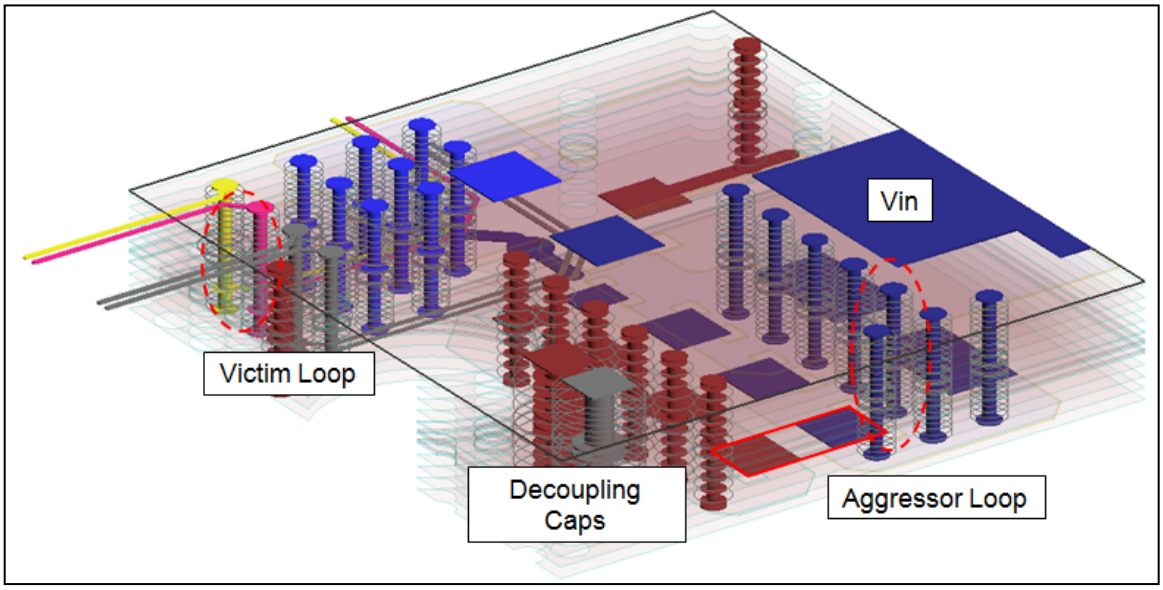

Figure 16: *3D view of layout showing aggressor and victim current loops.*

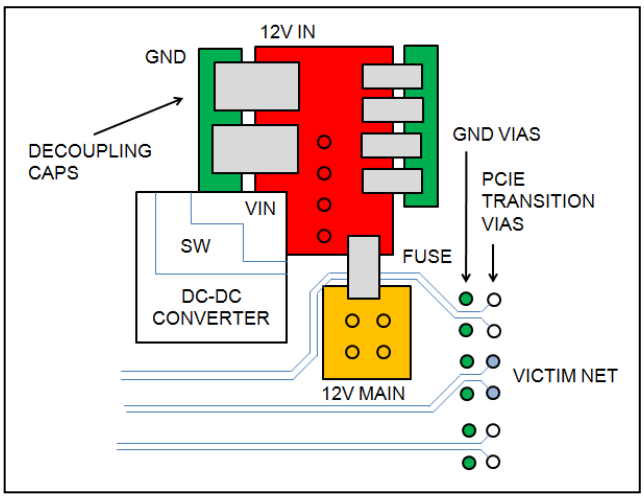

Figure 17: *Final layout of problem area as seen from the top of the board. Decoupling capacitors are placed the top of the board, and the victim PCIe transition vias are shielded by ground vias.*

Eventually all decoupling capacitors were moved to the top of the board, and adequate ground shielding vias were placed next to the PCIe transition vias on the next spin of the board. This can be seen in *Figure 17*.

3.6 Proof

Follow-up crosstalk measurements were made on the final revision of the board and compared to the earlier crosstalk measurements. The measurement results are shown in *Figure 18*.

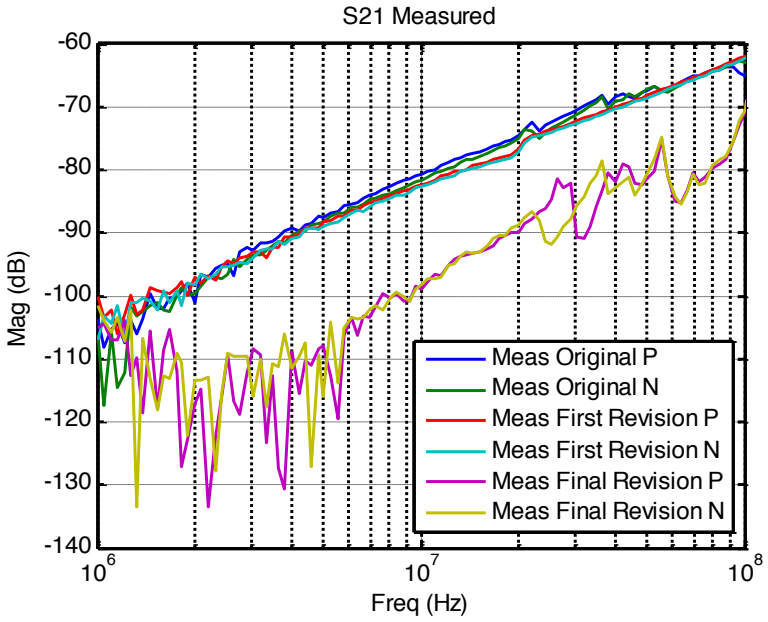

Figure 18: *Measured S21 on original board, first revision of board, and final revision of board.*

Crosstalk measurements on all the board revisions show that the final revision of the board has a considerable reduction in crosstalk between the 12V input to the regulator and the PCIe victim vias.

The system was then set to run with the final board, and an eye contour measurement of the victim lane was taken (as described earlier). The resulting eye diagram yielded a clean, compliant eye as can be seen in *Figure 19*.

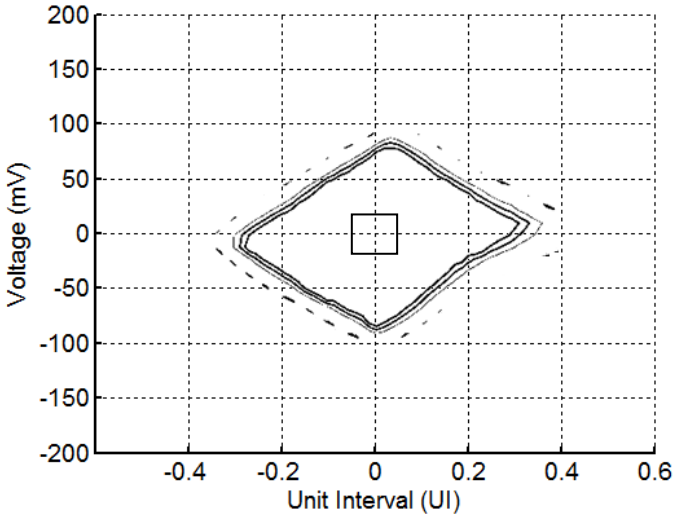

Figure 19: *Eye contour map of victim lane after final fix.*

Both the ***S***-Parameter crosstalk measurements and eye contour map show that by moving the decoupling capacitors to the same side of the board as the regulator and adding sufficient ground shielding vias near the victim, the noise coupling is effectively removed.

3.7 Understanding the Noise Source

After resolving the noise coupling in the design, it was important to understand the cause of the resonance waveform that was coupled onto the victim net. A SPICE model was created to simulate the parasitic ringing on the switching waveform. This model included elements of the user board as well as an accurate model of the FETs, including parasitic elements. This model was correlated to a measurement taken at the switch-node on an oscilloscope with the regulator drawing full DC load on the actual board. In this measurement, the regulator was the only active component on the board; all other supply rails were disabled.

The SPICE model included separate models for the upper and lower FETs provided by the vendor. The detailed FET models included parasitic inductances. Junction capacitances were modeled as non-linear voltage-dependent capacitances. Other parasitic components were also included, such as package inductances and parasitic elements of the simplified input and output capacitor banks.

Figure 20 shows the simplified SPICE model of the step-down switching regulator.

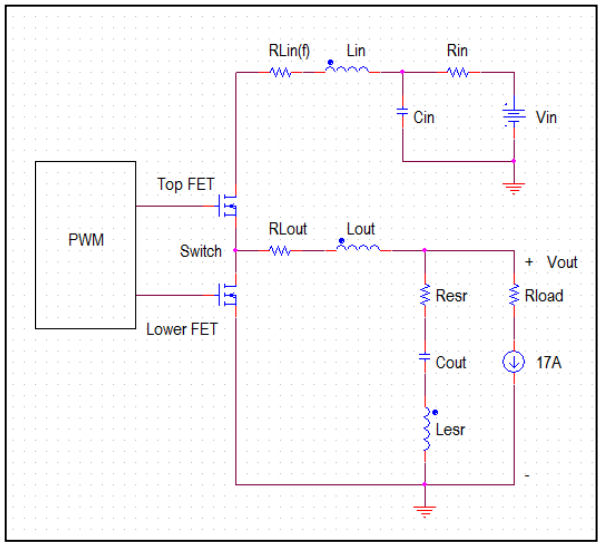

Figure 20: *Simplified SPICE model to emulate noise coupling. The model includes parasitic and external components of the layout.*

Apart from the FET models, key elements of the system board were also modeled. R_{in} represents the plane resistance connecting the V_{in} source up to the C_{in} input capacitor. C_{in} represents the input decoupling capacitors. The C_{out} output capacitor is a first-order C-R-L network with frequency-independent parameters. The main output inductor L_{out} is represented by a series R-L circuit with a resistor R_{Lout}, which accounts for its dc and ac ohmic losses.

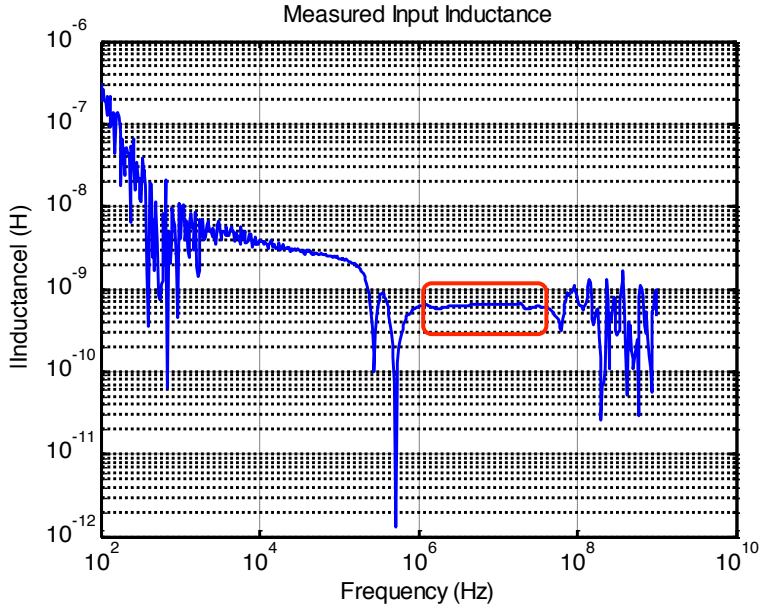

Figure 21a: *L_{in} inductance extracted from the imaginary part of the impedance measured at the input pin of the DC-DC converter.*

L_{in} accounts for the inductance of the supply rail seen at the converter input. R_{Lin} represents the real part of impedance associated with L_{in}. An ***S***-Parameter measurement was taken at the converter input, from which the values of the input inductance and real impedance could be extracted. This can be seen in *Figure 21*.

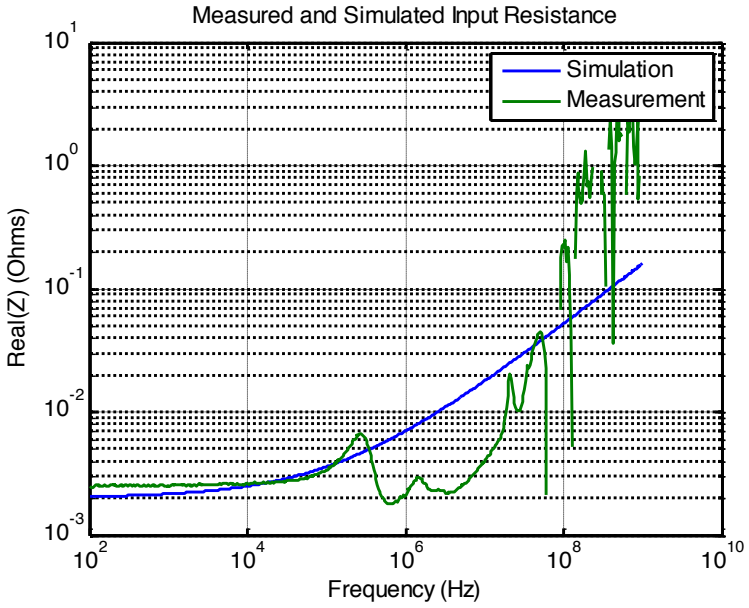

Figure 21b: *R_{Lin} real impedance measured at the input of regulator. Curve is fitted for frequency-dependent resistance.*

Figure 21a shows a frequency-domain measurement of the magnitude of inductance at the input of the regulator. This measurement was taken with a 3 GHz vector network analyzer. In the frequency range of interest, a frequency-independent value of 0.6nH for L_{in} can be extrapolated for simplification. In order to achieve a close damping factor, it was necessary to account for the frequency-dependent resistance associated with the input impedance. *Figure 21b* shows the measured input real impedance alongside a fitted curve to model for the SPICE simulation. This curve is modeled as:

$$R_{Lin}(f) = R_{dc} + R_{ac}\sqrt{f}$$

It then follows that the source impedance can be modeled as:

$$Z_{Lin}(f) = R_{dc} + R_{ac}\sqrt{f} + j2\pi f L_{in}$$

As discussed earlier, a damped ringing with the resonance frequency (110 MHz) was coupled onto the victim trace during the rising edge of the switch-node waveform.

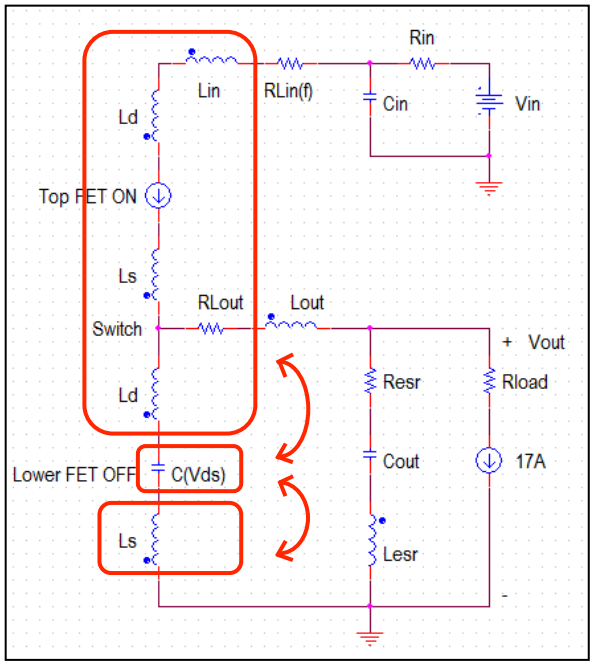

Figure 22: *Simplified equivalent circuit during the rising edge of switch-node waveform, resulting in the parasitic resonance.*

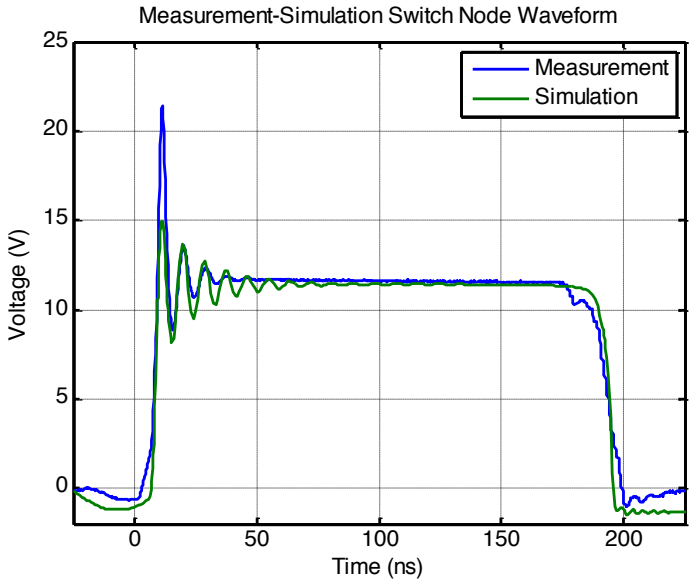

Figure 23: *Correlation between measurement and SPICE model waveform at the switch-node.*

Note that in the particular circuit the ringing associated with the falling edge of the switch-node waveform was much smaller, hence it was ignored. During the on time of the switching cycle, the top-side FET is on, while the low-side FET is off, and therefore its parasitic capacitance is dominant. The frequency of the ringing is a result of the resonance between the inductance of the power path, package inductances and parasitic capacitance of the low-side FET. A simplified circuit is shown in *Figure 22*. The waveform generated from the SPICE model at the switch-node plotted against a real-time measurement is shown in *Figure 23*.

There were a number of variables in the SPICE simulation that were adjusted to achieve a reasonable correlation between the simulation and measurement: rise time, fall time, dead-zone (rising and falling edge gap/overlap), package inductances, and parameters associated with non-ideal inductors and capacitors. The values of such parameters could be estimated, but the precise values were not known. These variables were adjusted until a reasonable correlation was achieved.

Even with a number of unknown variables, a good measurement-simulation correlation of the resonance frequency associated with the rising edge was met. The attenuation of the ringing was able to be modeled reasonably well while accounting for frequency-dependent series resistances. The actual values used in the simulation are shown in *Figure 24*.

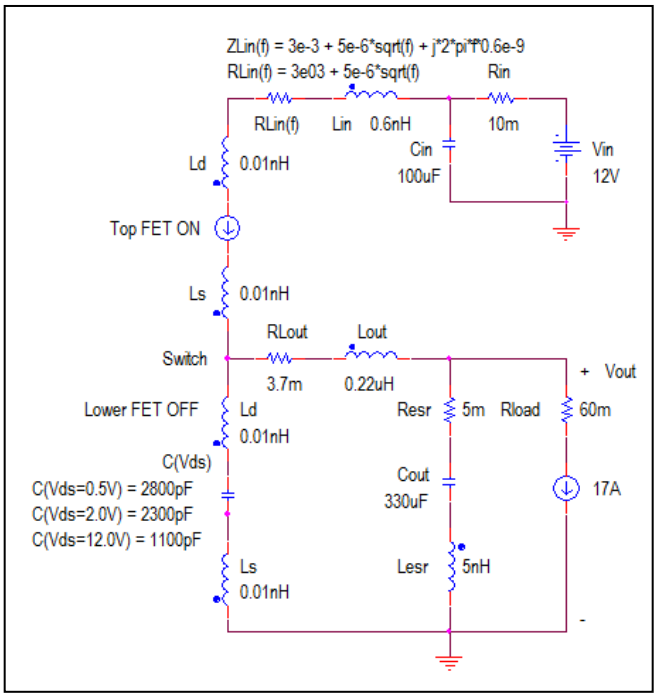

Figure 24: *Simulation model values for correlation.*

4. Conclusions

This case study reviewed a significant finding on how noise produced by the fast switching of a voltage regulator may be coupled onto a nearby signal trace. This noise coupling can seriously degrade signal integrity and, as observed, can cause high-speed lanes to fail. It is important to note that only one specific failure mechanism, the mid-frequency magnetic coupling, was reviewed in this paper.

In this case study, in contrast to capacitive coupling, inductive coupling was dominant in the mid-frequency range. At the 110 MHz resonance frequency, the source of the noise was the fast slew rate and associated high dI/dt of the switch-node waveform. On the rising edge of the switch-node voltage, the resonance frequency is set by the capacitance of the low-side FET and the parasitic inductance of the FETs packages and the inductance of the supply rail feeding the DC-DC converter input.

The aggressor noise loop was created by the decoupling capacitors across the input of the switching regulator. These capacitors were on the bottom side of the board. This created a physical loop from the top of the board (Vin power supply FET voltage) to the bottom of the board for the high current transients. As such, the best way to mitigate the inductive noise coupling is to place most or all of the decoupling capacitors and the switching devices on the same side of the board and/or add ground vias nearby the victim vias; this reduces the source and victim loop sizes dramatically. Adding ground return vias adjacent to high-speed differential pair vias in close proximity to the voltage regulator not only helps impedance control but provides common-mode shielding from such noise coupling. One of the two solutions, if not both, should be adopted when routing signal lines in close proximity to a switching regulator.

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