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Electrical and Thermal Consequences of Non-Flat Impedance Profiles

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SPEAKERS

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He is engaged in the design and characterization of high-speed signal interconnects and power distribution networks for high-performance server systems. He received his Ph.D. in Electrical and Computer Engineering from the Georgia Institute of Technology.

Ethan Koether

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He is currently focusing on system power-distribution network design, measurement, and analysis. He received his master's degree in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology.

SPEAKERS

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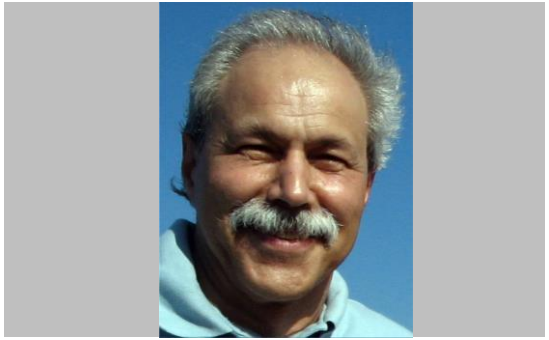

Besides signal integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is a Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies.

Outline

- Electrical and Thermal Impact of Antiresonance:
  - High-Q antiresonance
  - Effect of component tolerance
  - Components at elevated temperature
- Impedance Flatness and Worst-Case Transient Noise:
  - Target impedance and the reverse pulse technique
  - Obtaining the PDN step response
  - Getting the worst-case transient response
- Conclusions

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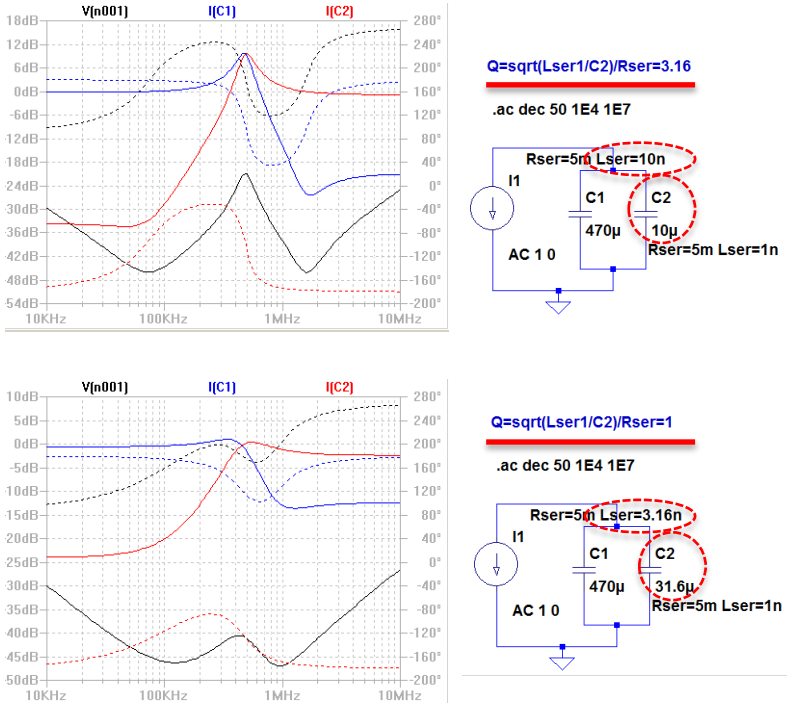
High-Q Antiresonance

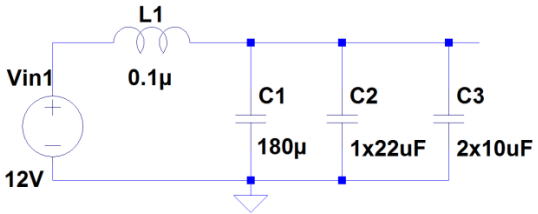
- We want to avoid high-Q antiresonances in any power distribution network
- What causes high-Q antiresonance?
  - Opposite-signed reactances of any component or structure
  - Ex1) Capacitor bank: Z_0 (=sqrt(L/C)) > ESR → antiresonance
  - Ex2) Band limitation of DC-DC converter control loops
  - Ex3) PCB plane modal resonance
- Component reactance may change because of
  - AC, DC bias
  - Temperature
  - Initial tolerance, aging



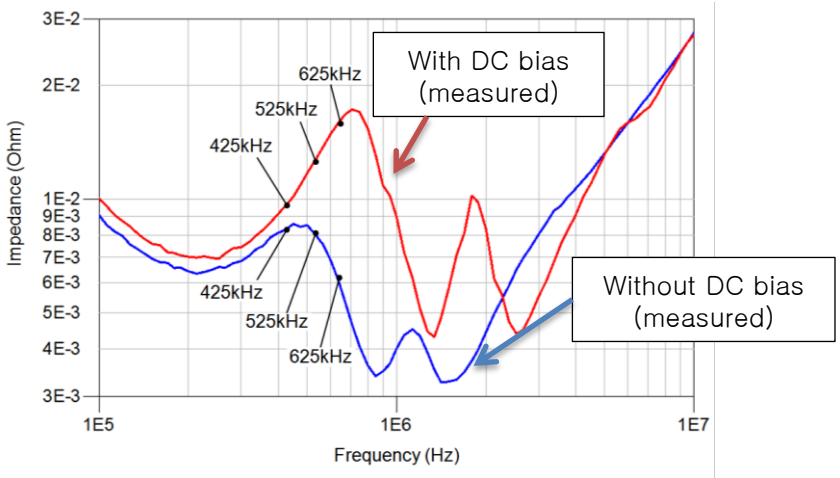
Current multiplication due to high-Q antiresonance can cause additional temperature rise in each capacitor

Impact of DC Bias on Antiresonance

- Ferromagnetic and ferroelectric materials used in filter components:
  - ➢ Need to consider DC bias and temperature
- Even under a normal operating condition, the antiresonance peaks can become noticeably high



Input filter of a DC–DC buck converter



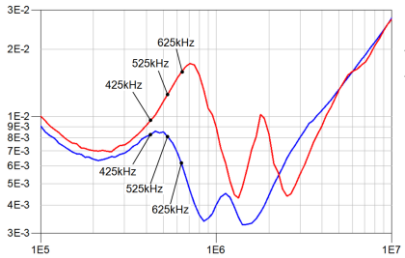
Drop significantly due to DC bias

DC Bias	Cc1	Lc1	Rc1	Cc2	Lc2	Rc2	Cc3	Lc3	Rc3
0V	167uF	2.7nH	7mOhm	15.16uF	2.2nH	4.8mOhm	15.6uF	0.74nH	4mOhm
12V	167uF	2.7nH	7mOhm	7.78uF	1.9nH	4.9mOhm	5.3uF	0.77nH	5mOhm

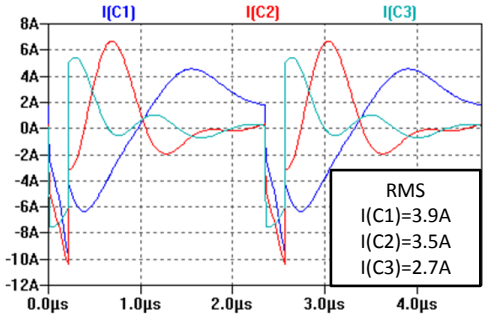
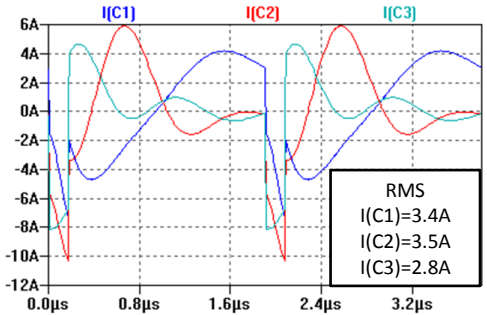
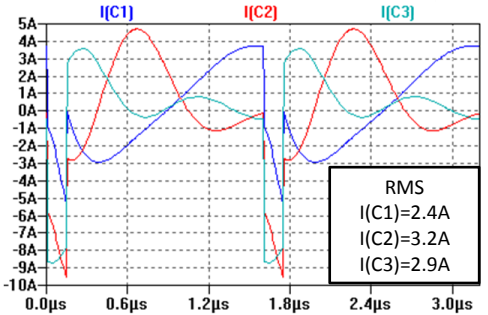
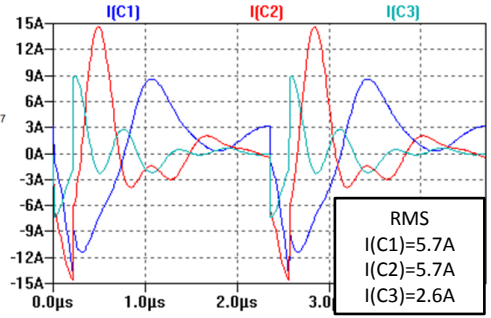
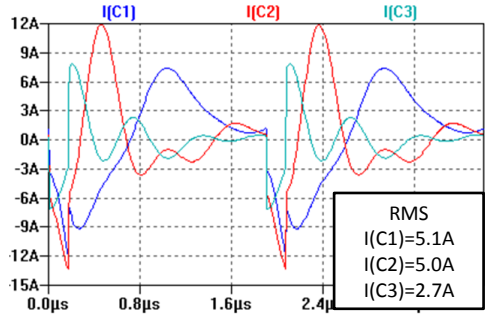
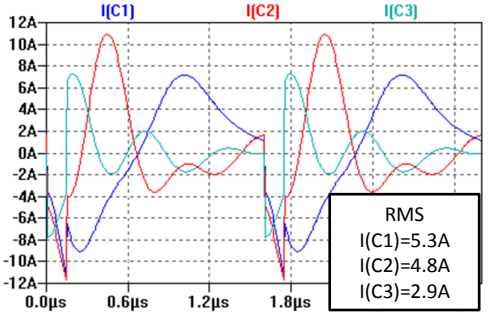
Values fitted to the measured impedance

Simulated Waveforms With and Without DC Bias

No DC bias



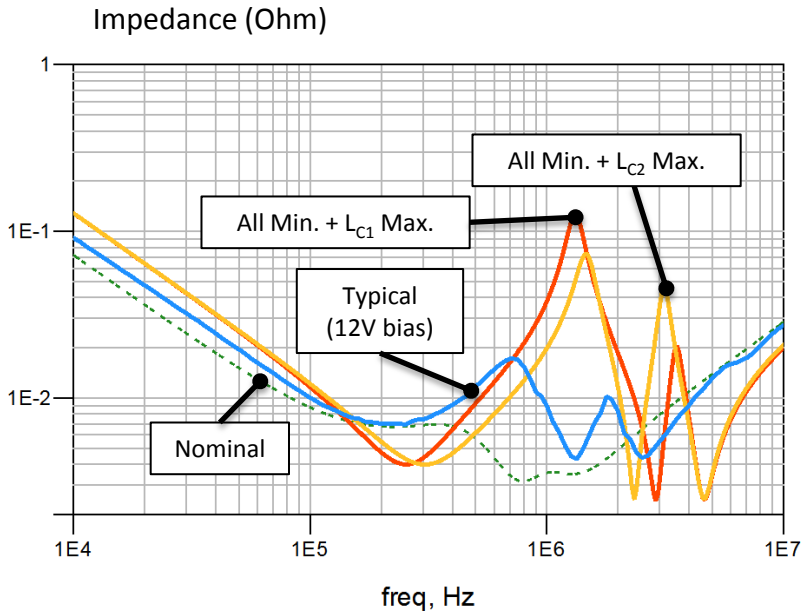
With 12V bias

425kHz	525kHz	625kHz
		
RMS I(C1)=3.9A I(C2)=3.5A I(C3)=2.7A	RMS I(C1)=3.4A I(C2)=3.5A I(C3)=2.8A	RMS I(C1)=2.4A I(C2)=3.2A I(C3)=2.9A
		
RMS I(C1)=5.7A I(C2)=5.7A I(C3)=2.6A	RMS I(C1)=5.1A I(C2)=5.0A I(C3)=2.7A	RMS I(C1)=5.3A I(C2)=4.8A I(C3)=2.9A

*I(C3): current per piece

Component Tolerance Effect

- Considerable spread of actual component values is expected in a volume production
- Capacitance used in large DC bias filter applications usually shows large variations across vendors
- Temperature dependence is specified as only a range
- Statistical impedance profiles including the worst-case can be created from the tolerance table

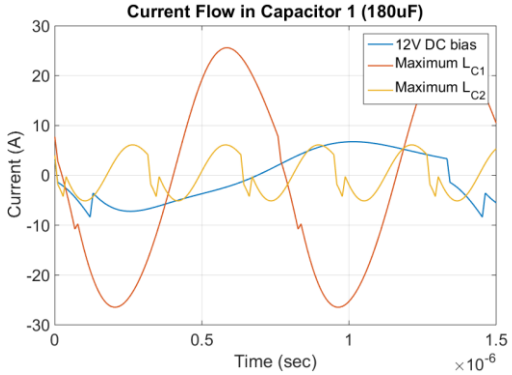


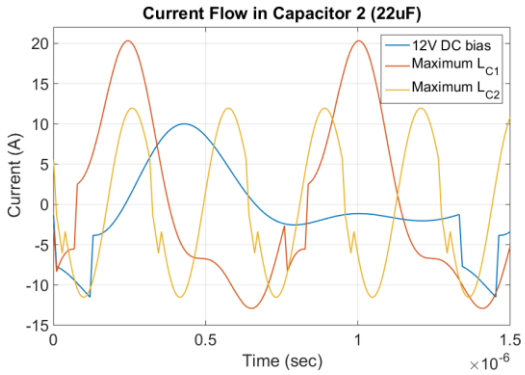
	C_{C1}	L_{C1}	R_{C1}	C_{C2}	L_{C2}	R_{C2}	C_{C3}	L_{C3}	R_{C3}
Min.	120uF	2.2nH	4mOhm	2uF	1.5nH	2.5mOhm	2uF	0.6nH	2.5mOhm
Nominal	180uF	2.7nH	8mOhm	22uF	1.9nH	5mOhm	20uF	0.77nH	5mOhm
Max.	200uF	3.2nH	10mOhm	30uF	2.3nH	10mOhm	30uF	0.93nH	10mOhm

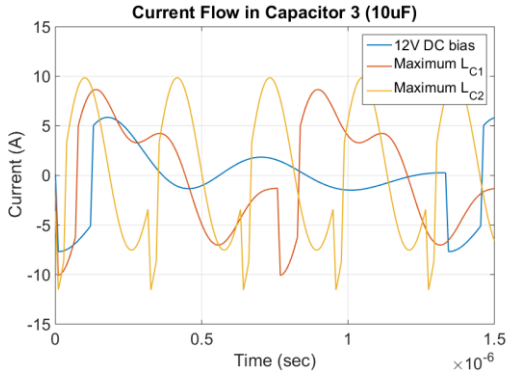
Assumed tolerance range of each component in the DC-DC converter input filter

Simulated Waveforms Considering Component Tolerances

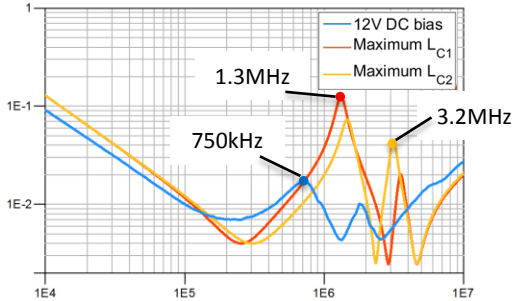
(*I_{C3}: current per piece)



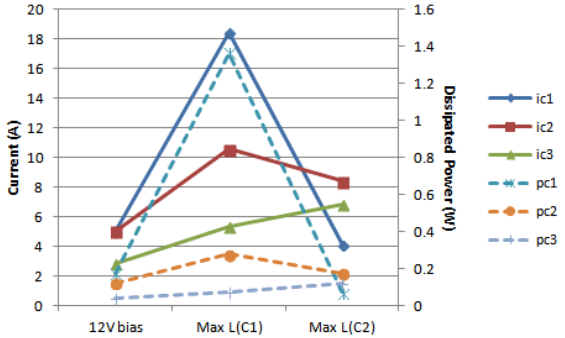




- Switching frequency for each case
  - 12V DC-bias: 750kHz
  - Maximum L_{C1}: 1.32MHz
  - Maximum L_{C2}: 3.16MHz

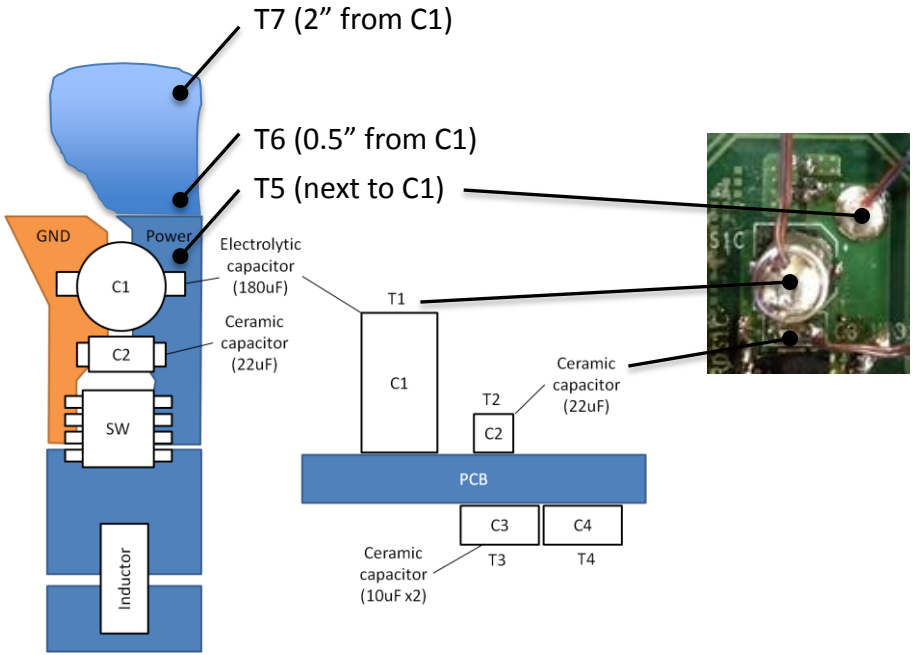


Impedance of tolerance corner cases



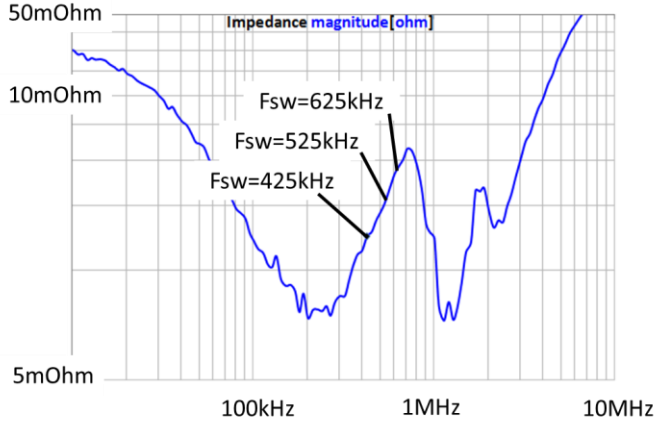
Simulated RMS current and dissipated power in the capacitors

Temperature Rise in Capacitors



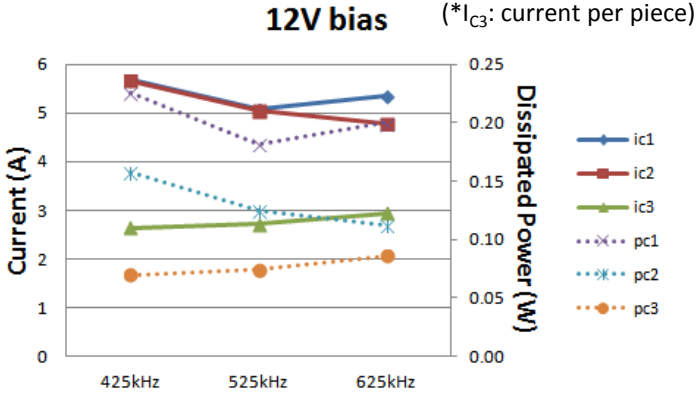
- Will more current dissipation heat up the capacitor more?
- Thermocouplers are attached to the capacitors and PCB as well.
- Temperature was measured after sufficient settling time (> 30min).
- Test setup had no forced air flow.
- PCB was placed horizontally ~0.5" above the bench surface.
- Except for the switching regulator under study, all other circuits were disabled.
- Ambient temperature was 20 degC

Thermal Resistance

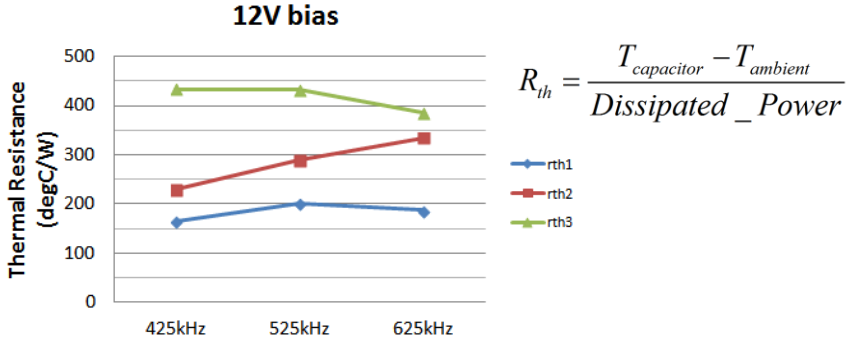


Measured impedance at different switching frequencies

- Thermal resistances were expected to be constant
- Contrary to the expectation, the resulting thermal resistance changes with different switching frequencies. Why?



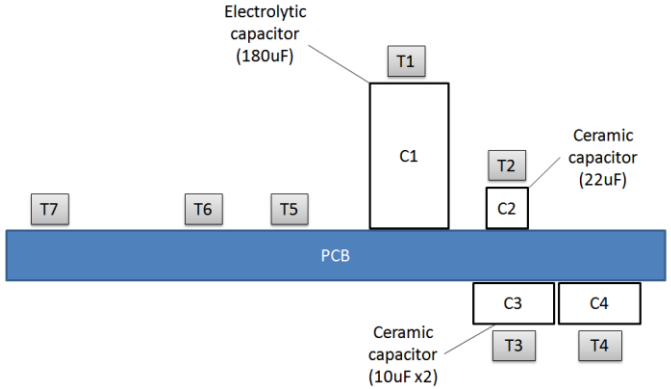
Simulated current and power dissipation in the capacitors

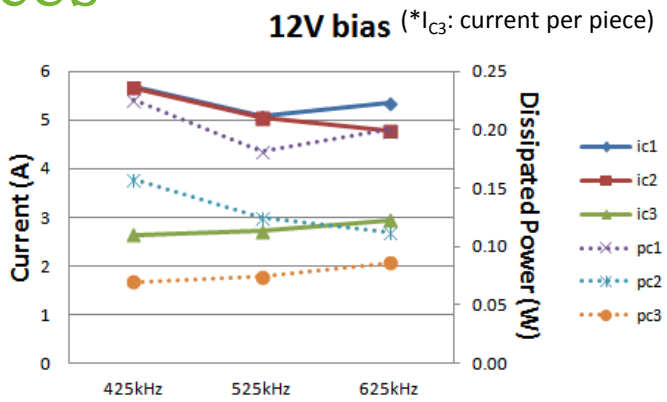


Calculated thermal resistance of each capacitor

Thermal Consequences

Measured temperature (˚C)			
F_{sw}	425 kHz	525 kHz	625 kHz
T1	56.2	55.5	56.3
T2	49.3	51.0	52.2
T3	54.9	54.9	56.5
T4	54.2	53.0	54.5
T5	58.2	58.0	59.9
T6	44.3	44.5	45.5
T7	33.9	34.4	35.6





Simulated current and power dissipation in the capacitors

- All capacitors heat up to 50~55˚C regardless of switching frequencies
  - ➢Heat spreads through PCB
  - ➢Capacitors are not the only heat dissipating components; Loss from the nearby power components dominates (e.g. input filter inductor, FETs, output inductor)
- The ambient temperature needs to account for the local temperature rise caused by the adjacent power components.

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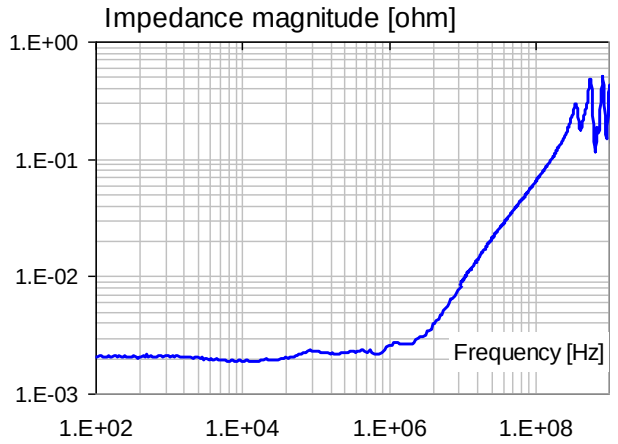
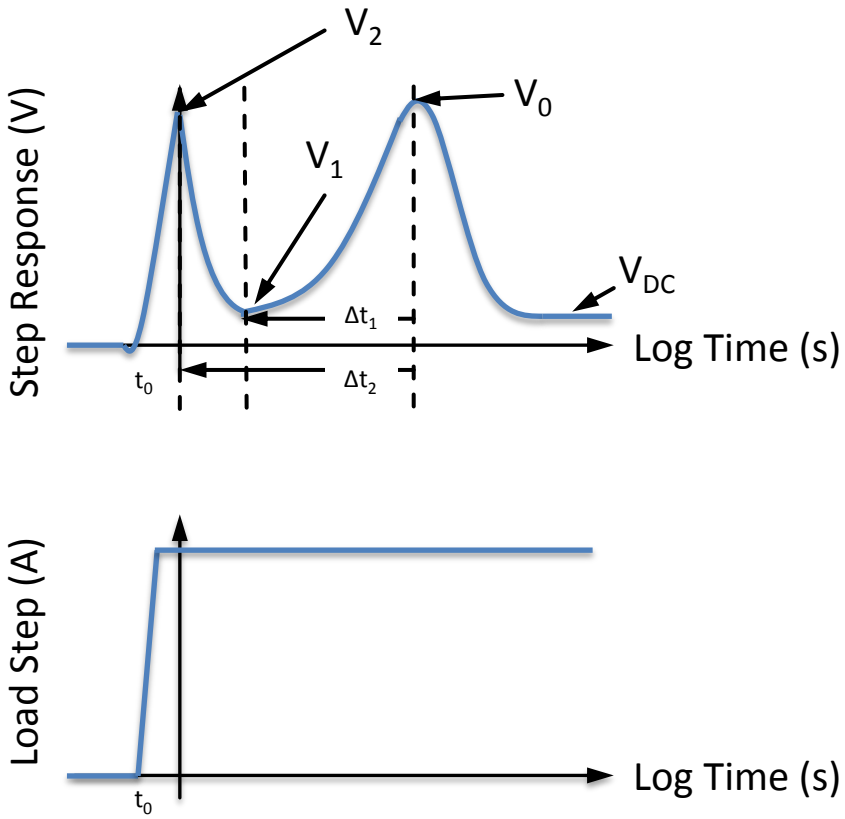
Target Impedance

- Estimates upper bound for rail's impedance
  - Voltage fluctuation on rail: ΔV
  - Maximum current step: ΔI
  - Target Impedance: $Z_{target} = \Delta V / \Delta I$
- Valid for linear and time-invariant PDN
- Approximation unless impedance strictly resistive

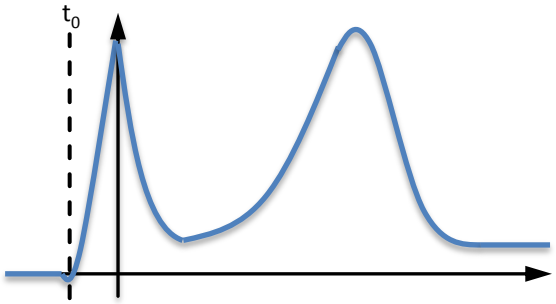


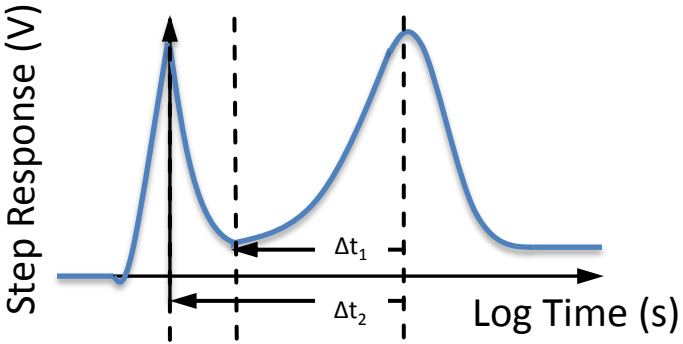
Reverse Pulse Technique (RPT)

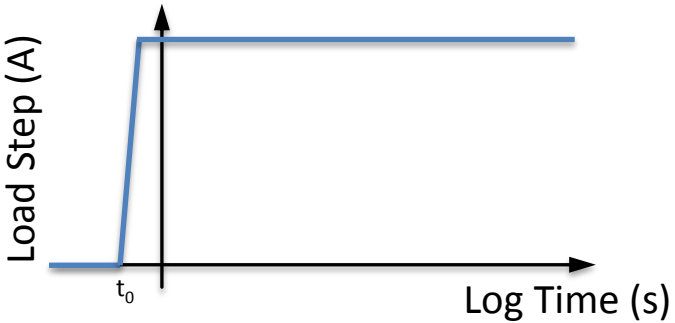
- RPT finds worst case transient response to arbitrary load step



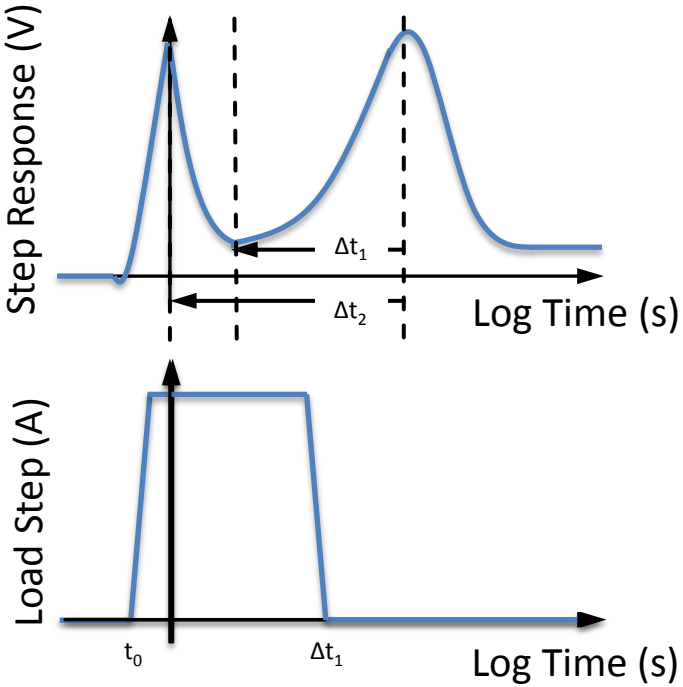
Reverse Pulse Technique (RPT)

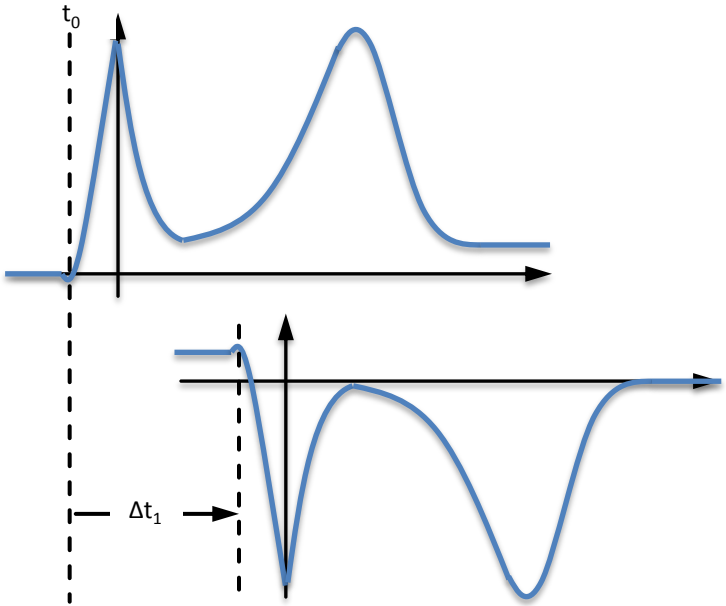






Reverse Pulse Technique (RPT)





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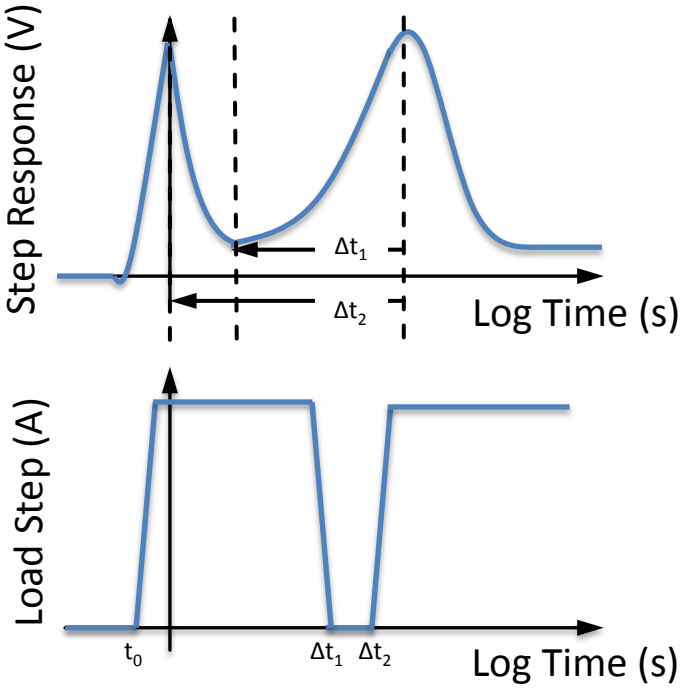

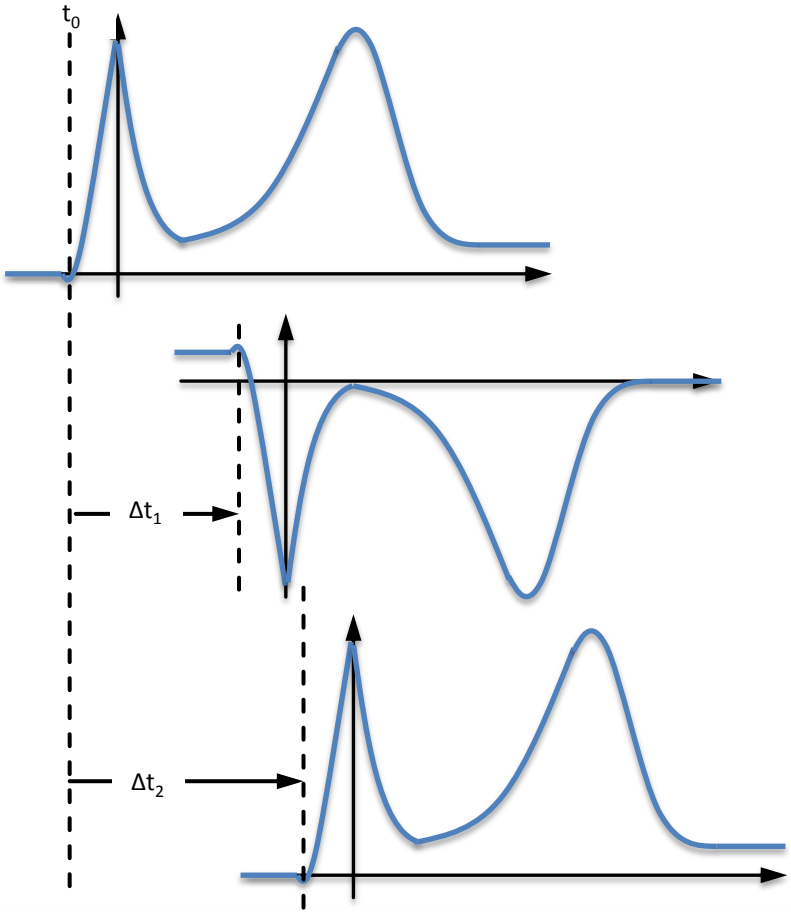

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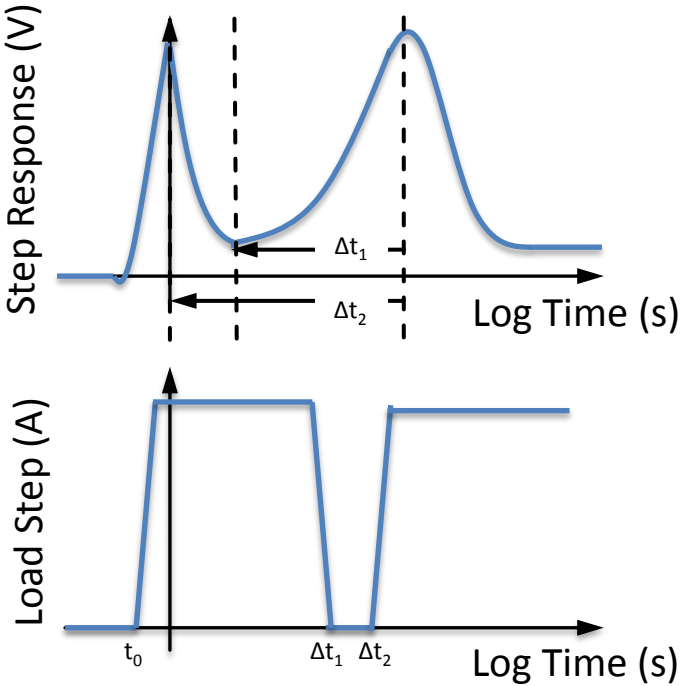
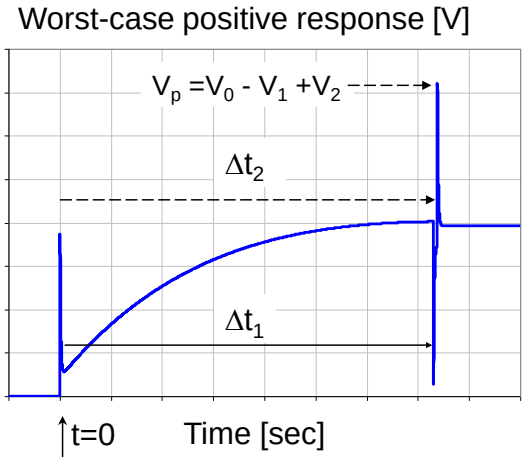
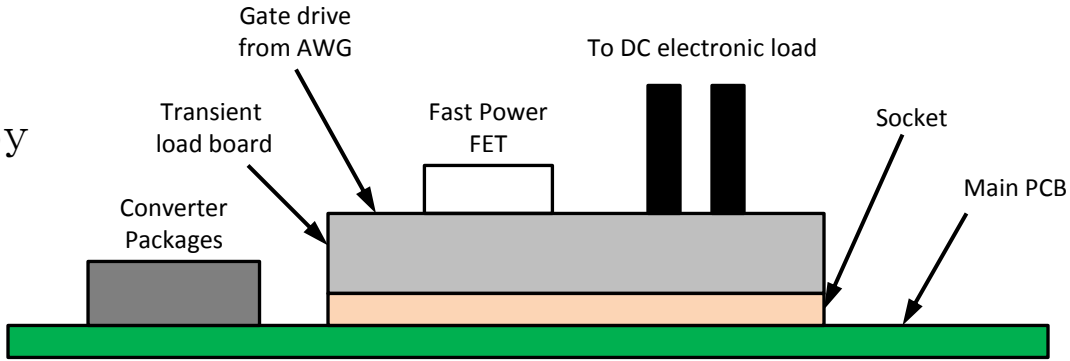




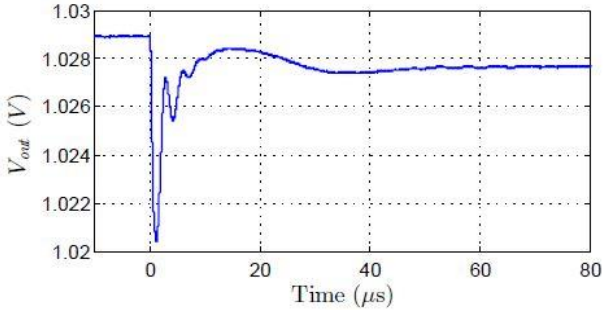
RPT Measurement Setup

- Multiphase DC-DC converter
- Medium-speed high-resolution real-time oscilloscopes from two vendors
- The fast power FET driven by an arbitrary waveform generator and a gate driver circuit
- Two-port shunt-thru measurement with VNA

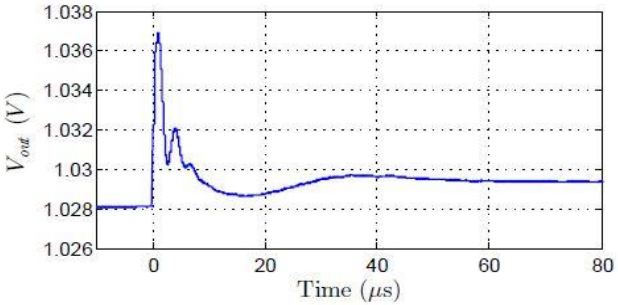


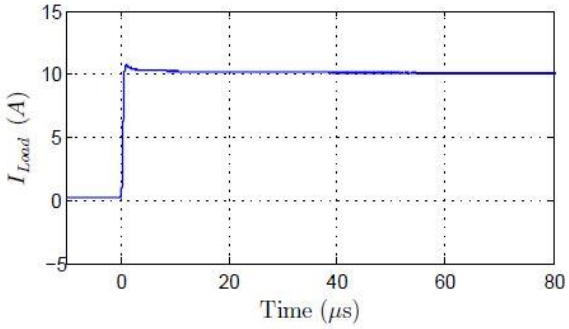
Measured Step Response

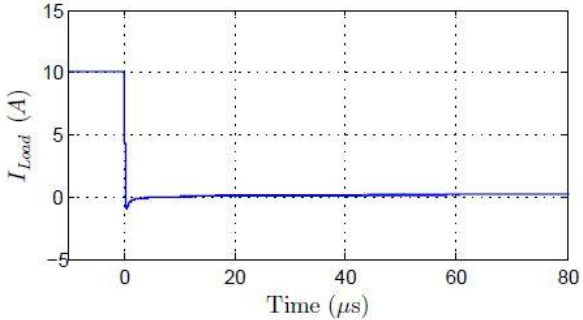
Positive going current



Negative going current

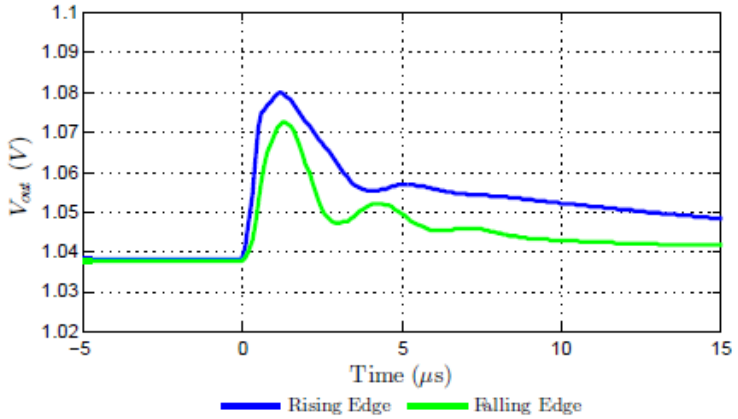


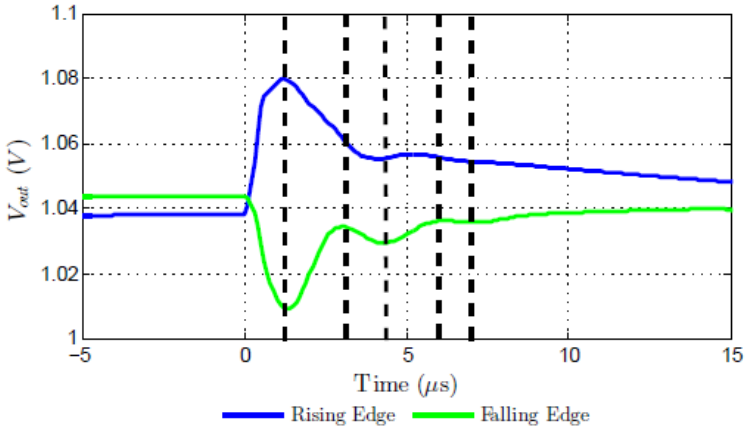




RPT Measurement Pitfalls (1)

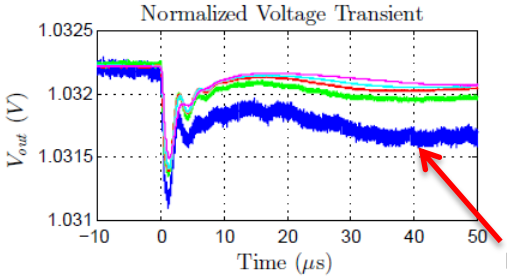
- Response to rising edge and falling edge of excitation step must be symmetric



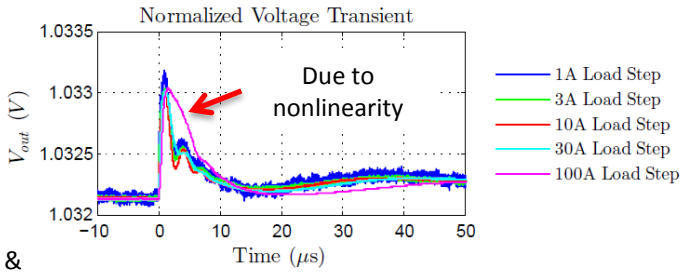


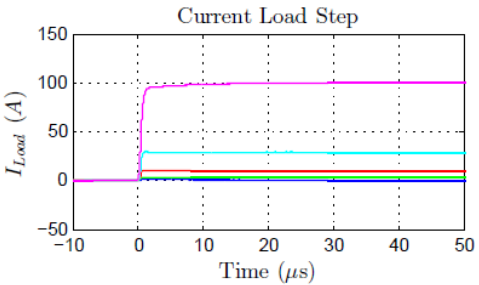
RPT Measurement Pitfalls (2)

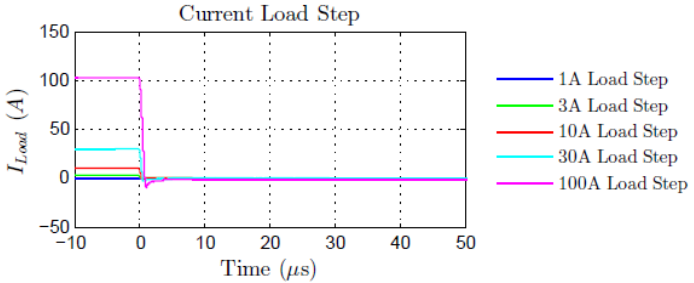
- Non-linearity of response limits application space (for large-signal excitations)
- Noise and thermal drifts may degrade small-signal responses



Due to noise & thermal drifts



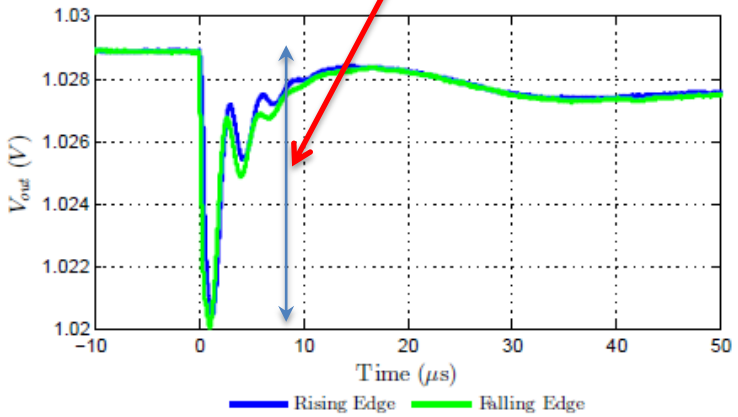




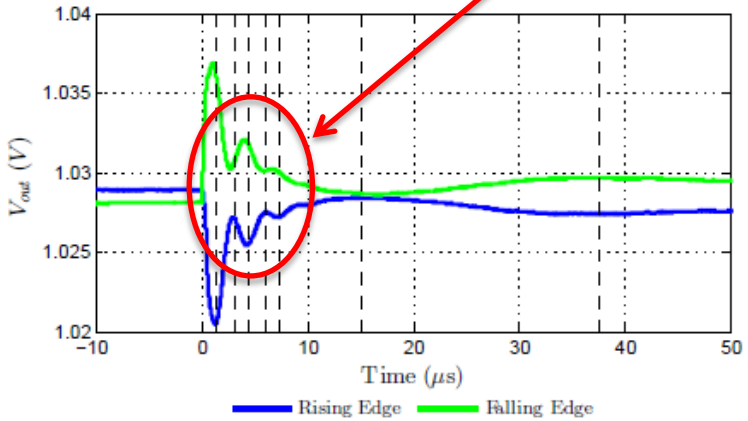
Measurement: Comparison of Edges

- Transient responses corresponding to rising and falling edges of load step compared.

Peak deviation in step response: 9mVp

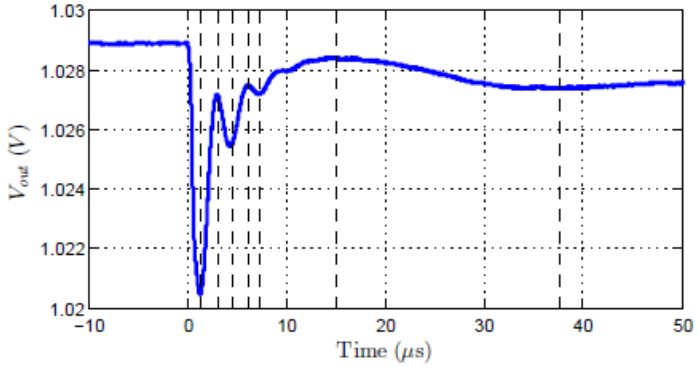


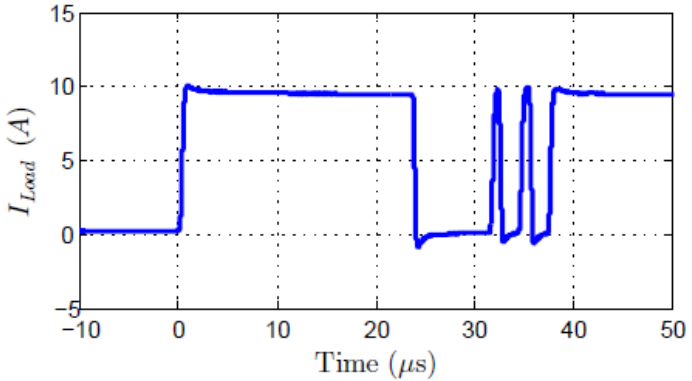
Peaks and valleys line up in time



Measurement: Worst Case Excitation Current

- Peaks and valleys of step response give timing for edges in excitation current



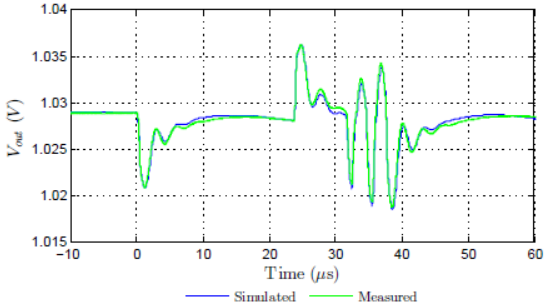


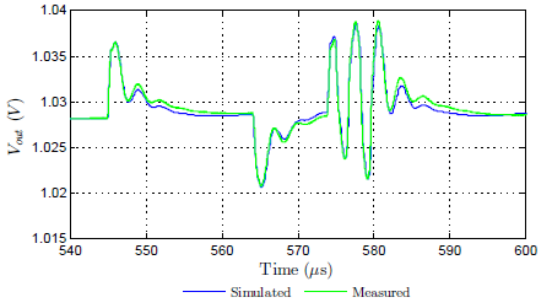
Algorithm to generate worst case excitation pulse pattern

Measurement: Worst Case Transient Response

- Worst case transient response generated by Reverse Pulse Technique.
- Good correlation between measurement and simulation

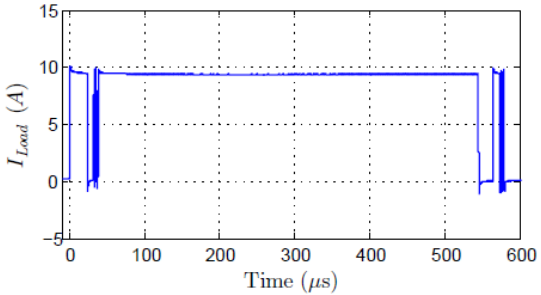
Worst-case low-to-high response.

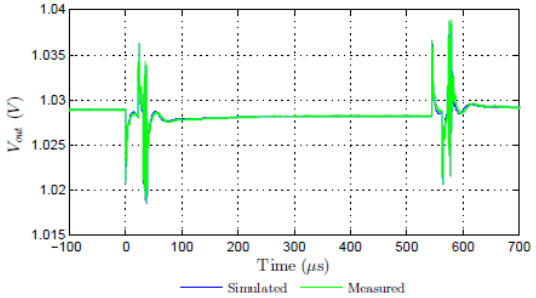




Worst-case high-to-low response.

Worst-case excitation pattern.

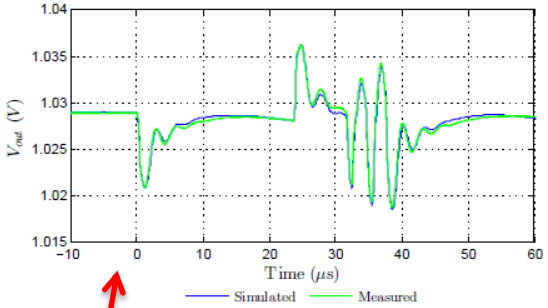


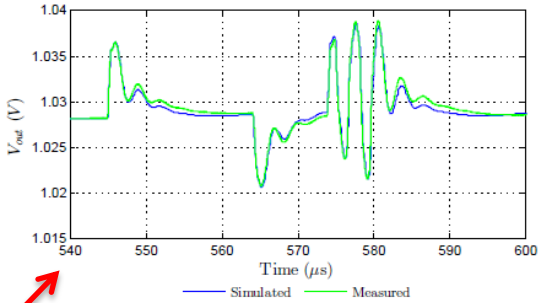


Measurement: Worst Case Transient Response

- Worst case transient response generated by Reverse Pulse Technique.
- Good correlation between measurement and simulation

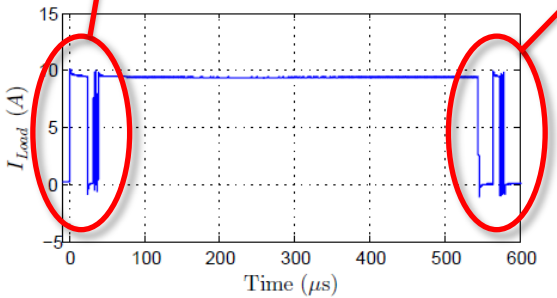
Worst-case low-to-high response.

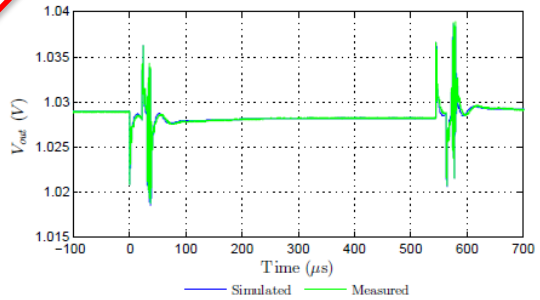




Worst-case high-to-low response.

Worst-case excitation pattern.





Measurement: Worst Case Transient Response

- Worst case transient response generated by Reverse Pulse Technique.
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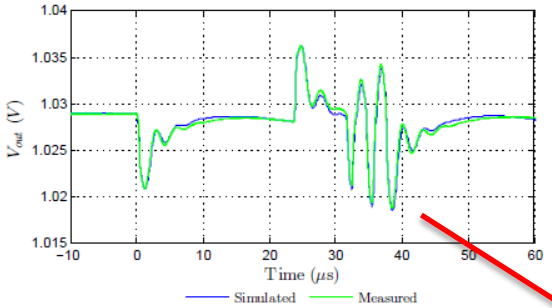
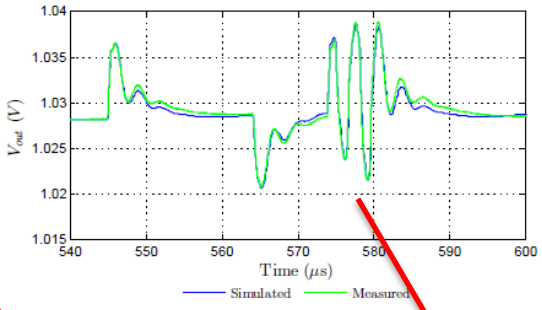
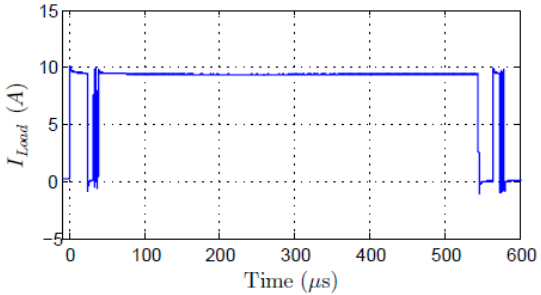
Worst-case low-to-high response.

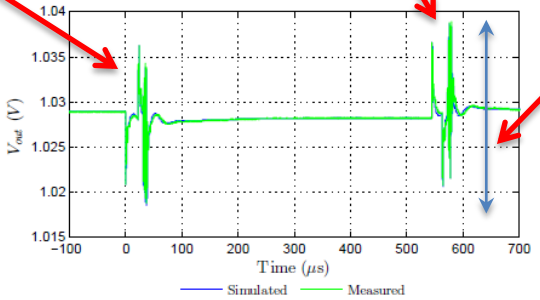




Worst-case high-to-low response.

Worst-case excitation pattern.



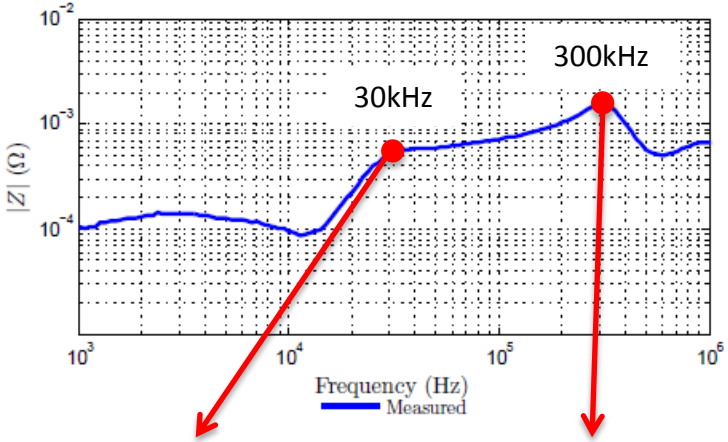


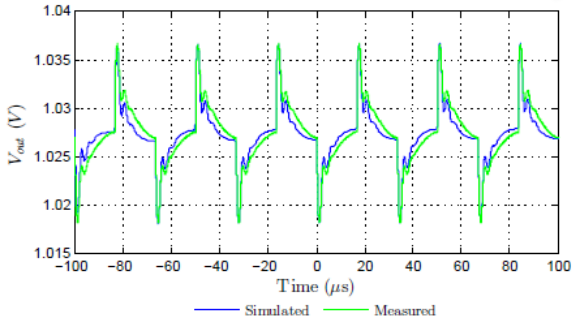
Worst case peak-to-peak response: 20.2mVpp

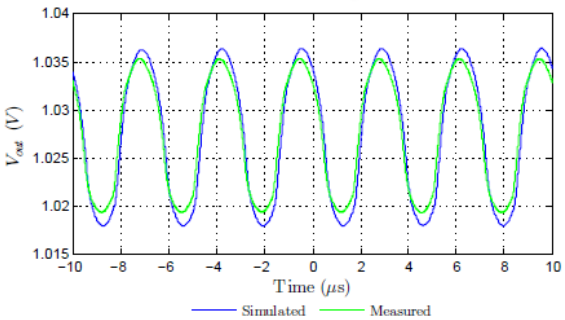
Shortcoming of Target Impedance Approach

- Impedance profile shows low-Q resonant peaks at 30kHz and 300kHz
  - Popular approach approximates worst case peak-to-peak voltage by repetitive excitation of the resonant peaks

- Voltage waveform due to load pulsed at 30kHz and 300kHz
  - 30kHz: 18.5mVpp (underestimates worst case noise by 8.4%)
  - 300kHz: 16.1mVpp (underestimates worst case noise by 20%)







Outline

- Electrical and Thermal Impact of Antiresonance:
  - High-Q antiresonance
  - Effect of component tolerance
  - Components at elevated temperature
- Impedance Flatness and Worst-Case Transient Noise:
  - Target impedance and the reverse pulse technique
  - Obtaining the PDN step response
  - Getting the worst-case transient response
- Conclusions

Conclusions

- Demonstrated causes and consequences of non-flatness of PDN impedance profiles.
- In the thermal design, the ambient temperature needs to consider the local temperature rise caused by the nearby power components.
- Reverse Pulse Technique can be used for the worst-case transient noise estimation.
- Estimating the noise by tuning a periodical waveform may underestimate the worst-case noise.

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Thank you!

QUESTIONS?