UBM

# Measurement and Simulation of a High-Speed Electro/Optical Channel

Shirin Farrahi, (Oracle)

Michael Cina (TE Connectivity), Jeffery Marquart (TE Connectivity), Andrei Kaikkonen (TE Connectivity), Xun Zhang (Oracle), Gustavo Blando (Oracle), Istvan Novak (Oracle)



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# SPEAKER

**Shirin Farrahi**

*Senior Hardware Engineer, Oracle*
shirin.farrahi@oracle.com

At Oracle, Shirin Farrahi is engaged in the design and characterization of high-speed signal interconnects for high-performance server systems. She received her Ph.D. in Electrical Engineering from the Massachusetts Institute of Technology in 2013.

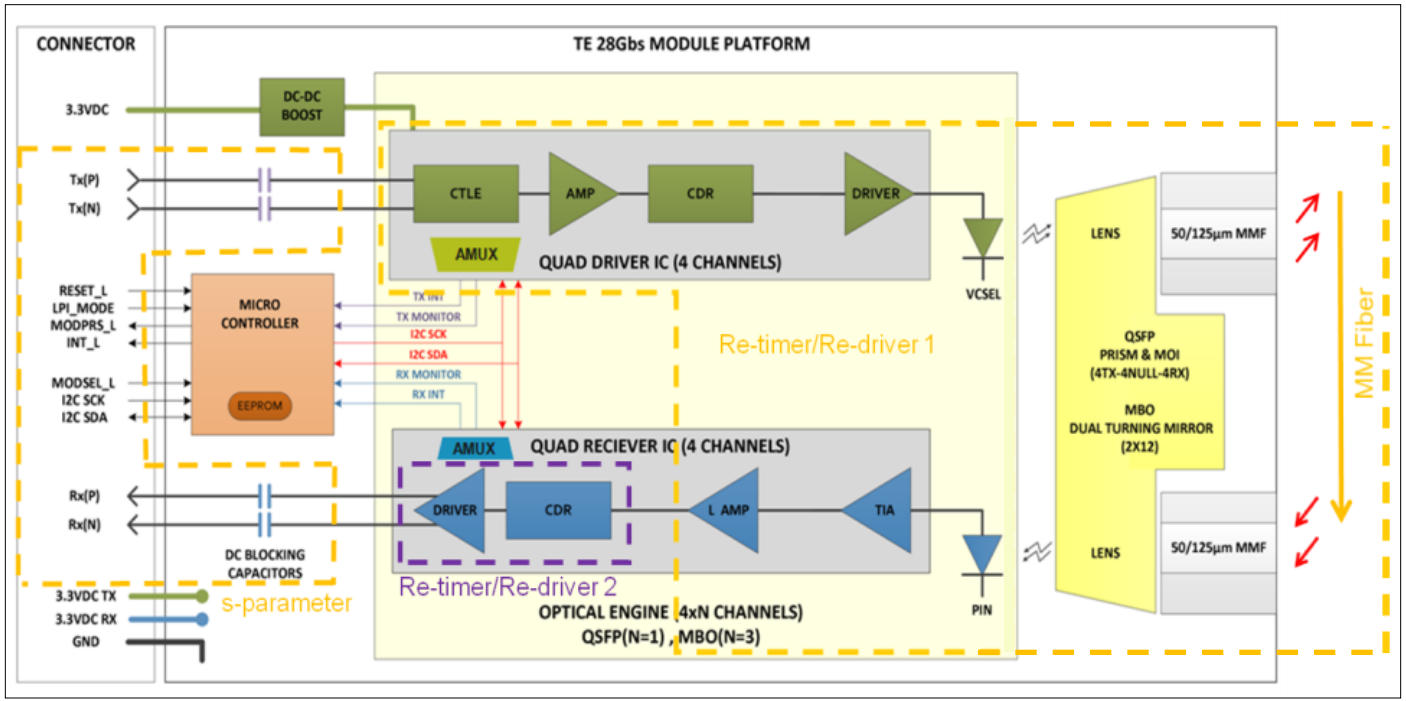
# MOTIVATION

- System bandwidths growing to multiples of Terabits per second
  - need for I/P devices with optical signaling close to the processor
- Mid-board optical module (MBOM)
- Cost and complexity of these systems makes simulations critical for system design decisions
- Is modeling these busses with IBIS-AMI useful for important architectural decisions?

# OUTLINE

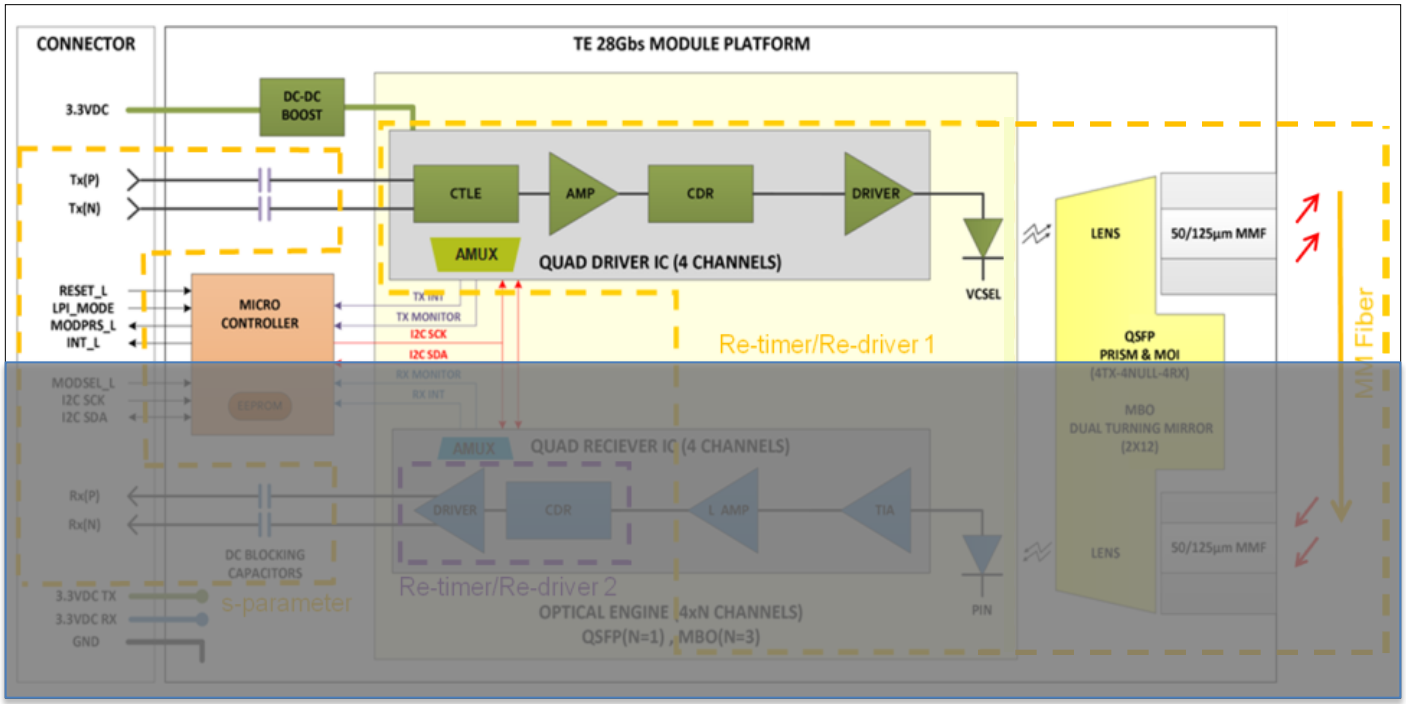
- **Generation of IBIS-AMI models:**
  - Modeling of linear and non-linear components
- **Description of test setup:**
  - Measurements
  - Simulations
- **Measurement and simulation correlation:**
  - FDR (14.625 Gbps)
  - EDR (25.78125 Gbps)
  - Varying temperature
- **Conclusions**

# MID-BOARD OPTICAL MODULE



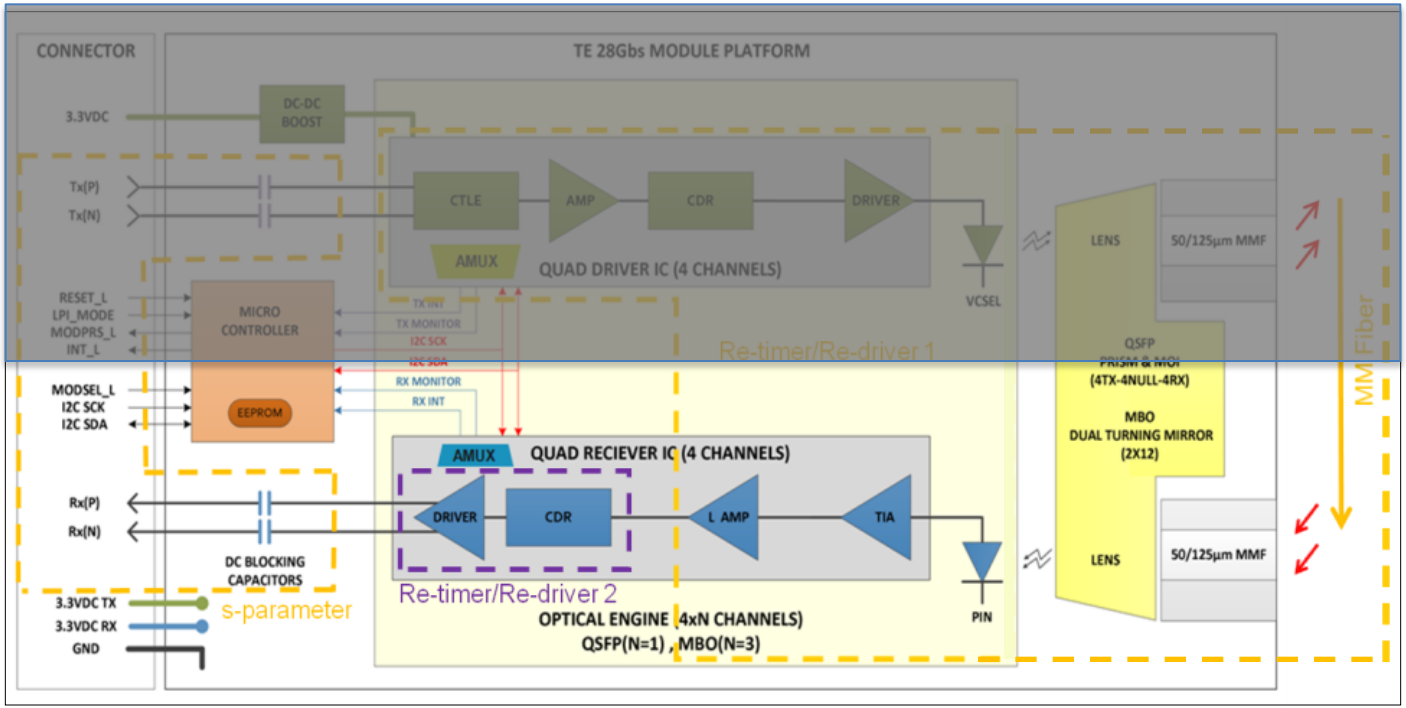

Highly non-linear and complex device to model

# MID-BOARD OPTICAL MODULE



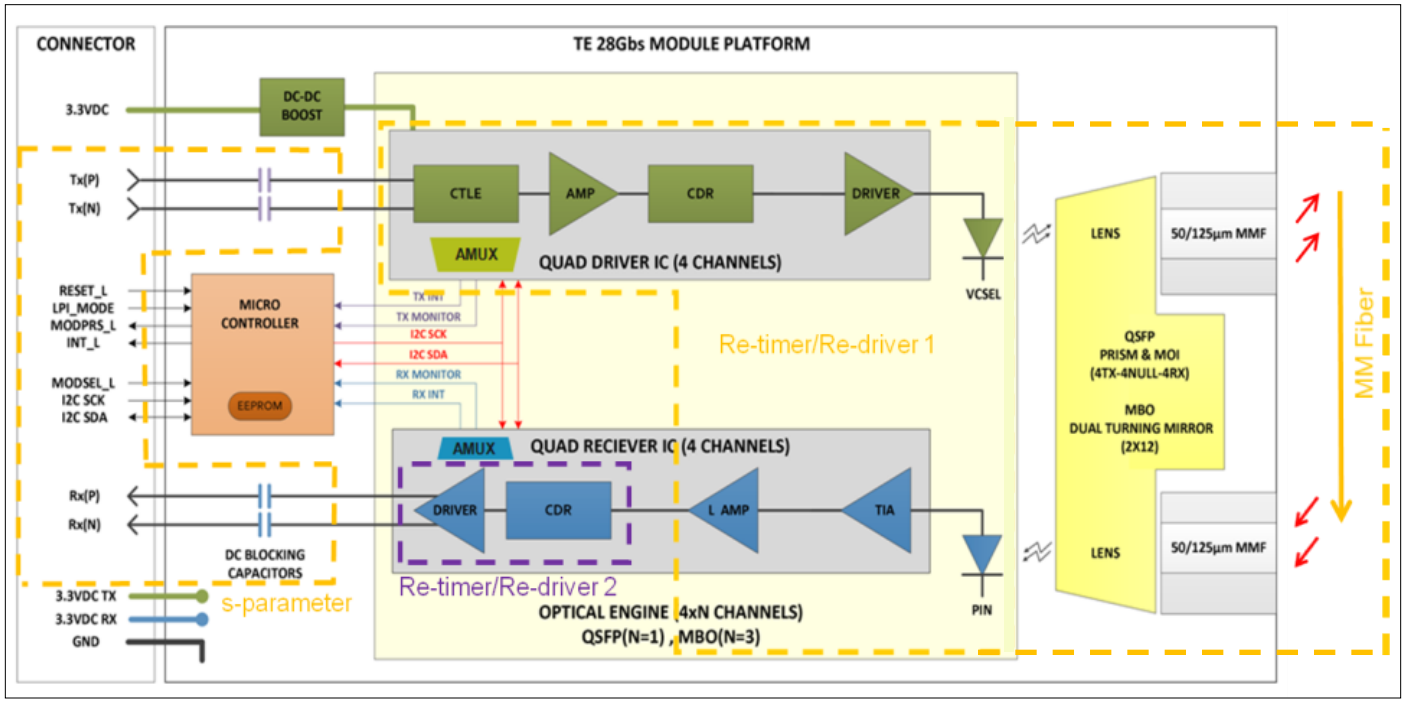

Optical Tx portion of MBOM

# MID-BOARD OPTICAL MODULE



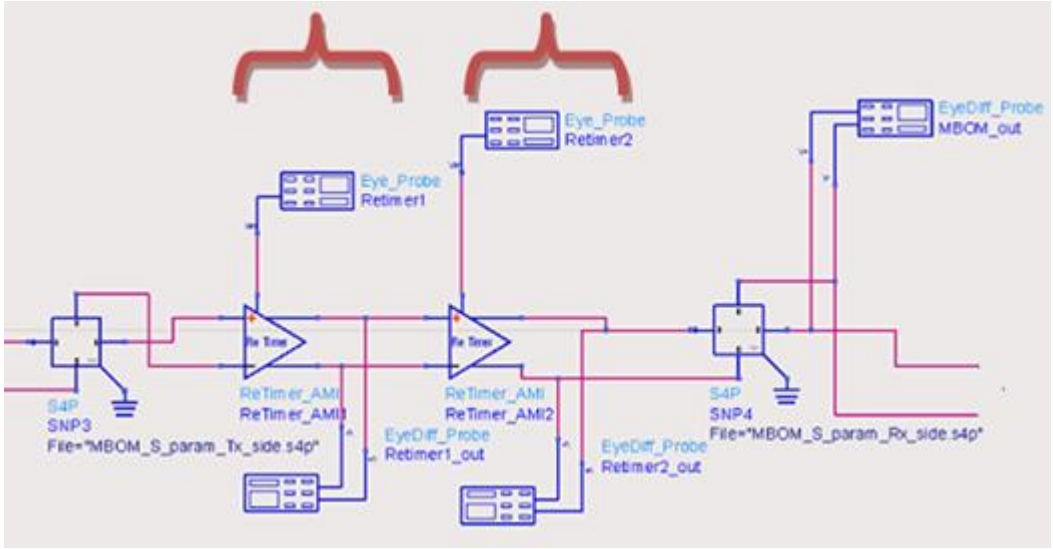

Optical Rx portion of MBOM

# MID-BOARD OPTICAL MODULE




Breakdown of component model

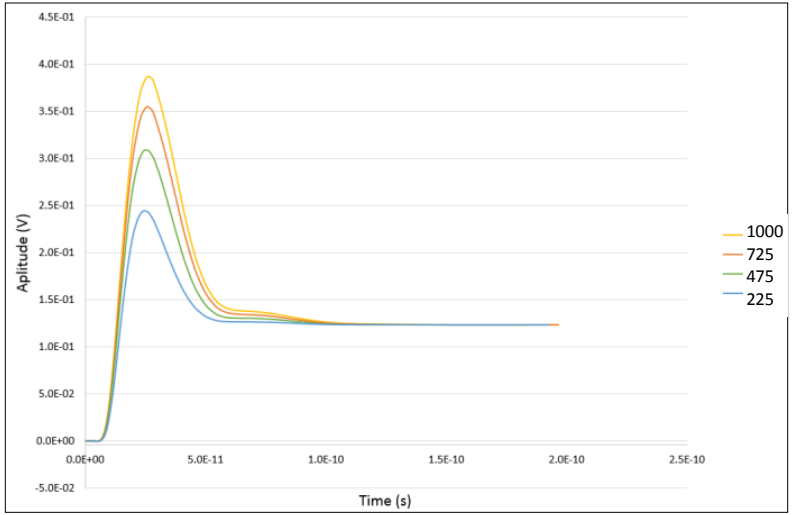
# MBOM IBIS-AMI MODEL



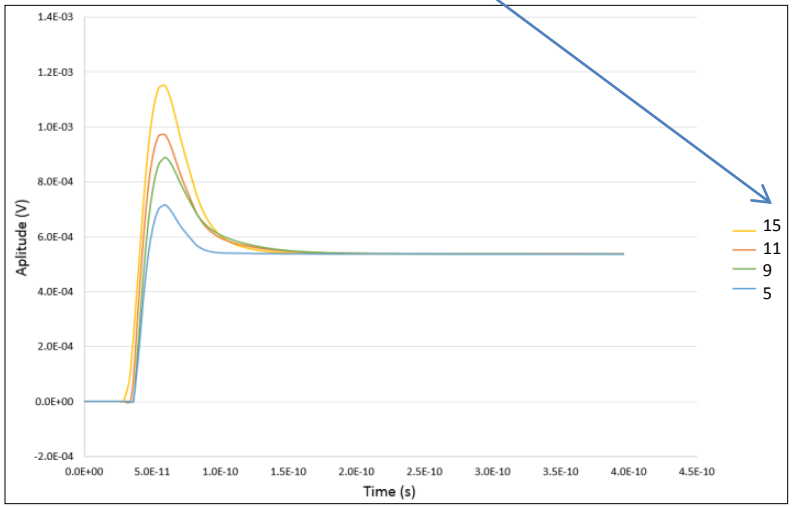

Model with passive and active components

# GENERATION OF IBIS-AMI MODELS

- Linear components modeled using step responses obtained from transistor level design
- Range of MBOM settings that can be selected in model



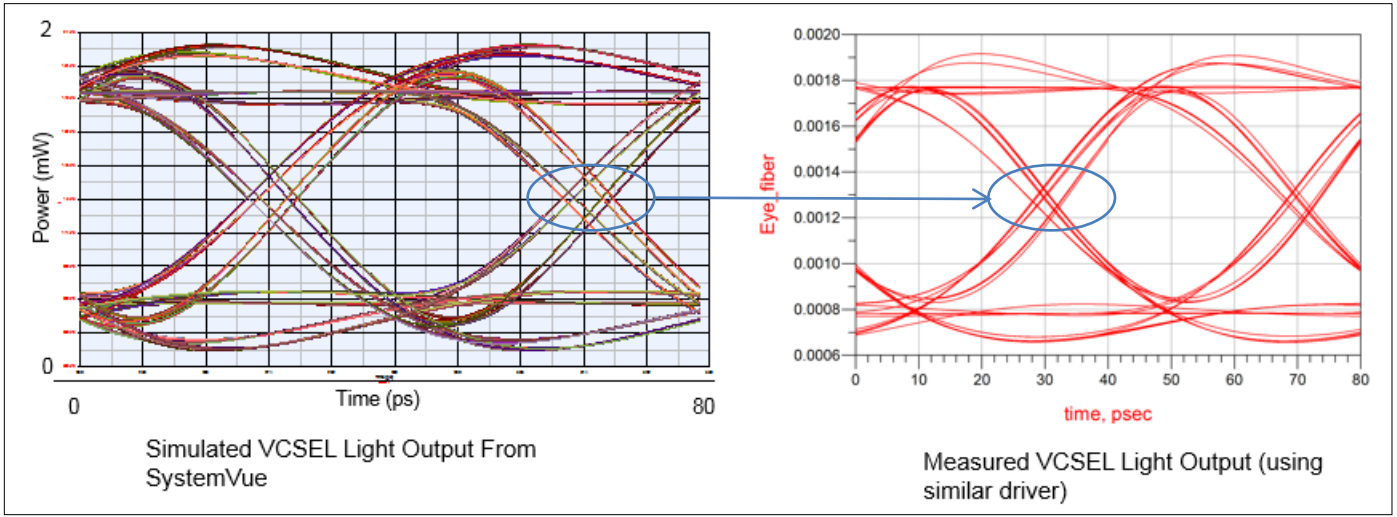

**Step response of MBOM CTLE**




**Step response of MBOM Pre-emphasis**

# GENERATION OF IBIS-AMI MODELS

- VCSEL (Vertical cavity surface emitting laser) modeled linearly
- Although highly non-linear, in our range of operation a small-signal model captures several important features

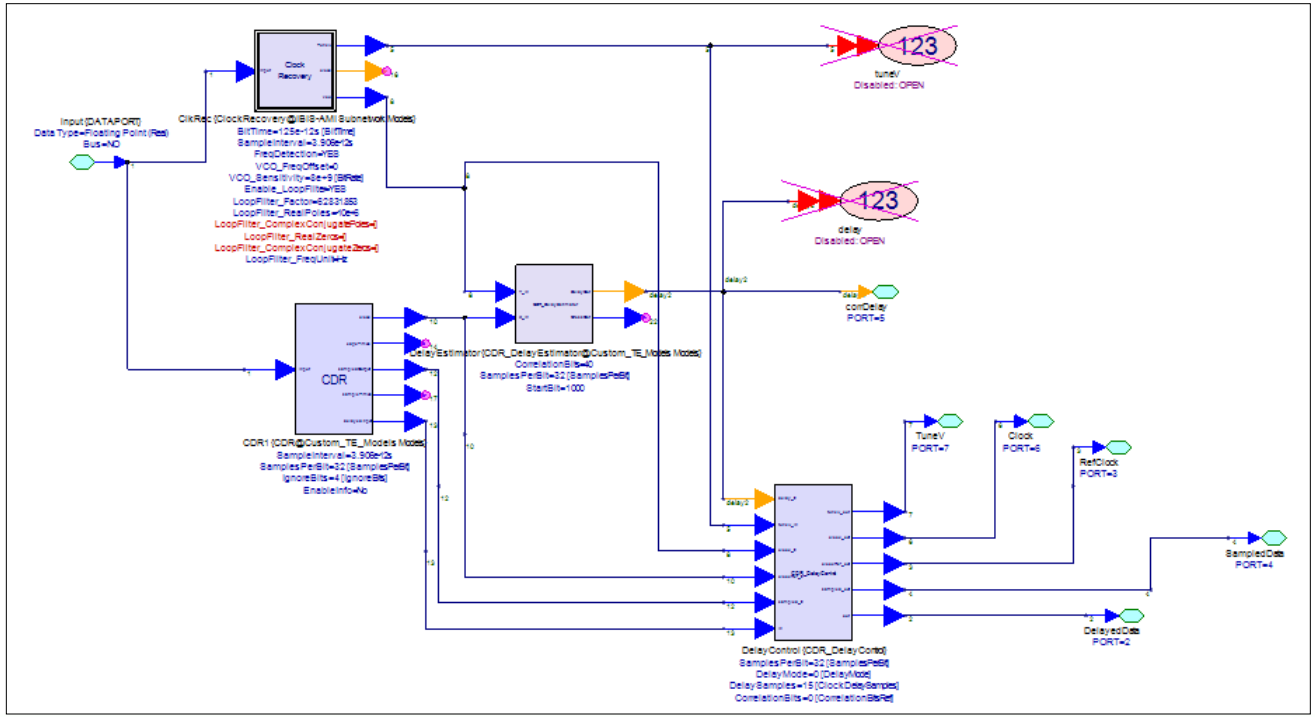



Simulated VCSEL Light Output From SystemVue

Measured VCSEL Light Output (using similar driver)

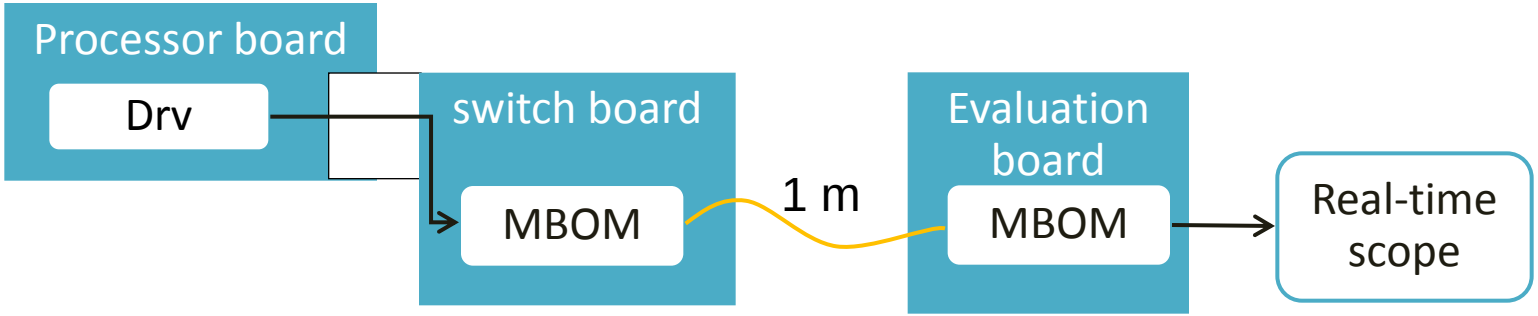
# GENERATION OF IBIS-AMI MODELS

- CDR modeled using SystemVue
- Idealized model that doesn't demonstrate problems in real hardware

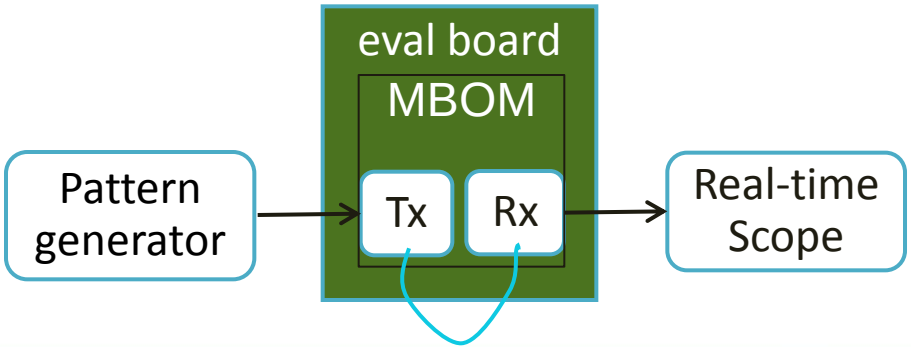


# TEST SETUP AT FDR AND EDR

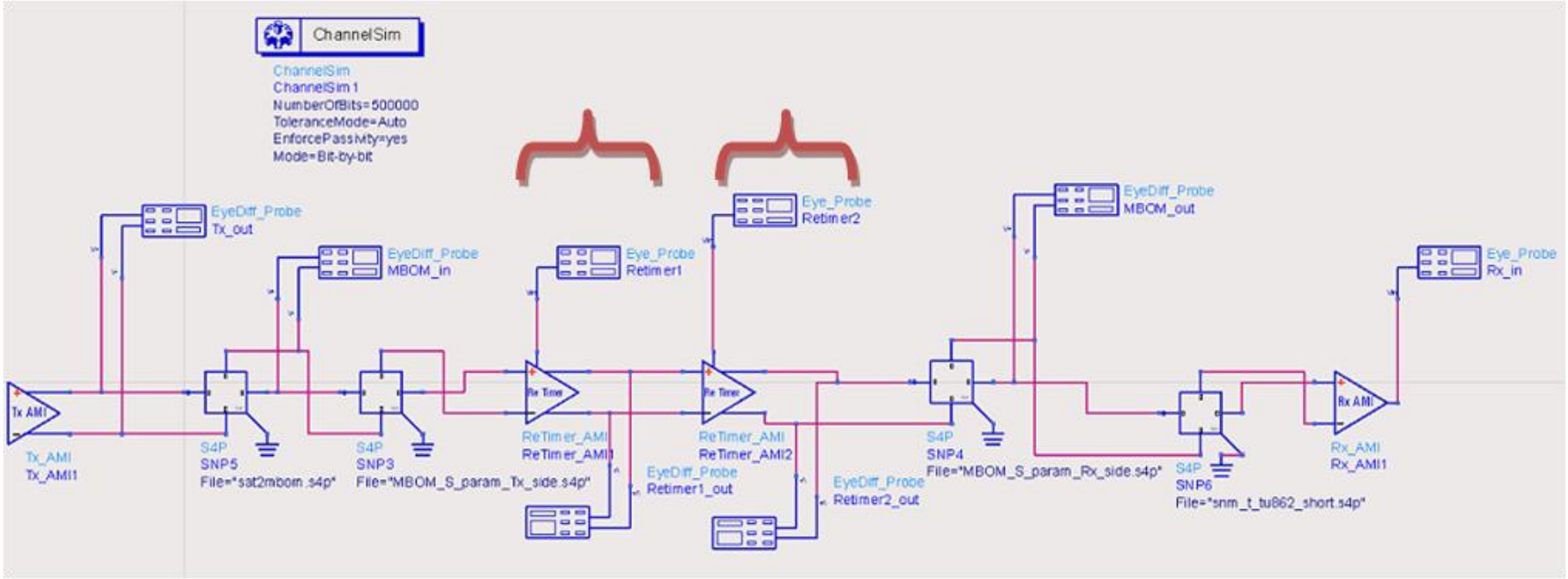
- FDR = 14.0625 Gbps. CDRs disabled on MBOM




- EDR = 25.78125 Gbps
- Tx CDR enabled on MBOM



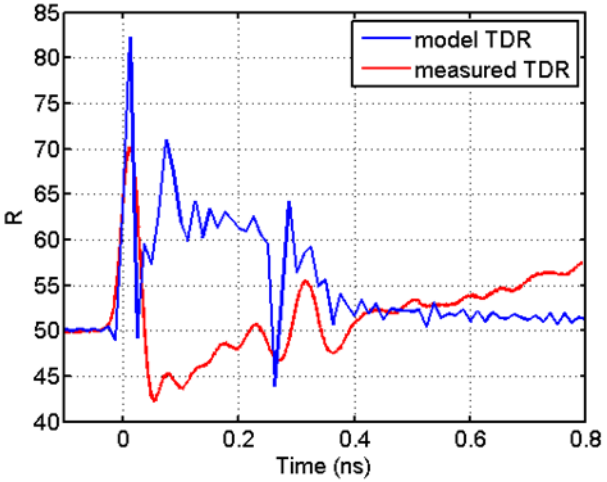
# SIMULATION SETUP

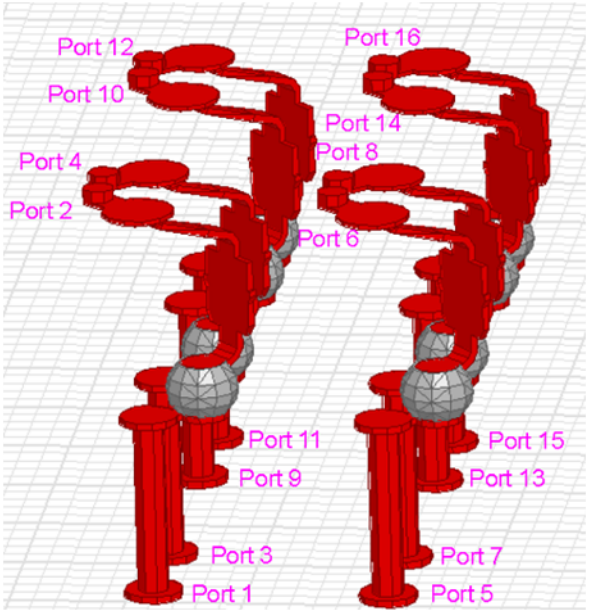



Simulating entire link allows us to see effect of jitter at input to MBOM at FDR where there are no CDRs.

We can correlate our measurements at a variety of points along the channel

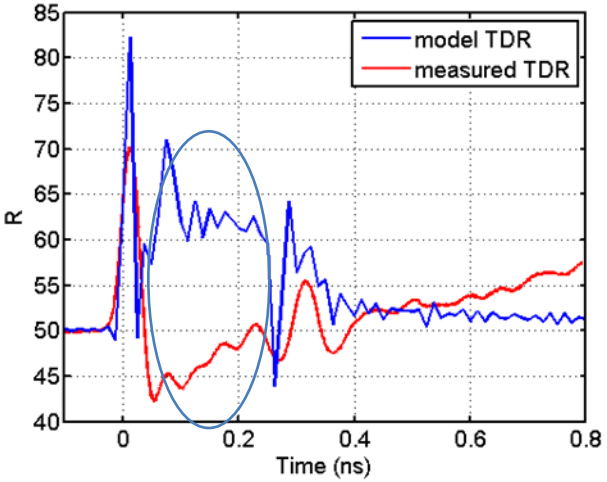
# MEASUREMENT SIMULATION CORRELATION OF PASSIVE COMPONENTS

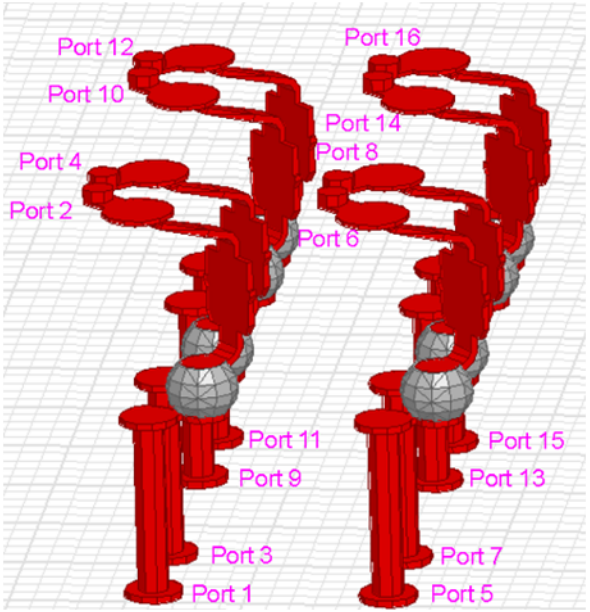



**MBOM socket model**

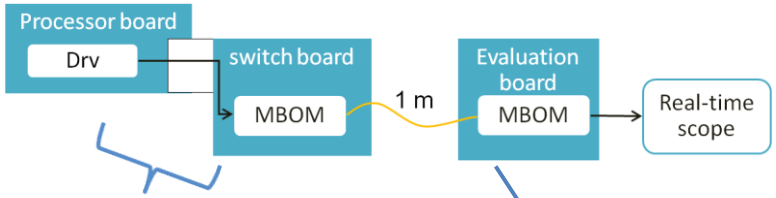
# MEASUREMENT SIMULATION CORRELATION OF PASSIVE COMPONENTS

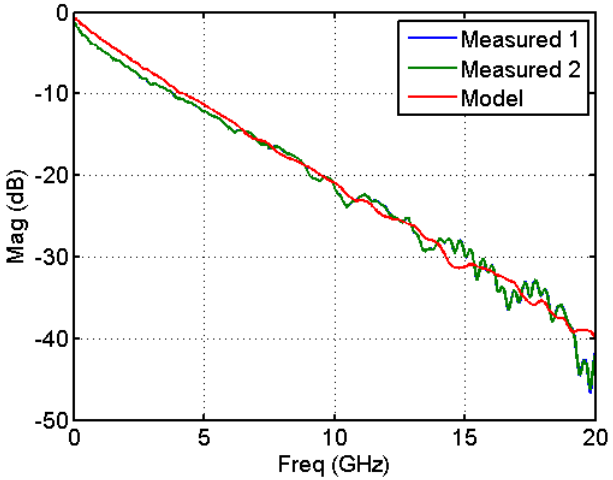


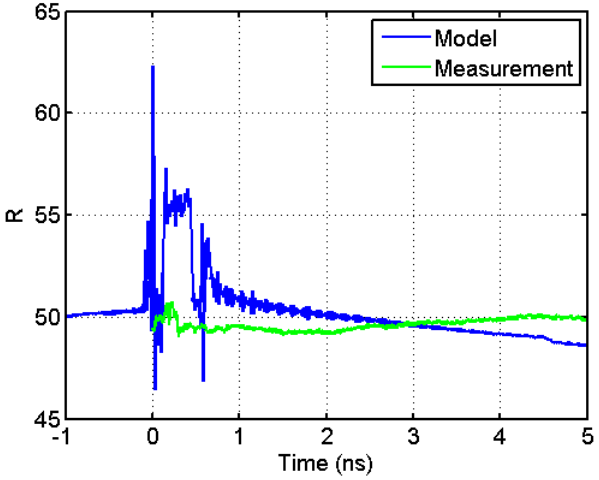

**MBOM socket model**

# MEASUREMENT SIMULATION CORRELATION OF PASSIVE COMPONENTS



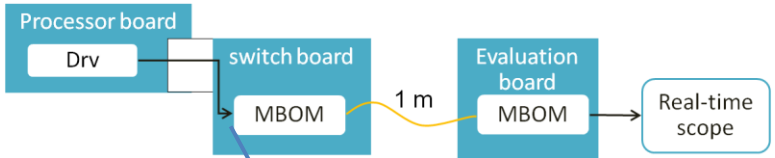



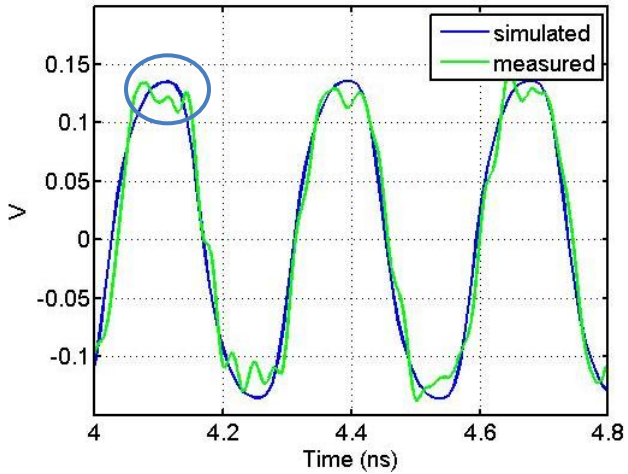

Processor board trace measured vs model



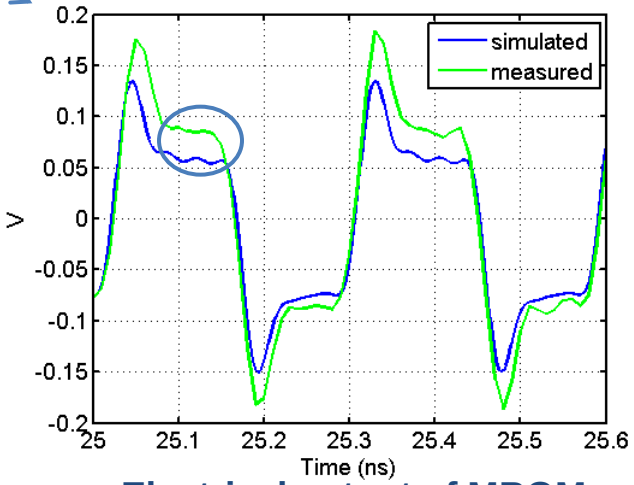

TDR of evaluation board trace

# MEASUREMENT SIMULATION CORRELATION AT FDR




**Electrical input to MBOM**

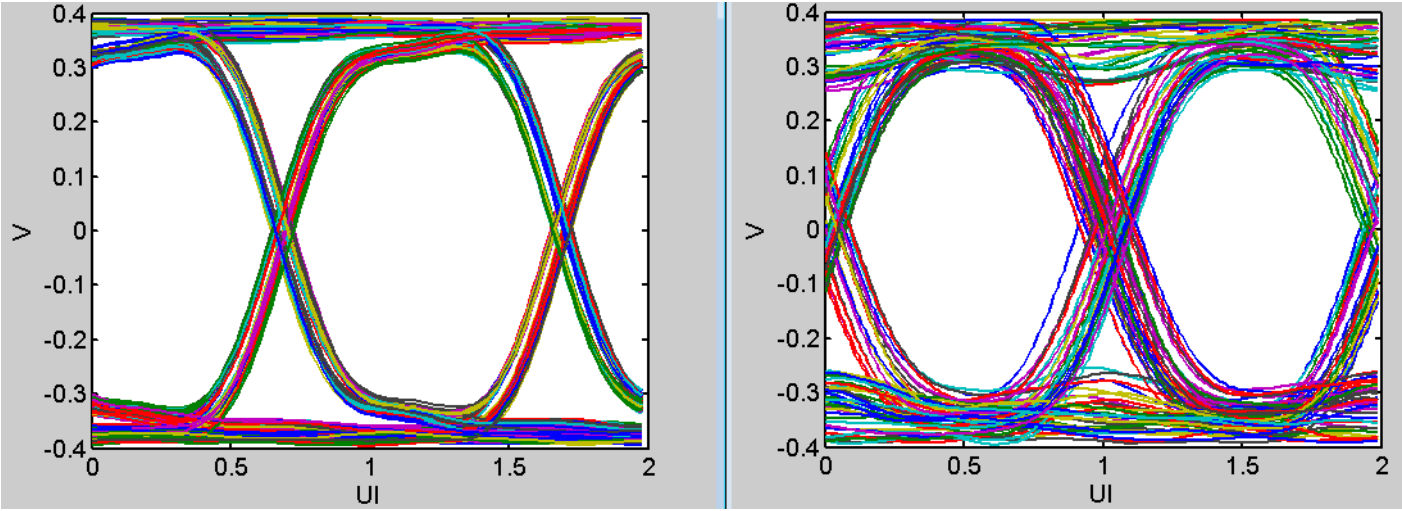



**Electrical output of MBOM**

Clock pattern measurements match to a first order but show differences in details

# MEASUREMENT SIMULATION CORRELATION AT FDR

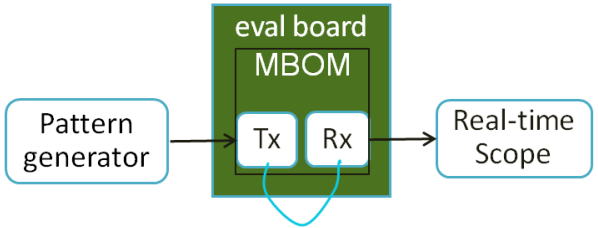
- PRBS31 stimulus
- Much more jitter present in measurement. None added in simulation

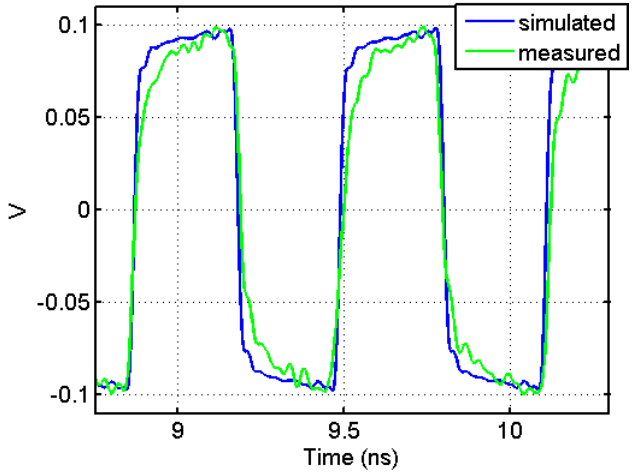



**Simulated (left) vs measured (right)**

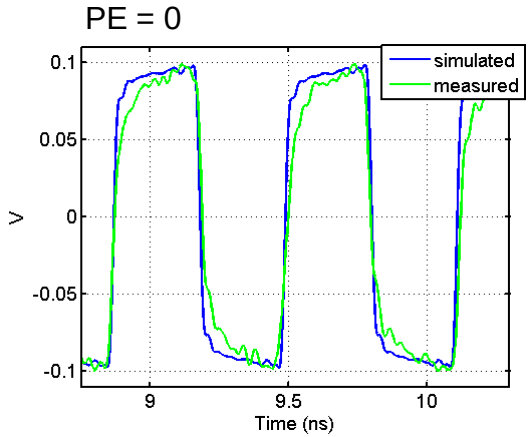
# MEASUREMENT SIMULATION CORRELATION AT EDR

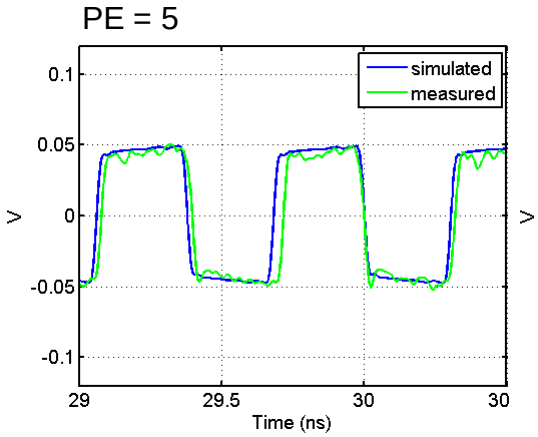
- Clock pattern slowed by 16x
- Minimum pre-emphasis setting
  - Model has faster rise-time than real hardware at this setting

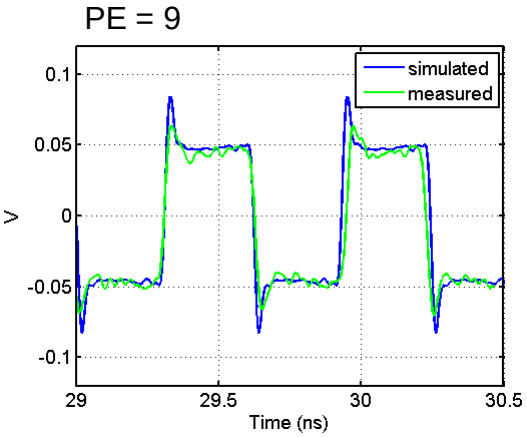


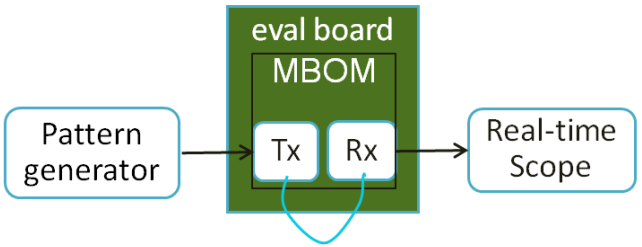



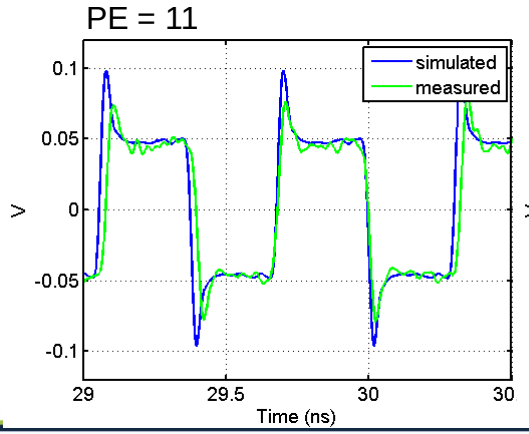
# CORRELATION OVER DIFFERENT MBOM SETTINGS AT EDR

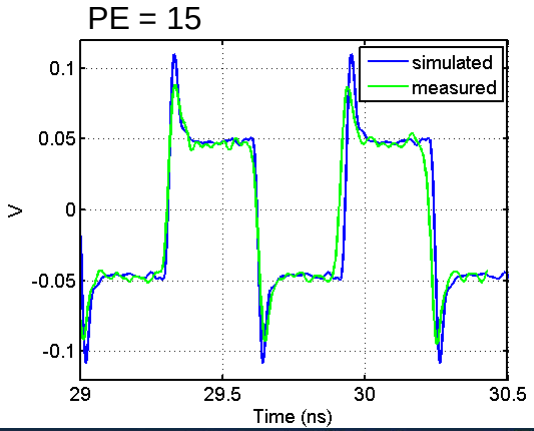


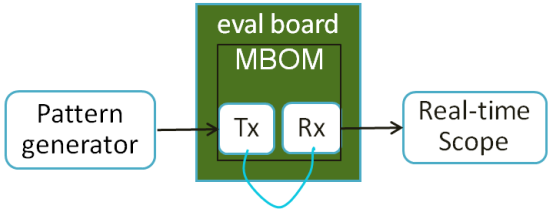



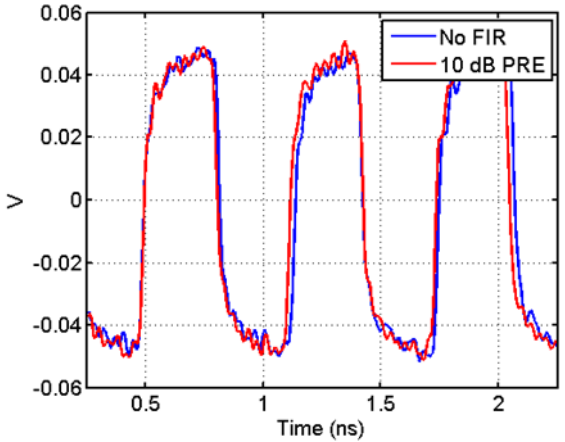



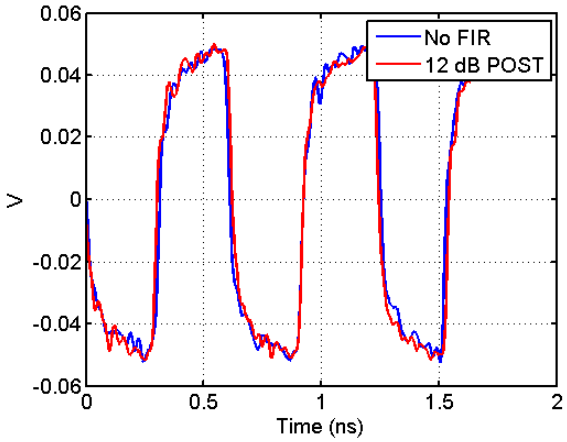



# EFFECT OF VARYING DRIVER FIR SETTINGS AT EDR

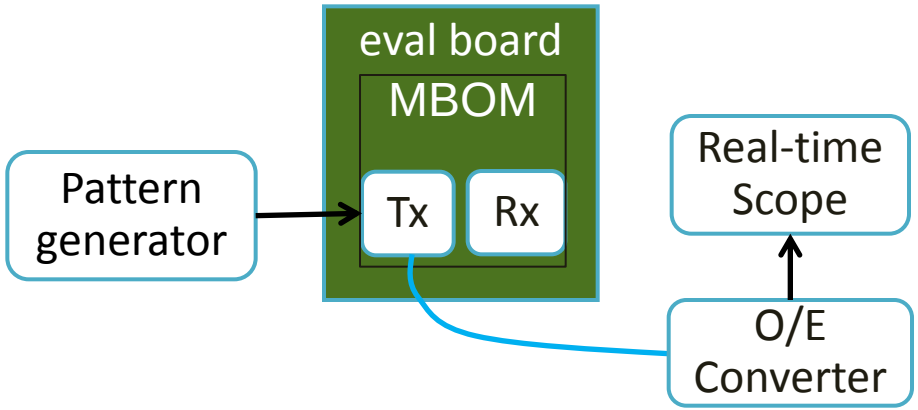


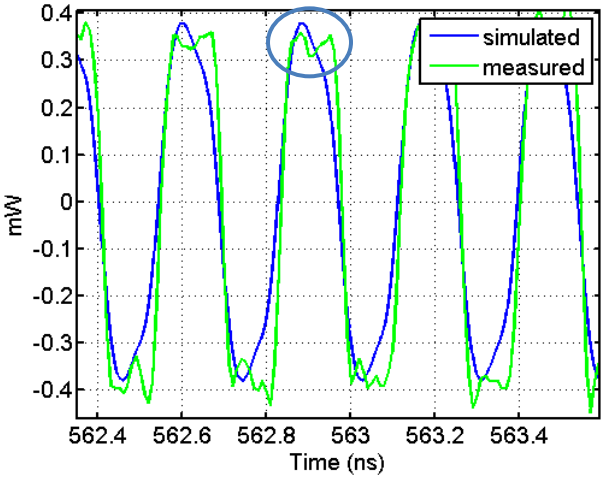




Drastic changes in pattern before MBOM Tx do not affect MBOM electrical output at EDR as long as signal at input to MBOM is not degraded

# OPTICAL MEASUREMENT SIMULATION CORRELATION AT EDR

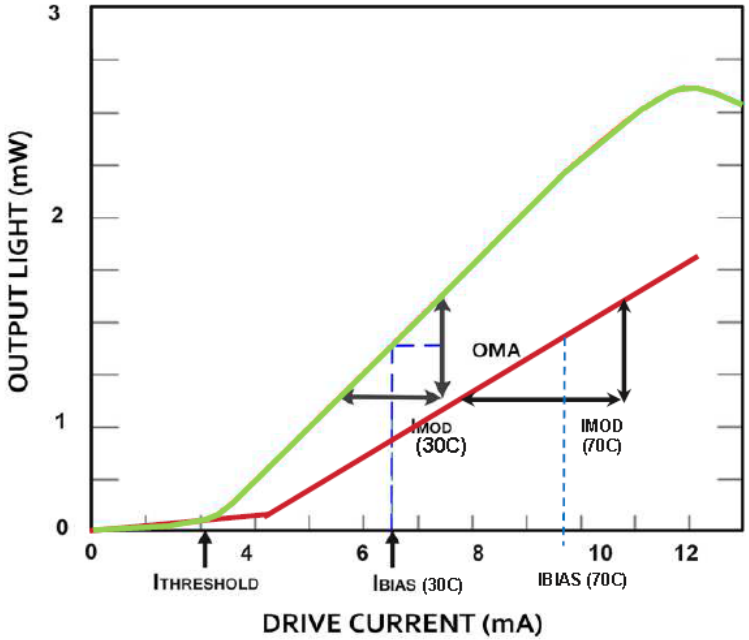


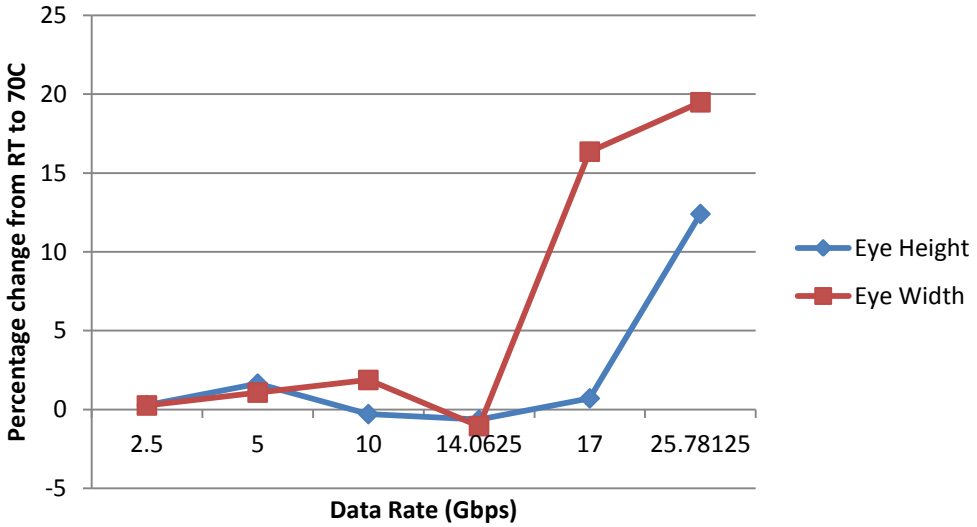

Optical measurement and simulation results provide an easy path for tuning the Tx portion of the link.

Similar to electrical results, match is good to a first order but not agreeing in details

# MEASUREMENT SIMULATION ACROSS TEMPERATURE AT EDR




VCSEL I/O curve with varying temperature




Variation in MBOM electrical output properties from 25°C to 70°C

# CONCLUSIONS

- IBIS-AMI modeling useful for first-order approximation of responses of electro-optical channels
- Without real hardware, we cannot rely on simulations for final tuning settings and other details
- Very important to know how model settings relate to real hardware

# ACKNOWLEDGEMENTS


- From Oracle
  - Seyla Leng
  - Ying Li
  - Greg Truhlar
  - Stephen Lindquist
- From TE Connectivity
  - Brent Miller
  - Jonathan Lee

# Thank you!

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## QUESTIONS?