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A Generic Test Tool for Power Distribution Networks

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Abstract

Power distribution network testing and validation is an important task in the system design flow. To avoid unnecessary testing time, the measurement setup, the instruments and the connections should be reusable for different tasks. Instruments and setups, therefore, whether they work in the time domain or frequency domain, limit the number of functions that can be performed without changing instruments, or cables or connections. The paper explores test setups and instrumentations that allow multiple tests being performed without changing the hardware connections. Real-life test results will illustrate the benefits and limitations of the setup.

Patent Disclosure

Portions of this document are the subject of patents applied for.

Disclaimer

This paper does not constitute as an endorsement by Oracle Corporation for any specific product, service, company, or solution.

Author(s) Biography

Istvan Novak is a Senior Principle Engineer at Oracle. Besides signal integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is a Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies.

Peter J. Pupalaikis was born in Boston, Massachusetts in 1964 and received the B.S. degree in electrical engineering from Rutgers University, New Brunswick, New Jersey in 1988.

He joined LeCroy Corporation (now Teledyne LeCroy), a manufacturer of high-performance measurement equipment located in Chestnut Ridge, New York in 1995 where he is currently Vice President, Technology Development, managing digital signal processing development and intellectual property. His interests include digital signal processing, applied mathematics, signal integrity and RF/microwave systems. Prior to LeCroy he served in the United States Army and has worked as an independent consultant in embedded systems design.

Mr. Pupalaikis holds forty-two patents in the area of measurement instrument design and has contributed a chapter to one book on RF/microwave measurement techniques. In 2013 he became an IEEE fellow for contributions to high-speed waveform digitizing instruments.

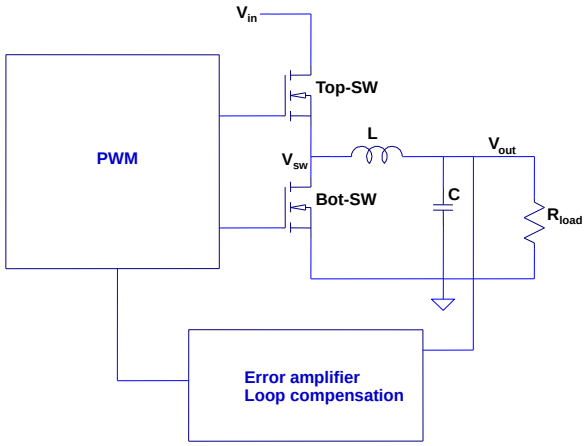
He is a member of Tau Beta Pi, Eta Kappa Nu and the IEEE signal processing, instrumentation, solid-state circuits, and microwave societies.

Introduction

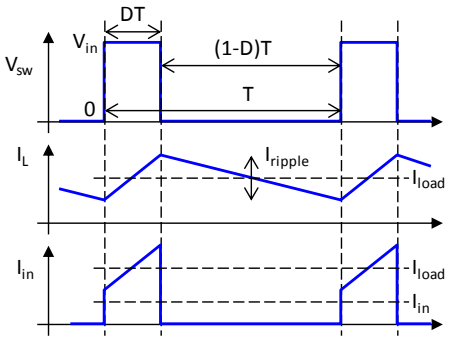
Testing, validation and debugging of power distribution networks (PDNs) of complex systems have a multitude of challenging tasks. These may include not only power-integrity related tests and measurements, but also checking signal-integrity and electromagnetic compatibility functionality that may be impacted by the PDN. Staying strictly in the area of power integrity, the possible tests are still numerous. The user first has to decide what parameter needs to be tested and in which domain. Passive PDN tests typically involve self or transfer-impedance measurements, but the complexity increases as we include in our tests active devices, linear and switch-mode voltage regulators as well. Most dynamic or alternating current (AC) tests can be done either in the time-domain or in the frequency-domain. Each category has its own pros and cons. Time-domain tests usually measure the switching ripple on the output voltage, the jitter of a switching converter's switch-node signal(s) or the transient responses to various load-change excitations, such as the common Step Response test. Time-domain tests are good to capture the nonlinear behavior of switching converters and the instruments are typically simpler to operate. Time-domain tests usually don't need (or lack) calibrations, but they also offer poorer sensitivity and more limited dynamic range. Frequency-domain tests usually measure transfer functions, which can produce self and transfer impedance results or transfer functions to various excitations, such as input-to-output transfer function, also called power supply rejection ratio (PSRR), output-to-input transfer function, or loop gain for measuring the stability of voltage or current-sharing loops. These can be based on swept-frequency measurements, and they produce a linearized response of the device under test (DUT) around a chosen direct current (DC) operating point. Nonlinearities are harder to capture and interpret this way, though the AC excitation level and the DC operating points can be varied and the linearized response be captured for a multitude of operating points. Frequency-domain testing offers the significant advantage of low noise floor, potentially very good spurious-response rejection and large dynamic range. Note that while many elements in typical PDNs in spite of their apparent slight nonlinearity can still be fairly well described with linear and reciprocal models (these are the interconnects, printed circuit board (PCB) traces, planes, vias, as well as many passive components, capacitors and inductors), active devices, such as power converter circuits are inherently non-reciprocal and many times are also unintentionally or intentionally nonlinear.

The test and measurement of passive and linear components of a PDN usually requires the measurement for the chosen ports of a selected network matrix, typically the S-parameter matrix, which later can be translated to impedance matrix. Symmetry of the physical structure typically does not apply, but reciprocity applies and therefore we have to measure only one half of the matrix, often just the self-impedance terms. Though the measurement details do vary with the selected frequency range, the basic instrumentation and data collection is the same or very similar for all of the tasks [1].

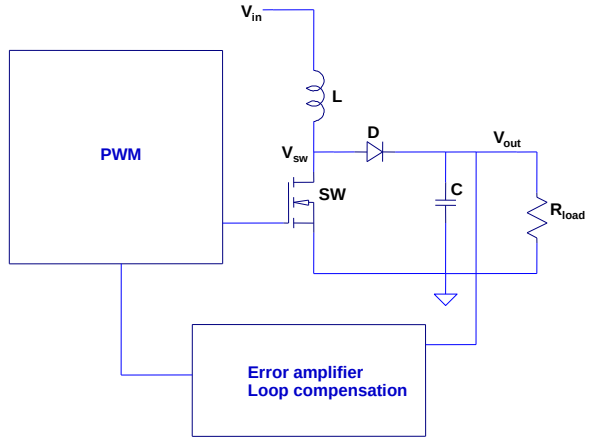
In contrast to passive PDN structures, the testing of active PDN circuits require a more diverse instrumentation and setup and therefore in the rest of the paper we will focus on testing the various parameters of DC power sources, more specifically linear and switch-mode voltage regulators. Power conversion circuits are everywhere in our electronic systems: they convert the AC line voltage to 48 V or 12 V DC for system-wide distribution, large and small DC-DC converters feed individual integrated circuits or clusters of loads, low-current analog regulators feed sensitive analog circuits. A common characteristics is that with a few exceptions they all have control loop(s) to stabilize one or more output parameters, for instance the output voltage, or control how current is shared in multi-phase and paralleled converters. The electrical characterization of the converter circuits have a multitude of tasks and with today's instrumentations and test methodologies they require many times different instrument and connections [2, 3].



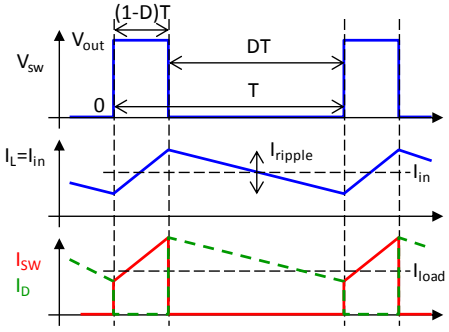
(a) simplied block schematic of non-isolated buck converter



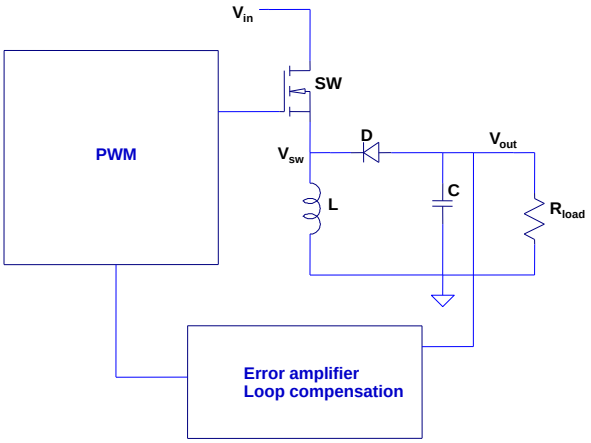
(b) typical waveforms of non-isolated buck converter



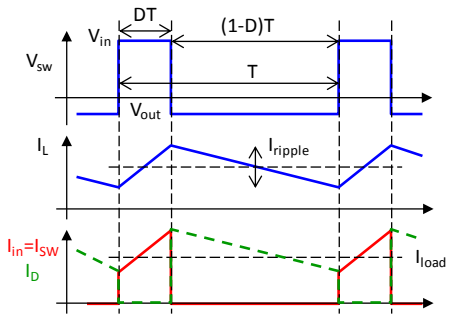
(c) simplied block schematic of non-isolated boost converter



(d) typical waveforms of non-isolated boost converter



(e) simplied block schematic of non-isolated buck-boost converter



(f) typical waveforms of non-isolated buck-boost converter

Figure 1: Block schematics and typical waveforms for non-isolated converter topologies

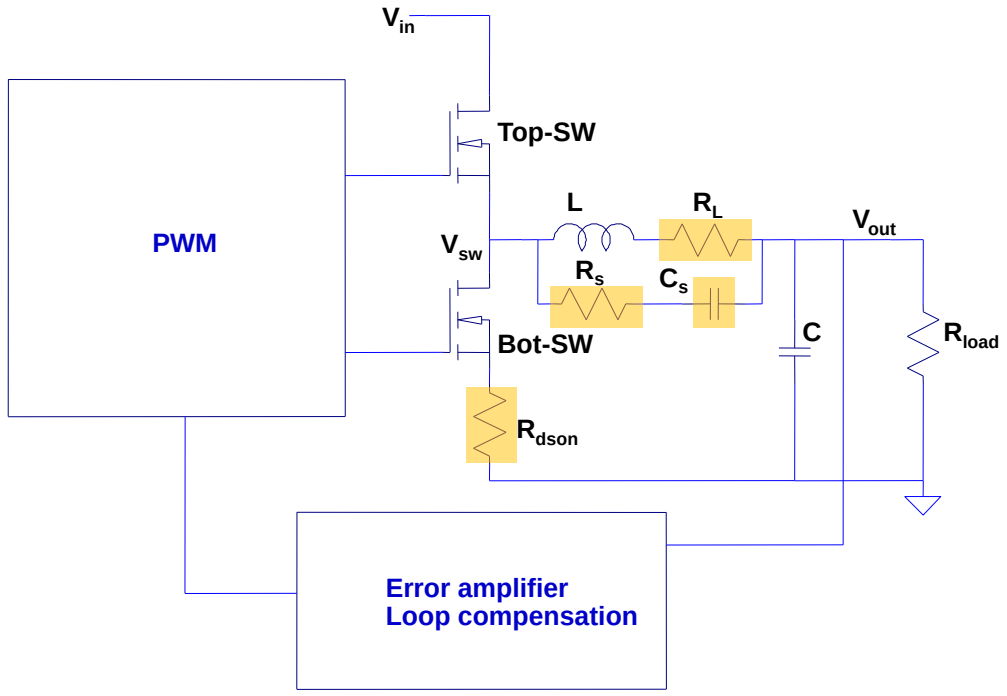


Figure 2: Two inductor current measurement options
highlighted components are used for the two options

Figure 1 gives a generic overview of the three major non-isolated DC-DC converter topologies: buck, boost and buck-boost regulators.

Common test and measurement tasks

In this section, without claiming completeness, we review some of the most common test and measurement tasks on active voltage regulators. Without limiting generality, the examples will be shown for non-isolated buck converters.

Input and output current and current-sharing measurements

Figure 1b shows that we know both the input and output currents if we know the current in the inductor. Traditional current measuring setups would require a dedicated shunt resistor placed in series to the current to be measured and looking at the voltage across the shunt resistor. We can measure the inductor current also indirectly, without adding losses, by making use of the fact that real-life inductors have series resistance (shown as R_L in Figure 2), which creates a one-pole exponential response for the inductor current for a constant voltage excitation. The time constant of the exponential change is L/R_L. If we place a series RC element in parallel to the inductor (R_s and C_s in Figure 2) and set the $R_s \cdot C_s$ time constant to equal the L/R_L time constant, the voltage across the C_s capacitor will equal the voltage across R_L. By measuring the voltage across the C_s capacitor and knowing R_L, we know the current through the inductor [4]. This

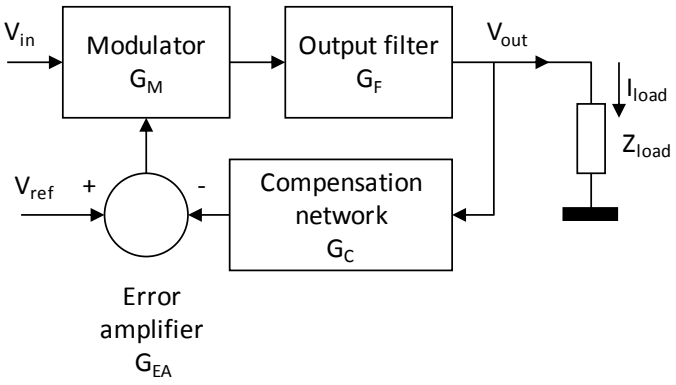


Figure 3: Simplified block diagrams of a power converter with feedback loop

saw-tooth current waveform usually has high-frequency parasitic ringing near the switching edges [5] and therefore blanking periods may have to be used to mask out a small percentage of the switching period near the rising and falling edges of the switch-node waveform. The DC average of the inductor current is the load current, the AC portion closes through the output capacitor bank. The current closing through the input source and input capacitors is the ON portion of the inductor current. Instead of or in addition to measuring the voltage across C_s, we can also make use of the voltage drops across the two switching field effect transistors (FETs): measuring the voltage across the ON resistance of the bottom-side switch (R_{dson} in Figure 2), we measure the inductor current during the OFF time.

We can also measure the voltage drop across the ON resistance of the top-side FET, though this has more practical challenges due to the large common-mode voltage associated with it. In either case, the accuracy of measured current across the loss resistance of components will depend on the accuracy of voltage measurement and accuracy of the estimate of loss resistance, which has not only unit-to-unit variations, but also temperature dependence and aging. We may want to measure input or output currents either with the system's own (random or unknown) excitation or with a user-generated load-current stimulus. This latter is particularly important and useful when the current measurement is done in all of the phases in a multi-phase regulator with transient load currents.

The tracking of the currents in the individual phases in a multi-phase converter is a useful metric for the stability of the current-sharing loop.

Voltage-loop gain

The stability of the voltage feedback loop is the first and highest priority. Traditionally this has been done in the frequency domain, by analyzing the phase and gain margins of the open-loop gain curve [6]. Under some circumstances other forms of stability requirements may prove to be more useful [7, 8], but they are all based on the evaluation of the open-loop gain as function of frequency. A simplified block diagram for a non-isolated buck converter is shown in Figure 3. By applying a linearized model to each block, we can calculate the overall loop gain around the closed feedback loop and apply the conventional stability criteria during the design and analysis processes. By denoting the Modulator gain by G_M, Output filter

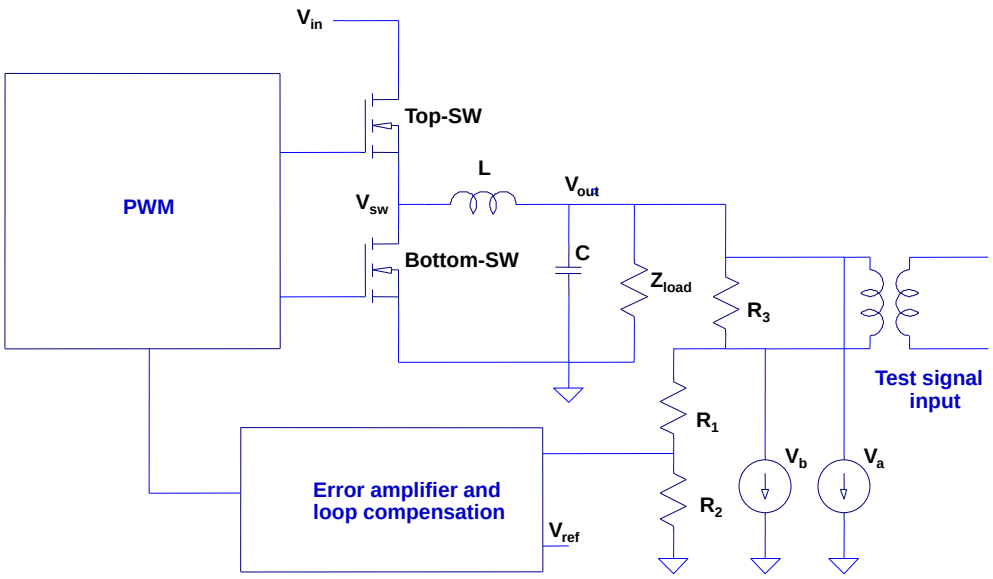


Figure 4: Typical connection scheme to measure the gain-phase open-loop characteristics

gain by G_F, Compensation network gain by G_C and Error amplifier gain by G_{EA}, the total loop gain can be described as:

$$G_{loop} = G_M \cdot G_F \cdot G_C \cdot G_{EA}$$

All constituents of the loop-gain product can be, and usually are, frequency dependent complex numbers. There are two major input variables that will affect the output voltage: drift and/or transients in the input voltage, drift and/or transients in the load current. In a linearized equivalent circuit of the converter, the effect of input voltage variation can be described with a $\Delta V_{out}/\Delta V_{in}$ voltage transfer function and the effect of load current variation can be described through a $\Delta V_{out}/\Delta I_{load}$ impedance.

$$\frac{\Delta V_{out}}{\Delta I_{load}} = Z_{out-closed-loop}(f) = \frac{Z_{out-open-loop}(f)}{1 + G_{loop}(f)} \tag{1}$$

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{G_M(f) \cdot G_F(f)}{1 + G_{loop}(f)} \tag{2}$$

The $1 + G_{loop}$ denominator of these expressions is called the characteristic expression.

Unless we want to validate and test each block in the feedback loop, from a stability point of view we need only the total G_{loop} function. The typical way of measuring the loop gain is to inject a small swept-frequency test signal into the feedback loop at a point where in one direction the impedance is much lower than the injection impedance and in the other direction it is much higher. The complex ratio of the voltages at the two terminals of the injector equals G_{loop}. Such a location is conveniently found where the output

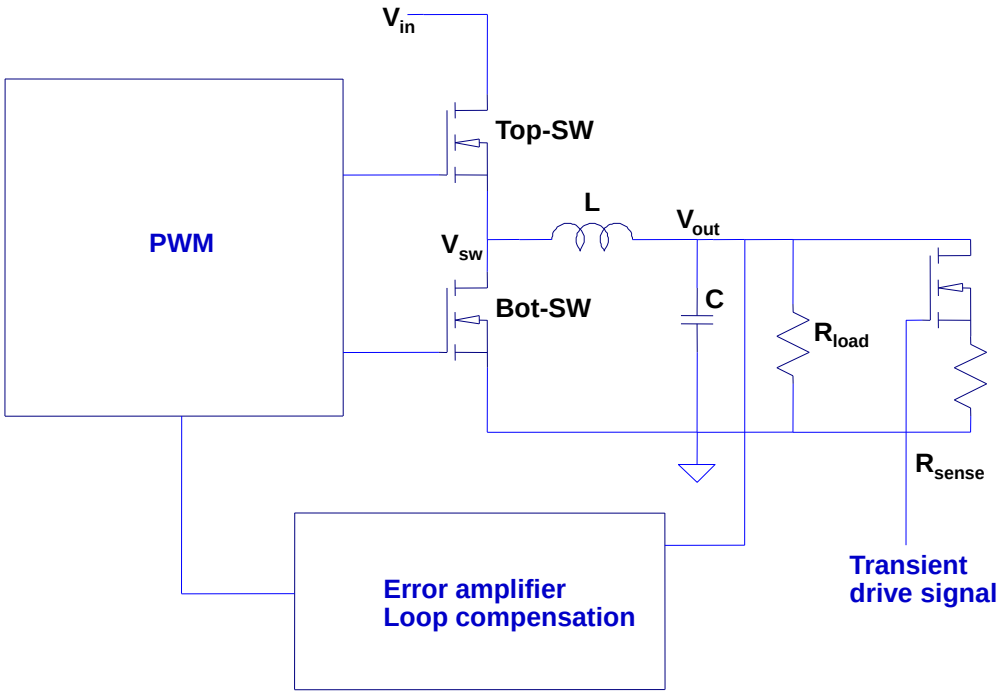


Figure 5: Transient load current test setup

voltage divider is connected to the converter output, as shown in Figure 4. The loop gain is the ratio of V_a to V_b shown in Figure 4.

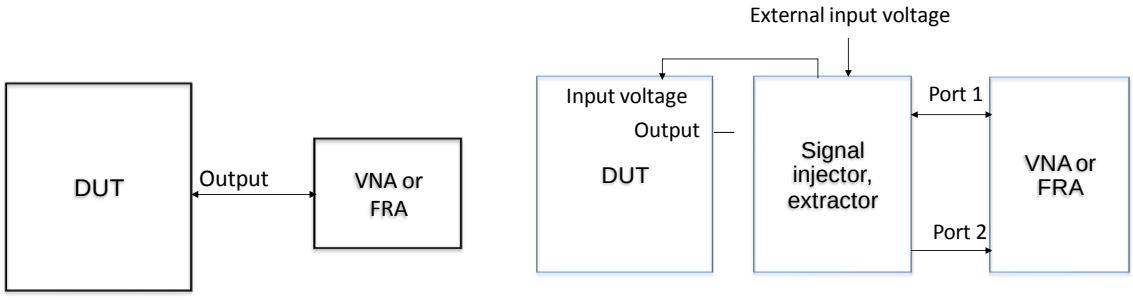
This measurement requires dedicated *Frequency Response Analyzers* with an output and two high-impedance inputs.

Transient response to load current change

This is a traditional time-domain test where the output of the converter is excited with a given step current and the output-voltage response is monitored with an oscilloscope. The magnitude, initial and final values of the current step as well as its transition time can be changed to map out potential non-linear behaviors. For high slew-rate excitations the challenge is to limit the inductance connecting the transient current source to the DUT. Custom hardware is available from various sources (e.g., [9]) and sometimes the output stage of the transient current source is built into the DUT, especially in case of evaluation boards. A simple, open-loop transient source output stage is shown in Figure 5.

Output and input impedance

Both impedances represent a small-signal frequency-domain view of the DUT, though the AC excitation level can be set to any small or large value. Output impedance is typically required for target-impedance based PDN designs [10]. Output impedance can be measured at different DC load currents and at different AC current magnitudes. The measurement methodology is well established and the measurement is noninvasive. The importance of input impedance is that its real part is negative, potentially creating instabilities



(a) input impedance measurement (b) output impedance measurement

Figure 6: Input and output impedance measurement setups

[11]. Also, measuring input impedance is challenging because the feeding impedance has to be low and the feed impedance is parallel to the injected test signal.

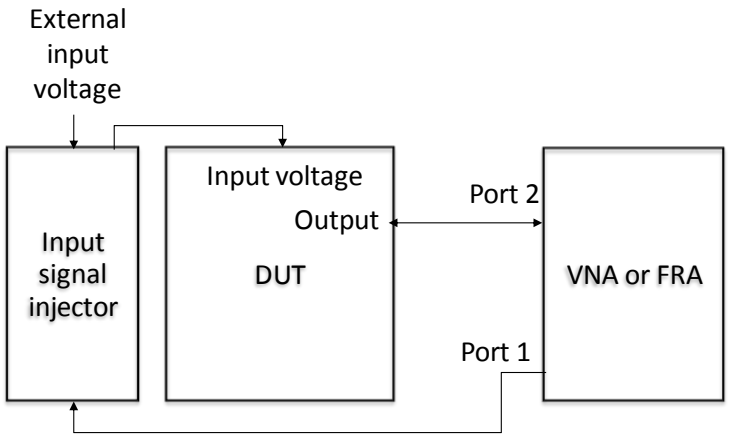
Input-to-output and output-to-input transfer functions

The input-to-output transfer function, also called the PSRR, can be measured by an external voltage excitation (transient step or swept-frequency sinewave) applied to the input voltage and measuring the V_{out}/V_{in} ratio. This parameter is an important metric for low-noise regulators, where noise transmitted from the input side has to be minimized. The reverse function, output-to-input transfer function, may be used less frequently, because on the input side of voltage regulators we typically assume and accept larger noise. To measure this transfer parameter, we need to excite the output with an external source with a transient or swept-frequency sine waveform and measure the complex ratio of V_{in}/V_{out}.

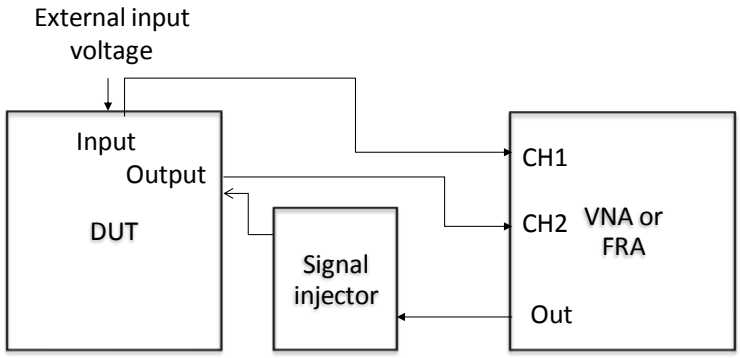
Universal PDN Test Tool

As the setup schemes of the previous section illustrate, to cover the wide variety of today's voltage regulators test needs, we need to use several different instruments and connection schemes. Though each instrumentation can be optimized for the particular task, increasing the dynamic range and spurious suppression of the measurement, overall the use of different instrumentation limits the usefulness, usability and universality of the solutions. Figure 8 shows an alternate solution, where the same instrumentation is used for all hardware measurement needs and the various functions are created by the different post-processing of the collected data.

The figure shows the full (optional) configuration, where external stimulus can be added from an arbitrary waveform generator (AWG). The AWG block may also contain additional current-boost circuits. The test points in the DUT will be typically the switch node(s), output voltage(s) and input voltage(s). With a known stimulus and with a few basic parameters of the regulator circuit, the voltages at the test points will provide a full description of the parameters we are interested in. For instance, if we know the inductance and resistance of the output inductor, the inductor current can be back-calculated from the voltages



(a) input-to-output



(b) output-to-input

Figure 7: Input-to-output and output-to-input transfer function measurement setups

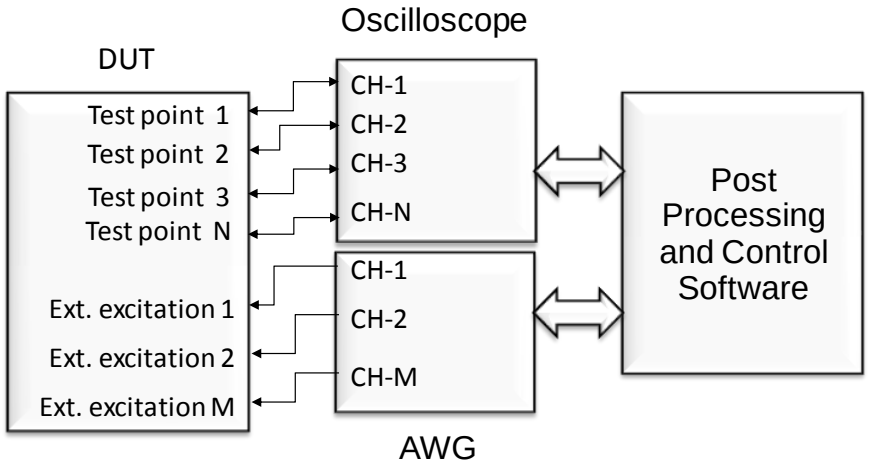


Figure 8: Block diagram of the Universal PDN Test Tool

at the switch node and the output. By knowing the inductor current waveform and by identifying the ON and OFF times of the switching waveforms, we can calculate all of the important validation parameters we may need to measure.

Implementation

Our first goal, which is the main topic of this section is to measure the inductor current. As mentioned previously, and provided in the reference [4], one way is to construct a circuit containing a combination of a series R_s and C_s shunting the inductor L and measure the differential voltage V_{cs} as shown in Figure 2. Since it might be desirable to avoid this kind of extra circuitry, we will use another method of inferring the inductor current current I_L from measurements of the switch node voltage V_{sw} and the output voltage V_{out}. We will use V_{cs} as a means for correlating the two measurements.

For the actual measurements shown in the following figures, a single-phase, low-current, non-isolated buck converter was used [12].

Based on our knowledge of the voltage regulator module (VRM), which has an inductor with a specified $L = 15\,\mu H$ with an internal resistance specified as $R_L = 26.4\,m\Omega$, we choose a matching $R_s = 2{\cdot}562\,\Omega = 1.124\,k\Omega$ and $C_s = 1\mu F/2 = 0.5\,\mu F$. Thus, the time constants are closely matched at:

$$L/R_L = 568\,\mu s \approx R_s \cdot C_s = 562\,\mu s$$

When matched in this manner, the current I_L can be measured as:

$$I_L \propto V_{cs} = \frac{V_{cs}}{R_L}$$

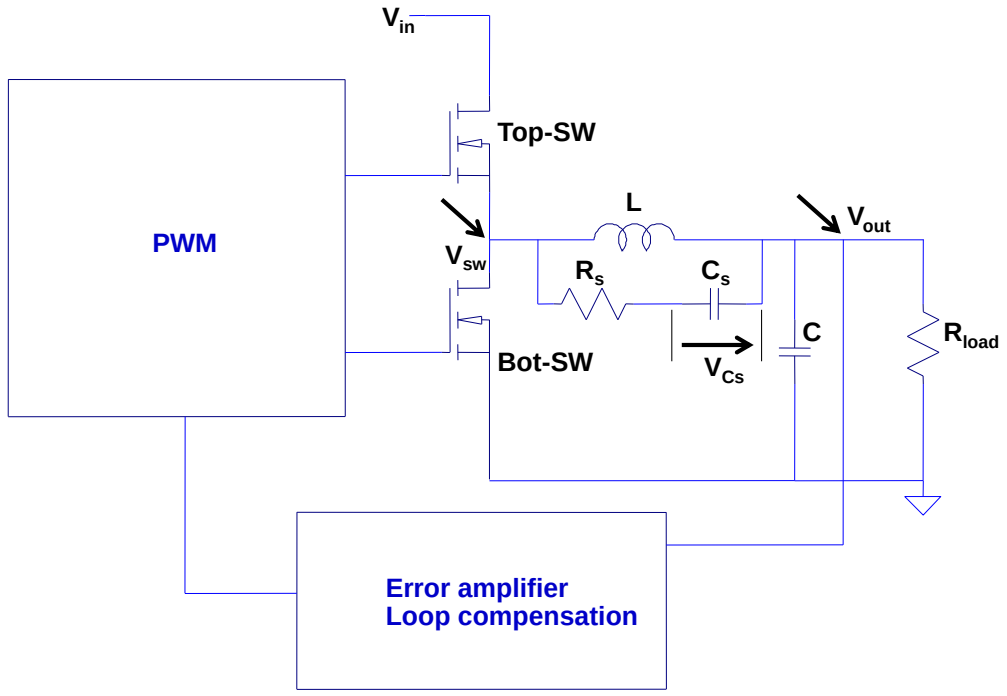


Figure 9: Probing locations for measurement of inductor current I_L

In this particular case, we have $1/R_L = 37.88$, which reduces to an extra gain of 3.788 applied to the measurement of V_{cs} when measured with a differential probe with a gain of 10.

Our plan was to use this measurement as our means for correlation to our alternative method explained in the next section.

Computation of I_L

Given the measurements of the switch node voltage V_{sw} and the output voltage V_{out}, we attempt to calculate the inductor current I_L through processing. Considering the voltage across the inductor, we solve:

$$I_L(s) = \frac{V_{out}(s) - V_{sw}(s)}{s \cdot L + R_L} = \frac{V_L(s)}{s \cdot L + R_L} \tag{3}$$

Note that V_L is simply the difference between V_{out} and V_{sw}. Also, since V_{out} is fairly constant, we can apply a lot of vertical gain (i.e. use a low voltage per division (VDIV) setting) to the channel measuring V_{out}. On the other hand, since V_{sw} encompasses the full swing at the switch node, swinging nominally between ground and V_{in}, in this case a low vertical gain (and therefore high VDIV must be used). This is somewhat problematic because absolute signal-to-noise-ratio (SNR) in the oscilloscope is mostly dependent on the VDIV setting.

Since we will process this digitally, our goal is create a digital filter for processing the sampled waveform. In sampled systems, we can use the approximation of the derivative that lets us convert from the Laplace transform to the z transform:

$$s \approx \frac{1}{T} \cdot \left(1 - z^{-1}\right)$$

Here, T is the sample period $1/Fs$, where Fs is the sample rate.

Making the substitution, we have:

$$I_L(z) = \frac{V_L(z)}{\frac{L}{T} \cdot (1 - z^{-1}) + R_L} = \frac{V_L(z)}{\left(\frac{L}{T} + R_L\right) - \frac{L}{T} \cdot z^{-1}} = \frac{V_L(z)}{\left(\frac{L + R_L \cdot T}{T}\right) - \frac{L}{T} \cdot z^{-1}}$$

$$I_L(z) = \frac{T}{L + R_L \cdot T}\left(V_L(z) + \frac{L}{T} \cdot z^{-1} \cdot I_L(z)\right) = \frac{T}{L + R_L \cdot T} \cdot V_L(z) + \frac{L}{L + R_L \cdot T} \cdot z^{-1} \cdot I_L(z)$$

Taking the inverse z transform, we obtain the difference equation of the inductor current with respect to the voltage across the inductor.

$$I_L[k] = \frac{T}{L + R_L \cdot T} \cdot V_L[k] + \frac{L}{L + R_L \cdot T} \cdot I_L[k-1]$$

The transfer function that produces the inductor current from the inductor voltage can be written as:

$$H_L(z) = \frac{I_L(z)}{V_L(z)} = \frac{\frac{T}{L + R_L \cdot T}}{1 - \frac{L}{L + R_L \cdot T} \cdot z^{-1}} = \frac{T}{L + R_L \cdot T} \cdot \frac{1}{1 - \frac{L}{L + R_L \cdot T} \cdot z^{-1}} = \frac{T}{L + R_L \cdot T} \cdot \frac{z}{z - \frac{L}{L + R_L \cdot T}} \quad (4)$$

When $L \gg R_L \cdot T$:

$$H_L(z) \approx \frac{T}{L} \cdot \frac{1}{1 - z^{-1}}$$

which means that:

$$I_L(t) \approx \frac{1}{L} \int V_L(t) \cdot dt$$

Returning to the transfer function for $H_L(z)$ in (4), we have the DC gain of the function as:

$$G = \frac{T}{L + R_L \cdot T} \cdot \left.\frac{z}{z - \frac{L}{L + R_L \cdot T}}\right|_{z=1} = \frac{T}{L + R_L \cdot T} \cdot \frac{1}{1 - \frac{L}{L + R_L \cdot T}} = \frac{1}{R_L}$$

It turns out that the series R_L is very important, because without it, the computation will diverge.

For nonzero R_L, we prefer to take the gain outside of the filter computation, making the new transfer function:

$$H_L(z) = \frac{1}{R_L} \cdot \frac{R_L \cdot T}{L + R_L \cdot T} \cdot \frac{1}{1 - \frac{L}{L + R_L \cdot T} \cdot z^{-1}} \quad (5)$$

and the new difference equation:

$$R_L \cdot I_L[k] = \frac{R_L \cdot T}{L + R_L \cdot T} \cdot V_L[k] + \frac{L}{L + R_L \cdot T} \cdot I_L[k-1] \quad (6)$$

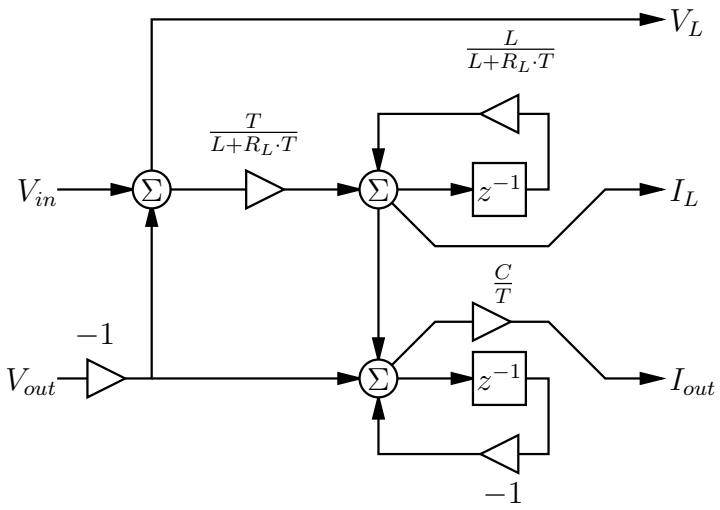


Figure 10: Processing Block Diagram

In our particular measurement, we sample at $100\,MS/s$ for a sample period of $10\,ns$. For our component values, we therefore have a pole in the transfer function in (4) located at:

$$\frac{L}{L + R_L \cdot T} = \frac{15\,\mu}{15\,\mu + 26.4\,m \cdot 10\,n} = \frac{15}{15 + 264 \cdot 10^{-6}} \approx 1 - 17.6 \cdot 10^{-6} = 0.9999824$$

This pole so close to unity can be very problematic in filtering and will require high precision and long filter startup times.

The time constant for this system is:

$$\tau = \frac{L}{R_L} = \frac{15\,\mu}{26.4\,m} = 568.2\,\mu s$$

If we use five time constants for settling, this requires the removal of the first:

$$5 \cdot \tau = 5 \cdot 568.2\,\mu s = 2.841\,ms = 284.1\,kS$$

This could be improved somewhat by sampling at a lower rate, if possible.

Computation of I_{out}

Given the inductor current I_L provided in the last section, we can sum the currents away from the voltage node at V_{out}:

$$-I_L(s) + \frac{V_{out}(s)}{\frac{1}{C \cdot s}} + I_{out}(s) = 0$$

$$I_{out}(s) = I_L(s) - C \cdot s \cdot V_{out}(s)$$

Again, we use the approximation of the derivative that lets us convert from the Laplace transform to the z transform:

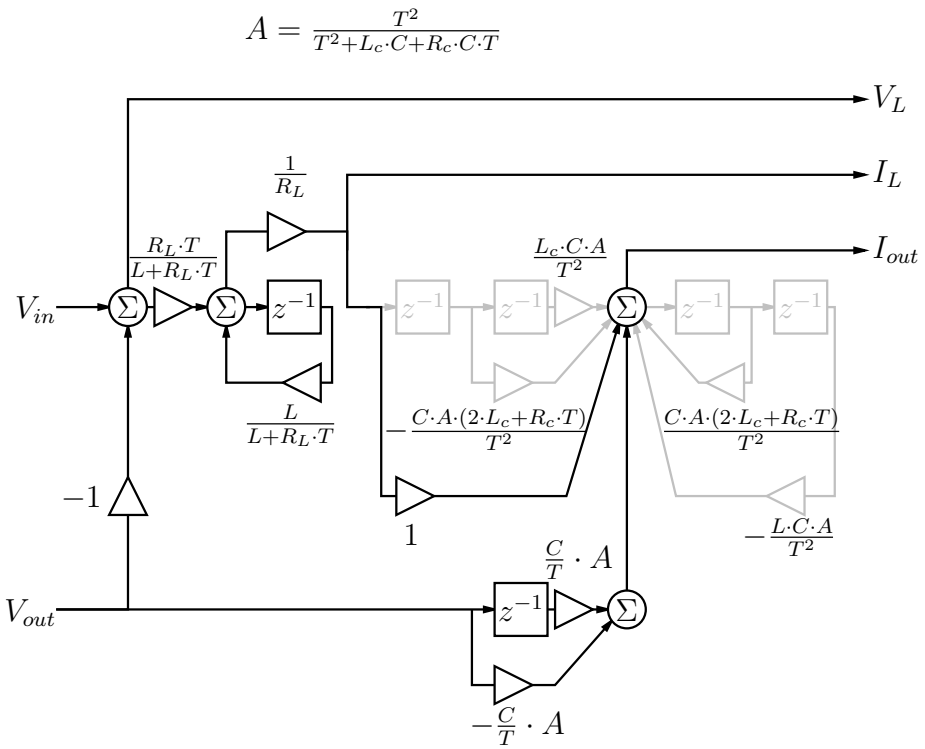


Figure 11: Processing Block Diagram (with capacitor parasitics added)

$$s \approx \frac{1}{T}\cdot\left(1-z^{-1}\right)$$

$$I_{out}(z) = I_L(z) - \frac{C}{T}\cdot\left(1-z^{-1}\right)\cdot V_{out}(z)$$

$$I_{out}[k] = I_L[k] - \frac{C}{T}\cdot\left(V_{out}[k] - V_{out}[k-1]\right)$$

Thus, provided measurements of V_{sw} and V_{out}, we can provide measurements of both the inductor current I_L and the output current I_{out} as shown in Figure 10.

Alternate computation with more parasitics

While the computation in the last section provides for a simple measurement of I_{out}, it does not consider traditional parasitics usually associated with the circuit, most importantly the parasitic inductance L_c and resistance R_c associated with the output capacitor. With the full set of parasitics inserted, we have:

$$-I_L(s) + \frac{V_{out}(s)}{\frac{1}{C\cdot s} + s\cdot L_c + R_c} + I_{out}(s) = 0$$

We define:

$$A = \frac{T^2}{T^2 + L_c\cdot C + R_c\cdot C\cdot T}$$

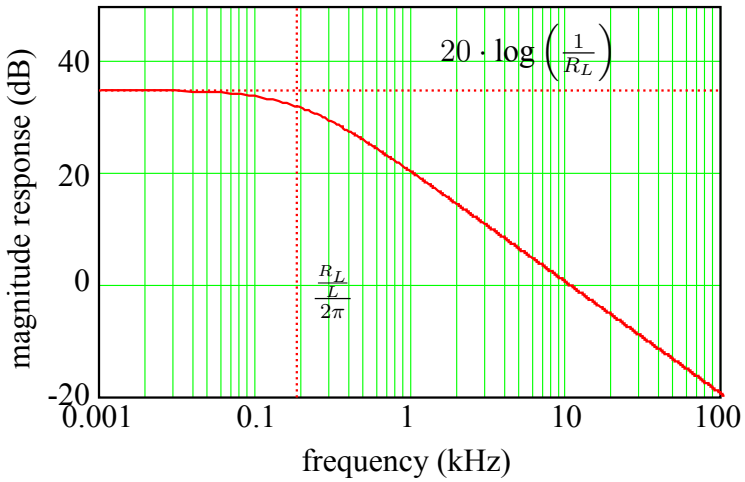


Figure 12: Response of I_L Calculation

and have the difference equation:

$$I_{out}[k] = I_L[k] + -C \cdot A \cdot \frac{2 \cdot L_c + R_c \cdot T}{T^2} \cdot I_L[k-1] + \frac{L_c \cdot C}{T^2} \cdot A \cdot I_L[k-2] + \ldots$$
$$\ldots + C \cdot A \cdot \frac{2 \cdot L_c + R_c \cdot T}{T^2} \cdot I_{out}[k-1] + -\frac{L_c \cdot C}{T^2} \cdot A \cdot I_{out}[k-2] + \ldots$$
$$\ldots + -\frac{C}{T} \cdot A \cdot V_{out}[k] + \frac{C}{T} \cdot A \cdot V_{out}[k-1] \quad (7)$$

It is comforting to find that if $L_c = R_c = 0$, then $A = 1$, and we have:

$$I_{out}[k] = I_L[k] + -\frac{C}{T} \cdot V_{out}[k] + \frac{C}{T} \cdot V_{out}[k-1]$$

In any case, the full processing system that produces all of the desired output waveforms is provided in Figure 11. Here we have grayed out the processing that is a function of the nonzero parasitics for the capacitor R_c and L_c to simplify the understanding.

Noise Considerations in the Measurement and Calculation of I_L

The calculation of I_L involves acquiring waveforms from the switch node V_{sw} and the output V_{out}, taking the difference to form V_L, and processing this voltage with a filter with a transfer function as in (3). There are two potential sources of problems in this measurement and calculation:

1. The measurement of V_{sw} must be taken at a high VDIV setting, which means lower SNR.
2. There is a large amount of gain in the calculation, as indicated in the frequency response in Figure 12.

To understand the meaning of this, consider that in a waveform acquisition channel with a given, specified (assumed white) SNR over a given frequency F, the noise density of the noise added to the waveform is, in dBm/Hz:

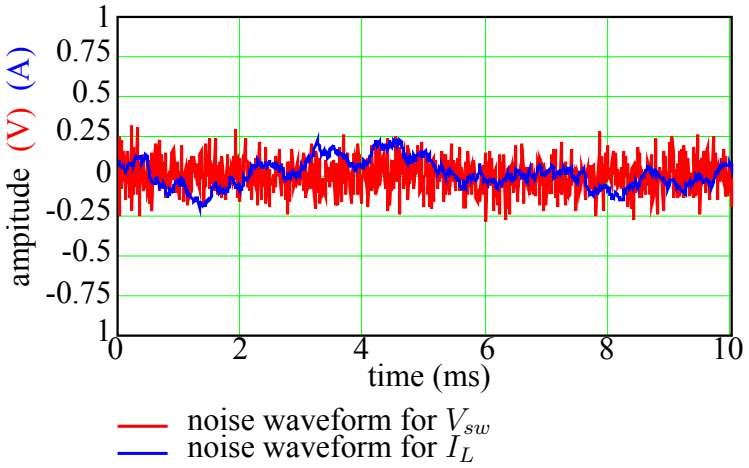


Figure 13: Example Noise Waveforms

$$\mathcal{N}_{dBm} = 20 \cdot \log\left(\frac{VDIV \cdot 4}{\sqrt{2}}\right) + 13.010 - SNR - 10 \cdot \log(F) \tag{8}$$

or, in $V/\sqrt{Hz}$:

$$\mathcal{N}_{rms} = \frac{VDIV \cdot 4}{\sqrt{2}\sqrt{F}} \cdot 10^{-\frac{SNR}{20}}$$

The effect on the noise density of the filtering operation is found by calculating the noise density in (8) and simply adding it to the response, like that calculated in Figure 12. Unfortunately, this does not provide much intuition, so if you want to see the effect, do the following:

1. Determine the sample rate Fs, the number of points in the time domain waveform K, the number of points in the frequency domain waveform $N = K/2$. Assume white noise to the Nyquist rate with $F = Fs/2$.

2. Determine the $VDIV$ as roughly as the peak-peak voltage of V_{sw} divided by 8 divisions.

3. Calculate the constant noise density $\mathcal{N}_{dBm}$ according to (8) and the amount of noise per discrete Fourier transform (DFT) bin as $\mathcal{N}_{dBmperbin} = \mathcal{N}_{dBm} + 10 \cdot \log\left(\Delta f = \frac{1}{N} \cdot \frac{Fs}{2}\right)$.

4. For $n \in 0 \ldots N$, Calculate the noise in the DFT bin as:

$$D_{[n]} = \mathcal{N}_{dBmperbin} + 20 \cdot \log\left(\left|H\left(s = j \cdot 2\pi \cdot \frac{n}{N} \cdot \frac{Fs}{2}\right)\right|\right)$$

5. Convert this to an root-mean-square (RMS) value as:

$$R_{[n]} = 0.223 \cdot 10^{\frac{D_{[n]}}{20}}$$

6. Convert this to an amplitude as:

$$A_{[n]} = \begin{cases} R_{[n]} \cdot \sqrt{2} & n > 0 \\ R_{[n]} & n = 0 \end{cases}$$

7. Convert this to a half DFT with random phase $\theta_{[n]} = \text{rnd}\,(2\pi)$ as:

$$X_{[n]} = \begin{cases} \frac{A_{[n]}}{2} \cdot e^{j \cdot \theta_{[n]}} & 0 < n < N \\ A_{[n]} & otherwise \end{cases}$$

8. Compute the other half of the DFT as, for $n' = 1 \ldots N - 1$:

$$X_{[N+n]} = X^*_{[N-n]}$$

9. Finally, compute the inverse discrete Fourier transform (IDFT).

Example waveforms are provided using $VDIV = 2$, $R_L = 18\,m\Omega$, $L = 15\,\mu H$, $SNR = 35$ in Figure 13. Here we plot the noise on V_{sw} in red and the noise on I_L in blue. The noise in I_L is shown in amperes where we see that the measurement wanders about $\pm 250\,mA$. In the next section, we will show how to deal with this wander.

Sampling V_{sw} to Provide Baseline Inductor Current

Up to now, we have shown that processing V_L to provide I_L should provide very good *dynamic* inductor current, meaning that the high-frequency portion of the inductor current should be accurate provided that the low frequency wander is removed. Thus, if we high-pass filter I_L calculated thus far (to something like $10\,kHz$ in our example), the wander is removed, but we lose the low frequency performance of the calculation.

To restore this low frequency portion, we sample either the difference between V_{in} and V_{sw} on the top portion of V_{sw} or the difference between V_{sw} and ground on the bottom portion of V_{sw}. Using the bottom portion of V_{sw} is somewhat preferable because a measurement between a voltage and ground is simply a single-ended voltage measurement, but a VRM may have a schottky diode in place of the low-side FET and the resistance in this path can be highly variable, and temperature dependent in the least.

No matter where this measurement is taken, it must be gated and must endure the full swing of V_{sw}. The good news is that external circuitry can be used based on the rising or falling edge of V_{sw} to gate the difference waveform in a region where the differential voltage is relatively small. Or, if this cannot be done, and the oscilloscope overdrive recovery is sufficient (these are relatively low frequencies), the oscilloscope can simply be zoomed in on the upper or lower difference portion of $V_{in} - V_{sw}$ or V_{sw}.

In the next section we will describe the processing of this waveform. We will speak in terms of waveform *processors*, which are integral, internal parts of the oscilloscope used for this test, and can even be used and configured by scope users using what is called the *processing web* [13].

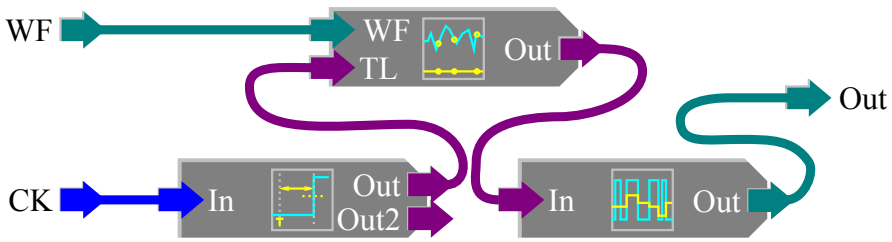


Figure 14: *WaveformSampler* Composite Processor Internals

WaveformSampler

The *WaveformSampler* processor is a composite processor. It has two inputs:

- WF - the waveform to sample
- CK - the clock waveform

It has a single output - the sampled waveform.

It consists internally of three processors:

- A *Time@Level* processor
- A *WaveformSamplerInternal* processor
- A *TrackOfParameter* processor

The internals of the *WaveformSampler* processor are shown in Figure 14. The *Time@Level* processor determines the locations of clock edges on the clock waveform based on specified polarity, threshold, and hysteresis values programmed and passes these values to the TL input of the *WaveformSamplerInternal* processor. The *WaveformSamplerInternal* processor then interpolates values on the waveform supplied at the clock edge times supplied and outputs parameter values that are the coordinates of the sampled waveform where the x ordinate is the clock edge time and the y ordinate is the value of the waveform at that time. The *TrackOfParameter* processor is utilized to turn the parameter values back into a waveform representing the sampled waveform. The track produces a waveform with the same sample locations as the supplied waveform to the *WaveformSampler*.

InductorBaselineCurrent

The *InductorBaselineCurrent* processor is a composite processor. It has one input: VSS - The voltage at the switch (saturated). This is the switch voltage severely overdriven but showing the switch on voltage on the screen. It has one output: ILB - The inductor baseline current.

The processor consists internally of three processors:

- An *Eres* processor
- A *WaveformSampler* processor
- A *Rescaler* processor

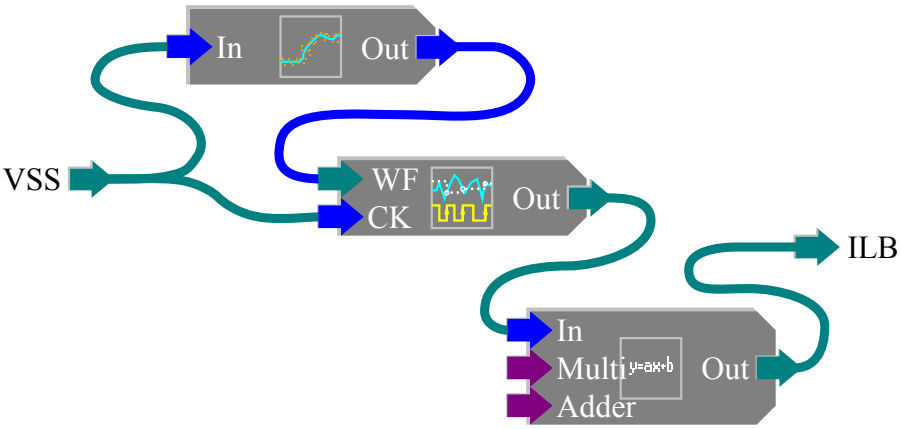


Figure 15: *InductorBaselineCurrent* Composite Processor Internals

The internals of the *InductorBaselineCurrent* processor are shown in Figure 15.

The baseline current is defined as the average inductor current over one cycle of the switched voltage waveform. It is used to augment the inductor dynamic current defined by dynamic voltage across the inductor. The inductor baseline current is calculated by sampling a smoothed version of the over-driven switch voltage somewhere around the middle to the end of the switch voltage cycle. Since this essentially a per-cycle measurement of the voltage drop across the FET switch when the switch is connected to ground, the inductor current is proportional to this voltage. Therefore, the *Rescaler* processor is utilized to provide the gain and offset for such a conversion, and to supply the new units of Amps. The gain and offset in the rescaler will need to be determined through some sort of calibration step.

Full Inductor Current Processing

In Figure 16 we see a processing web setup to perform the desired power integrity measurements. Specifically, the processing takes in three voltage waveforms:

- VS - the voltage at the switch (the voltage at the input to the inductor). This voltage waveform should be arranged such that it maximizes the vertical scale of the scope, but does not go offscreen.
- VO - the voltage at the output (the voltage at the output side of the inductor). This voltage waveform should be arranged such that under all conditions (including transient conditions, the waveform does not go offscreen. It should include zero volts.
- VSS - the voltage at the switch overdriven into the scope such that bottom portion of the switch voltage is onscreen where it settles after the overdrive recovery. The top portion of this waveform will be far offscreen above.

The output of this processing is three waveforms:

- VL - the voltage across the inductor, formed as a simple subtraction: $VL = VS - VO$.
- IL - the current through the inductor.

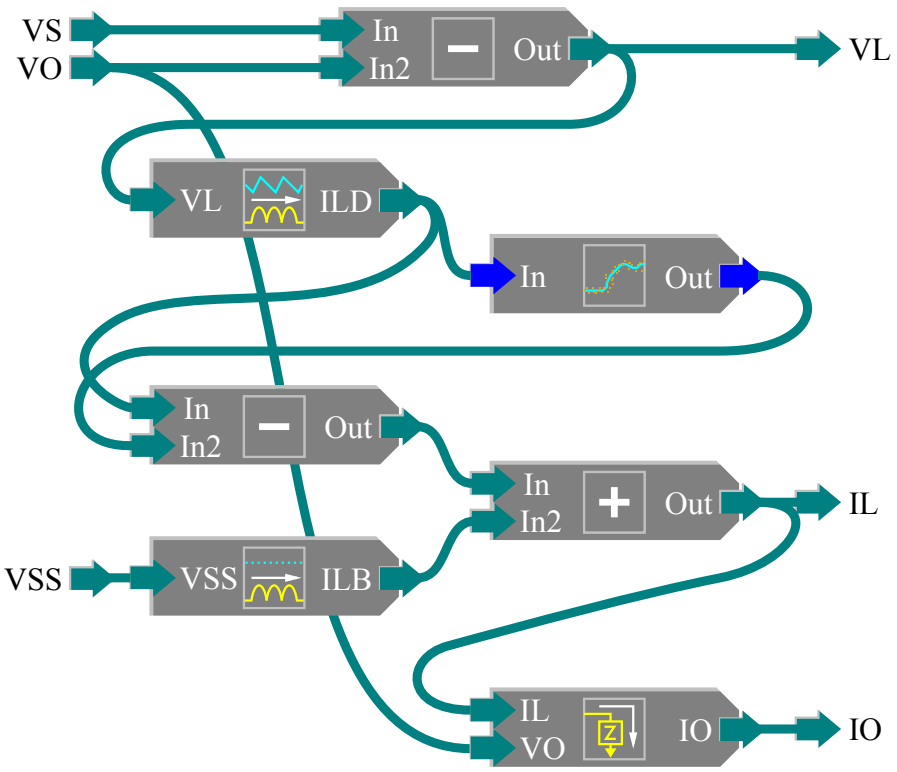


Figure 16: Power Integrity Scope Processing

- IO - the current into the load.

Optionally, we might want to provide power waveforms formed by taking the product of VO and IO and VS and IL, but that is simple processing.

The key complexity here is the computation of IL. The first part of the processing forms the *dynamic* inductor current ILD. This is performed by applying the difference equation in (6). Typically, because of small R_L, this will perform much like an integrator on V_L. The output will tend to look like a sawtooth current waveform. Because of integration, it will highly amplify very low frequency noise and the waveform will have a low frequency wander in it. This amplification can be seen by the DC gain $1/R_L$, where R_L tends to be very small. Therefore, the wander is removed by subtracting a smoothed waveform from the ILD waveform output. The result is the sawtooth current waveform with the wander removed.

To restore the baseline inductor current, the overdriven waveform VSS is supplied to a processor that produces the per-cycle baseline current ILB. This production of the baseline inductor current is provided in §. The baseline inductor current is added to the sawtooth dynamic current and output as IL.

Using the waveforms VO (supplied) and the computed IL, the output current IO is produced by a processor that implements the difference equation in (7).

Experimental Results

To test our measurement methods, we connected a VRM as shown in Figure 17. Here, we have a combination of a 1% $5\,\Omega$ static load with a parallel $0.975\,\Omega$ transient load. We used an AWG to drive the gate of

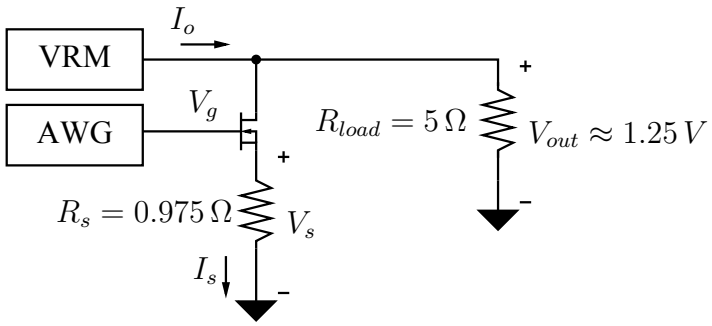
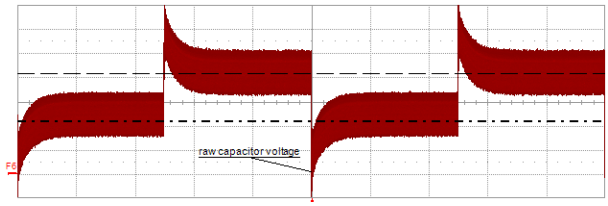


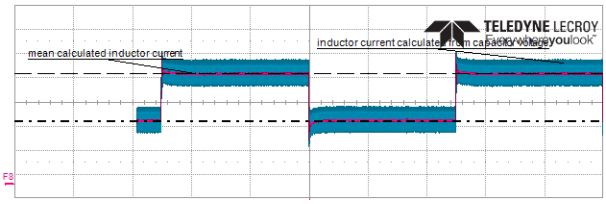
Figure 17: Transient Load Circuitry

Circuit Element	Expected Value	Actual Value
Inductance L	$15\,\mu H$	$15\,\mu H$
Parasitic Resistance R_L	$26.4\,m\Omega$	$18\,m\Omega$
Shunt R R_s	$1.124\,k\Omega$	$1.1\,k\Omega$
Shunt C C_s	$0.5\,\mu F$	$0.46\,\mu F$

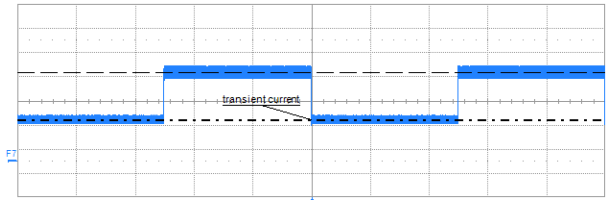
Table 1: Circuit Element Values



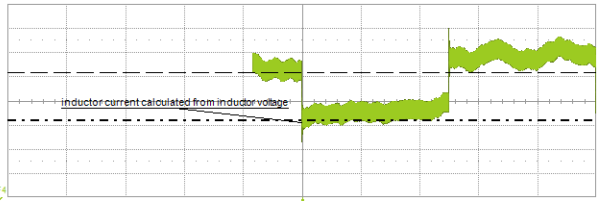
(a) raw capacitor voltage V_{cs}



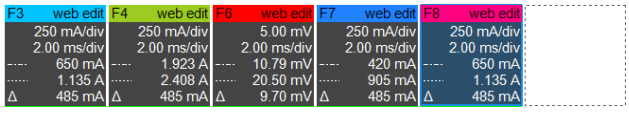
(b) inductor current calculated from V_{cs}



(c) transient current



(d) inductor current calculated from V_L



(e) scope settings

Figure 18: inductor current screenshots

a FET to modulate the transient load.

Originally, when trying to correlate inductor current measurements, we assumed that the inductor current would be directly proportional to the shunt capacitor voltage. This is because we assumed the values provided in Table 1 and thus:

$$\frac{R_L}{L} = 1760 \approx \frac{1}{R_s \cdot C_s} = 1779$$

This assumption leads to an assumed DC gain of:

$$\frac{R_s \cdot C_s}{L} = 37.467$$

or 3.7567 applied to the voltage measured by an active, differential probe with a gain of $10\times$ [14]. The assumed values would lead to a disparity of:

$$\frac{1779}{1760} = 1.011$$

or a 1.1% disparity. But when we measured the capacitor voltage waveform, we obtained the waveform in Figure 18a. This waveform led to improbable results in two ways:

1. There is clearly is mismatch between the high-frequency gain and the low-frequency gain exhibited in the shape of the waveform as the initial value after the step predicts the high-frequency gain and the final, settled value predicts the low-frequency gain. These values are off by about 50%.

2. The final, settled values were way off based on the nature of the static and transient load circuitry.

To address this, we performed a calibration of the system. This calibration was performed in two ways:

1. We measured the DC response of the system by stepping the voltage on the gate of the FET providing the transient.

2. We measured the AC response of the system by then sweeping sinusoids through various frequencies, measuring the capacitor voltage.

We swept various DC gate voltages and adjusted the offset on measurement and the gain value until we found good agreement with the load current, as shown in Figure 19. The load current was directly measured as the current through the 1% $5\,\Omega$ static load with a $1.25\,V$ output voltage and the voltage across the $0.975\,\Omega$ from the source of the FET to ground V_s. We found a voltage offset correction of $1.85\,mV$ and most surprising, a gain of 56, which implies that the parasitic resistance $R_L = 18\,m\Omega$. We obtained a good linear operating region of the FET between 2 and $2.4\,V$ where we obtain load currents of $650\,mA$ and $1.135\,A$ respectively.

Then, we swept various sinusoidal gate voltages of $400\,mV_{pp}$ with $2.2\,V$ of offset and measured the peak-peak voltage across the capacitor V_{cs}. Simultaneously, we monitored the peak-peak voltage ripple on the output and the peak-peak voltage V_s. This measurement is shown in Figure 20. Here we see the expected $10\,mV$ peak-peak voltage for frequencies below $100\,Hz$, after which it rises to approximately $15\,mV$. After $10\,kHz$, we see the voltage rise, then fall dramatically. This is, as we see, a result of the control loop running out of gas as the voltage ripple on the output increases. We recorded the peak-peak measurement of V_D in our calibration and found it to be constant to within a current of $\pm 10\,mA$ from DC to $10\,kHz$. If it weren't constant, we would have factored that into our calculations.

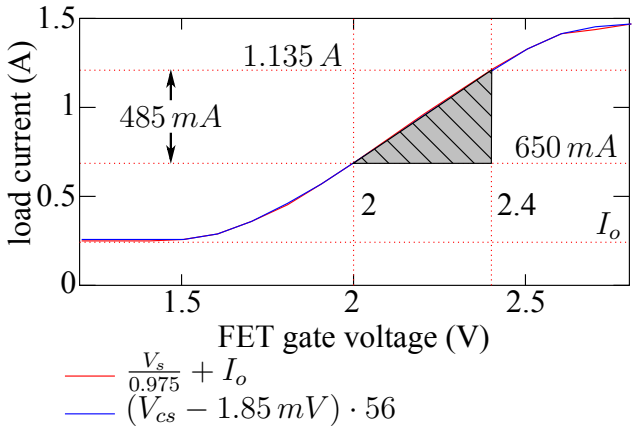


Figure 19: DC Current Calibration

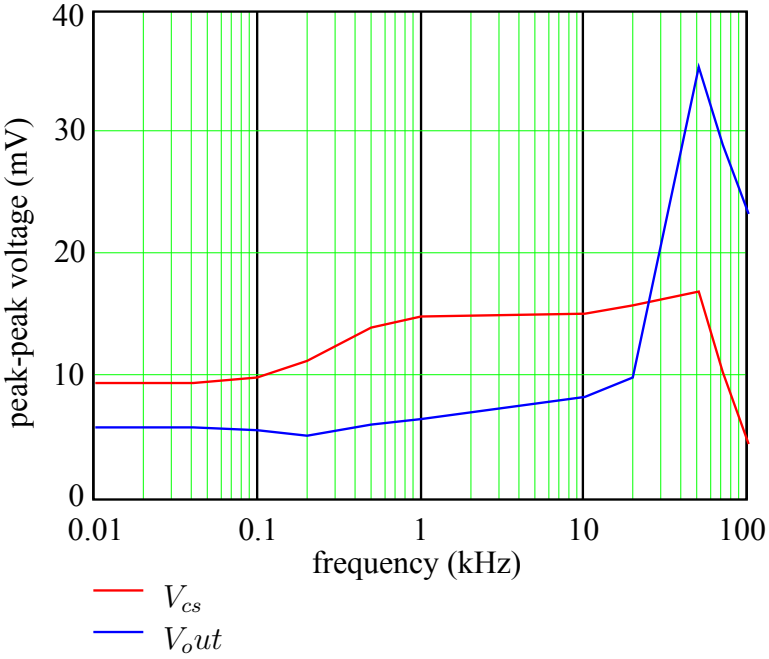


Figure 20: AC Current Calibration

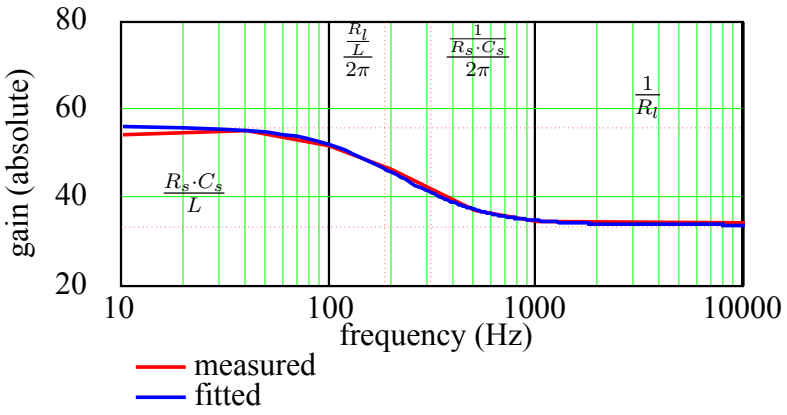


Figure 21: Fitted Gain

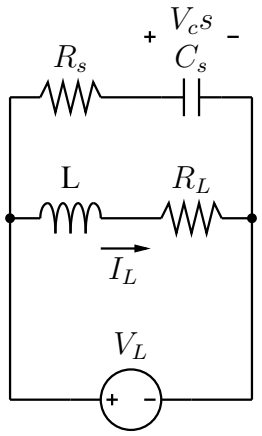


Figure 22: Inductor Current Sense Circuit

Looking only at the performance between $10\,Hz$ and $10\,kHz$, we fit the reciprocal of the response onto the model provided and obtained the agreement as shown in Figure 21. This agreement was obtained by adjusting the circuit values expected to those shown in the right column of Table 1. These changes were all found to be within the known tolerances of the components, except for the parasitic resistance of the inductor, whose tolerance is unknown.

Now that we know that a simple multiple of V_{cs} could not be used, we set about determining some processing that could be applied to V_{cs} to obtain a better measurement of the inductor current by examining the transfer function for the measurement

The equivalent circuit relating to the measurement of inductor current provided in [4] is shown in 22. Analyzing this circuit, we have:

$$I_L = \frac{V_L}{s \cdot L + R_L} = \frac{\frac{V_L}{L}}{s + \frac{R_L}{L}}$$

$$V_{cs} = \frac{V_L}{R_s + \frac{1}{C_s \cdot s}} \cdot \frac{1}{C_s \cdot s} = \frac{\frac{V_L}{R_s \cdot C_s}}{s + \frac{1}{R_s \cdot C_s}}$$

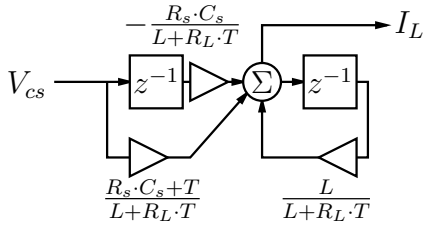


Figure 23: Inductor Current Calculation from V_{cs}

Therefore, the inductor current relative to the voltage across C_s is:

$$H(s) = \frac{I_L(s)}{V_{cs}(s)} = \frac{s + \frac{1}{R_s \cdot C_s}}{s + \frac{R_L}{L}} \cdot \frac{R_s \cdot C_s}{L}$$

In sampled systems, we use the approximation of the derivative that lets us convert from the Laplace transform to the z transform:

$$s \approx \frac{1}{T} \cdot \left(1 - z^{-1}\right)$$

and obtain:

$$H(z) = \frac{I_L(z)}{V_{cs}(z)} = \frac{\frac{R_s \cdot C_s + T}{L+R_L \cdot T} - \frac{R_s \cdot C_s}{L+R_L \cdot T} \cdot z^{-1}}{1 - \frac{L}{L+R_L \cdot T} \cdot z^{-1}}$$

which allows us to write the difference equation:

$$I_{L[k]} = I_{L[k-1]} \cdot \frac{L}{L + R_L \cdot T} + V_{cs[k]} \cdot \frac{R_s \cdot C_s + T}{L + R_L \cdot T} - V_{cs[k-1]} \cdot \frac{R_s \cdot C_s}{L + R_L \cdot T}$$

In utilizing this as an infinite impulse response (IIR) filter for processing, we need to estimate the time for this filter to settle. To do this, we make a good guess at the form of the step response as:

$$S_{[k]} = A + B \cdot \left(1 - e^{-k \cdot C}\right)$$

We know that when $k = 0$, we have $S_{[0]} = A$ and that A is the high frequency gain of the system[1]:

$$A = \lim_{s \to \infty} H(s) = \frac{R_s \cdot C_s}{L}$$

As $k \to \infty$ we should obtain the low frequency gain of the system:

$$A + B = \lim_{s \to 0} H(s) = \frac{1}{R_L}$$

and thus:

[1] We usually remember the initial and final value theorem as $f(0) = \lim_{s \to \infty} s \cdot F(s)$ and $f(\infty) = \lim_{s \to 0} s \cdot F(s)$, but this is for the *impulse response*. Here we are computing the initial and final values of the *step response* which involves first dividing by s.

$$B = \frac{1}{R_L} - \frac{R_s \cdot C_s}{L}$$

To obain the constant C, solve for the second point calculated $I_{l[1]}$:

$$I_{L[1]} = \frac{R_s \cdot C_s}{L} + \left(\frac{1}{R_L} - \frac{R_s \cdot C_s}{L}\right) \cdot \left(1 - e^C\right) = \frac{R_s \cdot C_s}{L} \cdot \frac{L}{L + R_L \cdot T} + \frac{T}{L + R_L \cdot T}$$

and obtain:

$$C = \ln\left(\frac{L}{L + R_L \cdot T}\right) = \ln\left(1 - \frac{R_L \cdot T}{L + R_L \cdot T}\right)$$

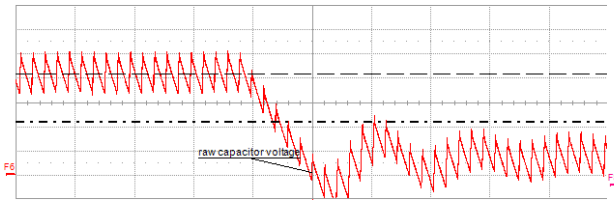
and since the amount added to one is very small generally, the time constant can be approximated as:

$$\tau \approx \frac{(L + R_L \cdot T)}{R_L}\, s = \frac{(L + R_L \cdot T)}{R_L \cdot T}\, samples$$

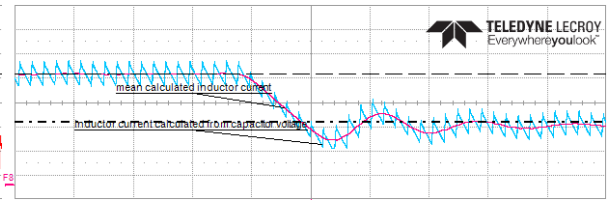
We generally use five time-constants, but we could economize this if we want if, instead of asking the filter to settle to 99% of the final value, we require that enough time is allowed for the high- and low-frequency gains to match. In other words, we could raise or lower the settling time allowed depending on the magnitude of the difference between the high- and low-frequency gains encapsulated in the magnitude of $1/R_L - R_s \cdot C_s/L$.

In our situation with the actual fitted values as shown in Table 1, we have a time-constant of $833\,\mu s$. With five time-constants allowed for settling, we have $4.167\,ms$ we must clip from the front of the processed waveform and at a sample rate of $100\,MS/s$, this amounts to $417\,kS$. The processed waveform is shown in the upper-right quadrant of Figure 18. To verify the proper functionality, in Figure 18c, we have a square-wave transient applied by applying a square-wave that moves between $2\,V$ and $2.4\,V$ to the gate of the FET, which applies a $485\,mA_{pp}$ current transient at the load. The cursors are placed at the bottom and top of the transient current and the measurements are shown in Figure 18e. In the Figure 18b, we see our inductor current waveform processed by passing the measured voltage across the capacitor in Figure 18a through the aforementioned IIR filter. We low-pass filter this waveform to provide the mean inductor current and we can see by looking at the cursor measurements in Figure 18e that there seems to be good agreement in a DC sense. Good AC performance is assumed based on the lack of the huge overshoot present in the raw capacitor voltage measurement. Note that the processed waveform in Figure 18b has the first $4.167\,ms$ removed.

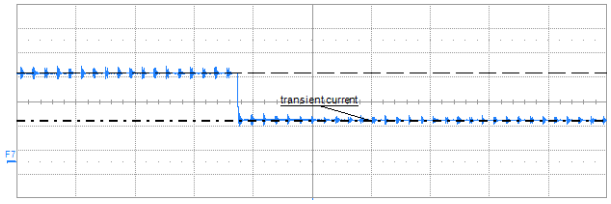
Now that we have a reasonable measurement of the inductor current that can be relied upon, we compare this measurement to that calculated from the voltage across the inductor as provided by the processing in (6). This calculation is shown in Figure 18d. As expected, the low-frequency response in this measurement is very noisy and the waveform wanders quite a bit. We will need to deal with the low-frequency performance in another way. Examining Figure 24 where we've zoomed in horizontally and aligned the waveform vertically manually, we see that the dynamic behavior shows quite good agreement and it seems that we only need to deal somehow with the low frequency behavior.



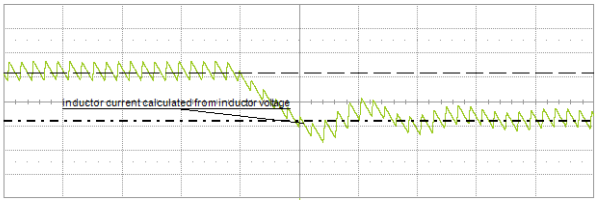
(a) raw capacitor voltage V_{cs}



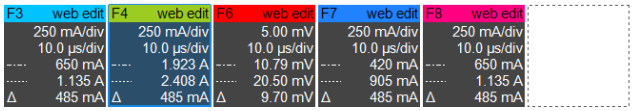
(b) inductor current calculated from V_{cs}



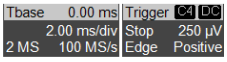
(c) transient current



(d) inductor current calculated from V_L



F3	web edit	F4	web edit	F6	web edit	F7	web edit	F8	web edit
	250 mA/div		250 mA/div		5.00 mV		250 mA/div		250 mA/div
	10.0 µs/div		10.0 µs/div		10.0 µs/div		10.0 µs/div		10.0 µs/div
	650 mA		1.923 A		10.79 mV		420 mA		650 mA
	1.135 A		2.408 A		20.50 mV		905 mA		1.135 A
Δ	485 mA	Δ	485 mA	Δ	9.70 mV	Δ	485 mA	Δ	485 mA



Tbase	0.00 ms	Trigger	C4 DC
	2.00 ms/div	Stop	250 µV
2 MS	100 MS/s	Edge	Positive

(e) scope settings

Figure 24: inductor current screenshots (zoomed)

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