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Measuring Current and Current Sharing of DC-DC Converters

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Abstract

The measurement of current in power converters, especially in switching DC-DC converters, is a very important task. This paper will establish a practical range for the time constants that we need to cover and will illustrate the effectiveness of DSP-based corrections for a few selected time-constant values. It will be shown and illustrated that even though the voltage across the capacitor of the RC element rides on the 'quiet' output voltage, for multiple reasons the common-mode voltage range and common-mode rejection of the measurement circuit is still very important. This paper analyzes the noise floor, dynamic range, confidence level and measurement speed of the impedance measurement solution.

Author(s) Biography

Istvan Novak: is a Senior Principle Engineer at Oracle. Besides signal integrity design of high-speed serial and parallel buses, he has been engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is a Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies and has twenty five patents in the areas of power distribution design and precision measurements.

Peter J. Pupalaikis was born in Boston, Massachusetts in 1964 and received the B.S. degree in electrical engineering from Rutgers University, New Brunswick, New Jersey in 1988. He joined LeCroy Corporation (now Teledyne LeCroy), a manufacturer of high-performance measurement equipment located in Chestnut Ridge, New York in 1995 where he is currently Vice President, Technology Development, managing digital signal processing development and intellectual property. His interests include digital signal processing, applied mathematics, signal integrity and RF/microwave systems.

Prior to LeCroy he served in the United States Army and has worked as an independent consultant in embedded systems design. Mr. Pupalaikis holds forty-three patents in the area of measurement instrument design and has contributed a chapter to one book on RF/microwave measurement techniques. In 2013 he became an IEEE fellow for contributions to high-speed waveform digitizing instruments. He is a member of Tau Beta Pi, Eta Kappa Nu and the IEEE signal processing, instrumentation, solid state circuits, and microwave societies.

Lawrence Jacobs was born in Palo Alto, California, in 1963. He received the B.S. degree in electrical engineering from Stanford University and the M.S. degree in electrical engineering from Santa Clara University in 1985 and 1990, respectively. He joined LeCroy Corporation (now Teledyne LeCroy), a manufacturer of high-performance measurement equipment located in Chestnut Ridge, New York in 1999 where he is presently managing the probe development group. His interests include precision analog and high frequency electronics design and measurement. Mr. Jacobs holds fourteen patents.

I. Introduction

The measurement of current in power converters, especially in switching DC-DC converters, is a very important task. The current information is needed also internal to the converter for the safe operation of the unit, by creating over and under current warnings and protection limits. High-current state-of-the-art converter designs may make current information available to the user through digital bus interfaces, or in some cases as an analog signal proportional to the current. Externally the current information can be used as part of the efficiency and power consumption calculations.

An important usage of current measurement is the quality check and design validation of the circuit. In multi-phase DC-DC converters a high-priority application and task of the current measurement is to check and validate the proper current sharing among the phases. While under static load conditions this may be an easy task, doing the same under dynamic conditions is not a trivial measurement. Measuring (or inferring) current is also essential in impedance measurements.

[1] introduced the concept of an oscilloscope-based time-domain measurement that in its most general form can perform various transfer-function, impedance and current measurements as well. The current measurement can be assisted by an external RC element connected across the switching inductor and by measuring the voltage across the capacitor, as shown in *Figure 1*.

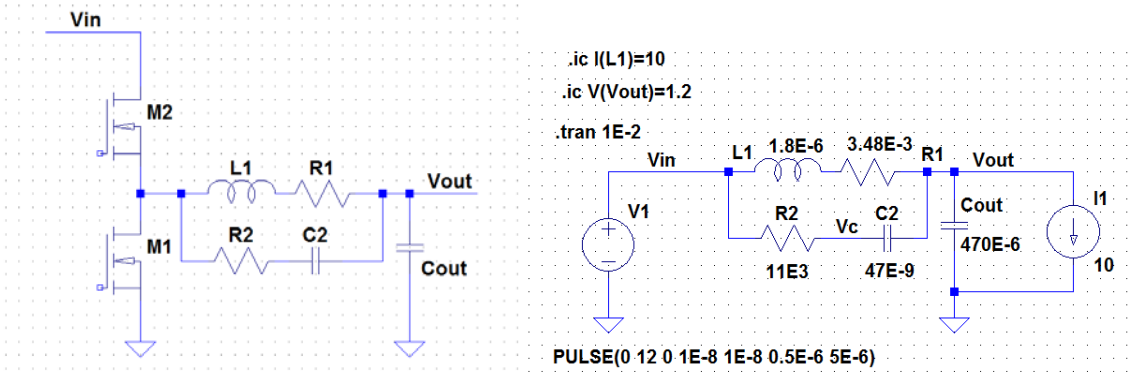

***Figure 1**: Current-measuring RC circuit in a buck switching regulator output (left). For sake of simplicity the control circuit and load are not shown. LTSPICE circuit to simulate the transient response is shown on the right.*

The Vin DC input voltage is chopped up by the two switches and a pulse stream feeds the L1-R1 main output path, where R1 represents the internal resistance of the L1 power inductor. The current in the inductor varies in a saw-tooth fashion with an average value equaling the load current. If we match the L1/R1 time constant to the R2C2 time constant, the voltage waveform across the C2 capacitor will be the same as the inaccessible voltage drop across R1. If we know R1, from the voltage across the C2 capacitor we can calculate the current through the inductor.

This long has been one of the favorite implementations to measure the inductor current in switching converters. While in discrete hardware implementations the time constants of the inductance and resistance of the inductor and the time constant of the external RC circuit have to match, as it was shown in [1], the differences in time constants can also be resolved and corrected by the DSP engine of the measurement setup. In Section II we establish a practical range for the time constants that we need to cover and will illustrate the effectiveness of DSP-based corrections for a few selected time-constant values. It will be shown and illustrated that even though the voltage across the capacitor of the RC element rides on the 'quiet' output voltage, for multiple reasons the common-mode voltage range and common-mode rejection of the measurement circuit is still very important. Since the RC element has to be connected across the switch node and the output of the converter, this is exactly the area of the converter where the stray magnetic and electric fields are the highest, making the connection geometry and connection topology very important. In the second section of the paper we look at important practical aspects of current measurements and correlate measurement data to simulation results. In the third section measurement data is shown on various boards. Note that the purpose of this paper is not to analyze or characterize the DUTs, which in some cases were set intentionally to states that different features of the measurements can be shown.

II. Practical implementation considerations

II.1. Current measurements

To illustrate the concept from *Figure 1*, we use one of the phases of a three-phase evaluation board [2]. The power inductor's inductance is nominally 1.8 uH, its maximum DC resistance according to the data sheet is 3.48 mOhm, the switching frequency is 220 kHz. The output voltage was set to 1.2V. The simulated lossless waveforms are shown in *Figure 2* for a 10A DC load.

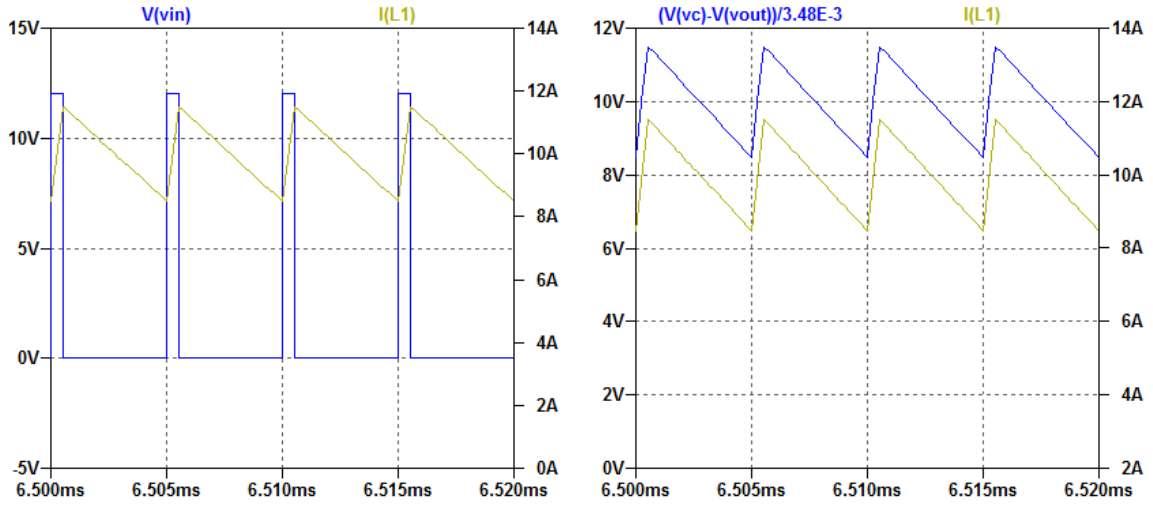

Figure 2: *Simulated waveforms of a buck converter with current-measuring RC elements across the inductor.*

On both plots the horizontal scales show time. The left plot shows the switch-node voltage fluctuating between 0 and 12V and the current through the inductor. The inductor ripple current is $3A_{p-p}$, the average current equals the 10A DC load current. On the right, the current through the inductor and the scaled voltage across the 47 nF C2 capacitor are compared. The two vertical axis are intentionally offset to allow easy comparison of the two waveforms.

The circuit in *Figure 1* has the component values of R2 and C2 selected such that their time constant matches the L1/R1 time constant. Note that we have one requirement (for the time constant) but two component values to select (R2 and C2). This means we can satisfy the requirement with an infinite number of different component values. Practical considerations will limit the choice. To allow repeatable and consistent measurement, the C2 capacitor should have low temperature and DC/AC bias sensitivity and should have low parasitics (low series resistance and series inductance). Small physical size is a plus. All these requirements favor the choice of NPO ceramic capacitors. Their available capacitance in small case sizes is limited though today to about 100 nF or less. There is an incentive to use the highest possible C2 value since this will minimize R2, which in turn minimizes the effect of any loading from the processing circuit (probe) differentially and/or in common mode. On the other hand, too low R2 value may interact with the inherent series resistance (ESR) of C2. For the circuit shown above, a 47 nF C2 value is assumed, yielding 11 kOhm for R2. *Figure 2* illustrates that in this nominal and ideal case the scaled voltage waveform across C2 is identical to the current waveform through the inductor.

While we get an exact replica of the current waveform across C2 if the time constants match, adjusting the time constant to each application is tedious and may be error prone. As it was suggested in [1], an easier way is to select an approximate time constant for R2*C2 that is close, but not necessarily identical and compensate for the difference in the post-processing of the voltage across C2. With this in mind, *Table 1* shows a choice of component values, which cover many of the applications in today's DC-DC converters.

	R2 [Ohm]	C2 [F]	Rs [Ohm]	Approximate.time constant [s]
Probe-tip 1	17.8k	5.6n	10	100u
Probe-tip 2	8.45k	47n	1.18	400u
Probe-tip 3	16k	47n	0	800u
Probe-tip 4	34k	47n	1.18	1600u

***Table 1**: A possible choice of four sets of probe tip values.*

The four probe tips cover a 16:1 range of time constants. The purpose of the Rs resistor will be explained later. To show the effect of the potential time-constant mismatch, we plot the simulated waveforms of the circuit from *Figure 1*, except we step R2 and C2 values through the choices shown in *Table 1*. The actual inductor current and switch-

node voltage waveforms will be no different and therefore only the comparison plots of currents are shown.

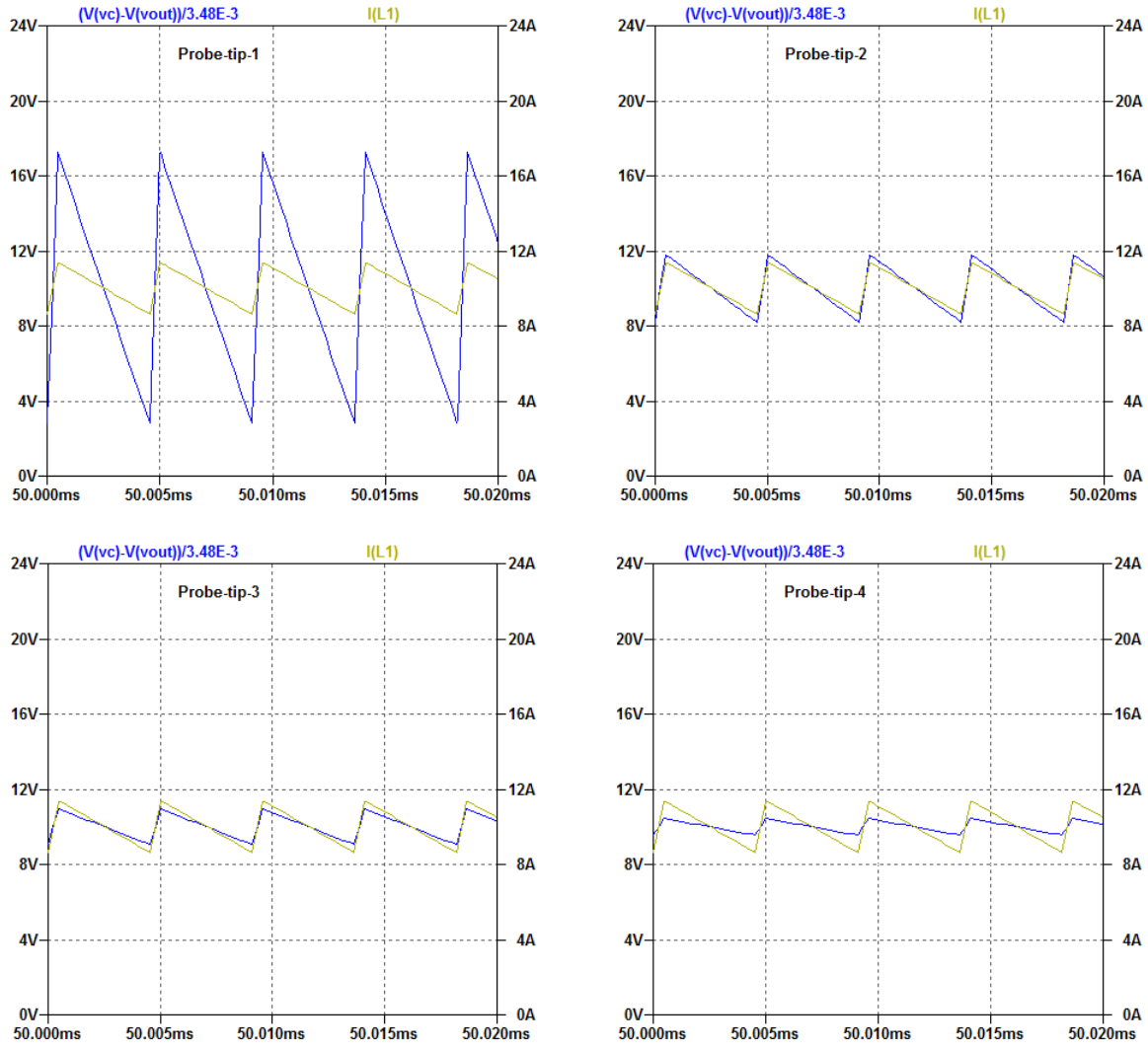

Figure 3: *Inductor current and RC probe-tip reading comparison for three different probe-tip time constants from Table 1. Upper left, probe-tip 1, upper right: probe-tip 2, lower left: probe-tip 3, lower right: probe-tip 4.*

Note that the average value of all three plots is equal to the 10A DC load current. What depends on the good or bad matching of the time constants is the AC portion of the ripple current. This is also illustrated in *Figure 4*, where we sweep the C2 capacitor value over a 100:1 range, from 1 nF to 100 nF. The frequency dependence and transfer function of this circuit implementation was shown in [3]. The correlation between the simulated and measured waveforms are shown in *Figure 5*. The three probe tips used for this correlation had the component values as shown in *Table 1* for probe tips 2, 3 and 4. The time constants cover approximately a 4:1 range. The DUT DC load current was zero.

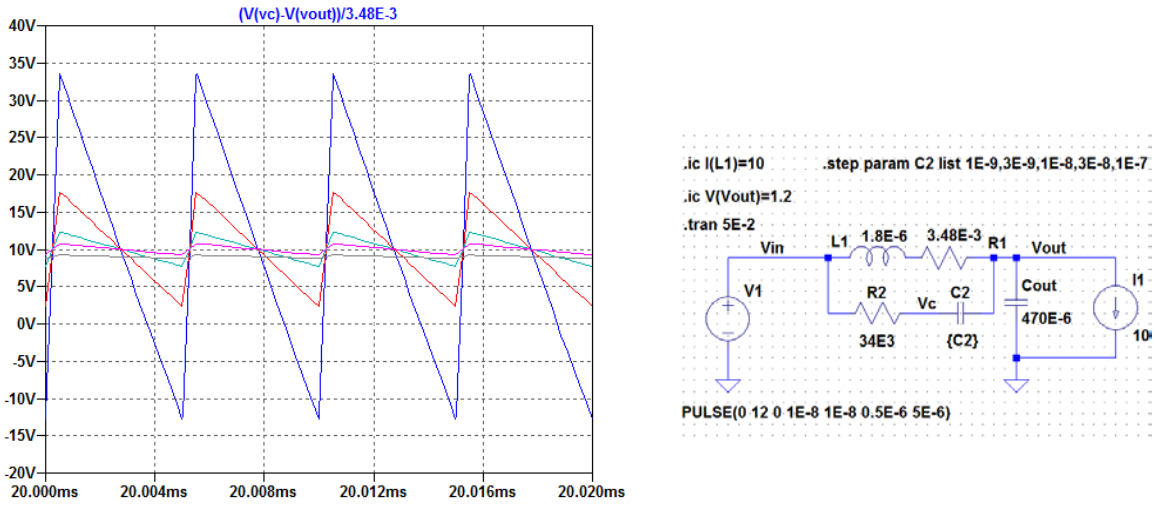

Figure 4: Reconstructed inductor current waveforms with different C2 values stepping through 1nF, 3nF, 10nF, 30nF and 100nF values.

Due to the forced continuous synchronous nature of the converter operating mode, the inductor current fluctuates above and below zero, with approximately zero average. The small offsets were left in on purpose to separate the waveforms vertically. The similar correlation with 10A DC load is shown in *Figure 6*. Here we see a systematic difference between the simulated and measured values. The simulated values average around 34.8 mV, which is the voltage drop we expect from a 10A current flowing through a 3.48 mOhm resistor. The measured waveforms, however, calculated for integer number of periods, average at 30.7 mV, 12% lower than expected. The reason for this difference is that for the simulations we used the guaranteed maximum value of the inductor's DC resistance. In reality, the resistance is likely less. If the DC load current is in fact 10A, it would suggest a 3.07 mOhm resistance. This was checked and correlated in two ways: the impedance of the power inductor was measured (with 0 DC bias current and small-signal excitation, see *Figure 7*) and the DC load current was measured with a precision shunt resistor and voltmeter. It was found that the low-frequency resistance of the inductor was 2.94 mOhm at 1 kHz (15% lower than the guaranteed maximum value on the data sheet) and the actual load current was 2% higher. The figure also shows the extracted series inductance. Below 1 kHz the curve slopes down because the extraction cannot work with an almost resistive impedance. We also need to ignore the extracted inductance values above 100 kHz, where the approaching parallel resonance of the part creates the sharp upslope in the impedance real part and extracted inductance alike. From the ESL curve we can conclude that at the 220 kHz switching frequency a 1.7 uH inductance is a good estimate.

As it is predicted by the simulation shown in *Figure 4*, the DC average does not depend on the RC time constant of the probe tip, but the size of the inductor ripple current does.

Since in the entire range of the probe tip time constants these values are much longer than the period of the DUT switching frequency, the shape of the extracted waveform stays

approximately the same, just its peak-to-peak value changes. Assuming that the ripple voltage on the output is small, we can estimate the peak-to-peak inductor current ripple from the DC output voltage and the OFF time:

$$v \cdot t = L \cdot i$$

After rearranging for L and substituting the nominal numbers, we get

$$i = \frac{v \cdot t}{L} = \frac{1.2 \cdot \frac{0.9}{220k}}{1.8\mu} = \frac{1.2 \cdot 0.9}{1.8 \cdot 0.22} = 2.73A$$

If we use the measured 1.7 uH inductance value, the calculated inductor ripple current becomes 2.89 $A_{p\text{-}p}$. The expression above also tells us that while the DC content of the voltage across C2 depends on the Rdc value of the inductor (R1 in *Figure 1*), the extracted inductor ripple current component does not depend on the resistance of the inductor.

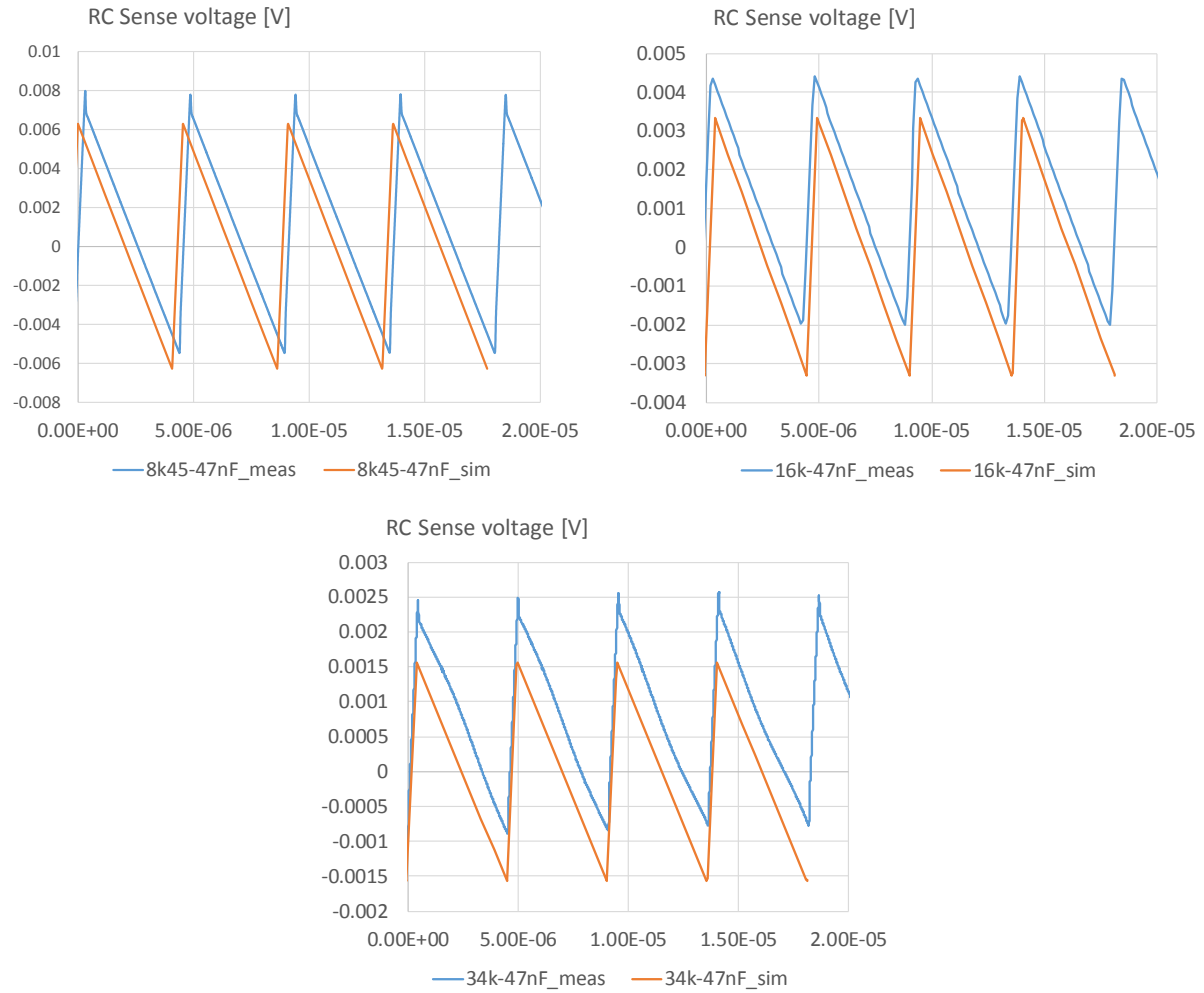

Figure 5: *Correlation between simulated (with nominal values, orange traces) and measured (blue traces) RC sense voltages with 0A DC load current.*

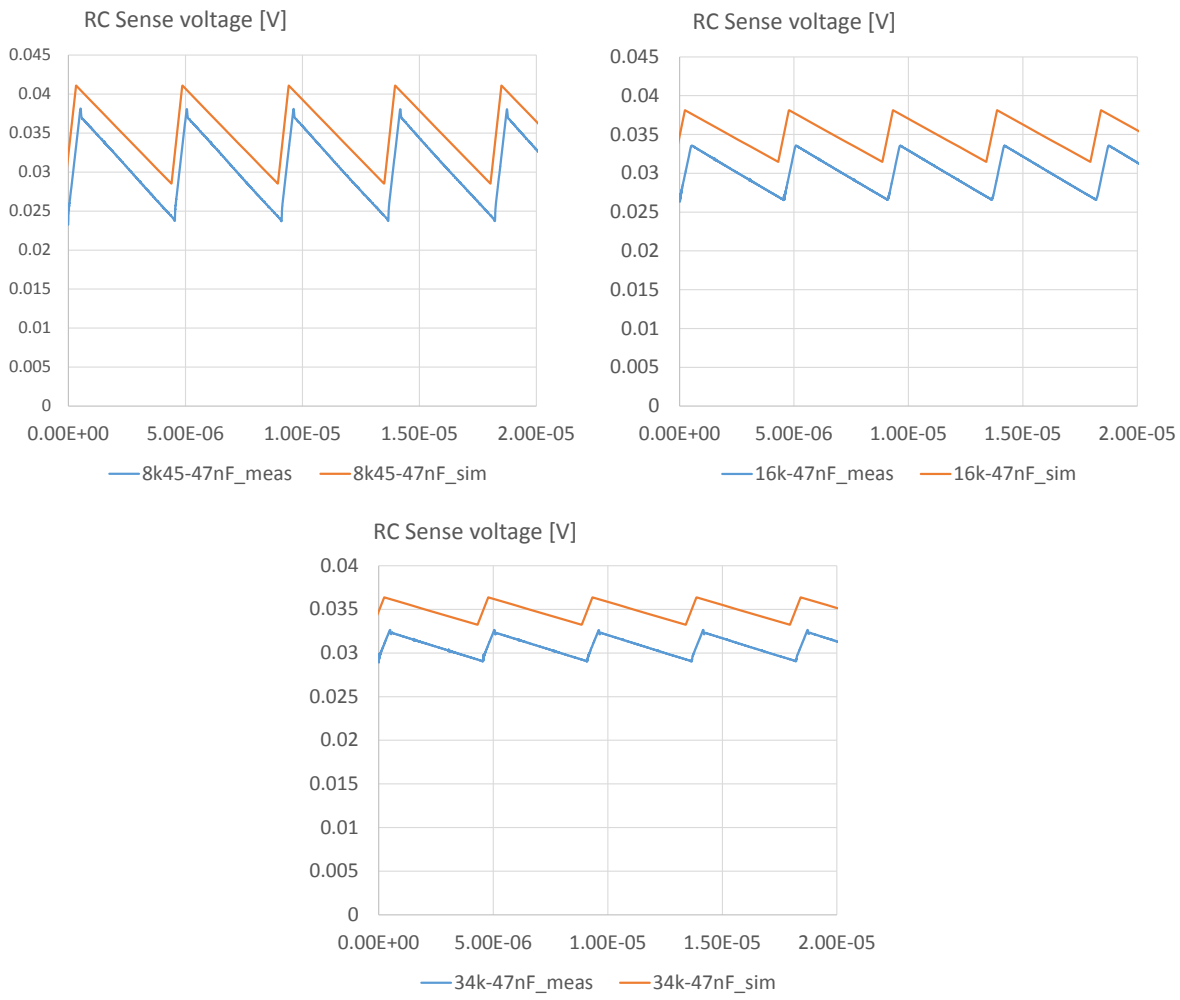

Figure 6: *Correlation between simulated (with nominal values, orange traces) and measured (blue traces) RC sense voltages with 10A DC load current.*

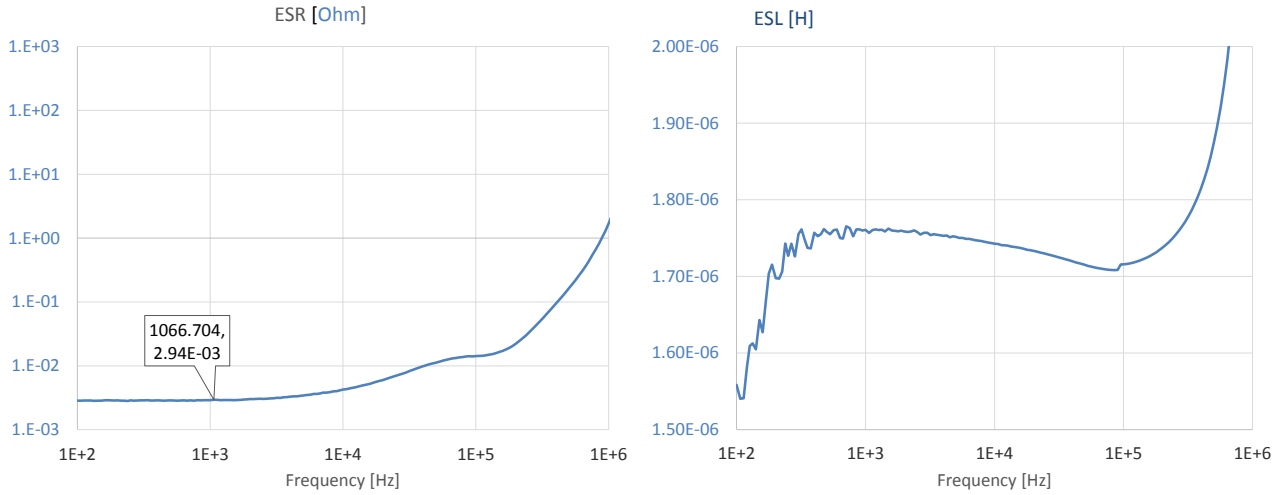

Figure 7: *Measured impedance real part (ESR, on the left) and extracted series inductance (ESL, on the right) of the power inductor used in the illustrations for Figures 5 and 6.*

The inductor ripple current depends on the inductance value, the input and output voltages and timing. To illustrate this with simple simulations, *Figure 8* steps the resistance value of the inductor logarithmically through the 3 mOhm to 1 Ohm range.

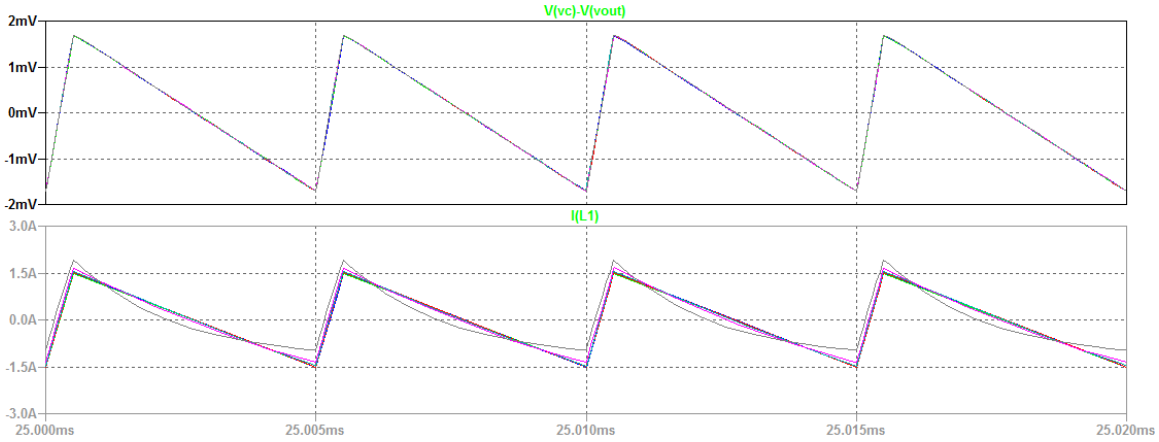

Figure 8: *Impact of the inductor's resistance on the extracted current-sense voltage (top) and actual inductor current (bottom).*

We can see that even in the most extreme case, when the assumed 1 ohm resistance of the inductor creates a 1.8us time constant, comparable to the switching period, the extracted current waveform is not changed, even though the actual inductor current (on the bottom plot) is already significantly distorted. In fact this is not surprising, since the R2-C2 network is not sensing the current through the resistance of the L1 inductor, it simply processes with its low-pass transfer function the voltage from which the inductor derives the current. This becomes important though when we consider other parameter variations, for instance tolerance, aging, temperature, nonlinearities and bias dependence.

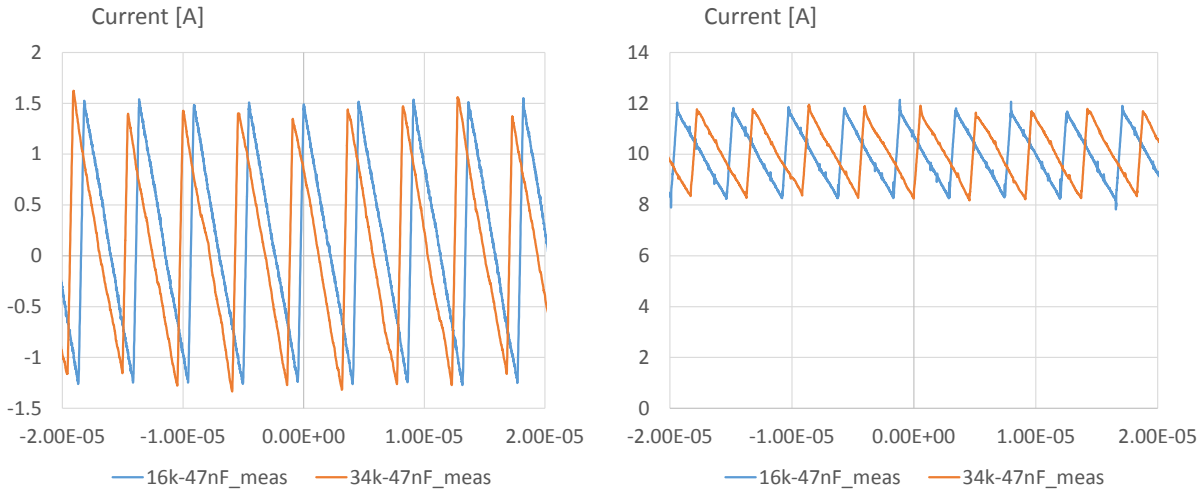

Figure 9: *Measured inductor current with two different probe tips as reported by the Virtual Probe. 0A DC load on the left, 10A DC load on the right.*

Next we show the end result of the correction for time-constant differences. We use two of the probe tips from *Figures 5* and *6* and plot the current waveforms after the Virtual Probe. *Figure 9* shows the measured inductor currents with two different probe tips with 0A and 10A DC load currents. There is some wobbling of the current envelope since we measure one phase of a three-phase converter and the phases negotiate the current sharing. The measured peak-to-peak inductor ripple current is 2.9A, in agreement with the expected 2.89 A_{p-p} after considering the measured value of the inductance. We can see that the inductor ripple current reported by the Virtual Probe does not depend on the time constant of the probe tip. The time constant of the inductor is approximately 600 us. The two probe tips we used for correlation had approximately 800 us and 1600 us time constants and the current waveform is still restored with reasonable accuracy.

There are two more circuit details we need to look at. One is to correct for a potential systematic error due to impedance imbalances and a second detail that can help with component parasitics in the probe tip.

In the conceptual schematics of *Figure 1* we just said that we need to measure the voltage differentially across the C2 capacitor. Unless we have an ideal voltage sensor with infinite differential and common-mode impedances, the finite input impedances of the sensing circuit will create errors. We illustrate the effect with the schematics shown in *Figure 10*, assuming simplified numbers for the RC probe tip and sensing probe equivalent circuit. We assume that the R2 resistor is 100 kOhm and the input impedance of the sensing probe can be modeled with a PI circuit of three 1 MOhm resistors. The L1/R1 time constant is 2 ms and it matches the unloaded time constant of the R2*C2 time constant. The three resistors in the sense amplifier equivalent input impedance scheme describe both the differential and common-mode input impedances. The only difference between the schematics on the left and right is the Rc compensation resistor, which balances the source impedance for the probe. In an actual implementation we also need a capacitor bypassing the Rc resistor to a quiet point in the circuit.

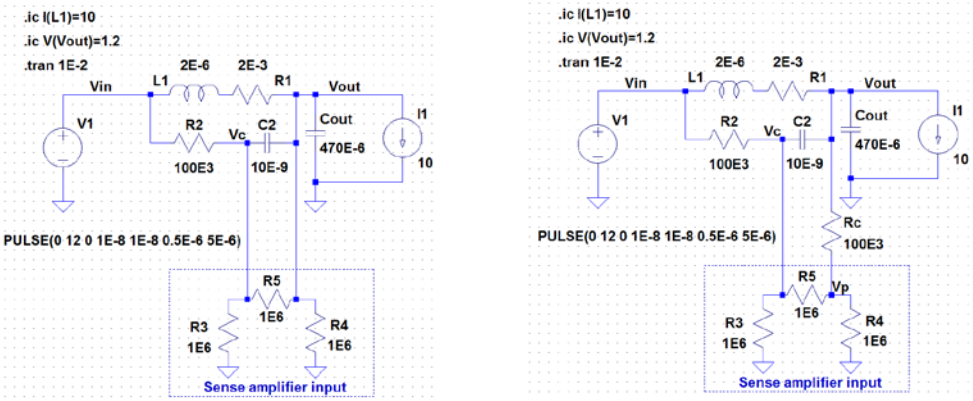

Figure 10: *Simplified schematics of a converter output stage with RC current sense circuit and a PI model of the sense amplifier, without the impedance balancing resistor (on the left) and with the impedance balancing resistor (on the right).*

Figure 11 shows the simulated current waveforms without the Rc compensation resistor, with and without the probe circuit connected. Seemingly the ripple waveforms are identical, just shifted vertically. The left plot shows the correct answer as the waveform averages around 20 mV, which is the product of the 10A DC load current and 2 mOhm Rdc of the inductor. The plot on the right would suggest a -82A DC current, which is incorrect. The shift occurs due to the imbalance of the source resistance feeding the two legs of the probe. Together with the different source resistances, the finite common-mode input resistance of the probe reduces the common-mode rejection ratio and part of the output voltage shows up in the current sense voltage. For the same reason, when we compare the waveforms closely, we can also notice that the reduced common-mode rejection ratio couples part of the output ripple onto the measured current waveform. The solution is shown on the right of *Figure 10*: we need to add an Rc compensation resistor in the leg of the probe circuit that otherwise would be directly connected to the output rail. By doing so we ensure that both input terminals see the same source impedance.

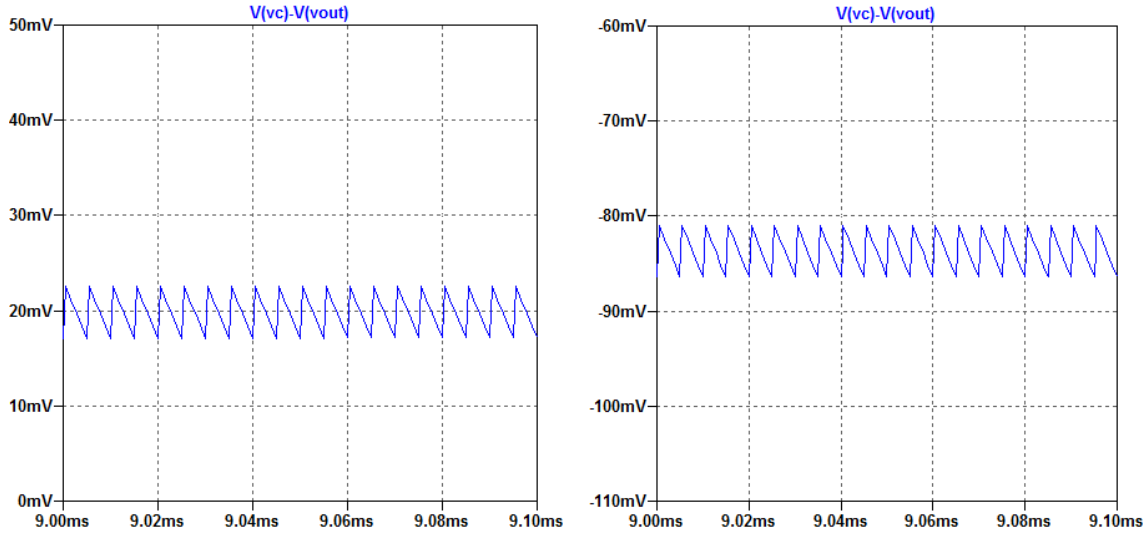

Figure 11: *Current-sense voltage waveforms for 10A DC load current, without the probe connected or with ideal probe (on the left) and with finite probe input impedance and without the Rc compensation resistor (on the right).*

The second circuit detail has to do with the parasitic component values in real implementations. Each circuit element in *Figure 1* has its parasitic components associated with it. For small surface mount two-terminal passive components we usually need to take into account parallel body capacitance and series resistance and inductance associated with the terminals and body. Which of these three needs to be taken into account depends on the frequency range of interest and nature of the component they are associated with. In our circuit in *Figure 1*, the most sensitive to parasitic elements is C2. The circuit expects a low impedance of this capacitor at high frequencies and it means that series resistance and/or series inductance will adversely affect the performance. To illustrate this, the schematic on the left of *Figure 12* explicitly calls out the series resistance and series inductance of C2. Assuming a 1 nH ESL value, the plot on the right

shows the transfer function of this low-pass filter from the (Vin-Vout) input to the (Vc-Vout) output. ESR stepped through the 10 mOhm, 100 mOhm, 1 Ohm and 10 Ohm.

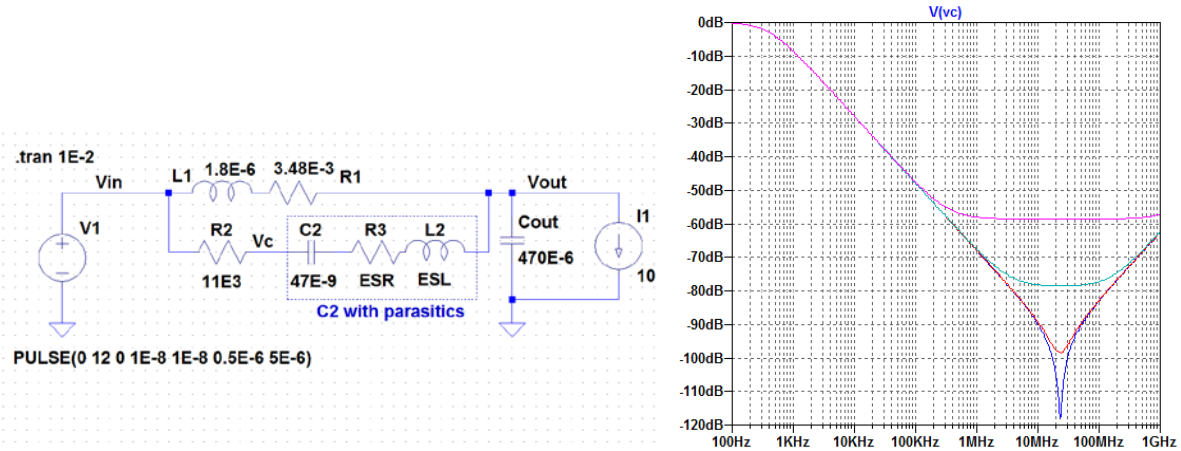

Figure 12: *Effect of series resistance of C2.*

If the C2 capacitor has low ESR, its impedance profile and the resulting low-pass filter transfer function will have a notch at the series resonance frequency (in this case a little above 20 MHz, beyond which the transfer function rises. If there is noticeable spectral content in this frequency range, it will create an error signature in the output voltage. Even worse, the details of the transfer function in this frequency range will strongly depend on second-order effects, which are harder to control. One possible solution is to increase the series resistance on purpose, in a controlled way. This component is Rs in *Table 1*. By adding a series resistor we introduce a zero in the transfer function, but it is straightforward to compensate for it during the processing of the sensed voltage across C2. This not only reduces the uncertainty due to the parasitic resistance of C2, it also has two additional benefits: the effect of ESL is reduced (by moving the related cutoff frequency to higher values) and it also provides additional high-frequency noise suppression for signals that may find their way around this filter.

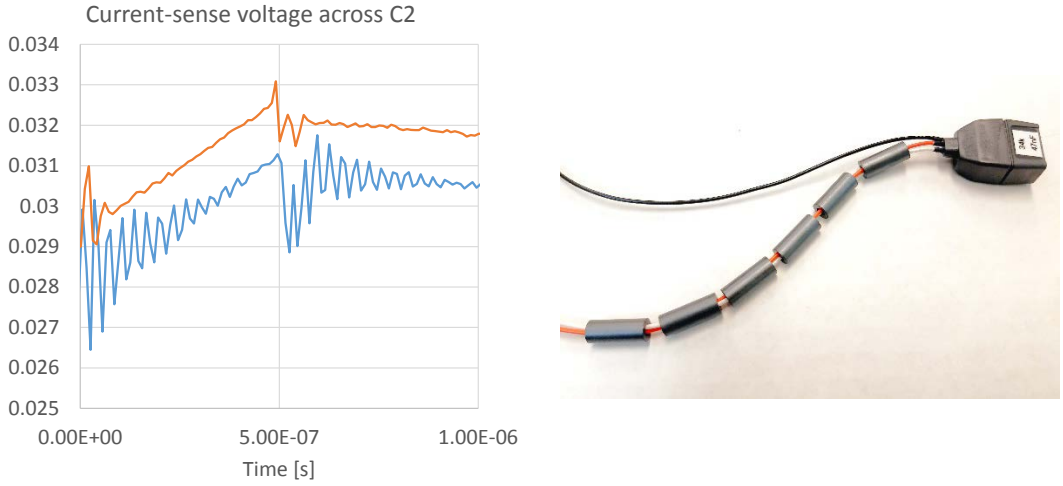

Figure 13: *Noise suppression with ferrite beads on the sense wires.*

In very noisy environment, when we have to measure within larger systems where there may be a number of unrelated noise sources, additional noise suppression measures may be necessary. This is illustrated in *Figure 13*. The plots on the left show the voltage across the C2 current-sense component in a noisy system. The blue trace has a lot of high-frequency ringing, generated by the fast switching edges and coupled through parasitics to the sense circuit. If rearranging the connections and wires does not provide enough improvement, adding ferrite absorbers along the probe tip wires can help. The physical arrangement is shown on the photo on the right, the resulting waveform is shown by the red waveform on the plot on the left.

Finally we need to remember that real circuit elements may have a number of additional side effects that we have to consider. In addition to the tolerance ranges of the component values, there are additional variations due to several factors, among others: temperature, DC bias, AC bias, frequency dependence and nonlinearity. Since R2 and C2 need to handle low currents and powers and therefore precision components can be used with low temperature and bias sensitivity, the major concern is to get the parameters of the power inductor correctly. High-current devices can exhibit nonlinearity, frequency dependence and change of parameters due to DC and AC bias.

Bias dependence (and implicitly through it, nonlinearity) is documented -though may not be guaranteed by specification- on data sheets of power inductors. Frequency dependence of inductance and series resistance, however, is easier to find on data sheets other than for low-current ferrite beads.

II.2. Impedance measurement noise floor

It can be shown that the bounds on the absolute error in an impedance measurement is:

$$B = \frac{\sqrt{2}}{I \cdot \sqrt{M} \cdot \sqrt{K}} \sqrt{\left[VDIV_V \cdot 10^{-\frac{SNR_{V_n}}{10}} + \left(\frac{Z}{R_S}\right)^2 \cdot VDIV_I \cdot 10^{-\frac{SNR_{I_n}}{10}} \right] \cdot (-\ln(1-F))}$$

where:

- B is the bounds on the error, in Ω such that for a measured impedance $\hat{Z}$:
  $\left|\hat{Z} - |Z| \cdot e^{j \cdot \Theta_Z}\right| < B$
  with a certainty of F/100%.
- Z is the actual impedance being measured
- R_s is the resistance of the sense resistor used to measure the transient current by inferring the current by a voltage measurement across the resistor.
- $VDIV_V$ and $VDIV_I$ are the volt/division settings of the oscilloscope channels measuring the voltage and the voltage across the current sense resistor, respectively.
- SNR_V and SNR_I are the normalized signal-to-noise ratios of the oscilloscope channels measuring the voltage and the voltage across the current sense resistor, respectively.
- M is the number of averaged measurements.

- K is the number of points in the acquisition
- I is the amount of transient current injected used to stimulate a voltage transient, and thus an impedance.

The bounds on the measurement of a zero impedance is interesting and determines a kind of measurement noise floor. When measuring a zero impedance, the current measurement channel becomes irrelevant:

$$\lim_{Z\to 0} B = \frac{\sqrt{2}\cdot VDIV_V \cdot 10^{-\frac{SNR_{V_n}}{10}}}{I \cdot \sqrt{M} \cdot \sqrt{K}} \cdot \sqrt{-\ln(1-F)}$$

The normalized SNR implies that, for frequency dependent noise, the noise density is frequency dependent. If the noise is white, or evenly distributed over frequency, then the normalized SNR is simply the signal-to-noise ratio of the oscilloscope channel calculated as the ratio between the largest full-scale signal based on the VDIV setting and the total noise in the channel. When the noise is frequency dependent, the normalized SNR is calculated as the noise density at a given frequency multiplied by the entire Nyquist band.

The normalized SNR is important because it tends to differ from the expected SNR due to bits of resolution, or effective number of bits of the channel. The largest deviation from expectations is at very low frequencies where 1/f noise tends to dominate, which is unfortunately also where the PDN impedance tends to be lowest.

Some example noise densities for a typical impedance measurement is shown in *Figure 14*. As an example, the voltage measurement normalized SNR at 20mV/div at 100 Hz is about 8 dB.

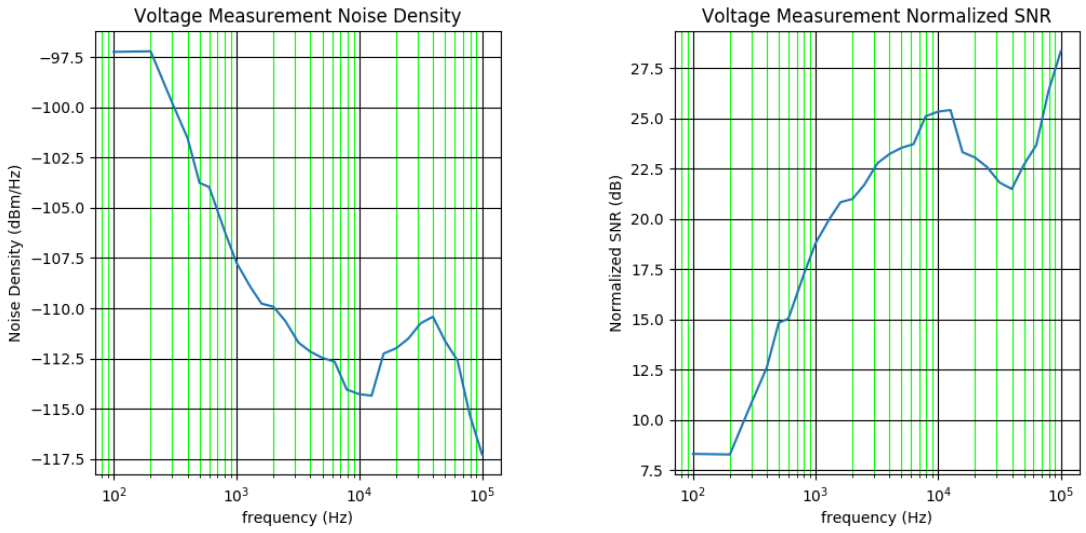

Figure 14.a: *Typical Noise Statistics on Impedance Measurements. Voltage Measurement Noise Density at 20mV/div (on the left) and Voltage Measurement Normalized SNR at 20mV/div (on the right).*

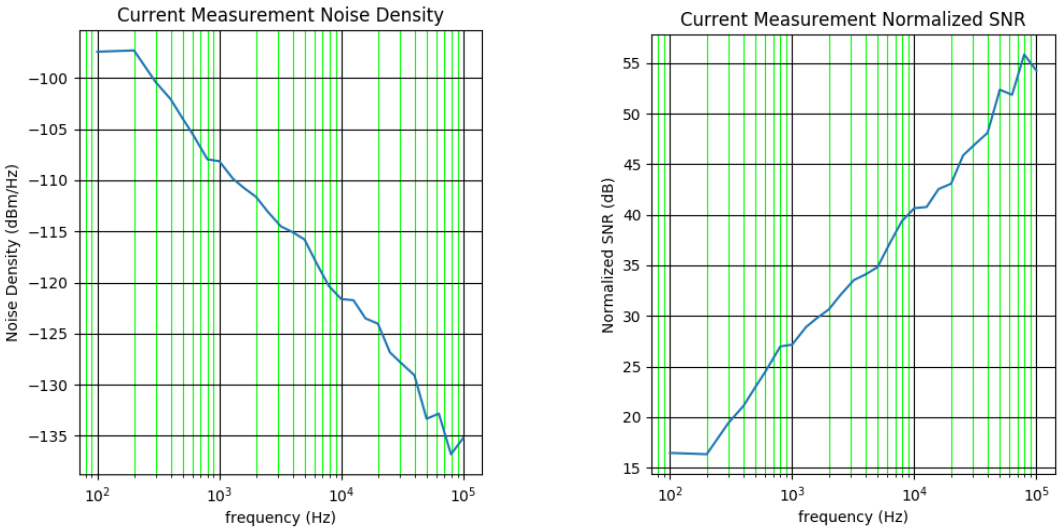

Figure 14.b: *Typical Noise Statistics on Impedance Measurements. Current Measurement Noise Density at 50mV/div (on the left) and Current Measurement Normalized SNR at 50mV/div (on the right).*

This means that for no averaging, a 10 Mpt acquisition and a transient current amplitude of 100 mA, a measurement of zero impedance is measured to 95% certainty with a bounds of:

$$\lim_{Z\to 0} B = \frac{\sqrt{2}\cdot 20\cdot 10^{-3}\cdot 10^{-\frac{8}{20}}}{0.1\cdot 1\cdot\sqrt{10^6}}\cdot\sqrt{-\ln(1-0.95)} = 194\mu\Omega$$

If one desired at least 100 μΩ error bounds with 95% certainty, one would need at least four averages. This is still a surprisingly low noise floor for an oscilloscope based measurement.

As an illustration for the potential DUT noise, *Figure 15* shows the Fourier transform of the output ripple for the two evaluation boards we use for *Sections III.2* and *III.3*.

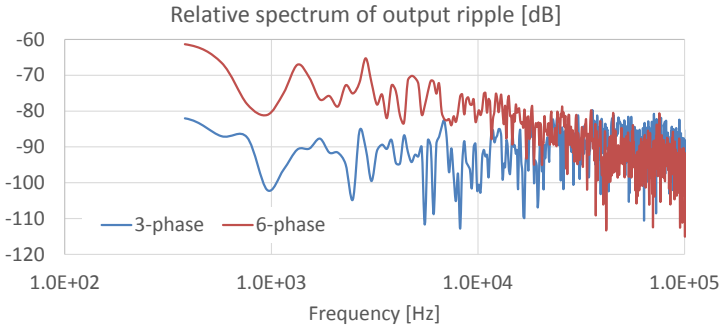

Figure 15: *Spectral density of output ripple for the three-phase and six-phase evaluation boards.*

The plot compares the low-frequency noise of two DC-DC converters, which will be looked at in more detail in the next Section. The comparison illustrates two different converter topologies and loop settings, one setting resulting in a significantly higher inherent noise.

III. Measurement results

In this section we show current, current sharing and output impedance measurement results of two different multi-phase evaluation boards as well as for a production board.

III.1 Three-phase evaluation board

The current-mode control evaluation board has three independent outputs as shown in *Figure 16*. The board was modified so that all three outputs produce the same 1.2V output voltage and track the same reference. For all test data shown here, a nominal 12V input voltage was used, which in turn sets the duty cycle in each phase to approximately 10%. The three outputs were then shorted together on the top side plane shapes. Each output is capable of producing up to 15A of current, a total of 45A, and each output has its own transient injector circuit on the back side. For the data shown here, the output connections and transient injector for Output2 were used.

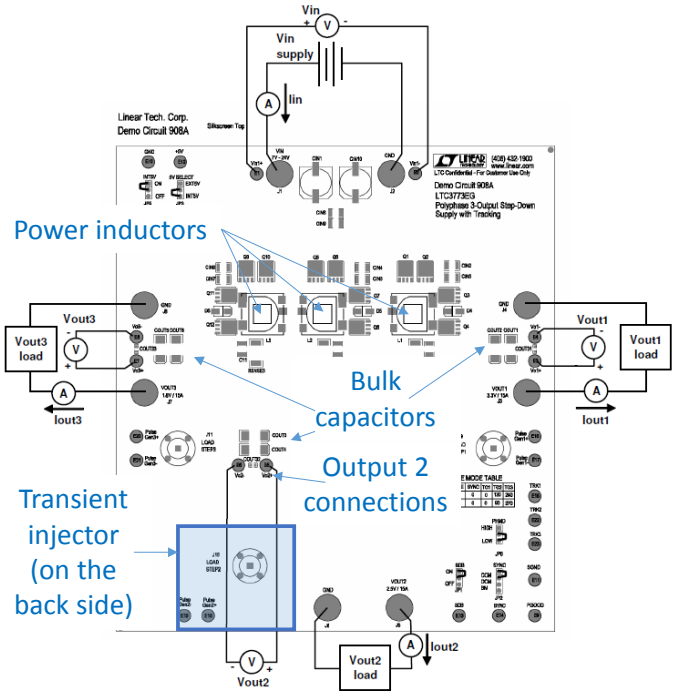

Figure 16: *Top view of the three-phase evaluation board from [2].*

The board's small-signal output impedance was first measured with a Vector Network Analyzer (VNA) in the frequency range of 100 Hz to 10 MHz with 10 dBm source power. Three different connections were used with two DC load current values: 0A and 30A. The VNA connections used RG178 coaxial cables with open pigtails, soldered to

the DUT. Each output has two small metal turrets, one connected to GND, the other to power. We used the turrets at Output2, as marked in *Figure 15*. The three connection options were: top-top, top-bottom and top-injector. The 'top-top' connection means that both VNA cables were soldered to the turrets on the top side of the board. 'Top-bottom' connection means that one VNA cable was soldered to the turrets on the top side of the board, the second VNA cable was soldered to the same turrets on the back side of the board. Finally the 'top-injector' connection means that one cable was soldered to the turrets on the top side of the board and the second cable was soldered across the FET injector circuit, identified by the blue square in *Figure 16*.

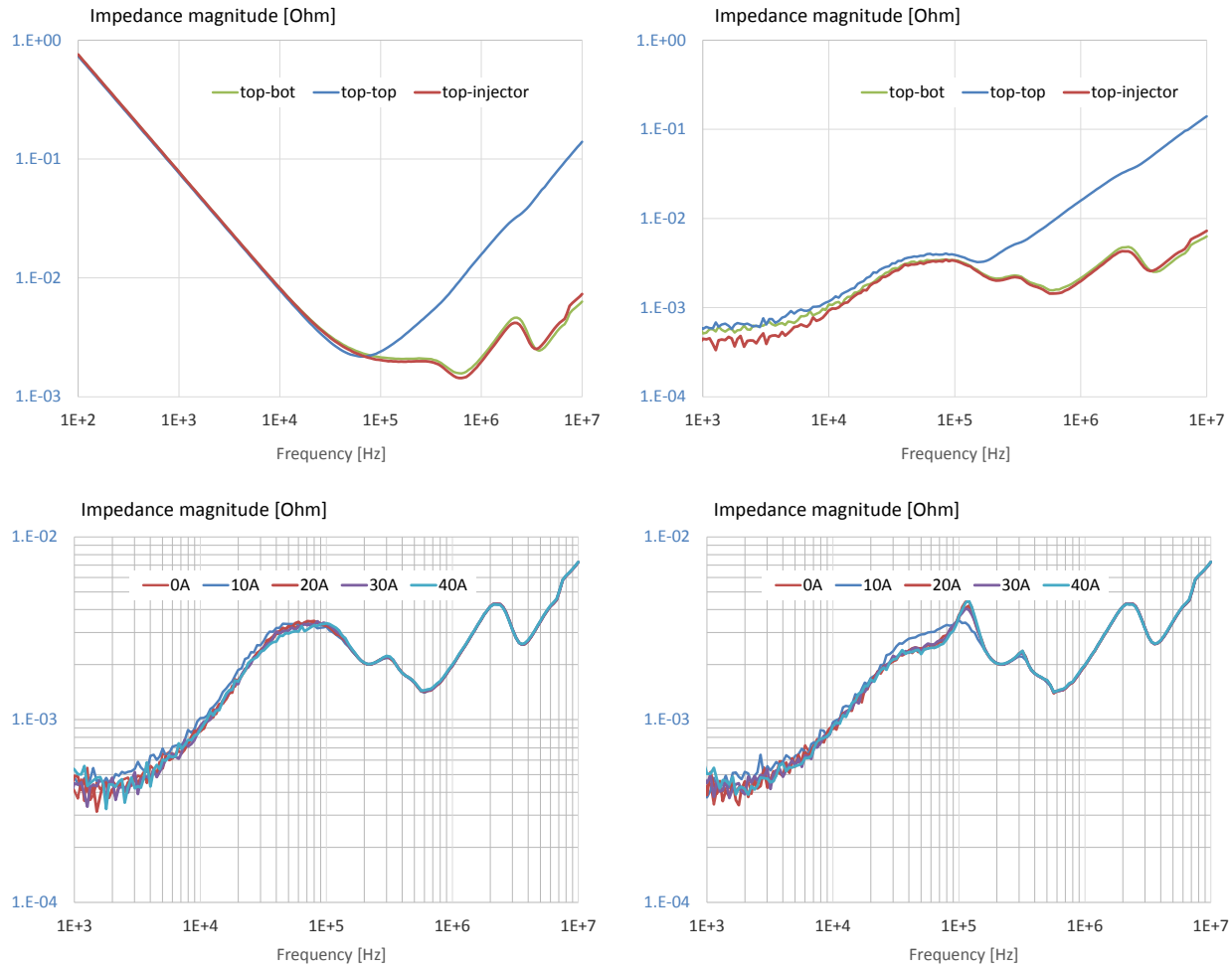

Figure 17: *Small-signal output impedance of the three-phase DC-DC converter, measured with a VNA with three different connection geometries. Top left: no input power, top right: 12V input and 30A DC load. Bottom left: 12V input and DC load stepped in 10A increments, bottom right: 7V input and DC load stepped in 10A increments.*

The impedance plots in *Figure 17* with no input power are all aligned up to almost 100 kHz, which is the capacitive region. Above 100 kHz there are differences among the

three connections: we get the highest impedance (inductance) when both cables are connected to the test points on the same (top) side of the board, because in this case we also measure the impedance of the posts in series to the DUT impedance. The other two curves track tightly all the way up to 10 MHz. The impedance curves do not change above 100 kHz when we apply input power, however, we do see differences at low frequencies. The 'top-top' case has consistently higher impedances due to the added small resistance of the posts. The plots on the bottom illustrate the consistency (or the lack thereof) of the small-signal impedance profile as a function of DC operating points. Both plots step the DC load current from 0A to 40A in 10A increments. The plots on the left and right used 12V and 7V DC input voltage, respectively. The impedance profile hardly changes with the DC load current at 12V input. With 7V input voltage, there is some noticeable change in the 20 kHz – 200 kHz frequency range, and the shape of the impedance profile also suggests reduced stability margin.

Figure 18 illustrates the DUT behavior to medium-signal excitations in the frequency domain with various DC load currents. The test signal was 1 $A_{p\text{-}p}$ and the frequency sweep was limited to 200 kHz due to the band-limited nature of the simple injection circuit. Note that in the entire DC load current range the impedance profile is very constant and agrees well with the small-signal VNA measurements.

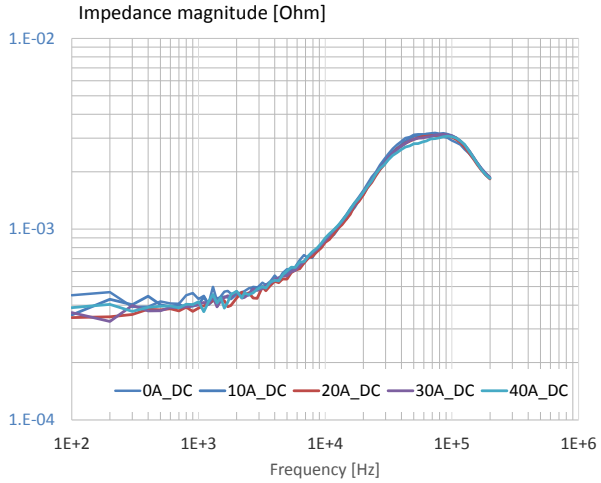

Figure 18: *Output impedance measured with medium-signal AC test current with DC load current in the 0A to 40A range, in 10A increments.*

Figure 19 shows the DUT output impedance measured with medium and large-signal pulse currents. The post-processing extracts the fundamental frequency of the pulse excitation and response and calculates the impedance as a complex ratio of those two signals. The left and right plots show the impedance curves with 0A and 20A DC load current. The pulse swing steps through the 0.3 $A_{p\text{-}p}$ to 30 $A_{p\text{-}p}$ range logarithmically. Except the 30 $A_{p\text{-}p}$ swing (which goes beyond the maximum rated current of 45A when 20A DC load is used), the calculated impedance profiles yield the same values regardless of the AC excitation level.

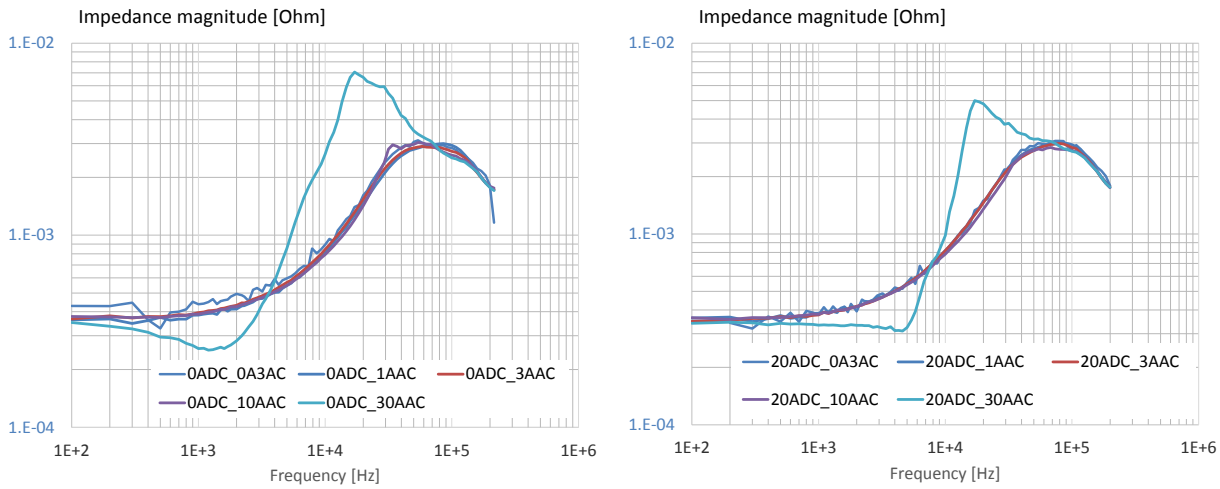

***Figure 19**: Impedance profiles calculated from medium and large signal repetitive pulse responses.*

Some of the corresponding time-domain transient responses are shown in *Figure 20*. The left plot shows three different transient load conditions: 0A DC load and 10A pulse load (blue line), 20A DC load and 10A pulse load (red line) and 20A DC load with 20A pulse load (grey line).

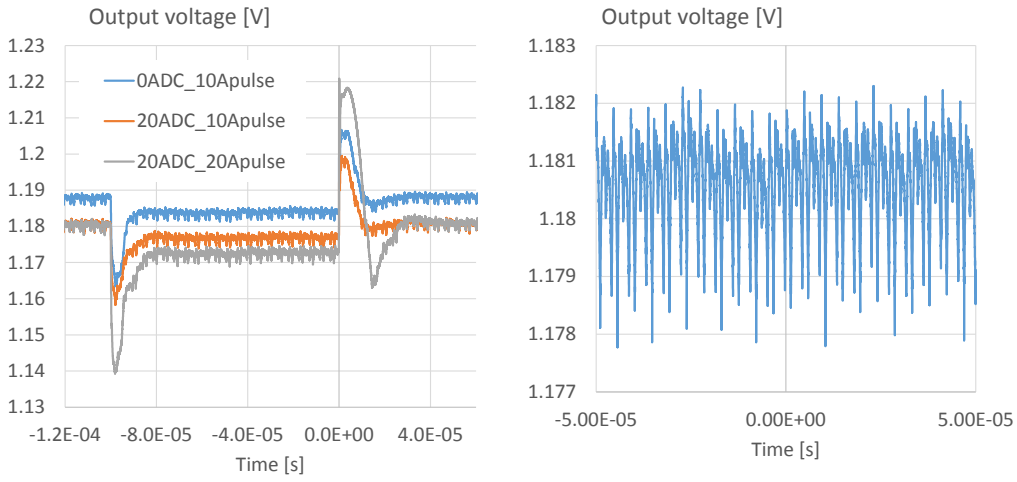

***Figure 20:** Time-domain transient response of the three-phase evaluation board.*

The load attack and load release responses are quite similar for the first two conditions; they become very different for the third case when the load toggles approximately between 50% and 100% load current. Even for this last case the load attack response is proportional to the load change; the major difference is on the load release line. This is

due to the fact that the converter has very small duty cycle, approximately 10%. The right plot shows the steady state output ripple of the converter with 20A DC load. The spectral view of the three-phase case in *Figure 15* was derived from the output ripple in this operating point. Some sub-harmonic contents and minor baseline wandering is visible, but otherwise the waveform has reasonably low noise and jitter.

Finally *Figure 21* shows the current sharing response with two excitations: 3 $A_{p\text{-}p}$ 50% duty cycle pulse excitation with 20A DC load (on the left) and 10 $A_{p\text{-}p}$ 20% duty cycle excitation with 20A DC load (on the right). The left plot uses the 10 kHz – 20 kHz frequency range, the plot on the right covers 10 kHz – 100 kHz. Note that due to the current-mode control of the converter, the current sharing is very good with 10 $A_{p\text{-}p}$ transients. With 20 $A_{p\text{-}p}$ transients at specific frequencies, notably at 24 kHz and 40 kHz we start seeing up to +-10% tracking differences.

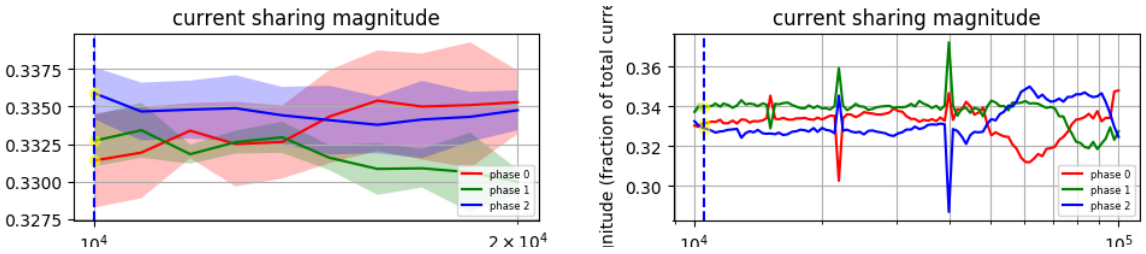

Figure 21: *Current sharing frequency response of the three-phase evaluation board with 3 $A_{p\text{-}p}$ (left plot) and 10 $A_{p\text{-}p}$ (right plot) excitation levels. Horizontal axis is frequency on both plots.*

III.2. Six-phase evaluation board

The approximate component placement of the six-phase evaluation board is shown in *Figure 22*. The board has a nominal 12V input and produces a 1V output with a maximum current in excess of 200A. The board has room for three arrays of bulk capacitors at different lengths from the converter outputs. For these tests, only Bulk capacitor array 1 was populated in a symmetrical fashion around the six phases. The total amount of bulk capacitance was 14,000 uF.

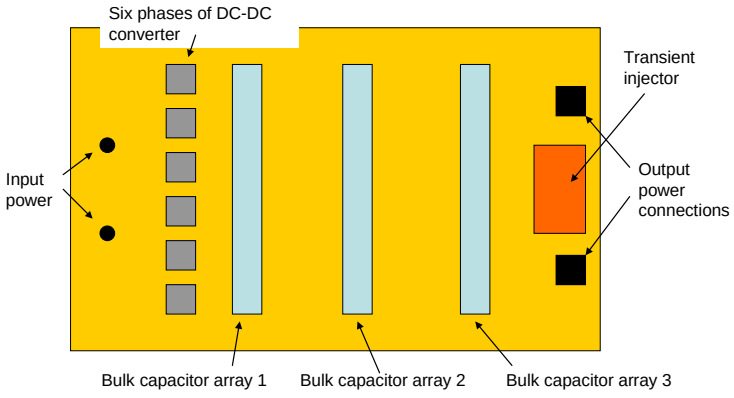

Figure 22: *Top view sketch of the evaluation board.*

The evaluation board has an open-loop transient injector circuit near the output connectors. With appropriate duty-cycle limitations it is capable of injecting up to 200A peak transient currents. The board was measured in different operating points with different instruments and stimulus. First, it was measured with a Vector Network analyzer in the 100 Hz – 10 MHz frequency range with 10 dBm source power and various static DC load current values in the 0 – 100% current range. Next, the same oscilloscope-based universal tester that was used for *Figures 18* through *21* was connected to the transient injector and the output impedance was measured with medium and large signal sinewave excitation. The sinewave excitation magnitude was stepped through the 0.1 $A_{p\text{-}p}$ to 10 $A_{p\text{-}p}$ range in 1, 3, 10 increments. Third, square-wave excitation was stepped through the 1, 3, 10, 30 and 100 $A_{p\text{-}p}$ values. The large-signal sweeps were limited to 100 kHz due to the band-limited nature of the simple injector circuit. All excitation and response-pickup connections were exactly at the same location, near the output power connectors. The impedance plots are summarized in *Figure 23*.

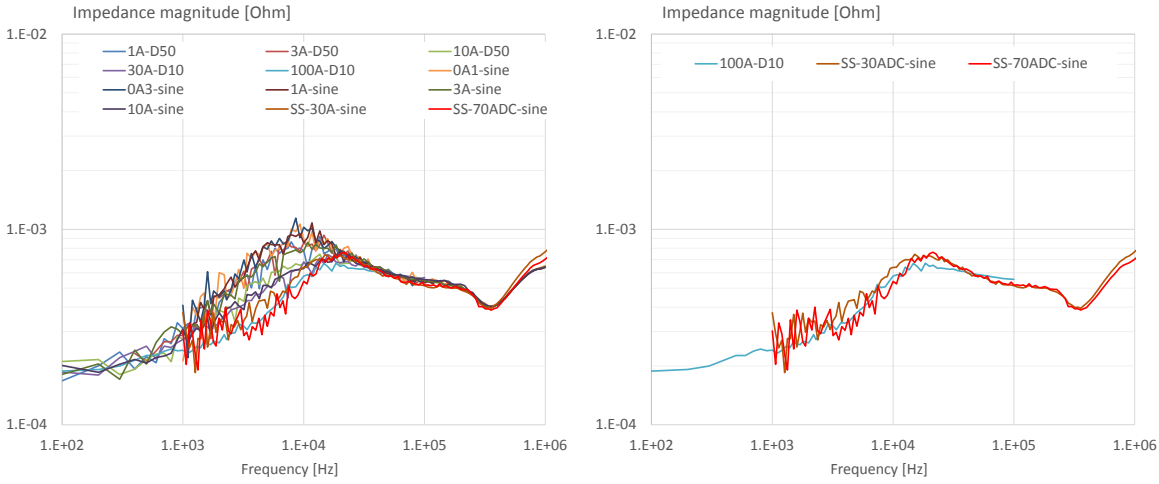

Figure 23: *Output impedance of the six-phase evaluation board under different conditions. Left: all measured conditions overlaid; right: 100 $A_{p\text{-}p}$ pulse and VNA small signal measurements with 30A and 70A DC load overlaid.*

The first observation is that in the 100 Hz – 1000 Hz and 30 kHz – 10 MHz frequency ranges the measured impedance does not depend on any of the measurement conditions: DC load current, small-signal, large-signal, sine-wave or square-wave excitation. This confirms that the connections for the different tests have been chosen properly and that in these frequency ranges the entire system behaves linearly. The left plot shows all measured data, the plot on the right is a subset to compare the 100 $A_{p\text{-}p}$ pulse measurements with the small-signal VNA measurement results. Note that in spite of the 10 dBm source power, there is considerable noise on the VNA results below 10 kHz. This is not a limitation of the measurement setup, rather an indication of the noise generated by the DUT itself, as it was shown in *Figure 15* above. The measured trace with 100 $A_{p\text{-}p}$ pulses shows very little noise, because the large excitation signal masks out the DUT's own noise.

The loop compensation chosen for these measurements resulted in a phase margin over 45 degrees under all operating points, but the large random low-frequency fluctuations showed up also in the current-tracking data. *Figure 24* shows the current-sharing magnitude and phase in the 100 Hz – 100 kHz logarithmic frequency range measured with 80 $A_{p\text{-}p}$ 10% duty cycle current pulses on top of 25A static DC load. Note that the ideal current-sharing magnitude value would be 1/6, which the traces gradually approach above 10 kHz. At low frequencies the current-sharing ratio appears to fluctuate in a 3:1 range.

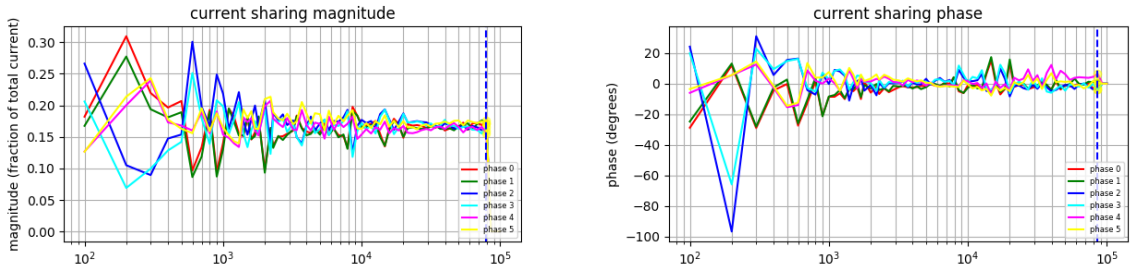

Figure 24: *Current-sharing magnitude (left plot) and phase (right plot) of the six-phase evaluation board, measured with 80 $A_{p\text{-}p}$ pulse excitation. The horizontal scale on both plots is logarithmic frequency in the 100 Hz to 100 kHz range.*

However, this apparent oscillation is not repeatable and has little dependence on the relative timing of the excitation edges with respect to the switching edges; the fluctuation is the manifestation of the random low-frequency wandering of current sharing. This is captured in the mosaic of a few time-domain screen shots in *Figure 25*. The six colors represent the six phases, each trace shows the current as a function of time. The repetition of current pulses was set to 300 Hz, which is much lower than the converter's switching frequency, this is why each trace appears like a band; in reality the band is how the saw-tooth inductor current shows up on this time scale.

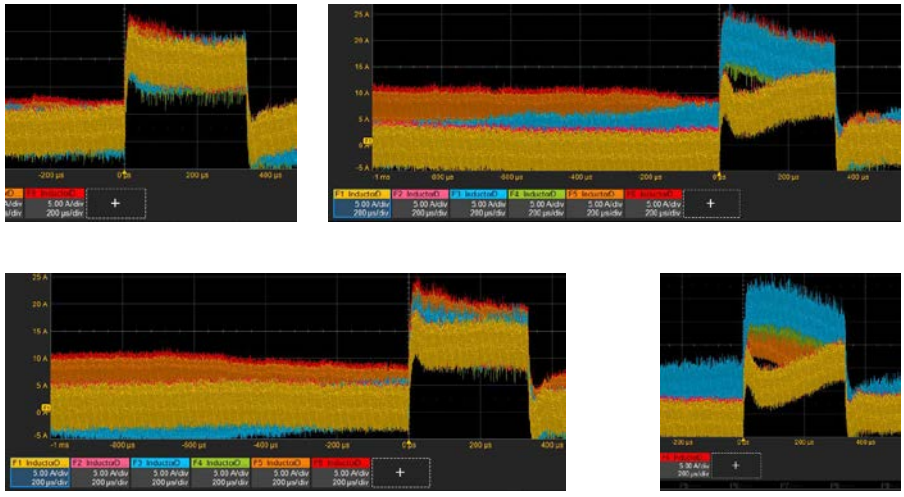

Figure 25: *Time-domain current sharing plots with 80A pulse excitation current.*

Even though the excitation frequency and magnitude is not changing, the low-frequency wander changes the current-sharing ratios noticeably. The correct current sharing is captured on the upper left insert; approximately all six traces run on top of each other. The other three plots capture different deviations. For instance, the plot on the upper left shows the blue trace ramping up slowly and the red trace ramping down before the current step and it is followed by a ringback on the yellow trace following the transient edge.

III.3. Production board

At the end we show data collected on a production board, measured in a full live system. The measured rail is powered by a six-phase converter, similar to what is shown in *Section III.2*. The test tool was set to automatically recognize the repetition frequency of the DUT (monitoring mode) and the plots in *Figure 26* show two illustrative results.

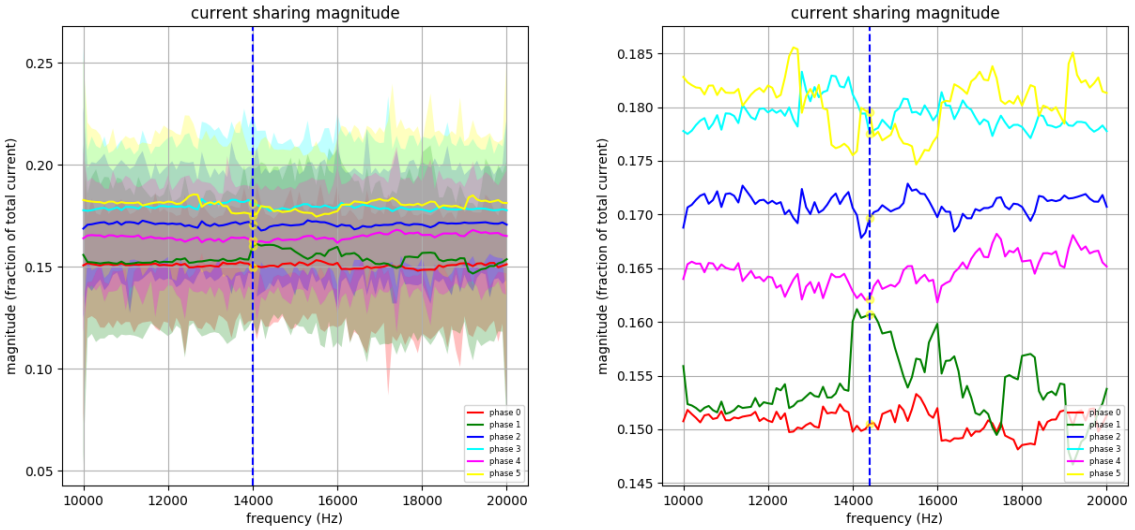

Figure 26: *Current sharing plots measured on a live system with a six-phase DC-DC converter, observed in monitoring mode.*

The plot on the left includes also the min/max values within each captured data frame; these are the colored shadows. The solid traces represent the average values within each captured data set. Note that while the average values tend to be grouped relatively tightly around the expected 1/6 value, the min/max values exhibit a considerable range.

Conclusions

In this paper we analyzed some of the practical implementation options of DC-DC converter current measurements using an RC network across the switching inductor. It was shown that the time constant of the inductor does not need to be accurately matched by the RC time constant; a reasonable difference can be compensated for during the post-processing of the data.

For applications where the RC network is connected to a differential probe with finite input impedance, the RC element has to be modified to equalize the source impedance seen by the two sides of the probe. A resistor in series to the capacitor and/or ferrite absorbers on the connecting wires can be used to suppress out-of-band high-frequency noise.

It was shown that oscilloscope-based setups can achieve sub-milliohm noise floor in impedance measurements. It was also illustrated that in multi-phase converters the constant negotiation among the phases can produce low-frequency wander with spectral density above the instrumentation noise floor. Data collected on a current-mode controlled three-phase and digitally controlled six-phase evaluation board showed that as long as the connections are set up exactly at the same locations, the measured output impedance is the same, regardless of how the measurement is done: performed by a Vector Network Analyzer or by an oscilloscope and a transient source. It was also shown that as long as we don't drive the DUT into nonlinear regions, the small-signal, large-signal, sine-wave or pulse-based results are in good agreement.

References

[1] Istvan Novak, "A Generic Test Tool for Power Distribution Networks," DesignCon 2017, available at http://www.electrical-integrity.com

[2] "DC908A - LTC3773EG Demo Board," http://www.linear.com/solutions/3262

[3] Peter J. Pupalaikis, "Current Sharing Measurements in Multi-Phase Switch Mode DC-DC Converters," EDICON 2017, September 11-13, 2017, Boston, MA, available at http://www.electrical-integrity.com