How Spatial Variation of Voltage Regulator Output Impedance Depends on Sense Point Location

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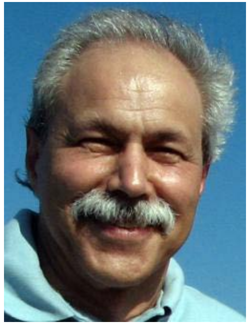
SPEAKER



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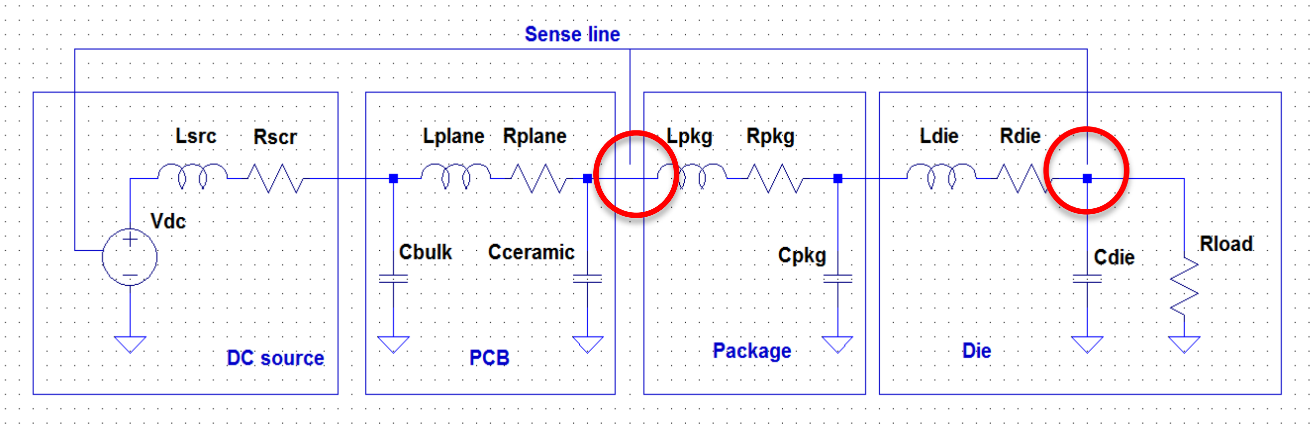
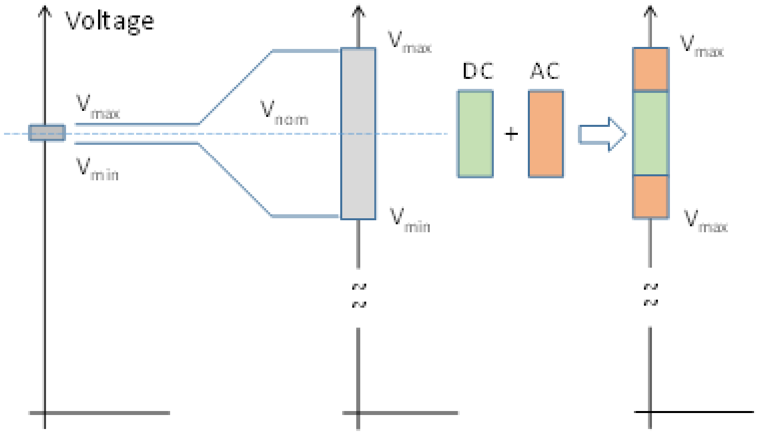
Istvan is a Senior Principle Engineer at Oracle. Besides signal integrity design of high-speed serial and parallel buses, he has been engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is a Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies and has twenty five patents in the areas of power distribution design and precision measurements.

Introduction



In competitive designs spatial attenuation and delay can not be ignored

The Noise Budget



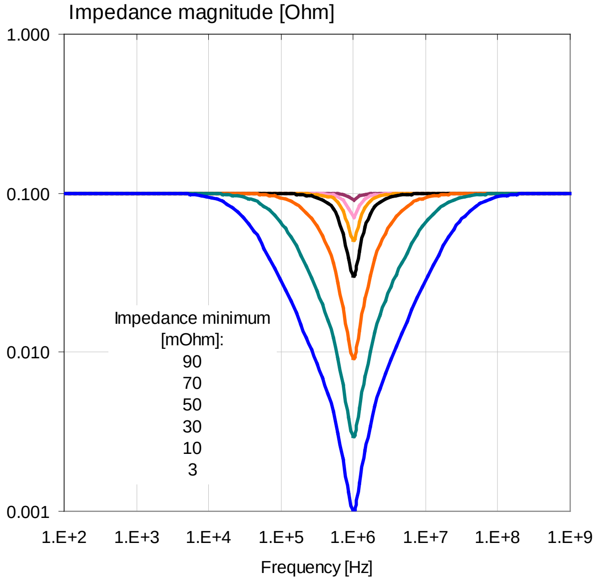
Assuming LTI system and flat impedance:

$$Z_{target} = \frac{\Delta V}{\Delta I}$$

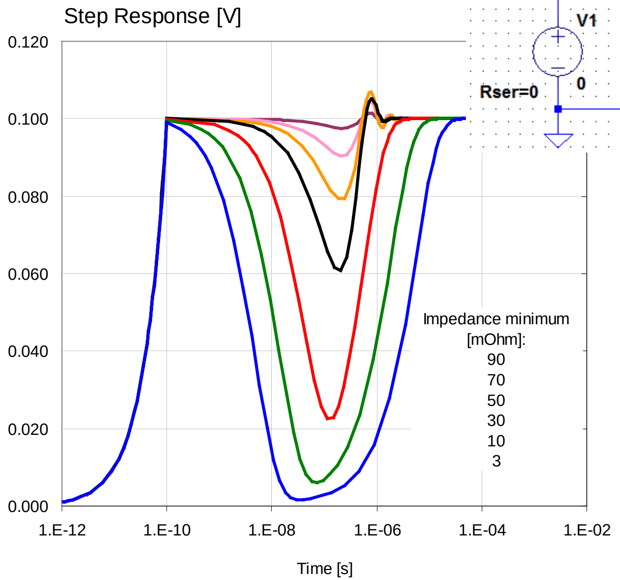
ΔV = (Vmax – Vmin) – DC_drop - PARD

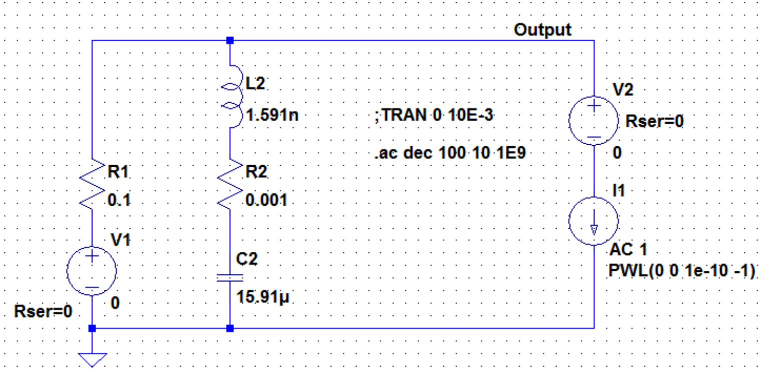
Non-flat Impedance: Depth of a Single Notch

Frequency domain



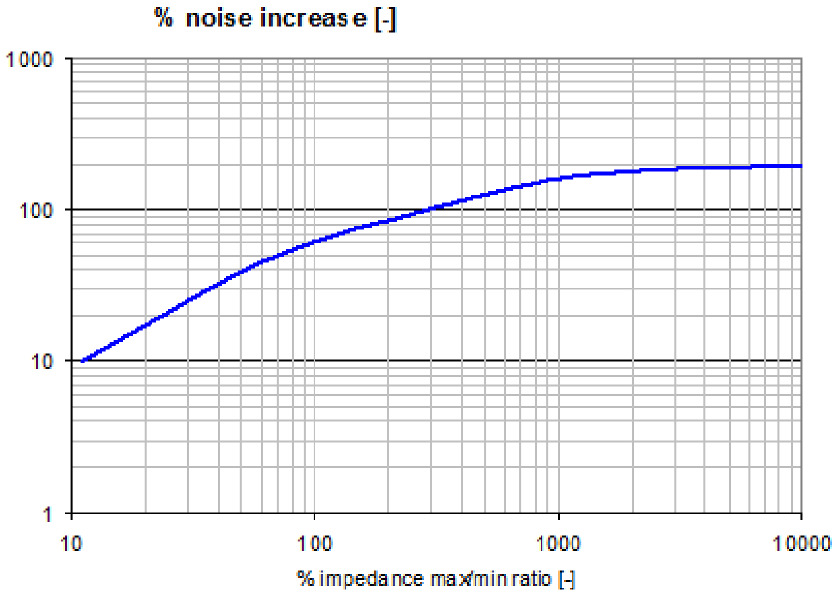
Time domain





SPICE deck

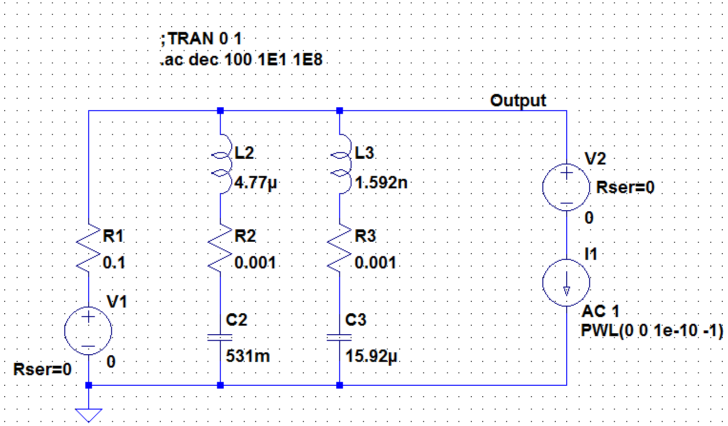
Non-flat Impedance: Depth of a Single Notch



Worst-case transient noise

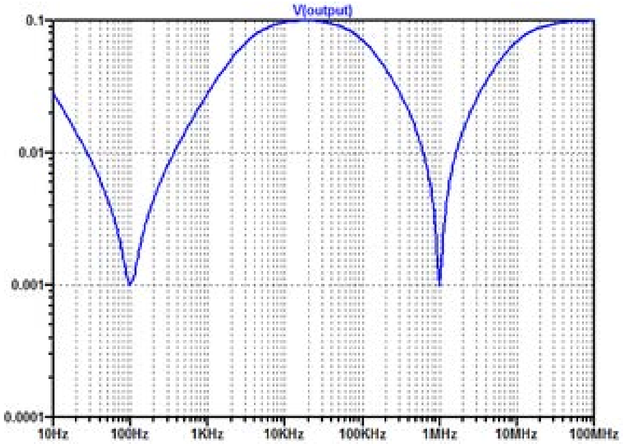
- Increases as depth of notch increases
- Relative increase is proportional at small blips
- Saturates at about 2x extra noise

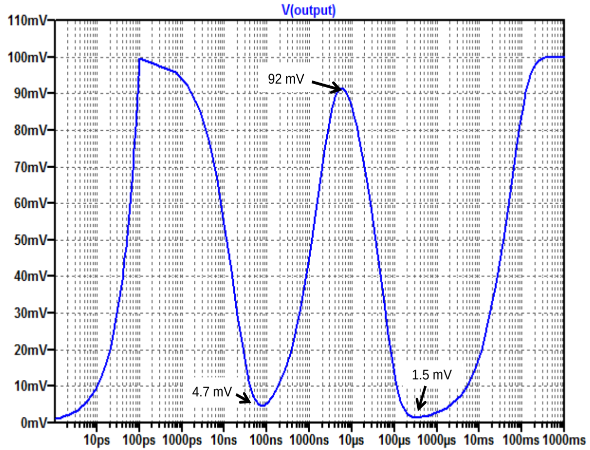
Non-flat Impedance: Number of Notches



Worst-case transient noise

- Increases with the number of notches
- Effect is additive for widely separated dips





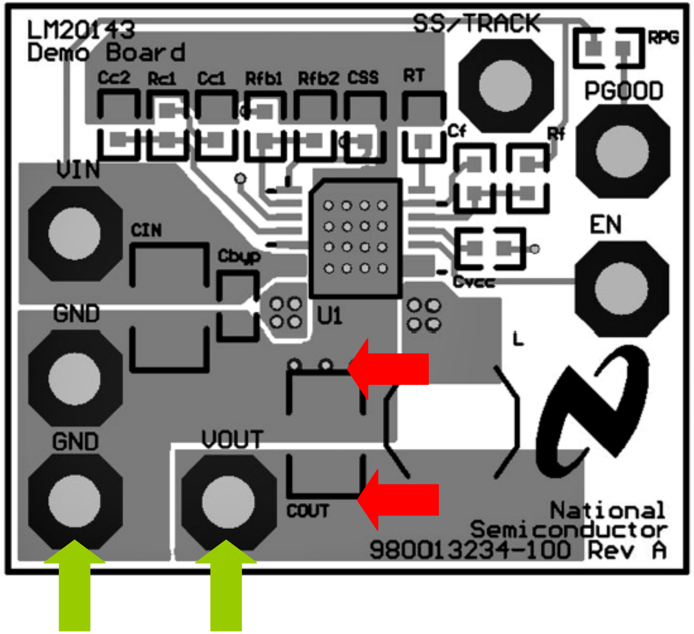
Correlation, DUT1: Measurement Location

DUT

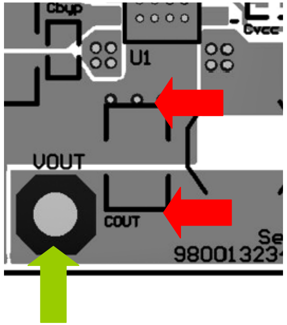
- Vin = 4.5V
- Vout = 1.2V
- 1.5A DC load current
- 0.5App transient step

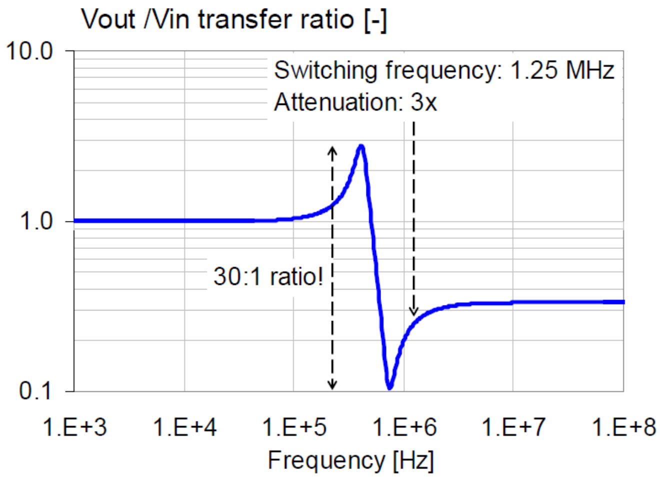
Instruments can be connected in a multitude of ways

- Across output terminals (*correct*)
- Across output capacitor (*wrong*)

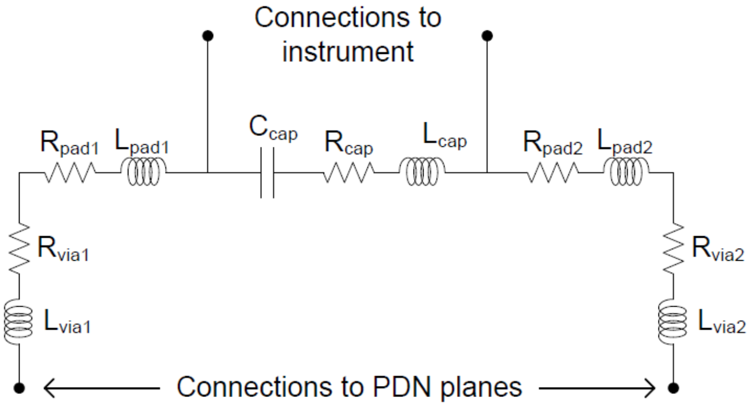


Correlation: Wrong Location



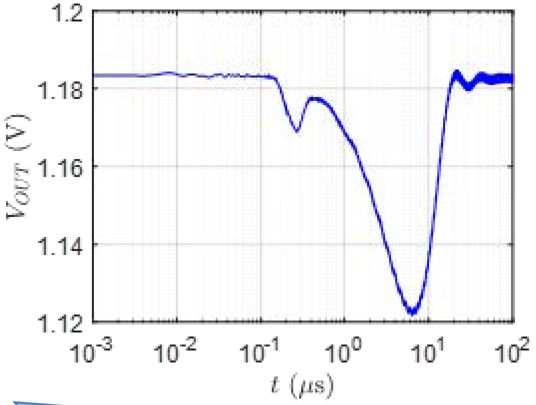


Low-ESR capacitors form resonant attenuators with via and pad impedance



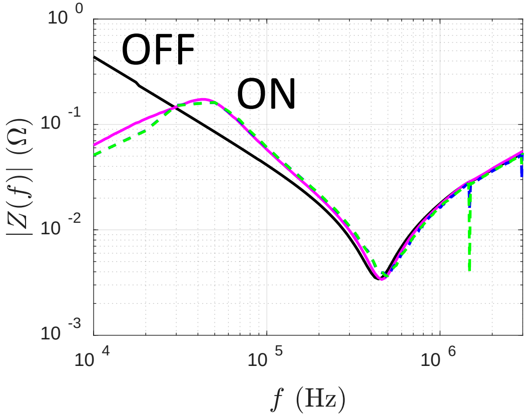
Correlation: Correct Location

Impedance curves:
- Measured with 0dBm VNA source power
- Calculated from falling transient response
- Calculated from rising transient response

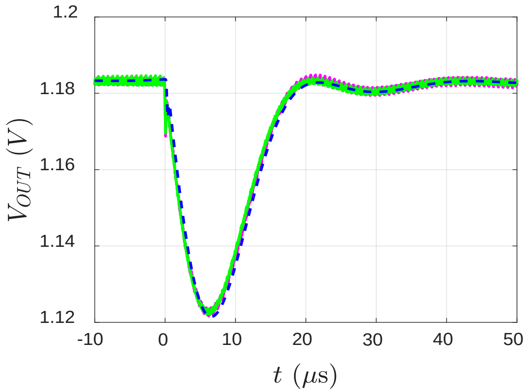


Logarithmic horizontal scale

Impedance vs. frequency

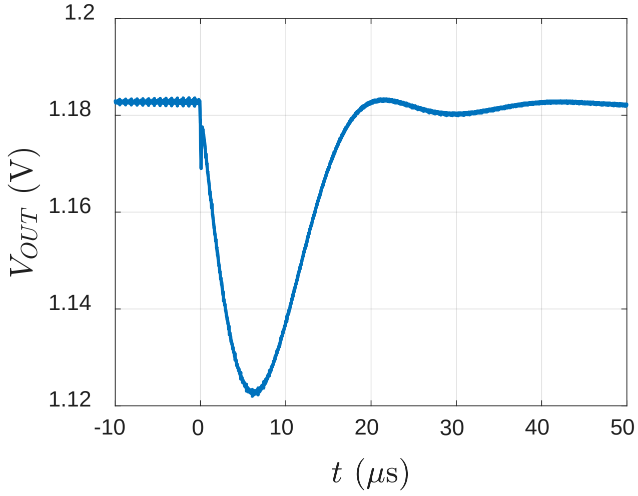


Normalized transient response



Transient curves:
- Measured falling response with oscilloscope
- Inverted rising response with oscilloscope
- Calculated from impedance

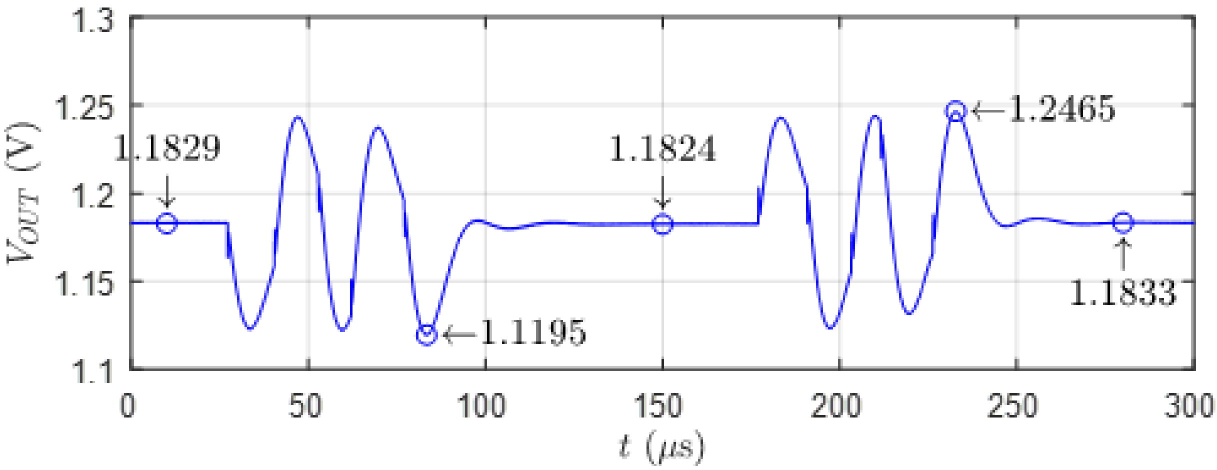
Step Response Details for Reverse Pulse Technique



Time (us)	Vout (V)
0	1.184
6.143	1.123
21.37	1.184
29.82	1.179
42.99	1.184
50.04	1.182

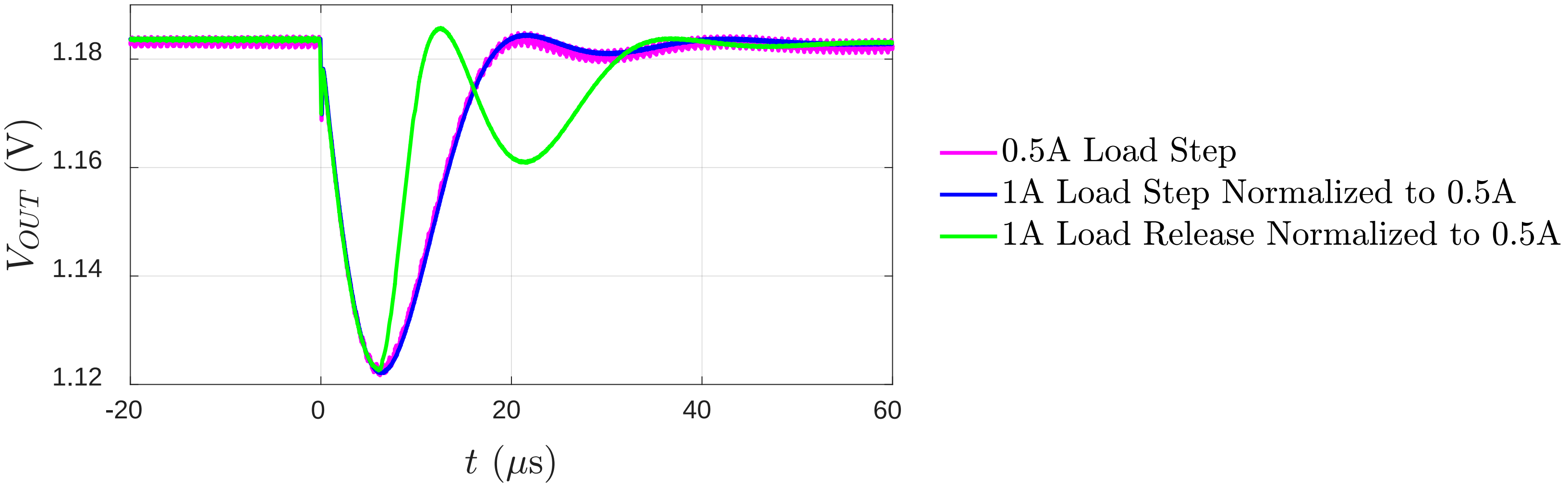
- Falling Step Response
- 1.5A DC load
- 0.5A step current
- Averaged to suppress switching ripple

Worst-Case Noise from Reverse Pulse Technique

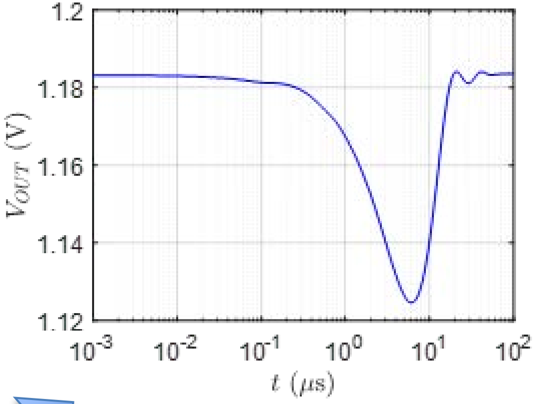


- Worst-case pattern
- 0.5A current steps
- Averaged to suppress switching ripple

Nonlinear Response



Distorted Data: Wrong Connections

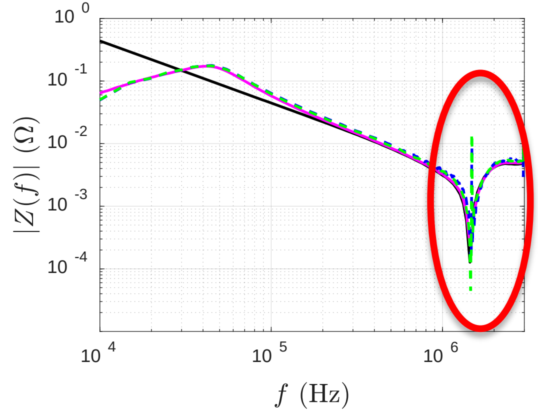


Impedance curves:

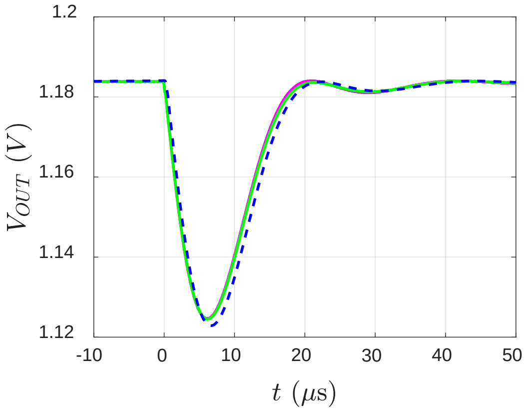
- Measured with 0dBm VNA source power
- Calculated from falling transient response
- Calculated from rising transient response

Logarithmic horizontal scale

Impedance vs. frequency



Normalized transient response



Transient curves:

- Measured falling response with oscilloscope
- Inverted rising response with oscilloscope
- Calculated from impedance

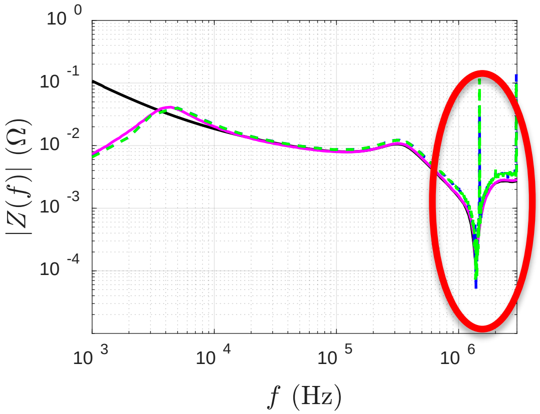
Wrong Connections, Added Capacitor

Impedance curves:
- Measured with 0dBm VNA source power
- Calculated from falling transient response
- Calculated from rising transient response

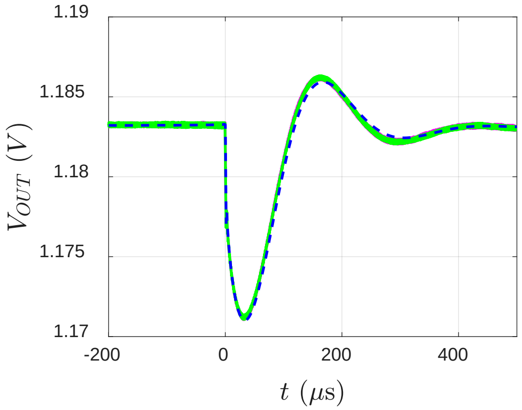
Transient curves:
- Measured falling response with oscilloscope
- Inverted rising response with oscilloscope
- Calculated from impedance

1500 uF polymer tantalum capacitor added to the output

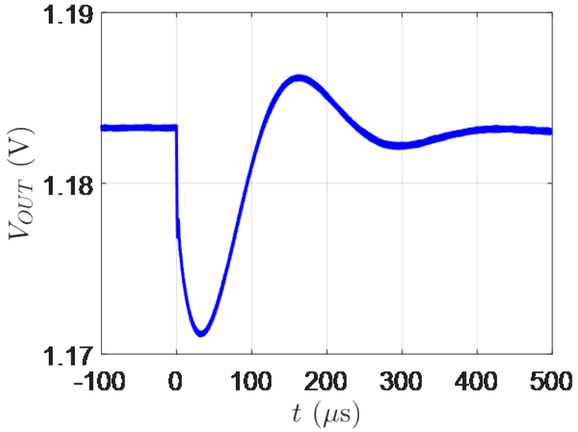
Impedance vs. frequency



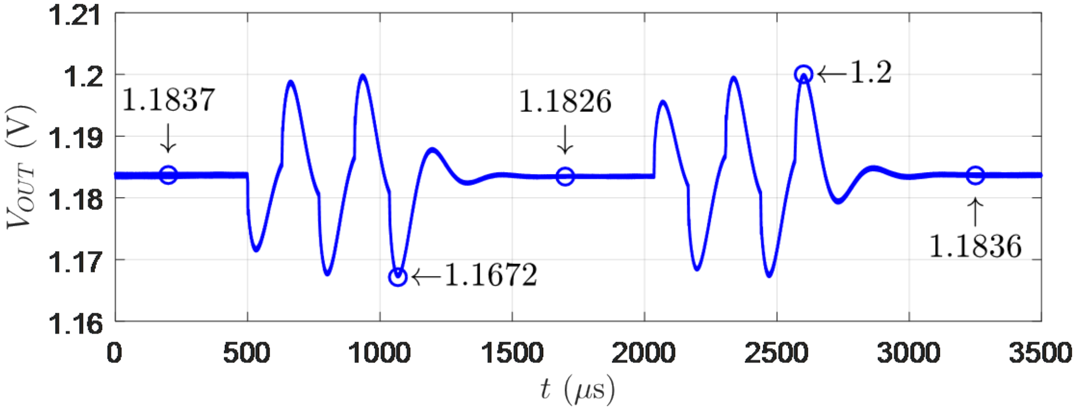
Normalized transient response



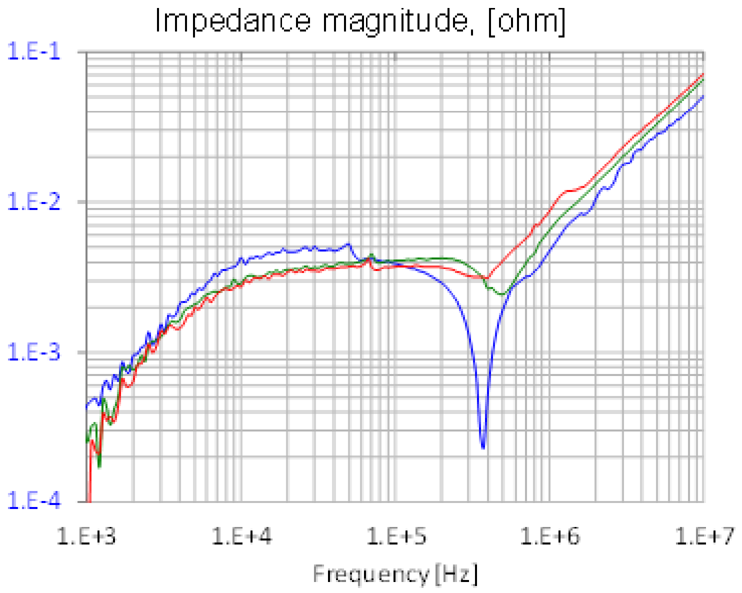
Added Capacitor, Worst-Case Transient Noise

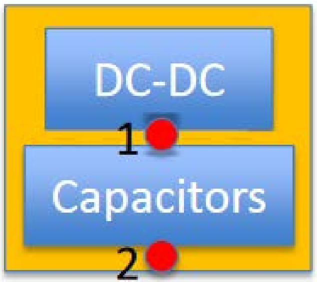


Time (us)	Vout (V)
0	1.183
33.63	1.171
164.4	1.185
303.7	1.183
433.0	1.182
565.0	1.1823



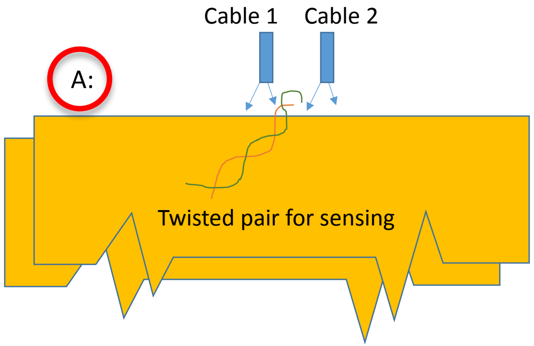
Location of Connections, DUT2

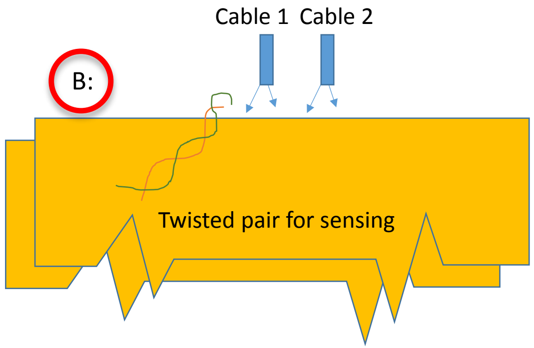


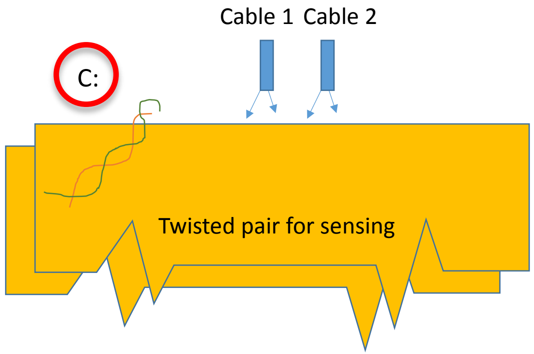


Output impedance curves at three different combinations of sense-point and measurement locations (from [8]). Red curve: measure at point 1, sense connected to point 2. Green curve: measure at point 2, sense connected to point 1. Blue curve: measure at point 2, sense connected to point 2.

Location of Connections, DUT2

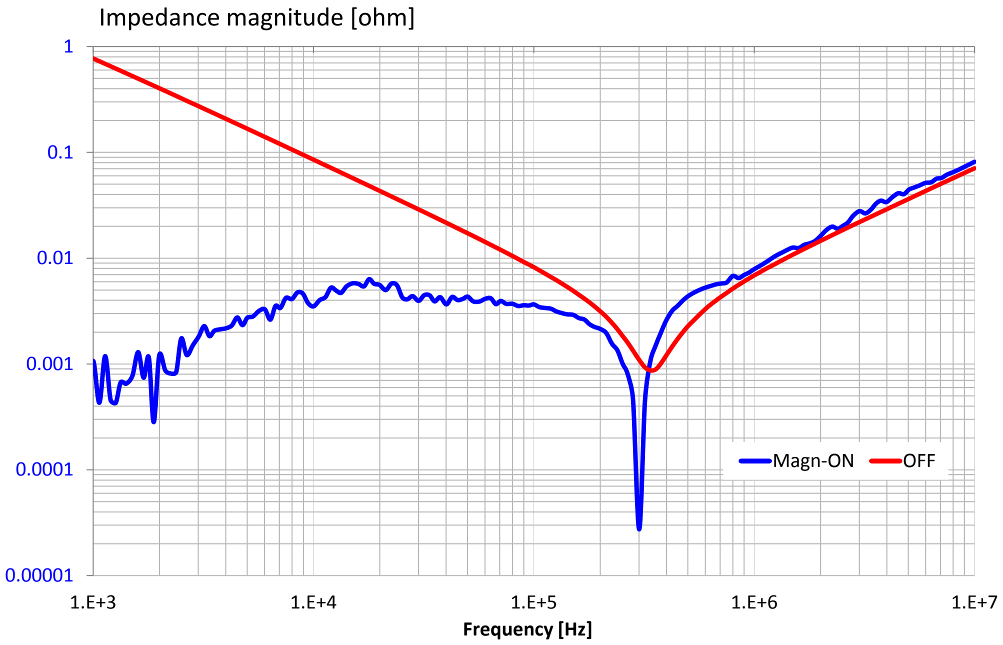






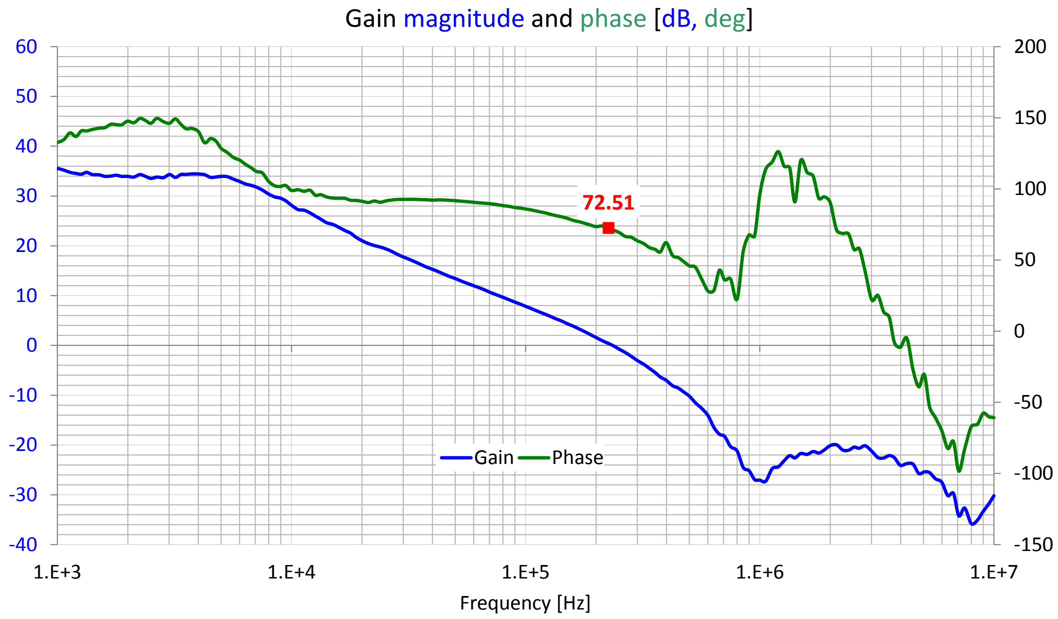
- Impedance measured with VNA
- Impedance measuring cables are Cable1 and Cable2
- Three sense-point connections

DUT2, Zout, Connection Scheme A



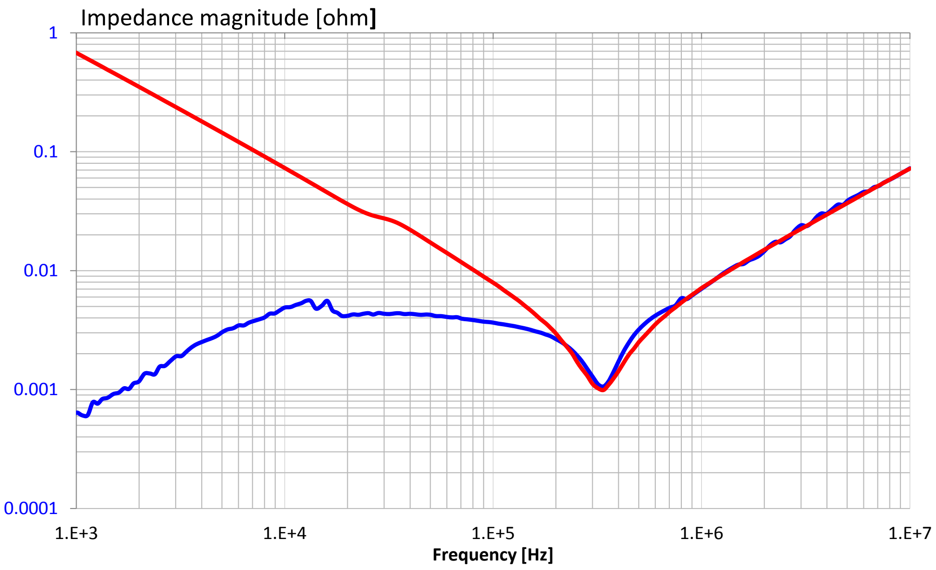
Coupling in connecting cable pigtail results in unrealistically low impedance at SRF.

DUT2, Gain-phase, Connection Scheme A



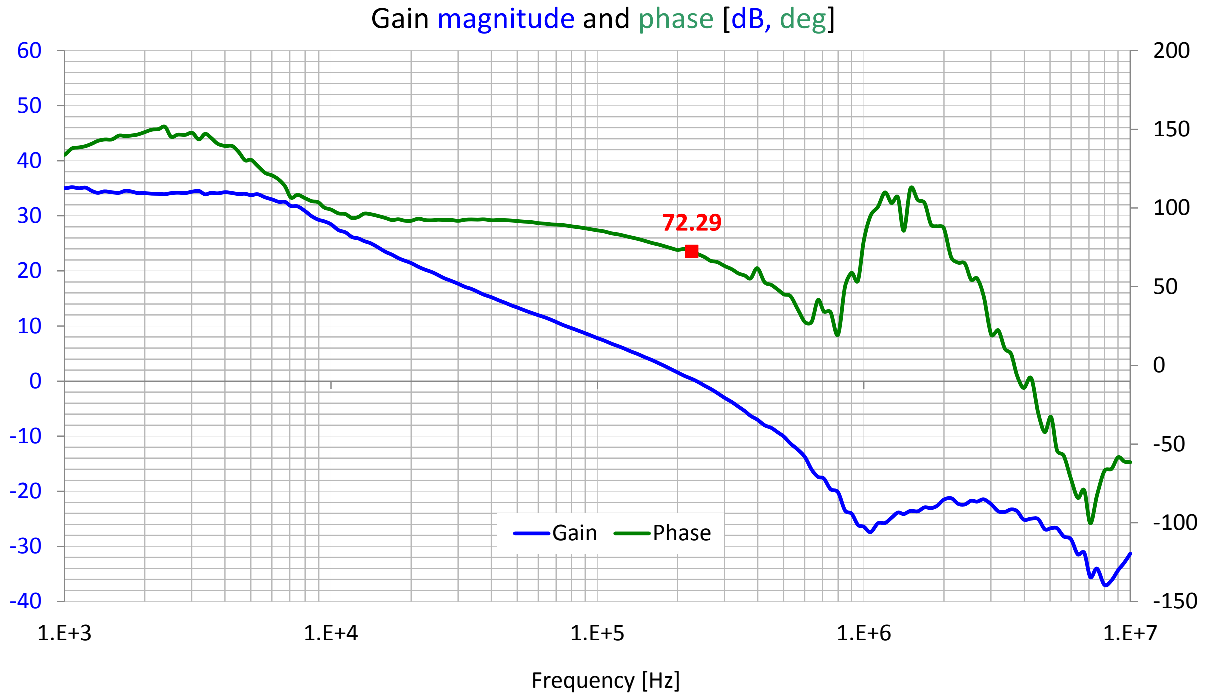
72.51 degree phase margin

DUT2, Zout, Connection Scheme B



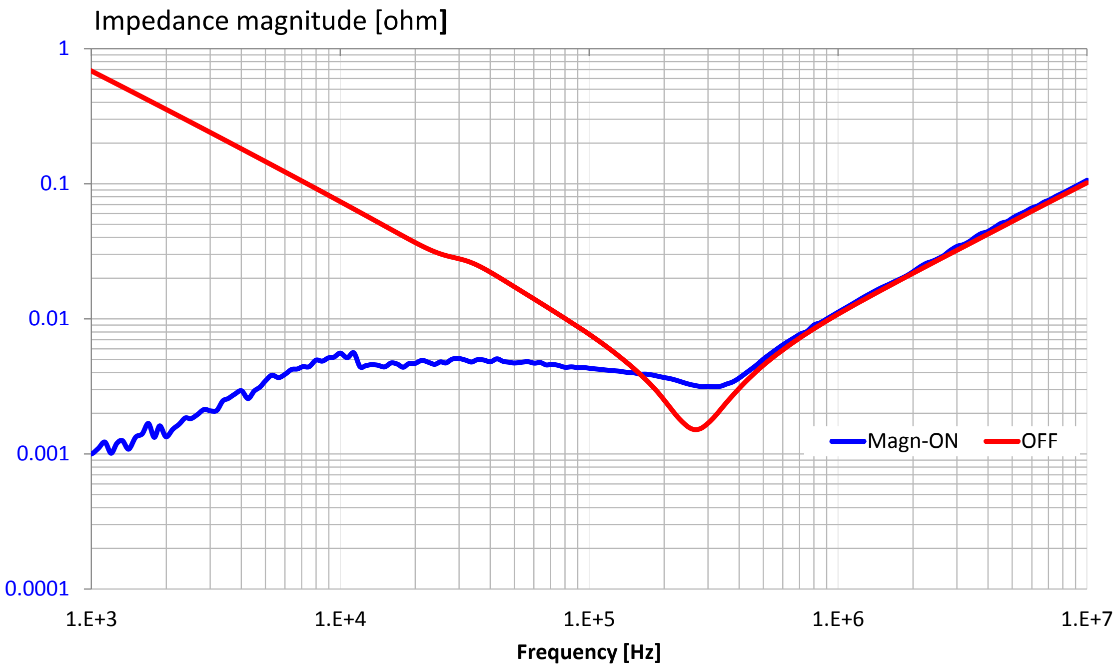
Coupling in connecting cable pigtail is at acceptable level.

DUT2, Gain-phase, Connection Scheme B



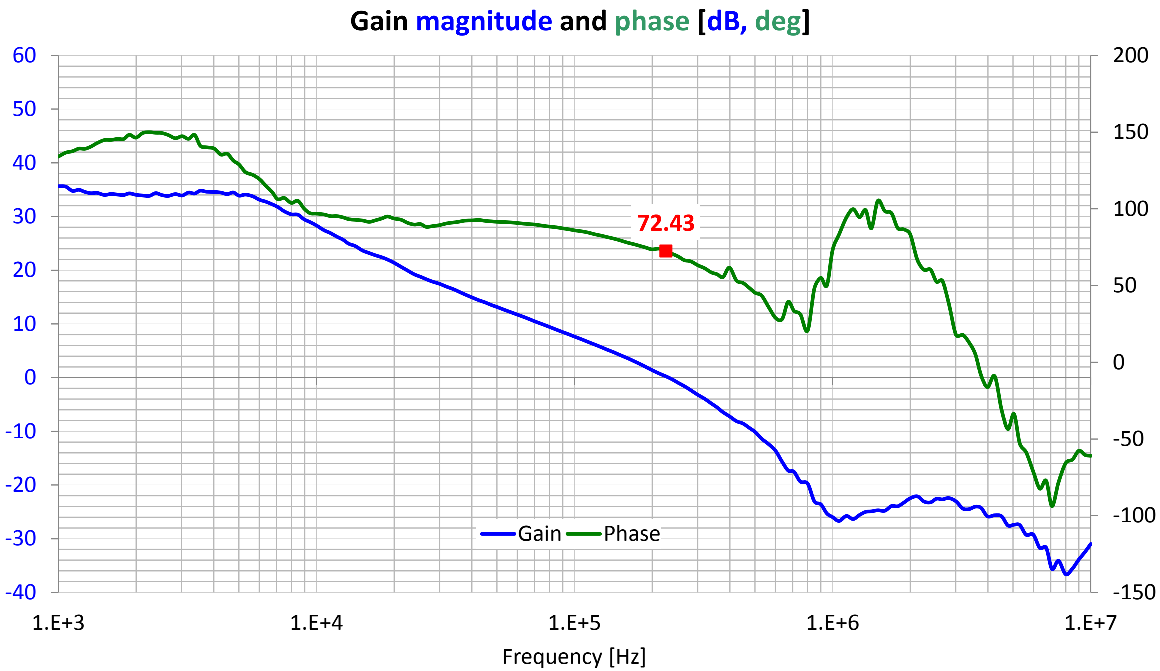
72.29 degree phase margin

DUT2, Zout, Connection Scheme C



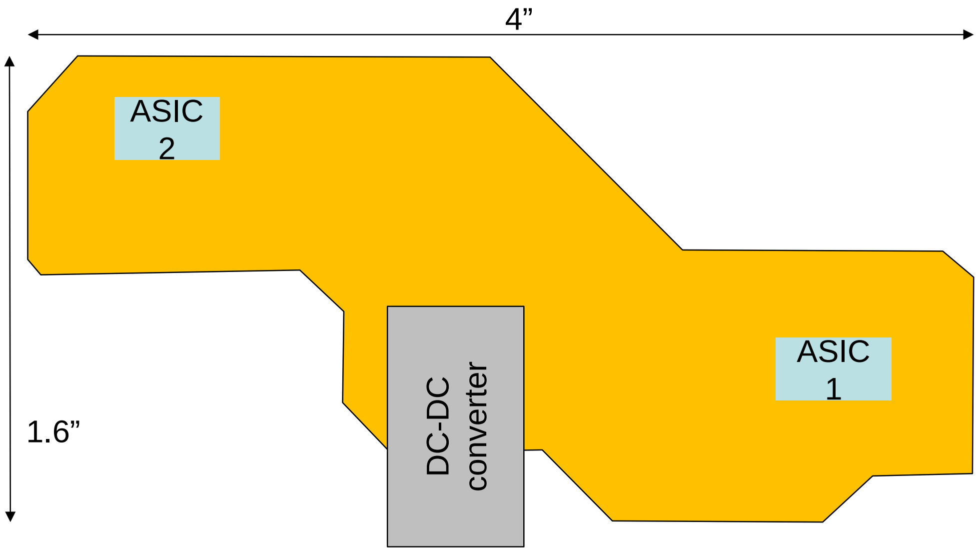
Coupling in connecting cable pigtail is at acceptable level.

DUT2, Gain-phase, Connection Scheme C



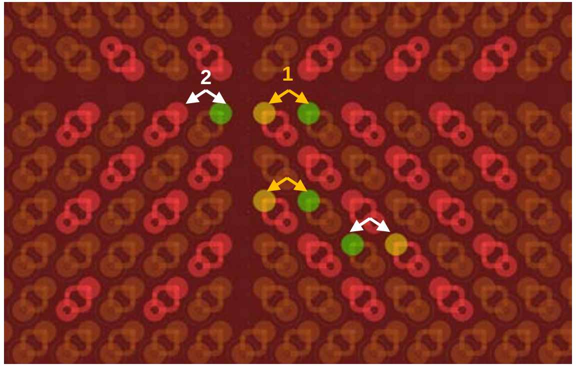
72.43 degree phase margin

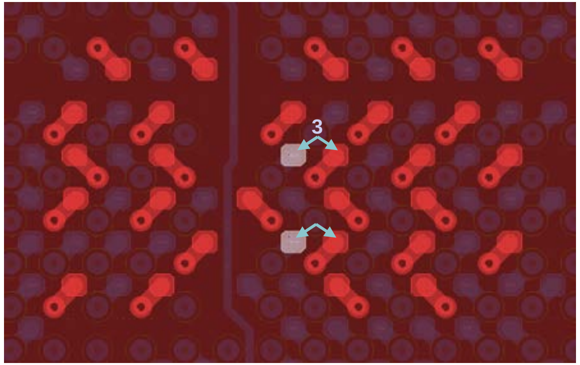
Impedance Variation by Design Choice, DUT3

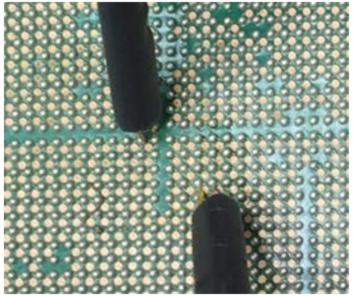


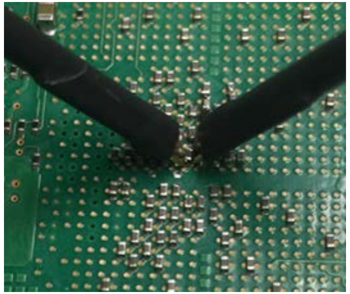
- Core rail for two ASICs
- Rectangles show core pin arrays
- DC-DC converter in the middle
- Sense-point options:
  - At ASIC1
  - At ASIC2
  - Average of ASIC1 and ASIC2
  - At DC-DC converter output

DUT3, Measurement Locations



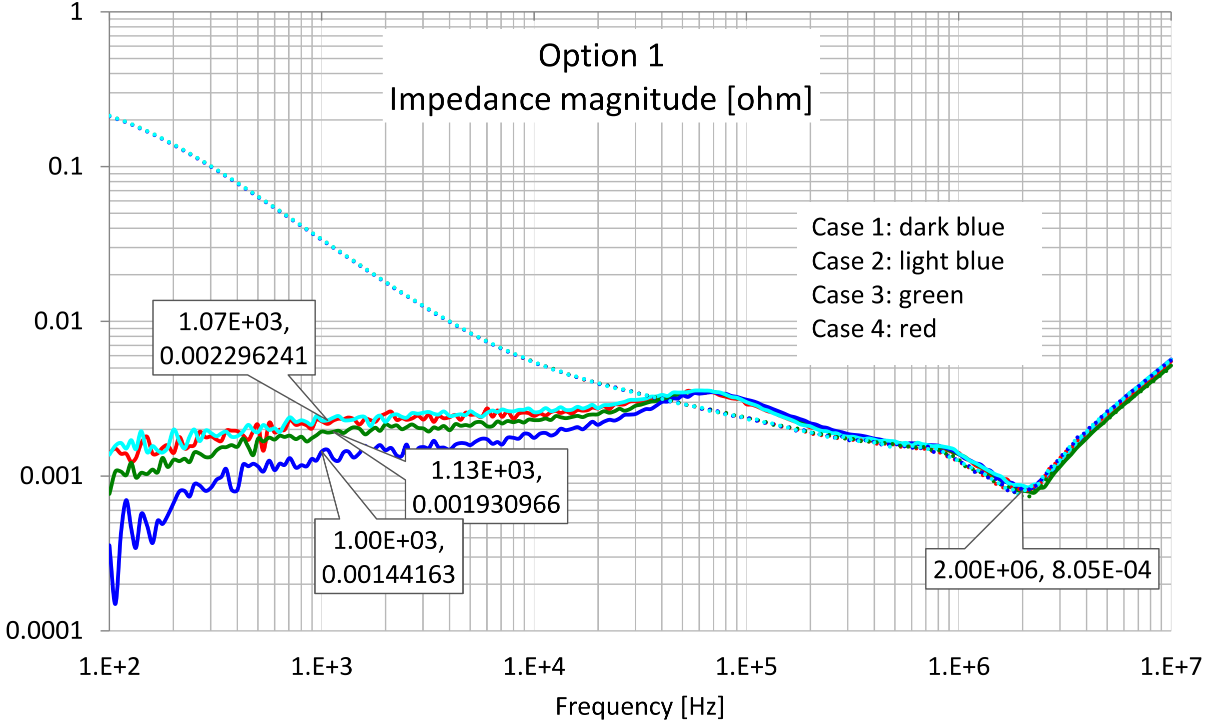






- Two-port connections in the ASIC core pinfield
- Option1: self impedance across adjacent pad pairs (top)
- Option2: partial transfer impedance (top)
- Option3: transfer impedance pad-to-capacitor (bottom)

DUT3, Option1



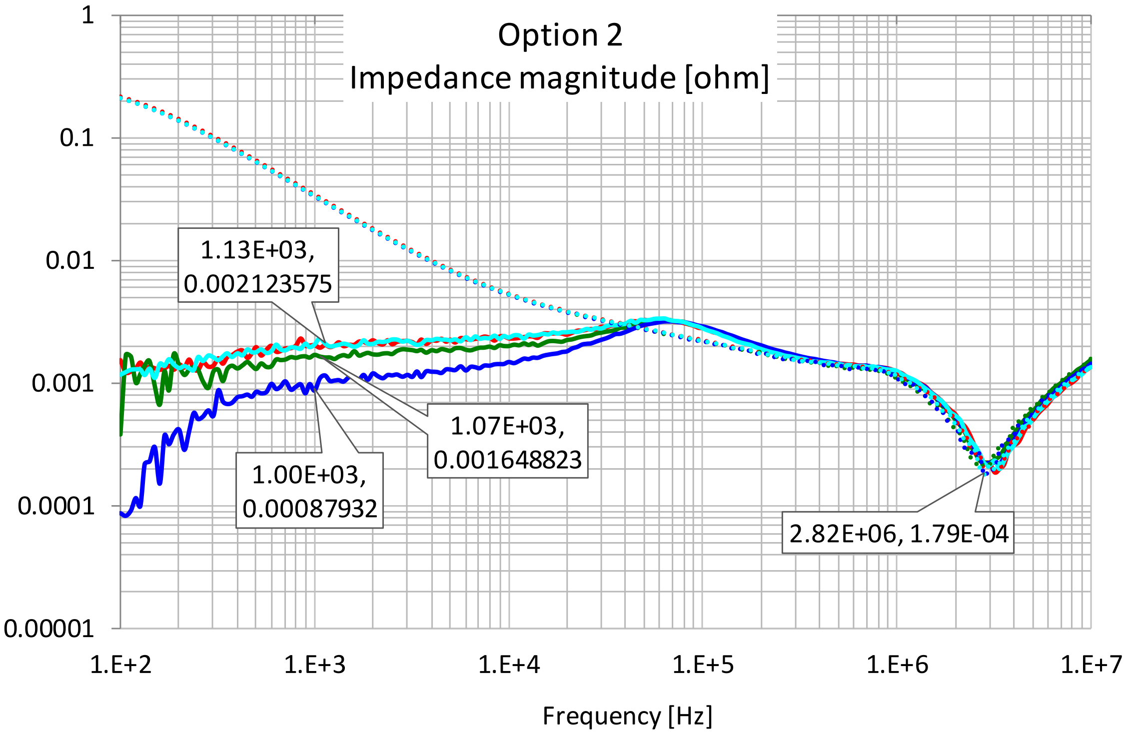
- Self impedance at ASIC1 pinfield

Sense connection:

- Case1: at ASIC1
- Case2: at ASIC2
- Case3: ASIC1 and ASIC2 average
- Case4: DC-DC output

Cases differ only below the crossover frequency

DUT3, Option2



Partial transfer impedance at ASIC1 pinfield

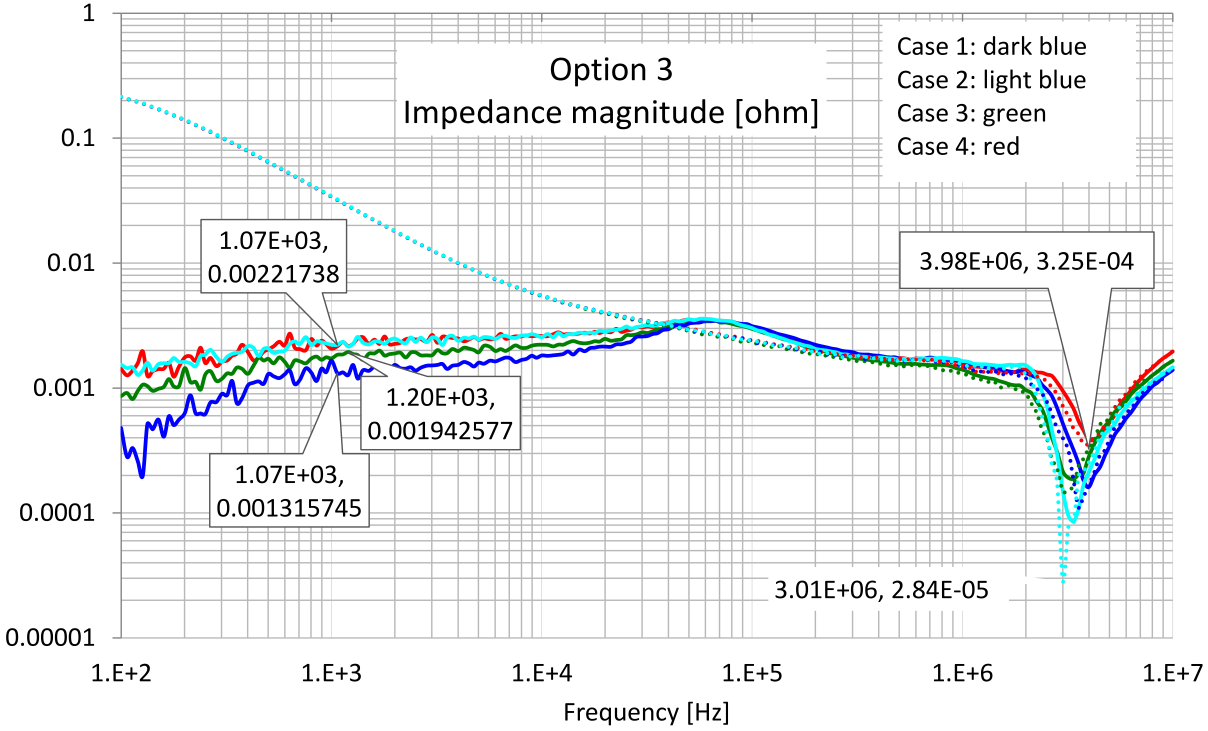
Sense connection:

- Case1: at ASIC1
- Case2: at ASIC2
- Case3: ASIC1 and ASIC2 average
- Case4: DC-DC output

Cases differ only below the crossover frequency

Deeper notch

DUT3, Option3



Pad-to-capacitor transfer impedance at ASIC1 pinfield

Sense connection:

- Case1: at ASIC1
- Case2: at ASIC2
- Case3: ASIC1 and ASIC2 average
- Case4: DC-DC output

Cases differ below the crossover frequency and at SRF

Conclusions

- For linear and time invariant systems, time and frequency domain results are equivalent
- Connections must be identical
- Worst-case transient noise increases with depth of notch in impedance
- Noise increase is additive for multiple notches
- Measurement probe placed on capacitor will alter data
- Further away from sense points the impedance is also influenced by plane resistance

Thank you!

QUESTIONS?