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Effect of Power Plane Inductance on Power Delivery Networks

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Abstract

Power plane loop inductance is an important metric in Power Delivery Network (PDN) design, but it is not easy to visualize how PCB design changes impact a power plane's loop inductance. This paper considers the impact on loop inductance of common power plane design changes such as the placement of vias, the anti-pad pitch and periodicity in a pin field array, and the placement of decoupling capacitors. The analysis considers tradeoffs of parametric values and provides guidance to engineers for PDN designs that meet a desired frequency response, minimize ground bounce, and reduce coupling due to power plane loop inductance.

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Shirin Farrahi is a Principal Software Engineer at Cadence Design Systems, Inc working on the development of Signal and Power Integrity tools. Prior to joining Cadence, she spent four years as a Hardware Engineer in the SPARC Microelectronics group at Oracle, working on the design of high-speed electrical and optical interconnects in servers. She received her Ph.D. in Electrical Engineering from the Massachusetts Institute of Technology.

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Istvan Novak is a Principle Signal and Power Integrity Engineer at Samtec, working on advanced signal and power integrity designs. Prior to 2018 he was a Distinguished Engineer at SUN Microsystems, later Oracle. He worked on new technology development, advanced power distribution, and signal integrity design and validation methodologies for SUN's successful workgroup server families. He introduced the industry's first 25 µm power-ground laminates for large rigid computer boards, and worked with component vendors to create a series of low-inductance and controlled-ESR bypass capacitors. He also served as SUN's representative on the Copper Cable and Connector Workgroup of InfiniBand, and was engaged in the methodologies, designs and characterization of power-distribution networks from silicon to DC-DC converters. He is a Life Fellow of the IEEE with twenty-five patents to his name, author of two books on power integrity, teaches signal and power integrity courses, and maintains a popular SI/PI website.

Introduction

As Power Delivery Network (PDN) designs continue to become more challenging, engineers require the ability to understand the impact of design changes on a PDN's frequency response. Among the many factors to consider in PDN design is power plane to return plane loop inductance. Inductance is not only important in determining the PDN frequency response and ground bounce noise on a printed circuit board (PCB) but under some circumstances it is also difficult to intuitively estimate. When the inductance is formed by a series chain of traces and/or vias, the inductance may be reasonably easy to estimate by looking at the geometry. In many PDNs, on the other hand, there may be odd shapes of planes, potentially coupled or changing to other layers through via transitions interconnected with multiple vias over large areas. Under such circumstances simple estimates of self and coupling inductances become much more challenging. In this study, we look at a series common power plane design changes to give engineers a more intuitive understanding of power plane inductance to reduce the number of simulations needed when designing a PDN.

We start by correlating our power plane loop inductance simulation results with measurements from two different PCB designs. In the first, we use a small PCB and add decoupling capacitors to show the impact on power plane loop inductance in both measurement and simulation. In the second board, we show power plane loop inductance for a single power plane covering a small portion of a large motherboard. We measure and simulate two versions of the motherboard design with variations to this power plane.

In addition to looking at power plane loop inductance, we correlate the impact of loop inductance on coupling to nearby signal traces using the large motherboard with a known coupling issue due to power plane loop inductance from a DC-DC converter to a nearby high-speed signal [1].

Measurement to Simulation Correlation

A hybrid field solver is used for extracting loop inductance throughout this paper [2]. The solver uses combinations of numerical methods and approximations to solve for electromagnetic fields and extract S-parameters for power and ground nets in package and PCB structures. Corresponding impedance elements are then postprocessed to deduce loop inductance values for the nets on the PCB. The technique used in this paper is similar to that used in [3] where the authors extracted inductance values based on a modal-based cavity method. Their solution is suited for ideal package geometries where assumptions such as perfect metal conductor (PMC) walls are justified. The authors also assume no vertical electric field exists in that structure. Such an assumption is not justified for general package and PCB structures, like the ones considered in this paper, due to existence of vias and coupling through anti-pads in power and ground planes. The Hybrid solver technique used in this paper is general in that it does not assume horizontal fields only and does not need PMC walls to terminate the fields. It can be applied to any general structure as will be shown in next sections.

A three-way correlation was pursued by an unknown Cadence employee in order test the validity of the solver. The correlation was done on the same structure relative to measurement values and extractions obtained using other field solvers. A 2'x2'organic Ball-Grid Array Package was used for both extraction and measurements. Figure 1 shows an isometric view of the package. It is composed of two thin buildup layers on top and bottom; and a core layer of 800 um in between.

High quality probes were used for S-parameter measurements for a power net. Two ports were setup and used for the measurements. The results were postprocessed to obtain corresponding impedance curves from 50 MHz to 20 GHz.



Figure 1: Ball-Grid array package used for measurements and simulations

Impedance plots are shown in Figure 2. Impedance values extracted from measurements are shown in black. Impedance values extracted from the Hybrid solver are shown in green. The DUT in this case is the unpopulated open-edge plane pair across the package's 800 um core cavity. Good agreement is achieved among results obtained using the solver and those from measurements. To further verify the results two more extractions were done: using a 3D Finite-Element Method solver (3DEM) and a third-party tool. Those extractions are shown in blue and red, respectively. All extracted results agree with each other well. This agrees with measurement to simulation correlation from a recent study on power planes of thin laminate test boards [4], which shows open-edge plane capacitance but also shorted-edge plane inductance correlations.

To validate our simulation approach further, we looked at the correlation of our inductance simulations to measurements at lower frequencies than shown in Figure 2 on two boards: i) a small integrated circuit (IC) test board and ii) a large motherboard.



Figure 2: Measured (black) vs simulation (green, blue, and red) impedance of the ball-grid array package

Small IC test board

The first board was designed to test a small IC. It is a ten layer board with four ground planes, and two power planes sandwiched on layers five and six. We performed simulations and measurements on a 0.85V power plane covering roughly one-quarter of the board on layer 5 of the stackup (Figure 3). All of the ground layers are connected together by ground vias. The plane is fed by a switching voltage regulator on the lower right. It has eight decoupling capacitors, and it connects to the main IC on the upper left.

Layer	Material	Thickness (mils)
TOP	Copper	2.1
	FR4	3.7
LAY2 – GND Plane	Copper	1.2
	FR4	6
LAY3 - SIG1	Copper	1.2
	FR4	5.8
LAY4 – GND Plane	Copper	1.2
	FR4	4
LAY5 – PWR1 Plane	Copper	1.2
	FR4	15.4
LAY6 – PWR2 Plane	Copper	1.2
	FR4	4
LAY7 – GND Plane	Copper	1.2
	FR4	5.8
LAY8 – SIG2	Copper	1.2
	FR4	6
LAY9 – GND Plane	Copper	1.2
	FR4	3.7
BOTTOM	Copper	2.1

Figure 3: Stackup of small IC test board with layer used for power plane measurement circled in red

To cover the 100 kHz to 200 MHz frequency range, the measurements were done with a low-frequency Vector Network Analyzer [5] in two different configurations, and the results were combined in external post-processing. At around 100 kHz the measured loop impedance of the PDN is dominated by the plane and via resistance, producing magnitude values in the milliohm range. Moreover, the typical PDN device under test (DUT) is not connectorized, and therefore if we attempt to measure such low impedances with a one-port measuring setup, the impedance of discontinuity of the connection will mask the correct data [6]. Two-port shunt-through measurements will work, but the cable-braid loop formed by the two measuring cables must be opened [7]. The instrument we used [5] has a low-frequency section that has semi-floating connector returns, which greatly suppress the cable-braid loop error, but above 30 MHz we still need to switch to the S-parameter side of the instrument.

We chose the S-parameter side of the instrument and used home-made pigtail connections to measure the small IC test board and wafer-probes and a probe station to measure the large computer board. The frequency range was split into two: 100 kHz to 10 MHz and 1 MHz to 200 MHz. To suppress the cable-braid loop error in the lower band, a home-made common-mode toroid transformer was added in series to the port 2 cable. In the low frequency range a response THRU calibration was used, by connecting the probe tips together. The transformer had a useful frequency range up to about 50 MHz, above which it had to be removed. Since the cable-braid loop error above 1 MHz is naturally suppressed by the cable's inherent braid inductance, the upper frequency range used direct cable connections and full two-port short, open, load, thru (SOLT) calibrations to the end of the cables. Both boards under test were measured with both setups.

To perform our power plane loop inductance measurements and simulations, we shorted the pin on the voltage regulator source to its nearby ground pin then took measurements from the power and ground pins on the main IC from 100 kHz to 200 MHz. We started with the bare board (Figure 4). We see that both measurement and simulation show a loop inductance in the several nano-Henry range with similar behavior across frequency in both measurement and simulation. Figure 5 shows the impedance magnitude and phase for the simulation data shown in Figure 4. From measured or simulated data, the inductance is extracted from the imaginary part of the series impedance, which has an equivalent circuit topology of a resistor in series to an inductor:

$$Z_s(f) = R(f) + j\omega L(f) = Re\{Z_s(f)\} + jIm\{Z_s(f)\}$$

Knowing the frequency where the measurement or simulation was taken, we can compute the L(f) inductance by dividing the imaginary part of the impedance by the radian frequency, $2\pi f$.



Figure 4: Measured (blue and green) vs simulated (pink) inductance of the bare board



Figure 5: Impedance magnitude (top) and phase (bottom) for simulation of the bare board

To test our correlation further, we soldered three of the larger decoupling capacitors to the power plane, adding one at a time and taking measurements. Adding each capacitor decreased the inductance as will be shown in the simulation results later. The right panel of Figure 6 shows the measurement to simulation correlation with all three decoupling capacitors present. They were 47μ F, 22μ F, and 1μ F capacitors located as shown in the

left panel of Figure 6. The 1μ F capacitor was contained within the pin field of the main IC. For the simulation, we used s-parameter models of each capacitor.



Figure 6: Left panel: One-quarter board diagram top view showing locations of three capacitors and approximate shape of power plane being measured. Right panel: Measurement (blue and green) to simulation (pink) correlation for the 0.85V power plane with three decoupling capacitors present.



Figure 7: Impedance magnitude (top) and phase (bottom) of 0.85V power plane with decoupling capacitors from simulation

Large Computer Motherboard

We next performed measurement to simulation correlation on pre-production prototypes of a large Oracle motherboard containing 24 layers and two processors with four PCIe

ports per processor. The first version of this motherboard was previously shown to have mid-frequency noise coupling onto a PCIe lane from a nearby DC-DC converter [1]. We performed measurements and simulations on the power plane that was causing the noise on both the original and fixed versions of the motherboard.

The rails of interest on the board had their converter ICs removed such that the only components remaining on the rail were PDN capacitors and components that form the current path of the inductive loop. The measurements on this board were taken using a low-frequency VNA [3] with a wafer probe station and rigid wafer probes (Figure 8). The pads to be probed on the board were large, so the wafer probe station was necessary to obtain repeatable measurements consistent with the port locations from the simulation software (Figure 9). As done with the measurements on the smaller board previously discussed, a two-port shunt-through S21 measurement was executed, and the inductance data was extracted in post processing.



Figure 8: VNA used with wafer probe station to measure S21 of power rail



Figure 9: Comparison of wafer probe measurement locations (left) and simulation port locations (right)

Figure 10 shows the measurement to simulation correlation for the aggressor power rail on the original version of the motherboard. We see correlation within 20% for most of the frequencies above 1 MHz. In the final version of the motherboard (Figure 11), the decoupling capacitors were moved to the top of the board to significantly reduce the aggressor loop size. We see that both simulations and measurements show this decrease by roughly a factor of two in the power plane loop inductance. The three measurement curves in Figure 11 were taken with no choke (blue), with a common-mode choke (yellow), and with a Picotest J2102B-N common-mode transfer (purple). Readers should note the variability seen between the three measurements.



Figure 10: Measurement (blue) and simulation (orange) of loop inductance on aggressor rail from first version of large motherboard



Figure 11: Measurements (blue, yellow, and purple) and simulation (orange) of loop inductance on aggressor rail from final version of large motherboard

Power Plane Variations

After validating our simulation approach for power plane loop inductance over a variety of conditions, we now use the flexibility of the simulator to explore a wider variety of design parameters on power planes to determine their impact on loop inductance. The trends described here sometimes have complex frequency-dependent behavior. We have chosen a single frequency point to simplify the comparisons and have selected the frequency point to be at a location where the phase of impedance is not close to zero where small changes in the imaginary part of impedance will be difficult to detect.

Plane Width

With increasingly limited board space available, designers are continually shrinking the size of power planes to make them fit. To understand how this could impact power plane loop inductance, we took a square power plane with 1.4" sides and cut the corners off sequentially to make a gradually narrower plane from the source to the sink. Figure 12 shows the impact that this has on the power plane loop inductance. We see that until the power plane becomes less than 500 mils wide, the power plane loop inductance only increases by a factor of 3%. However, once the plane gets much thinner than 500 mils, the power plane loop inductance increases much more significantly.



Figure 12: Impact of plane width on power plane loop inductance at 2 MHz. Plane width varied by cutting corners off a square plane as illustrated in the inset diagram.

Anti-Pads

We looked at the impact of anti-pad holes in the ground and power plane on power plane loop inductance by varying the number, spacing, and diameter of anti-pad gaps. We found that with a few anti-pads on the plane, the number and spacing had little impact on power plane inductance. A much more significant factor was the diameter of anti-pad holes. Figure 13 shows that to have a significant impact on power plane inductance, we had to make the holes much larger than would normally be used in pin fields. For each diameter selected, we place enough holes to cover the entire width of the plane with 5 mil spacing between the holes.



Figure 13: Impact of anti-pad hole diameter on power plane loop inductance at 2 MHz

Vias

We studied the impact of power and ground vias near the source on power plane inductance. The vias were connected to a small power plane shape on the surface within 150 mils of the source. We found that placing them far from the source or sink had very little impact on inductance at the frequencies we studied. As shown in Figure 14, the power plane inductance decreased significantly between one and two power vias. As we added more vias, the inductance continued to decrease, but the rate of decrease.



Figure 14: Impact of number of power vias near source on power plane loop inductance at 2 MHz. The vias were added in the region shown in the inset diagram.

On the case shown in Figure 14 with eight vias, we also looked at the impact of via barrel size. We found that changing the via barrel size from 4 mils to 20 mils changed the loop inductance by only 2 pH or 0.2%. With a larger via array, the impact might be greater.

We also looked at the impact of the number of ground vias near the source on power plane loop inductance and as shown in Figure 15 found a similar impact to the addition of power vias shown in Figure 14. The greatest decrease in inductance came from going from no ground vias to four. The addition of further vias decreased the inductance further but not as significantly.



Figure 15: Impact of number of ground vias near source on power plane loop inductance at 2 MHz. The vias were added in the region shown in the inset diagram.

Number of Decoupling Capacitors

Using the IC test board from our correlation work, we looked at the impact of removing each of the eight decoupling capacitors on the power plane. As shown in Figure 16, the power plane loop inductance continued to increase as we removed each capacitor. The largest impact was seen when the last 1 μ F capacitor was removed because this was the last decoupling capacitor connecting the plane to ground on the top layer of the board as shown in the diagram on the left. The return current then had to make a much longer path to the bottom of the board, causing the loop inductance to increase significantly from 618 pH to 1630 pH.



Figure 16: Impact of decoupling capacitor removal on power plane loop inductance at 1 MHz

Power to ground short

We shorted the power plane to ground using a via and moved the location of the short from near the sink to the source. As expected, the inductance see by the sink increased as we moved the short away from the sink since the size of the loop increased (Figure 17). Although shorting the power and ground planes is not a common design change, we can think of this as an approximation of a power to ground capacitor with ESL at its lowest impedance.



Figure 17: Impact of power to ground short on loop inductance at 2MHz

Power to ground inductance

We replaced the power to ground from the previous case with a 1 nH inductance to mimic a capacitor's ESL. As expected, the inductance see by the sink increased as we moved the inductance away from the sink since the size of the loop increased (Figure 18). Although the inductance was 1 nH, the inductance as seen by the sink is less than 1 nH because the source pin is shorted to ground giving a parallel path for the current. The total inductance is the parallel combination of these two loops.



Figure 18: Impact of power to ground inductor on loop inductance seen from the sink at 2MHz

Effect of Loop Inductance on Coupling

Since return path discontinuities which can impact power plane loop inductance can have a large impact on noise coupling, we looked at measurement to simulation correlation for the power plane on the first prototype version of the Oracle motherboard known to have noise coupling onto a PCIe lane from a power plane. The left panel in Figure 19 is from a DesignCon 2016 paper [1] where the S21 coupling from the power plane to the victim PCIe legs was shown to decrease from the original to the final versions of the board. Our simulated results in the right panel show a similarly dramatic difference in S21 coupling between the original and final versions of the board, but the overall magnitude of S21 predicted by our simulator is significantly lower than the measurements show. We believe that this is partly due to the noise floor of the measurement system since the higher frequency results match more closely than the low frequencies. However, another factor could be that the coupling presented here takes place over a large portion of the motherboard. To allow the simulations to complete with limited memory, we disabled all the nets except the aggressor and victims. The absence of other structures or a mismatch in the ESL values of simulated capacitors from the real ones could also explain some of the difference in S21 magnitude between measurement and simulation.



Figure 19: S21 from aggressor to victim PCIe lane from measurements (left) and simulation (right)

The most significant technique used to reduce coupling from the original to the final version of the board was to move decoupling capacitors on the aggressor rail from the bottom to top of the board so that they would be on the same side as the DC-DC converter sourcing the rail. This greatly decreased the loop size on such a large board as seen by the loop inductance values in our measurement and simulation results, but it also changed the orientation of the aggressor loop so that the victim loop would not pick up as much of the noise being produced. There were also several ground vias added near the victim layer transition points. However, from our simulations, we found that the addition of ground vias decreased the aggressor loop inductance by only a few percent; whereas, the change in decoupling capacitor location had a huge impact on power plane loop inductance.

Conclusion

Power plane loop inductance is an important metric in PDN design not only because it impacts PDN frequency response but also because it can play a role in coupling of noise from power planes to high-speed signal traces. In this study, we correlated hybrid simulation results with power plane loop inductance values on a variety of boards then used this efficient simulation engine to predict the impact of common design parameters on power plane loop inductance. We showed which design parameters would have the biggest impact on reducing power plane loop inductance to reduce ground bounce noise and coupling in high-speed PCB designs. Our hybrid simulator has been shown to be an efficient tool in gaining insight into the consequences of layout on power rail inductance as well as the effects of this inductance on important peripheral nets.

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