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Etch Factor Impact on SI & PI

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Abstract

High frequency losses, crosstalk, impedance discontinuities, DC losses etc. are some of the physical phenomena that make us, SI/PI engineers spend most of our time. The slanted etch characteristics of traces called etch factor, affects all the above. This study will show how important or not is this effect for different type of applications. With the objective to provide simple guidelines to the practitioner engineer, we look at many cases where the etch factor may play a role, ranging from the effect on traces at high speed, to the effect on heavily perforated planes at DC for current distribution.

Biographies

Gustavo Blando is a Senior Principle Engineer leading the Principal SI/PI Architect at Samtec Inc. In addition to his leadership roles, he's charged with the development of new SI/PI methodologies, high speed characterization, tools and modeling in general. Gustavo has twenty plus years of experience in Signal Integrity and high speed circuits.

Rula Bakleh is Signal and Power Integrity Consultant specializing in aiding customers with their high-speed SerDes, parallel interfaces (e.g. DDR), RF/microwave, and power integrity designs and analysis for IC packages, circuit boards and systems. Her accomplishments include many first-pass-success high-speed/high-power designs. Ms. Bakleh is member of DesignCon's Technical Program Committee and Signal Integrity Journal editorial advisors committee. Ms. Bakleh is currently working for Samtec-Teraspeed Consulting and has also worked at Woodward-McCoach, L-3 Communications, BAE Systems and Raytheon. She received her BSEE in 1997 from SUNY Binghamton and her MSEE in 2003 in Microwave/RF Engineering from UMASS Amherst.

Jim DeLap is an electronics product manager for Ansys, working with the company's customers and research team to provide the highest quality simulation workflow. He has an MSEE from the University of Virginia, and has been working in the microwave and signal integrity field for over 20 years. He has designed products ranging in frequency from DC to mm-wave, and has several published trade journal and conference articles. His current interests include helping customers solve challenging electro-thermal problems.

Scott McMorrow is an expert in high-performance design and signal integrity engineering, with a broad background in complex system design, electromagnetics, interconnect modeling, measurement methodology, and professional training spanning over 30-ish years.

Ethan Koether is a Hardware Engineer at Oracle Corporation. He is currently focusing on system power-distribution network design, measurement, and analysis. He received his master's degree in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology.

Istvan Novak is a Principle Signal and Power Integrity Engineer at Samtec, working on advanced signal and power integrity designs. Prior to 2018 he was a Distinguished Engineer at SUN Microsystems, later Oracle. He worked on new technology development, advanced power distribution, and signal integrity design and validation methodologies for SUN's successful workgroup server families. He introduced the industry's first 25 µm power-ground laminates for large rigid computer boards, and worked with component vendors to create a series of low-inductance and controlled-ESR bypass capacitors. He also served as SUN's representative on the Copper Cable and Connector Workgroup of InfiniBand, and was engaged in the methodologies, designs and characterization of power-distribution networks from silicon to DC-DC converters. He is a Life Fellow of the IEEE with twenty-five patents to his name, author of two books on power integrity, teaches signal and power integrity courses, and maintains a popular SI/PI website.

I. Introduction

I.1. Why etch factor may matter

High frequency losses, crosstalk, impedance discontinuities, DC losses etc., are some of the physical phenomena that make us, SI/PI engineers spend most of our time. Depending of the application, some of these impairments are more important than others. For example, if our concern is PI, we will be very closely looking at DC resistance and global current distribution on planes. On the other hand, if we are mostly interested in clean point to point transmission at high speed, we might be much more concerned about crosstalk between traces.

On PCB structures, all these impairments are, one way or the other, related to manufacturing processes and tolerances affecting the full frequency range, from DC to GB/s data transmission. One of these manufacturing impairments is the slanted sidewalls of edges present on traces and planes after they've been etched on the board. This phenomenon is normally called etch-factor by the SI/PI community.

Over the years, engineers have had to deal with this physical anomaly, but not many studies have been published to understand the real impact it has on a multitude of applications.

At high frequencies, mostly in SI applications, the etch-factor on traces will have the effect of changing the characteristic impedance [1], increasing copper losses, increasing crosstalk, and depending of the trace configuration, it might interact differently with its surrounding dielectrics.

At low frequencies, for power distribution on heavily perforated planes, the etch factor that is present on plane anti-pads might take away the needed copper for current distribution, effect that will be compounded as we increase the copper thickness.

In this study we'll start by showing why the etch-factor occurs and what would be its expected value for normal manufacturing processes. Then we'll analyze several cases where the etch factor might play an important role to determine its importance or lack thereof. For SI applications we'll look at the impact the etch-factor has on impedance, losses and crosstalk for many different cases, covering stripline over full and perforated planes. For PI applications we'll analyze the increased plane perforation resistance from the slanted etch and how that might affect the current distribution and power distribution of the system.

Since in most of these problems the devil is in the details and they might be very important in one case, and not important at all in others, we'll perform different parametric sweeps to highlight the ranges were the etch factor effect needs to be considered or not. The ultimate objective is to provide practical guidelines to the SI/PI practitioner engineer of when to worry or not about this effect.

I. 2. Etch Factor definition, back to basics

Etch factor is a consequence of imperfect manufacturing. The process by which traces are created on printed circuit boards is done by a manufacturing process called etching. It removes the excess amount of copper on a particular layer, leaving behind the required pattern of traces, pads, plane shapes, etc. The wet etching process does not result in a perfect rectangular trace cross section, the trace is somehow slanted forming a "sort" of trapezoidal shape. The angle of the sidewalls depends of the manufacturer and the process they use. *Figure I.2.1* shows cross section photos of slanted side walls.

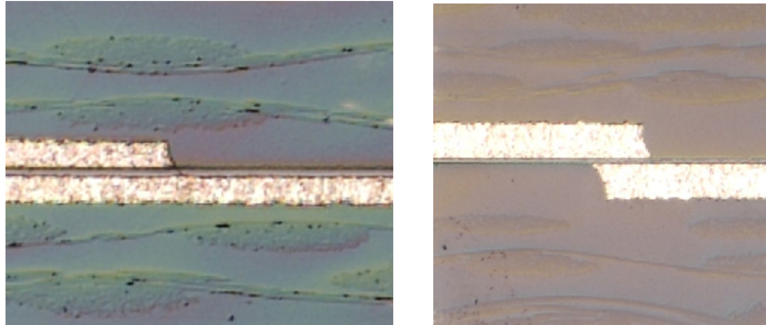


Figure I.2.1.: *Copper edge cross-section photos on inner layers. One-ounce copper (left), two-ounce copper (right). Test boards and cross sections courtesy of DuPont.*

As you can imagine, changing the shape of the trace with respect to its original rectangular form will have electrical implications. One of the most prevalent implication is the change of characteristic impedance (Zc) of the trace, but also as you might imagine, as we are removing copper and ultimately reducing the perimeter of the trace, we would expect increased losses at higher frequencies and at DC alike. Furthermore, for differential traces (and in odd mode), we know that due to proximity effects the current crowds close to the inner side walls of the differential pair. We could then infer to expect some change on the current distribution when moving from rectangular to an angled etch.

Even though it's expected and known, that the change in electrical parameters due to etch factor is not necessarily a first order electrical effect, it's degree must be understood and accounted for in order to properly estimate impedances and losses at higher frequencies.

Let's start off by establishing the etch-factor nomenclature that we will carry on throughout the paper, since there are several different ways one may see etch-factor defined in different literature. *Figure I.2.2* shows the formal etch-factor definition from [2] and the approximation we will use in the paper. As we see on the cross-section photos, the side walls are not really straight: they are slightly angled and more curved on thicker copper. With the usual wet etching process, the 'bottom' width, *w1*, which faces the core dielectric, is wider than the 'top' width, *w2*. Note that 'top' and 'bottom' in this context refer to the trace surface being away or next to the dielectric, respectively, regardless of the actual geometrical meaning. On a core laminate the trace cross section trapezoidity on the top is the mirror image of the trapezoidity on the bottom, as shown in

Figure I.2.3. As such, in an actual printed circuit board stackup we need to know the construction to determine the 'bottom' and 'top' sides of traces. The figure shows a portion of a typical construction with multiple internal stripline layers, but with other construction options, for instance assuming one or more sequential lamination boundaries on these layers, the 'top' and 'bottom' of a trace may flip on one or both signal layers.

It is customary to approximate the sidewalls with straight contour lines such that the $w1$ bottom width is the sum of the V trace thickness and $w2$ top width: $w1 = w2 + V$. This corresponds to the side-wall angle of $\alpha = 60$ degrees. A 90-degree angle corresponds to vertical sidewalls, the 'ideal' case. In this paper we will look at the effect of side-wall angle on the extreme range of 45 to 90 degrees.

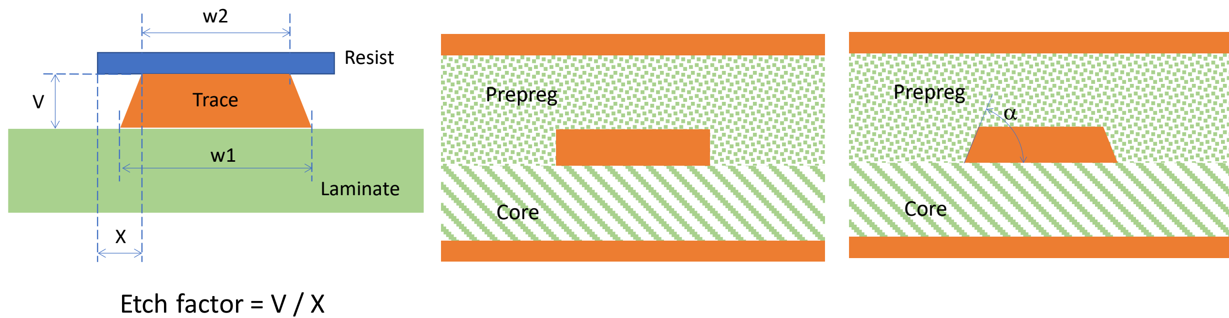


Figure I.2.2: *Definition of etch factor from IPC-2221-1 (left). Rectangular baseline case in stripline, (middle). Etch factor represented by an angle in this paper (right).*

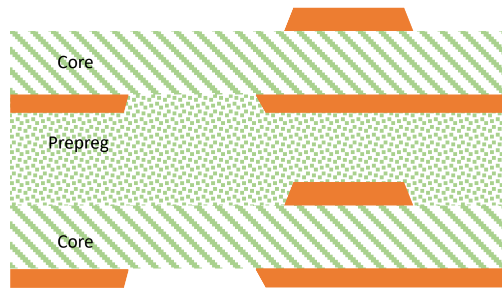


Figure I.2.3: *Partial stackup with etch factor allocation around core and prepreg. The stackup portion shown here is typical, but other permutations are also possible.*

Before we start the simulations, it is also important to point out that even though the etch factor today is a user-defined input option in all major layout tools and also in field solvers, this information does not yet (as of the time of writing) propagate automatically between different vendor's tools. In the downstream field solver software this information has to be manually entered again. It is also important to point out that not all field solvers can take the etch slanted sidewall into account, especially hybrid solvers on plane layers.

II. Baseline simulations

II.1. Geometry and characteristic impedance

Let's start with a very simple differential transmission line as a baseline and let's change the etch factor in two bounding steps (90° and 45°).

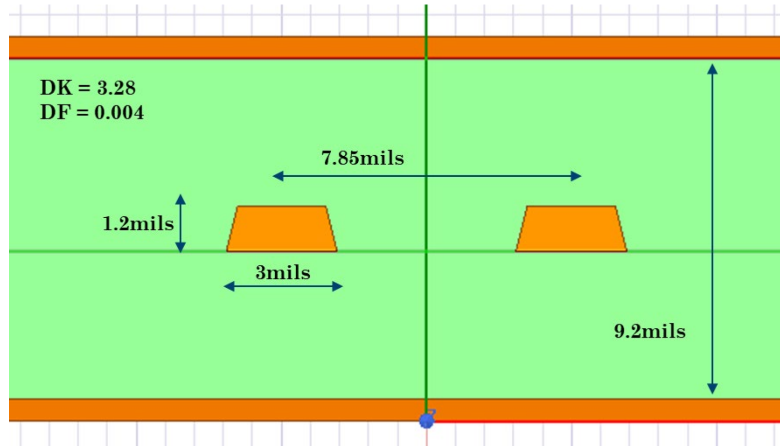


Figure II.1.1: *Baseline 2-D simulation case.*

Looking at the impedance in the time and frequency domain as shown in *Figure II.1.2*, we can see a 4 Ohms difference on the Differential Characteristic impedance. This is expected when we recall

$$Zc = \sqrt{\frac{R(f)+j2\pi f L(f)}{G(f)+j2\pi f C(f)}}$$ General case

$$Zc = \sqrt{\frac{L(f)}{C(f)}}$$ Lossless approximation

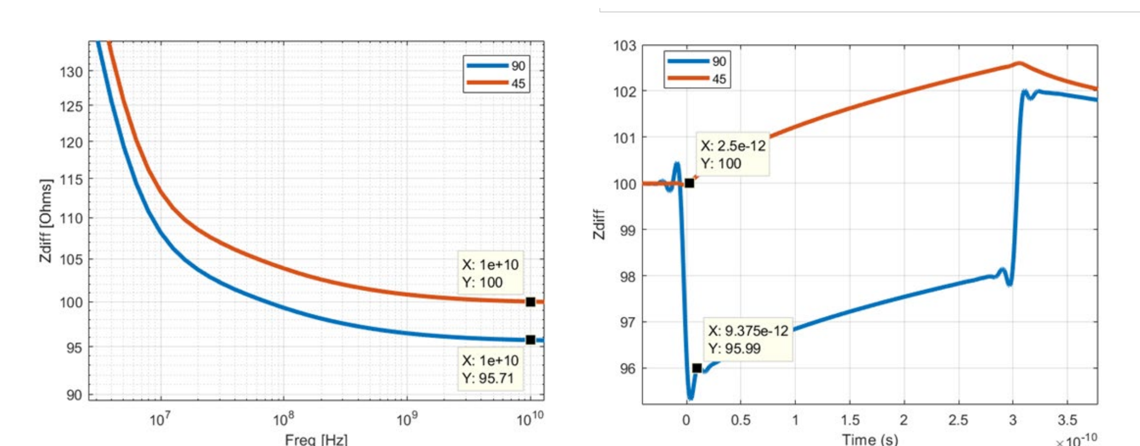


Figure II.1.2: *Impedance profile of 90 and 45 cases (left) frequency domain, (right) time domain.*

As the line width is decreased on the top due to the etch factor, we know that L(f) would be approximately the same since inductance is dependent on the loop area, and loop area is not changing much. On the other hand, C(f) is directly proportional to the conductor areas, hence the as the area decreases, the capacitance decreases and the characteristic impedance increases as seen in the figure.

II.2. RLGC parameters

The change of capacitance between these two cases can be clearly seen when we plot the LC parameters as shown in *Figure II.2.1*. The change in frequency of capacitance is due to the Djordjevic-Sarkar material model frequency extrapolation. The change in inductance over frequency is due to the internal inductance of the traces.

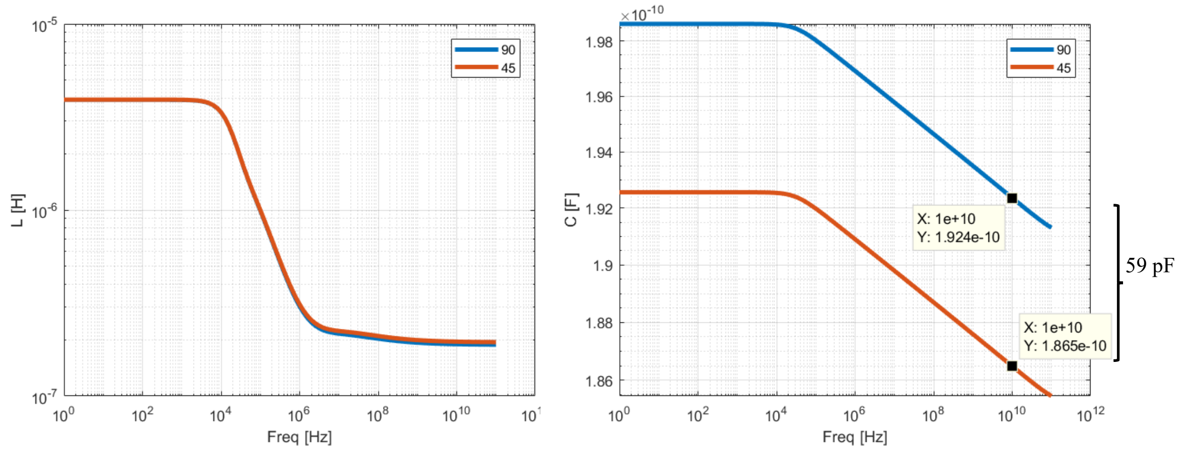


Figure II.2.1.: *Inductance and Capacitance variation; (left) inductance, (right) capacitance.*

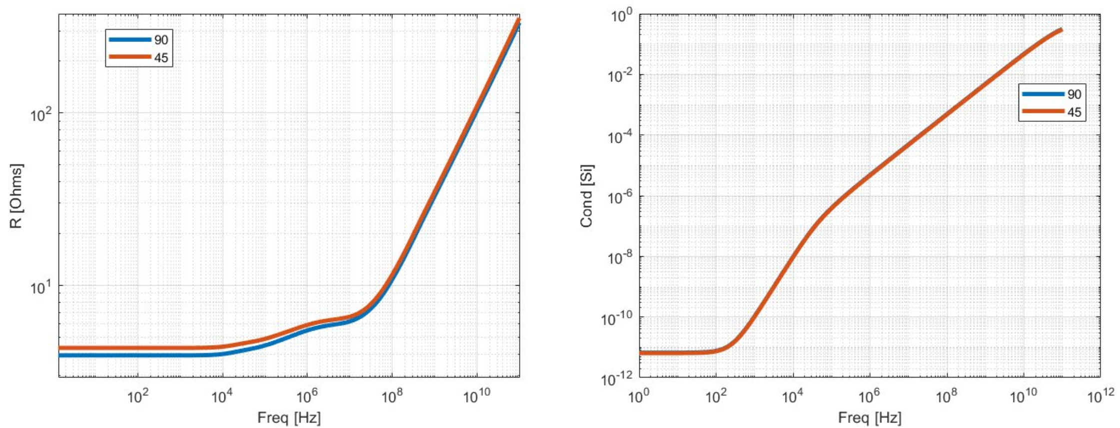


Figure II.2.2.: *RG parameters; (left) resistance over frequency, (right) conductance over frequency.*

At lower frequencies, fields penetrate the inside of the conductor cross section and hence

increasing the loop area and increasing inductance. At higher frequencies, all the current is on the surface of the trace, hence the only inductance is the constant "external" inductance.

As shown in *Figure II.2.2*, conductance does not change at all. This is to be expected as the conductance is directly determined by the dielectric material. On the other hand, we can see a little bit of a difference on the resistance. This is directly related to skin effect. At low frequency there is a bit more difference since the current is using the whole cross-section to travel finding less cross-sectional area with slanted side walls. At higher frequencies, due to skin effect, all the current goes to the perimeter of the trace, and even though the perimeters between the etched and rectangular case are different, the difference is small enough that very little change is observed.

Please remember all the plots above are for the differential propagation mode, in which case, we can't forget about proximity effect, since most of the current will tend to travel on the inner face of the traces (facing each other).

Zooming enough at high frequencies and using data from the lower plot of *Figure II.2.2*, we can see, as expected, a difference in the resistance. It is approximately 6 Ohms/meter, or 5.5%. However, with 45-degree side walls the perimeter of trace cross section becomes 17% lower, so relatively the resistance increase is much less than the loss of surface area.

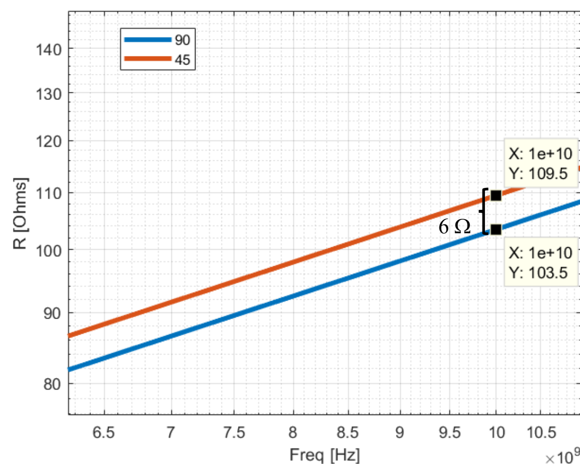


Figure II.2.3.: *High frequency skin loss and difference between etched and rectangular case.*

It's clear and expected that the effect of etch factor is relatively small as compared to other maladies that we experience in high frequency interconnects. Other than the impedance variations, at least on the simple baseline case, we can't really see a big impact.

III. Routing under a BGA; simplification with a 2D solver

Let's keep looking and slowly enhancing the simulated baseline assuming we'll be routing under a BGA section. When routing under BGA, due to mis-registration and tight antipad pitch, we could expect one of the traces might find itself being routed over the antipad void without a reference plane.

III.1. Geometry and fields

Even though, this case is a truly 3D case, we'll start simply by representing it on a 2D field solver. With the understanding that this is a worse-case bound and not a real case, we believe these quick simulations can provide useful insights.

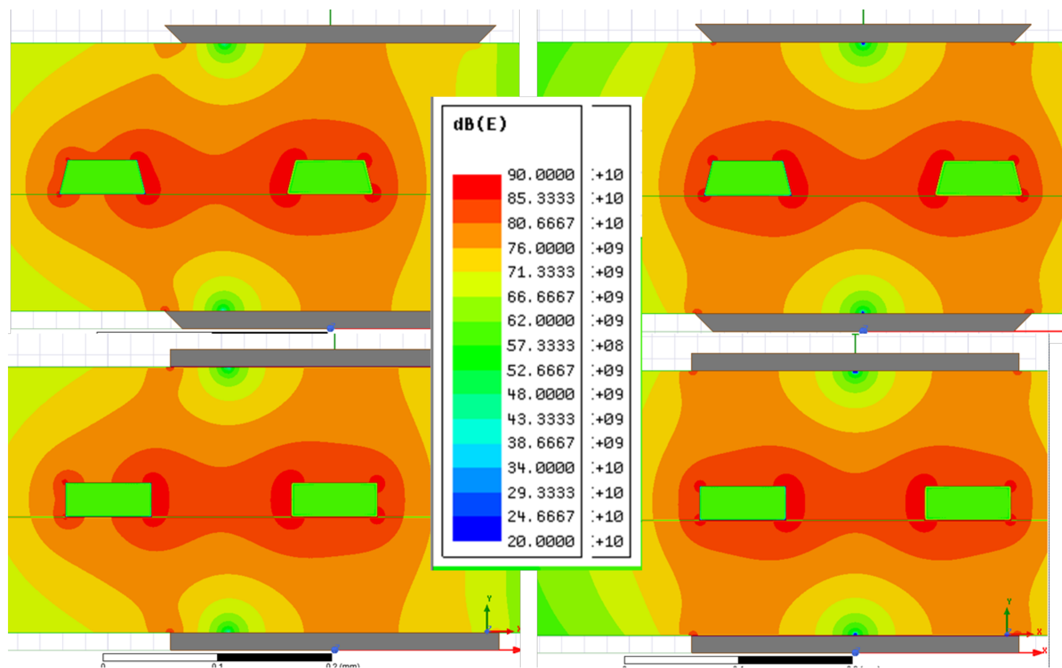


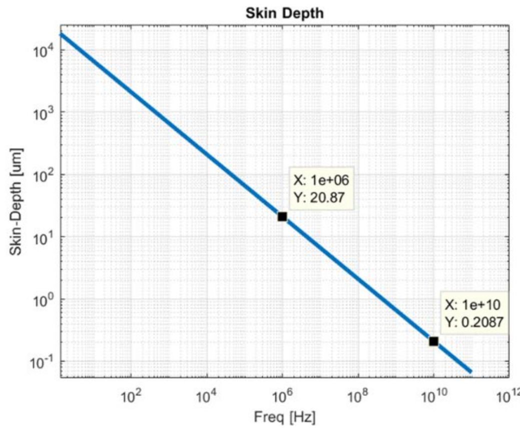
Figure III.1.1.: *Electric fields (top-left) 45 degrees, offset trace, (top-right) 45 degrees center, (bottom-left) 90 degrees offset, (bottom-right) 90 degrees centered.*

Four cases have been simulated, both rectangular and with 45°. On each of those cases we've moved the differential pair towards the anti-pad by approximately 4 mils.

Please take a close look at the field distributions in *Figure III.1.1*, it's obvious for a differential mode how the fields are deformed (not perfectly symmetrical), when one of the traces is facing the antipad. This is to be expected of a non-symmetrical structure.
In terms of the rectangular vs the trapezoidal case, there is no much difference that can be appreciated by the E plots.

Not much can be seen either if we plot the current density, since as you can imagine, at 10GHz the skin depth is such that all the current is running on the periphery of the trace.

In the picture below, at 10GHz, the current is bounded to 0.2um from the edge of the trace, within the surface roughness range. For currents to start having some penetration into the copper, the frequency has to be dramatically lower. At 1MHz there is only 20um penetration, or approximately 66% of a 1oz trace.



$$\partial = \sqrt{\frac{2\rho}{(2\pi f)(\mu_0 \mu_r)}}$$

$\rho = conductor\ resistivity$
$f = frequency$
$\mu_r = relative\ permeability$
$\mu_0 = free\ space\ permeability$

Figure III.1.2.: *Skin depth from 1 Hz to 100 GHz (left), skin depth formula on the right.*

III.2. RLGC parameters

In the plots below, we can see how the differential RLGC parameters change as we move the traces towards the antipad, both for the 90 and 45 cases. What we can still not see is any appreciable difference between the different etch cases.

As expected, as we move the traces closer to the antipads, we see, inductance increasing, capacitance decreasing, (hence impedance increasing), resistance increasing but conductance decreasing. The conductance decreasing is simply an artifact of the simulation deck. In this deck, we have air in the outside of the structure. As the traces move over the antipad, more of the fields close through air, so the effective average loss will decrease a little since for air we don't have any dielectric losses.

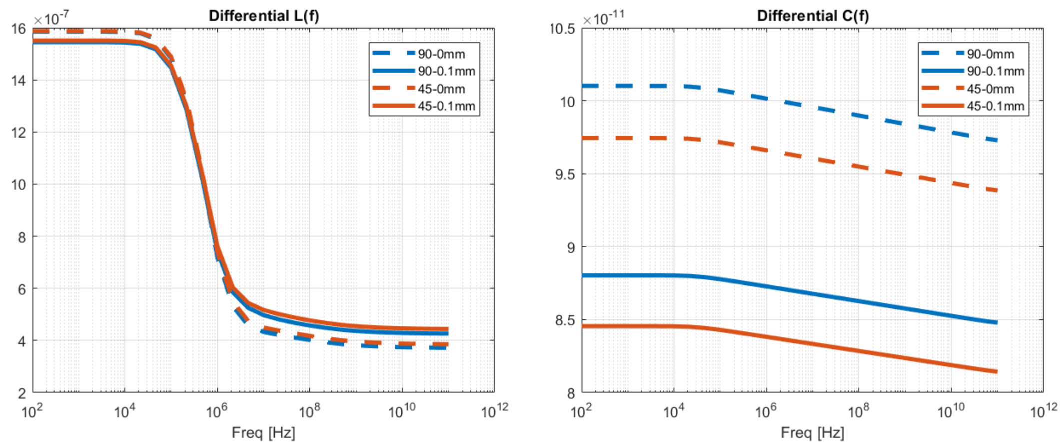


Figure III.2.1.: *LC comparison for 90° and 45°, centered and offset. (left) inductances, (right) capacitance.*

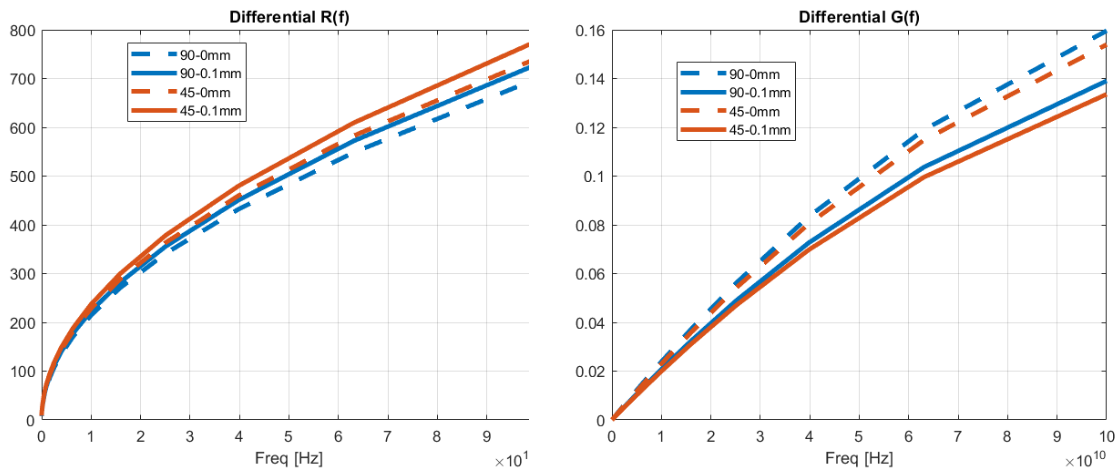


Figure III.2.2.: *RL comparison for 90° and 45°, centered and offset. (left) resistance, (right) conductance*

Even though the figure above tells the history, and shows us not much difference, we'll post-process it a bit more and we will plot the difference for each etch case as the trace is moved towards the antipad.

In the next couple of figures, we are looking to see which case (rectangular or etched), shows a bigger difference as we move the traces towards the antipad. For L(f) we see no appreciable difference between the two etch cases. C(f) has a similar trend, they are both changing at the same rate with different absolute values, with a bigger value for the rectangular case. Conductance is pretty much the same, but the interesting plot comes on the resistance, since in this case we can see that the 45° angle changes at a more rapid rate as it moves towards the antipad. We are observing an additional 15% loss increase for the 45° case as compared to the 90° case.

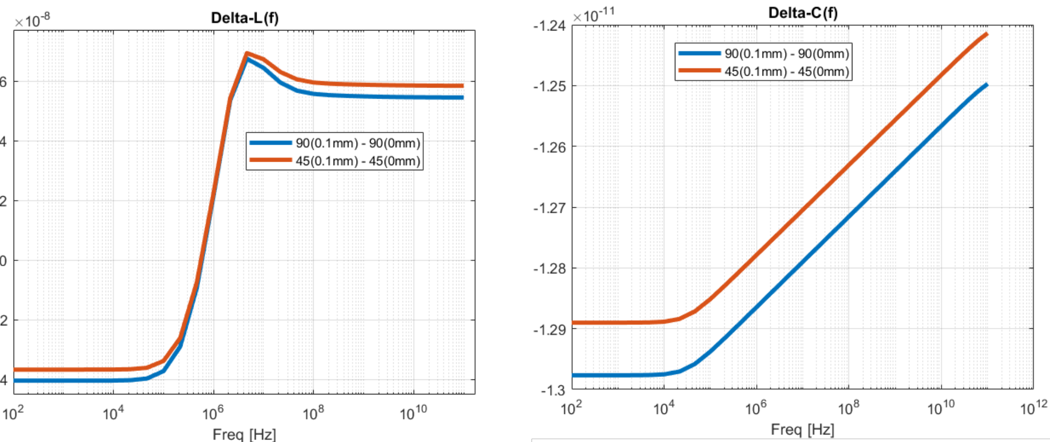


Figure III.2.3.: *LC difference, (left) inductance difference offset-centered, (right) capacitance difference offset-centered.*

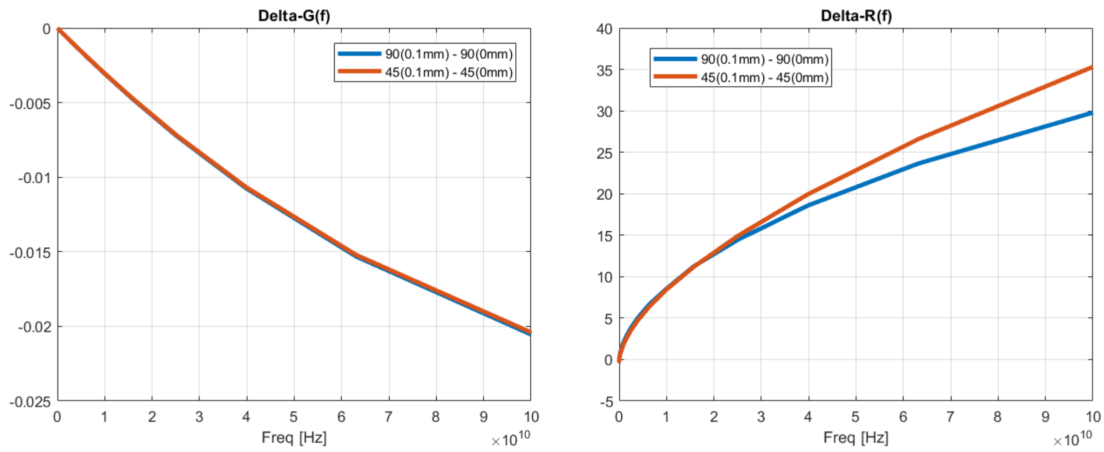


Figure III.2.4.: *GR difference, (left) conductance difference offset-centered, (right) resistance difference offset-centered.*

In this section we've shown, in a very simplistic and pessimistic case, that an etch factor of 45° on a 1oz trace running over antipad will increase the relative loss with respect to a rectangular case by about 15% at 10GHz.

In general, we can say that, other than impedance there is not much difference in any parameter, even under perforations, since ultimately the absolute loss, for short traces running under the BGA are small as is shown in *Figure III.2.5*.
Imagine you have to do a simulation of a 1" trace under a BGA and you decide not to include the etch factor and just create a model with a rectangular trace. The figure below shows the extra loss you'll see if you had simulated with a proper etch factor. As observed, the difference is very small.

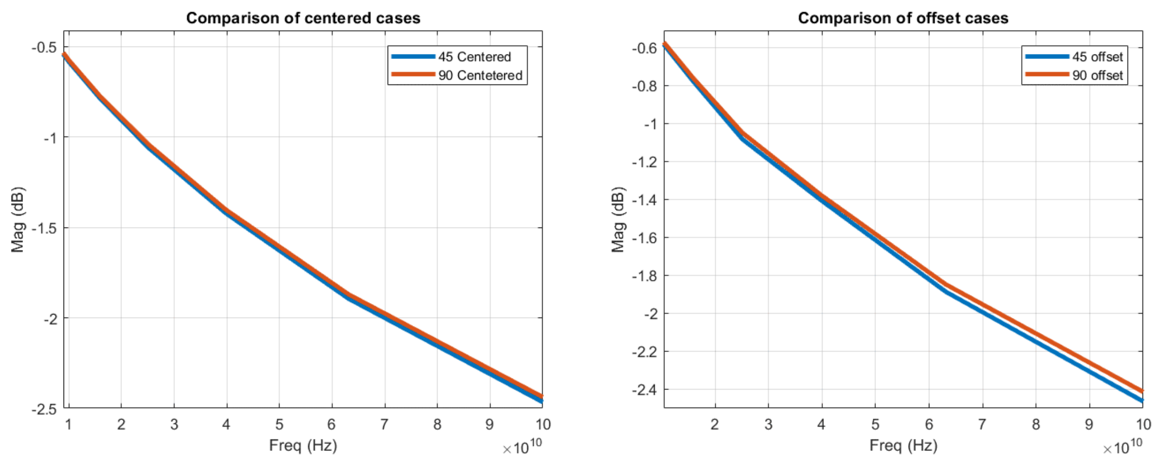


Figure III.2.5.: *Comparison of losses for 1" trace, (left) centered case, (right) offset case.*

Please note, the analysis above are on simplified cases, since we know, the structures under a BGA are not uniform on the propagation direction (circular holes).

Let's push a little harder and see if we can find something changing at higher frequencies when we simulate this problem in a full fledge 3D field solver such as HFSS.

IV. Etch factor over perforation (real case)

In the previous section we've looked at the fundamental effect of the etch factor. And on the simplified 2D simulation we've clearly seen the effects on impedance and to a much lesser degree on losses.
In this section, with the help of a 3D field solver, we'll be looking to the effects of real perforations, not only with respect to losses and impedance but also crosstalk. To do this, we'll create a unit cell approach.

IV. 1. Three-dimensional (3D) geometry
Figure IV.1.1 shows the 3D problem setup. It consists of either x2 or x4 perforations with two strip lines. The objective is, in a more realistic setting, determine the difference between rectangular vs etch cases for:

- Impedance changes
- Losses increases
- Crosstalk increases

The approach complication is that to highlight the effects and make longer structures, we have to concatenate many cells. In the concatenation process if we are not very careful as to how we treat ports, we could be creating an artificial discontinuity that when concatenated becomes periodical.

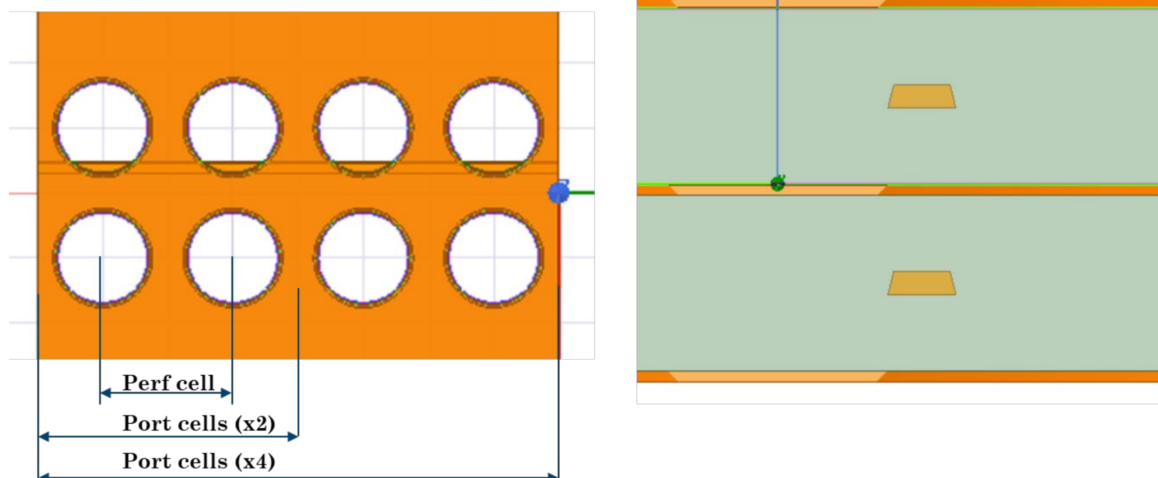


***Figure IV.1.1**: 3D problem setup, (left) x4 unit cells top view, (right) cross-section showing crosstalk.*

IV.2. Impedance over perforated planes

As we did before we'll start with a uniform plane, (no perforations), and then including perforations we'll start by centering the trace in the middle and sweep the trace position by offsetting towards the antipad. All the simulations will be done using a x2 unit cell (2mm), meaning two perforations in the direction of propagation.

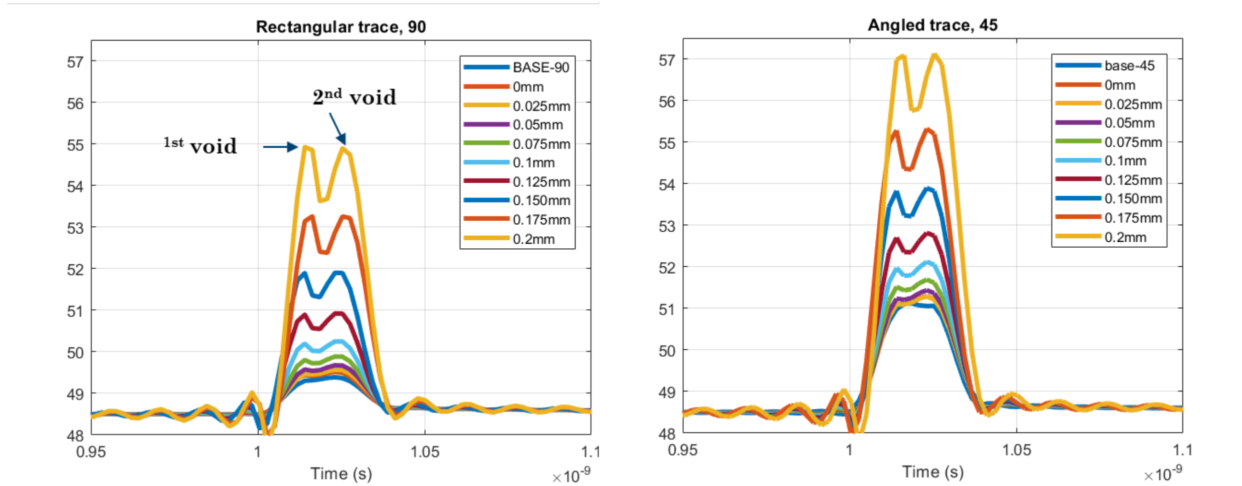


Figure IV.2.1.: *Impedance variation, (left) rectangular case, (right) 45° case.*

The TDR of *Figure IV.2.1* using a 10ps edge rate, shows a clear 2 Ohms difference in impedance between the two etch cases. Another feature that is obvious is the extra impedance seen as the traces passes through the holes.

If I pick the tip of the first hole and compare the impedance between these two cases, we can see the variation of impedance between these cases for a x2 cell is very similar

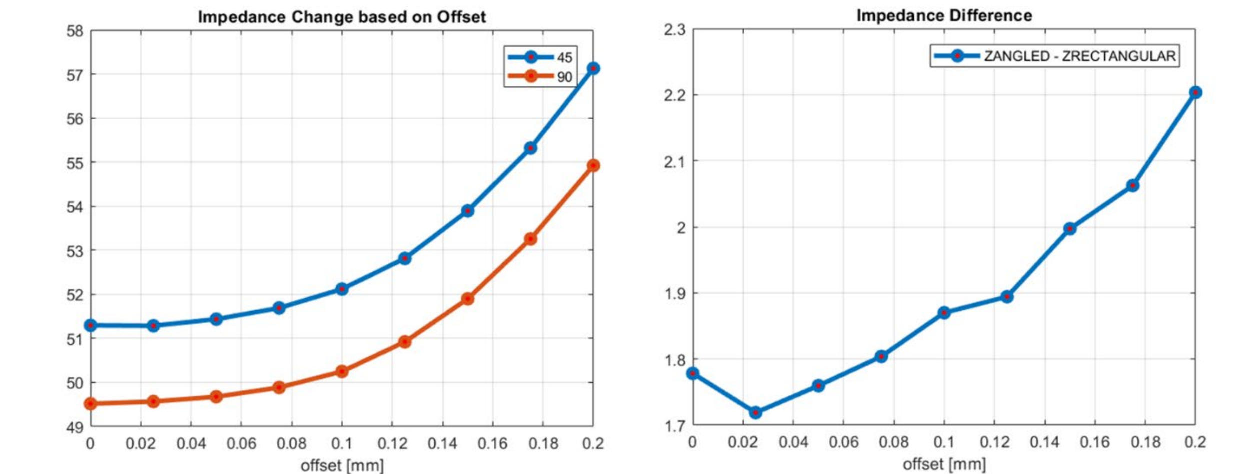


Figure IV.2.2.: *Impedance change based on offset, (left) 90° vs 45°, (right) 45° - 90°.*

But if we subtract the rectangular case from the 45° angle variation, we can see that the etched case is growing at a slightly higher rate, showing an approximate 0.4 Ohms increase as compared to the rectangular case as can be seen in *Figure IV.2.2*.

Still with that, it’s difficult to see a meaningful difference between the cases for a x2 unit cell. Let’s now look at crosstalk

IV. 3. Vertical crosstalk

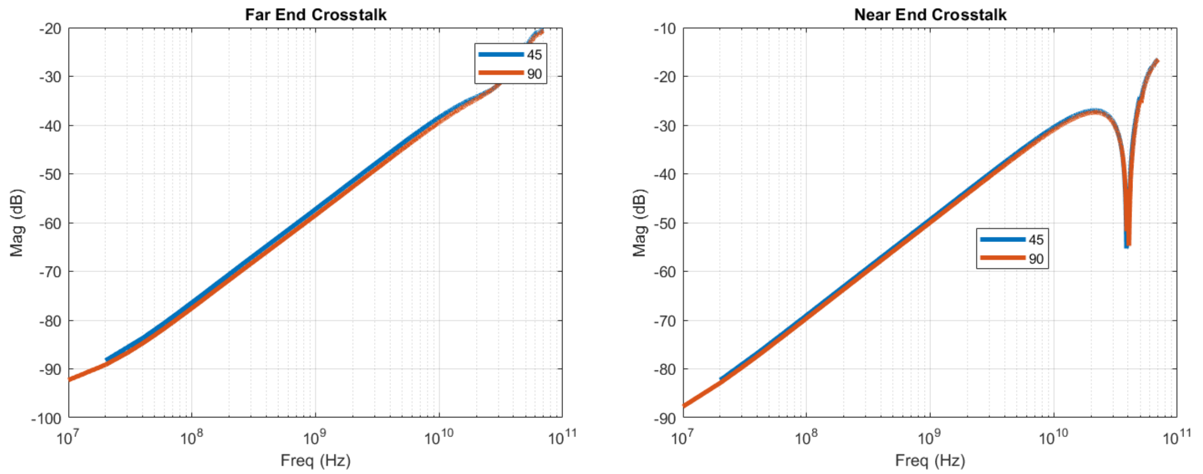


Figure IV.3.1.: *Vertical crosstalk with maximum offset, (left) far end, (right) near end.*

Not much difference seen in crosstalk either. If we compute the crosstalk change as we offset the trace and compare between cases we see a similar trend and absolute value as seen in *Figure IV.3.2*. Although we could see a little difference in absolute value, this can be attributed to S-parameter renormalization impedance.

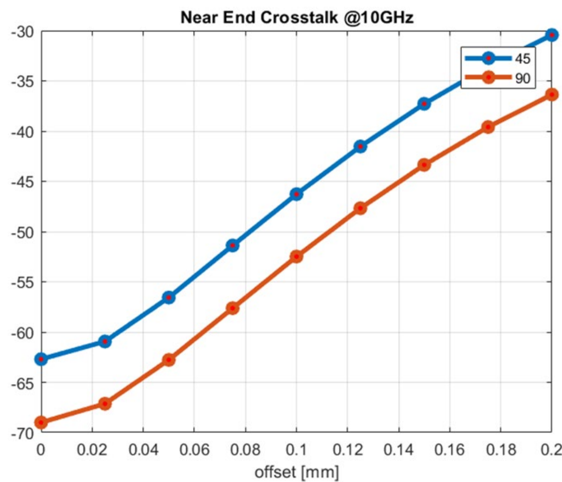


Figure IV.3.2.: *Crosstalk vs. horizontal offset.*

So far, we have not seen for a x2 unit cell of 2mm any appreciable difference, other than impedance variation, between these two cases. The question remains, what would happen if we concatenate many of these cells together?

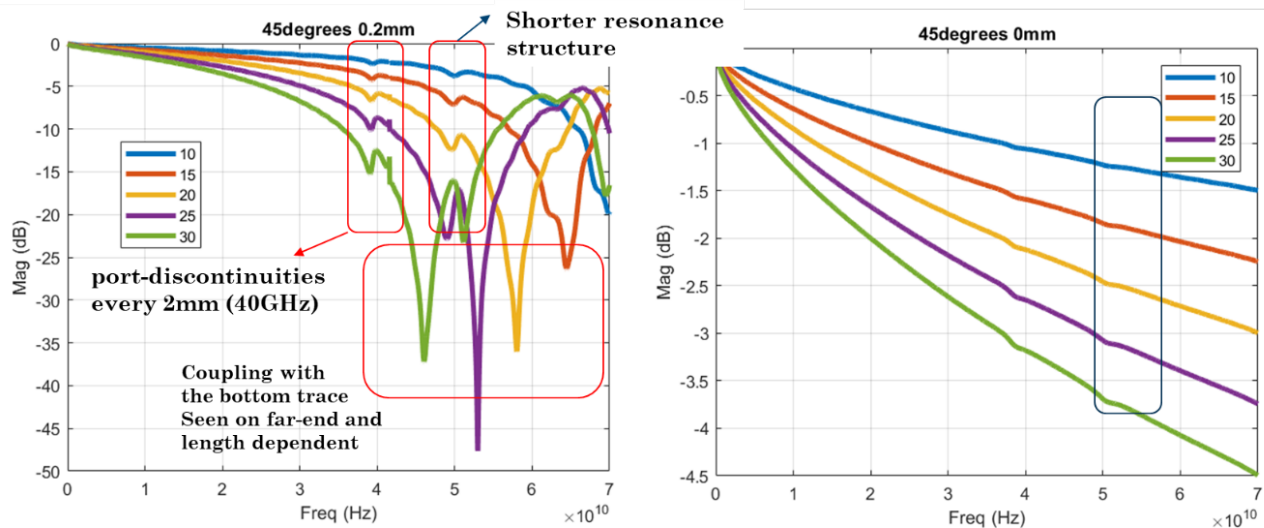


Figure IV.3.3.: *Many x2 cells concatenations for the 45° case, (left) maximum 0.2mm offset, (right) centered.*

Figure IV.3.3 has been created by concatenating from 10 to 30 (x2) 2mm cells in intervals of 5. This means the longer trace will be 30*2mm = 60mm or approximately 2.4" and the shortest would be 10*2mm=20mm or approximately 0.8".

Let's start analyzing these curves by looking at the centered case (right side of the figure). As expected we see as length increases the losses increases with it. In addition to that we do see a little dip (very small) at around 40GHz, and another at a little higher frequency. These reflections come from the ½ wave resonance formed between the non-perfect wave ports used in simulations and have nothing to do with the real structure. No matter how much care we put into the ports, we always have a little bit of reflection that when concatenating, due to periodical discontinuities, gets amplified at the resonance frequency [5].

When we move to the full offset of 0.2mm on the left we see the same resonance but better defined. This can be explained by the fact in this structure there are more reflections since the trace is going over the holes and the mean impedance of the trace is higher making the ½ wave resonance more apparent.

One other important aspect on these curves are the big dips observed. As we increase the length, the dips move to a lower frequency, so clearly frequency dependent. We can track this to coupling to the trace below. As these two traces gets longer and longer and they couple more and more, there are frequencies where most of the energy is sucked from the

trace and sent to the victim [6].

Now, all this is very interesting, but it's not really saying anything about the differences between different etch cases. To do that, we will compare the 90° and 45° in the next figure.

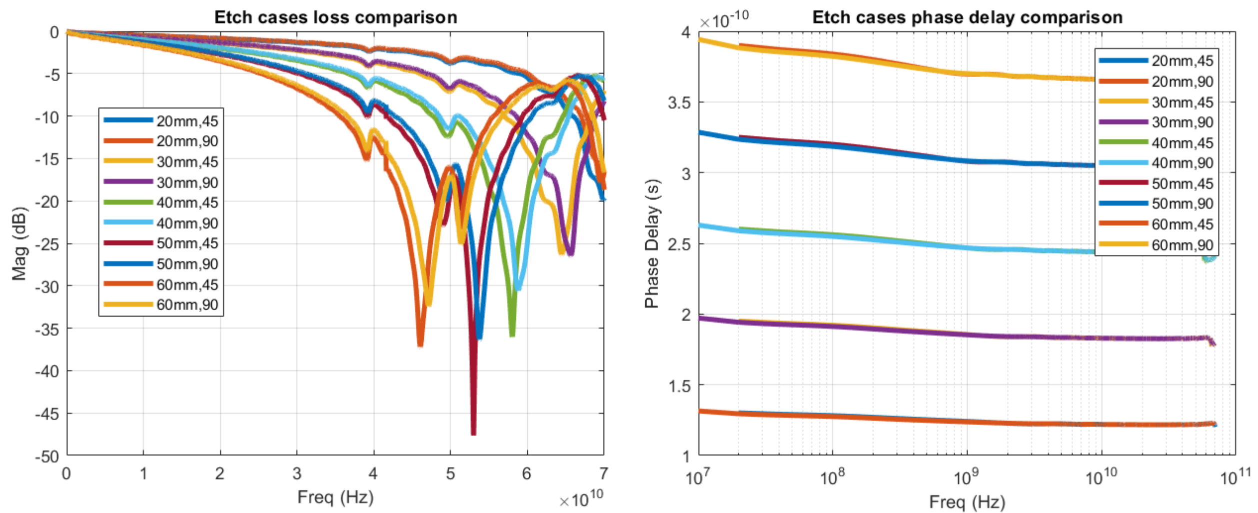


Figure IV.3.4.: *Etch cases comparison for longer concatenated cells, (left) insertion loss, (right) phase delay.*

In *Figure IV.3.4* we can see some difference in losses, but really very small as compared to the all the other more prevalent effect. Phase delay is virtually identical between cases.

We can see that no matter how hard we look, at the end of the day, whether it's simplified model, complex models, unit cells, concatenated cells, the only parameter we see changing between these cases in a meaningful way is the impedance; loss does change as a very distant second effect, but really nothing much.

It's safe to conclude that etch effect at higher frequencies does not really affect dramatically any aspect of transmission other than impedance matching.

We've looked at very high frequencies so far, but what about DC? In the next session we look at the impact of etch factor on DC resistance and current density.

V. DC effect of etch factor in plane perforations

We usually tend to think that resistance at DC is easy to calculate, we just need to apply Ohm's law and divide voltage with current. However, when we look at it under the microscope, maybe literally, applying Ohm's law in its simple form comes with prerequisites: when dimensions are finite along all three geometry axes, Ohm's law applies only if the current density through the entire entry and exit surfaces is constant.

V.1. Geometry and definition of DC resistance

Figure V.1.1 shows a typical scenario, when we need to calculate the DC resistance of a trace.

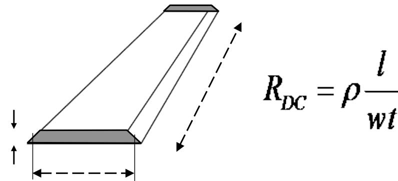


Figure V.1.1.: *DC resistance calculation of a PCB trace. Strictly speaking the formula applies only as long as the current density through the grey shaded areas is constant.*

In many practical situations, namely when the length of the trace is much bigger than the width or thickness of the trace, if we ignore or forget about the requirement of uniform current density on the entry and exit surfaces, the resulting error in DC resistance is still negligible. In case of plane shapes, on the other hand, where by definition the length-to-width ratio is not extreme big, the uniform current density requirement becomes important, or else we can not uniquely apply Ohm's law.

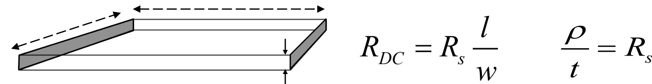


Figure V.1.2.: *DC resistance calculation of a rectangular PCB plane shape. The formula applies only as long as the current density through the grey shaded areas is constant.*

When the current density is not uniform, or when we want to calculate the resistance of a different shape, we can integrate the varying current density over the entry and exit surfaces to get the current, but the potential on those surfaces will not be constant and therefore we do not have a unique voltage to use for Ohm's law. Under such circumstances a unique definition of resistance can be obtained based on dissipation in the DUT [3]: the resistance can be obtained as the volume integral of the square of the current density, divided by the conductivity of the material.

$$R_{nn} = \int_V \frac{1}{\sigma}\left(J_n\left(x'\right) J_n\left(x'\right)\right) dV$$

With this definition we can uniquely calculate resistance, but it will be dependent on the connection and surrounding geometry.

V.2. Resistance of perforated planes

For power considerations there are two major potential concerns: if current density is too high, the local temperature may exceed safe limits and if the equivalent resistance between selected points or surfaces becomes too high the corresponding voltage drop and power loss (even if thermally it may not create a problem) could exceed our design targets.

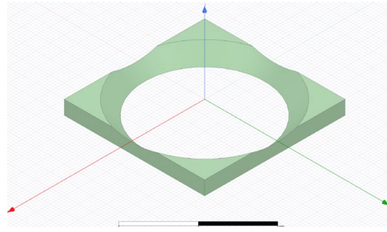
These calculations become more important for high-power systems when copper usage is optimized. We try to use the minimum number of layers and reuse power and ground layers by assigning multiple odd-shaped power patches to various supply rails on the same plane layer. Under these conditions the resulting geometry seldom lends itself to simple approximations of current density and voltage-drop calculations. In recent years a number of commercial tools have become available (for the major hybrid solvers see [4]) to calculate the DC current density, voltage drop and power dissipation in large and complex geometries, in full multi-layer boards. One missing element in these simulations though is the etch factor: today's hybrid solvers don't take this information into account, even if the layout tool from which we import the board geometry has this information. We can speculatively conclude that the most critical situation in this regard is when we have a lot of antipads perforating a plane shape used for a high-current supply rail. If we have to go through these plane layers with high-speed vias, the SI requirements may call for larger antipads, which together with a fixed BGA or LGA pitch will result in more swiss-cheese effect. Moreover, as illustrated in *Figure V.2.1*, if we use heavier copper layers, the fixed antipad pitch and fixed sidewall angles will result in less and less copper left on the 'top'. This not only increases the effective resistance, but further distorts the current-density distribution, increasing the chances of creating hot spots.

Figure V.2.1.: *Cross-section side view of perforated plane with fixed antipad pitch and lower copper weight on the left and higher copper weight on the right.*

To simulate such scenarios, we need to use a 3D solver that unfortunately will not take full-board geometries and therefore we need to simplify the simulation task. We will start with a unit cell on a plane with a uniform sea of antipads. After we establish the baseline, we do parametric sweeps along a few key parameters.

V.3. Unit cell and results

Figure V.3.1 shows the 3D view of a unit cell with a large antipad. The *a* side dimension of the scaled unit cell is 1 cm. The circular co-centric antipad (bottom opening) had a diameter stepped from 0.05 to 0.95 cm in 0.05 cm steps, with an extra case of zero diameter (no antipad, full plane). The side-wall angle was stepped in 15-degree increments from 45 degrees to 90 degrees. The metal thickness was stepped from 0.05 cm to 0.25 cm in 0.05 cm increments. The conductivity was set to the textbook 5.8E7 S/m value. Ports were assigned across the opposite side walls and the mesh was set to properly capture the fine details of the geometry.



Name	Value	Unit	Evaluated Value
a	1	cm	1cm
metalThickness	0.1	cm	0.1cm
d1	0.85	cm	0.85cm
numFacets	0		0
etchFactorAngle	45	deg	45deg
etchFactorExt	metalThickness/tan(etchFactorAngle)		0.1cm
d2	d1+2*etchFactorExt		1.05cm

Figure V.3.1.: *3D view of a unit cell with a large antipad with 45-degree sidewalls (left) and major parameters in the simulations (right).*

The unit cell was simulated with equipotential port surfaces in 380 permutations of etch factor (side-wall angle), antipad diameter, and sheet thickness. The results of relative resistance increase compared to the sheet resistance with the sheet thickness used for the given permutation step. Data is shown for four different sheet thicknesses in *Figure V.3.2*.

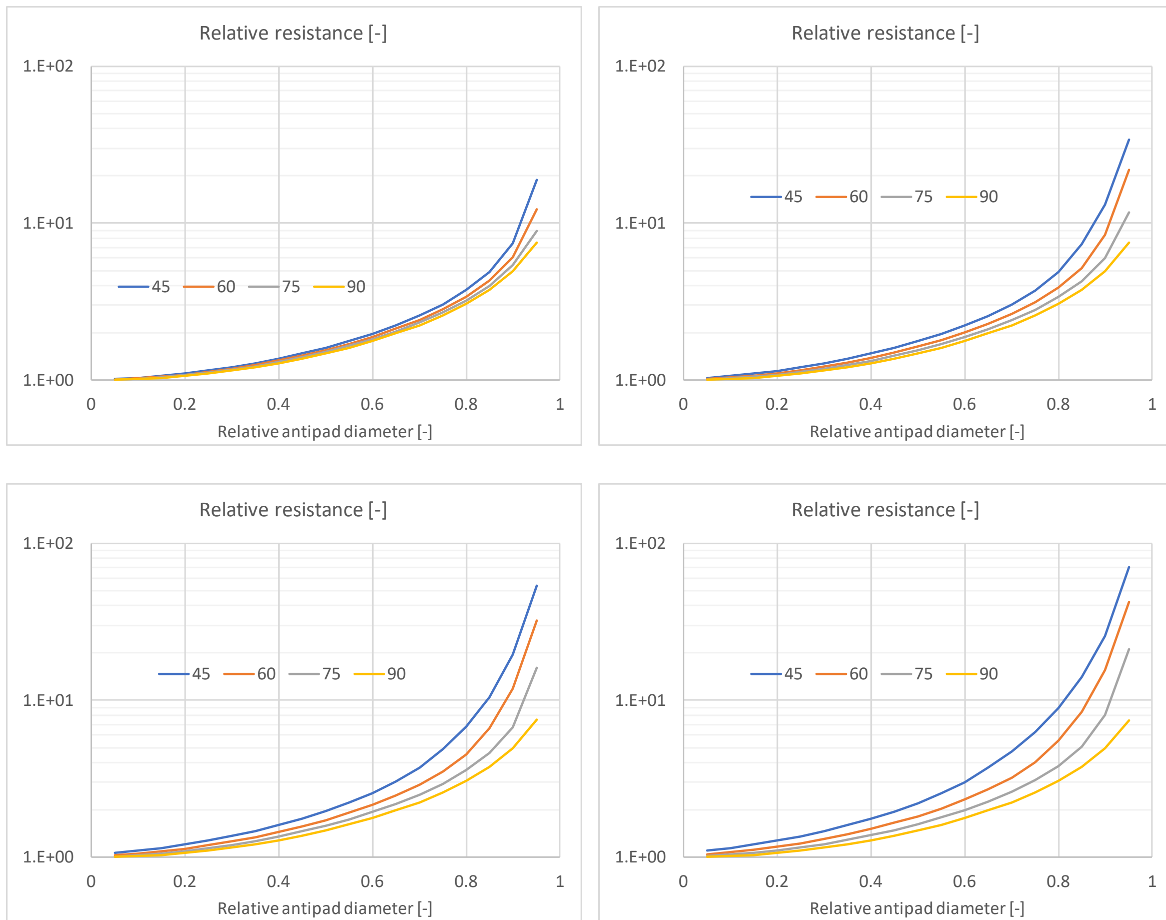


Figure V.3.2.: *Relative increase of resistance of a unit cell with respect to the sheet resistance of the same sheet with no antipad. The sheet edge size was 1 cm, the sheet thickness for the upper left and right and lower left and right plots were 0.05, 0.1, 0.15 and 0.2 cm, respectively.*

The upper left and right plots refer to 0.05 and 0.1 cm sheet thickness, respectively, while the bottom left and right plots show the relative resistance increase for 0.15 and 0.2 cm sheet thickness, respectively. Note also that these simulations purposely stressed the limits by going up to an 0.95 relative antipad diameter, which results in loss of copper around the narrowest areas of the rim, as illustrated in *Figure V.3.1*. This is the reason for the inflection and break points of the lines in the plots with a relative antipad diameter of 0.9 and 0.95. Similarly, we stressed the etch factor by going all the way to 45 degree antipad sidewall, whereas in typical processing the angle is closer to 60 degrees. We also know that thicker copper may have a tendency of producing higher average side-wall angles.

If we zoom on the typical data range with linear vertical scale and exclude the extreme corners, the same data set plotted in *Figure V.3.3* gives a better visual feel about the impact of etch factor.

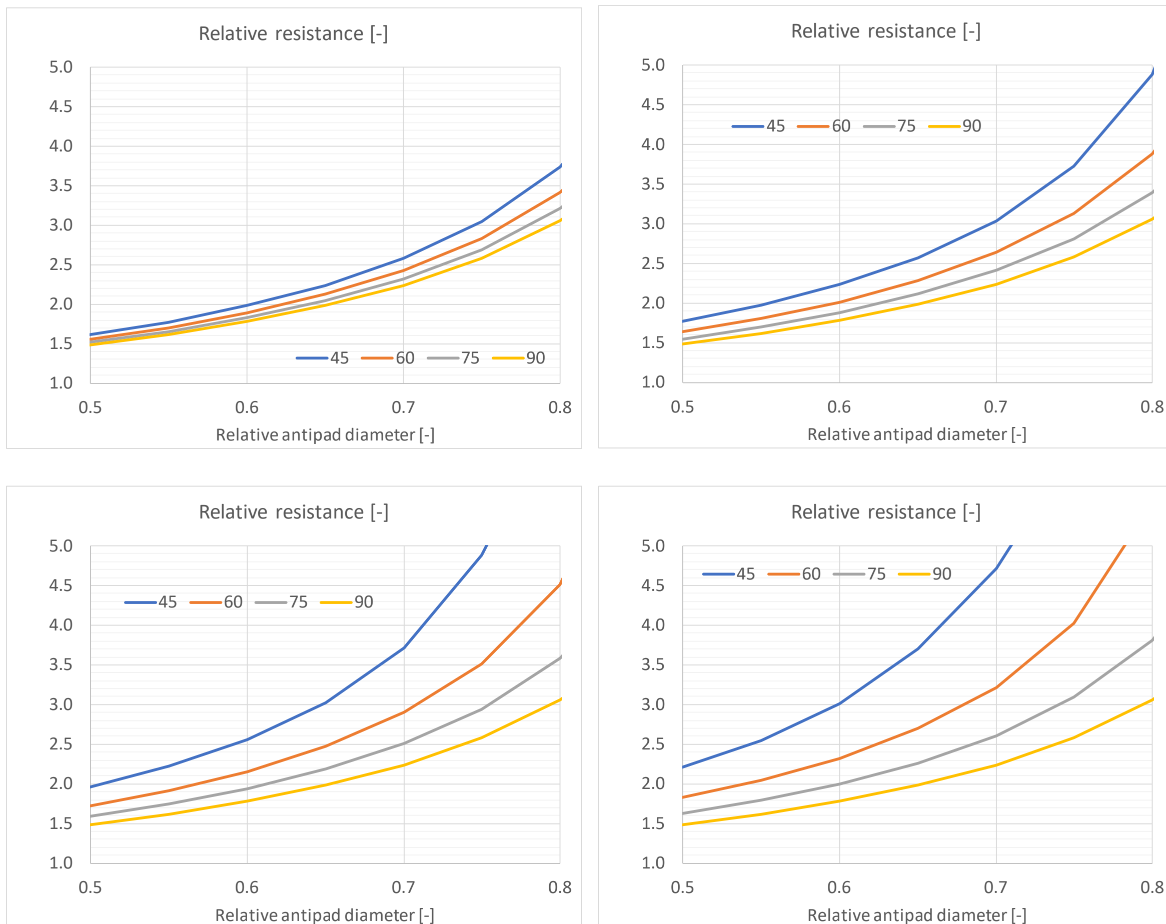


Figure V.3.3.: *Relative increase of resistance of a unit cell with respect to the sheet resistance of the same sheet with no antipad. Same data as in Figure V.3.2, zoomed. The sheet edge size was 1 cm, the sheet thickness for the upper left and right and lower left and right plots were 0.05, 0.1, 0.15 and 0.2 cm, respectively.*

With all the above notes, the trend is clear from the plots: as the antipad gets bigger with respect to the unit-cell size, and as the copper gets thicker, there is a bigger increase of relative resistance as we go from vertical side walls to slanted slide walls. With heavy copper and big antipads, the resistance increase can be bigger than 2x with respect to the same antipad perforation but with vertical side walls.

These plots are generic and the results can be scaled and applied to our particular geometry. For instance, if we scale the results to a 40-mil (1 mm) antipad pitch with 28 mil antipad size, the resistance increase from 90-degree to 60-degree sidewall angle will be 8%, 18%, 29% and 44% for 50, 100, 150 and 200 um copper thicknesses, respectively.

In addition to the resistance increase, the current density will also change locally due to the slanted side walls. This is illustrated with two current-density plots in *Figure V.3.4*.

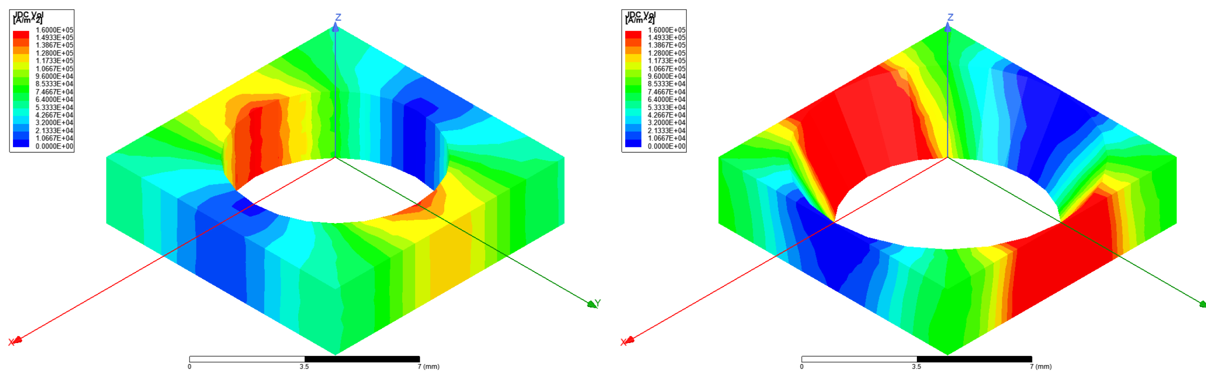


Figure V.3.4.: *Current density in a unit cell with 1A current, 70% antipad diameter and 90-degree and 60-degree side-wall angle on the left and right, respectively.*

As expected, the antipad itself already increases the current density. With the chosen geometry the current density with no cutout would be $4*10^4$ A/m^2. Instead, the maximum current density with this cutout becomes four times higher, or $1.6*10^5$ A/m^2. Moreover, as the density plots illustrate, with slanted side walls a larger volume of the conductor carries close to this maximum current density, raising the risk of local overheating.

V.4. Array of 9 x 9 antipads

The unit cell with a cutout analyzed in the previous section comes with non-uniform current density along the entry and exit surfaces and this implies that the surrounding of the unit cell may have an influence on its effective resistance. To test a more realistic scenario, the simulations with all permutations were repeated with an array of 9x9 unit cells, forming a square, see *Figure V.4.*1.

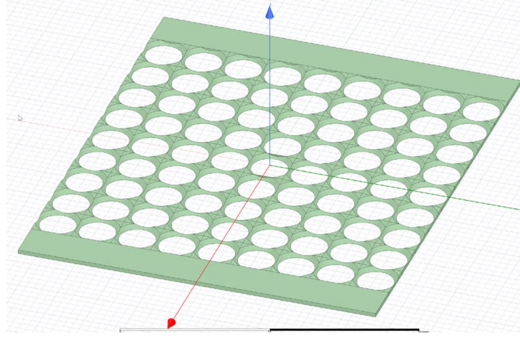


Figure V.4.1.: *Array of 9x9 unit cells with high-conductivity connecting strips.*

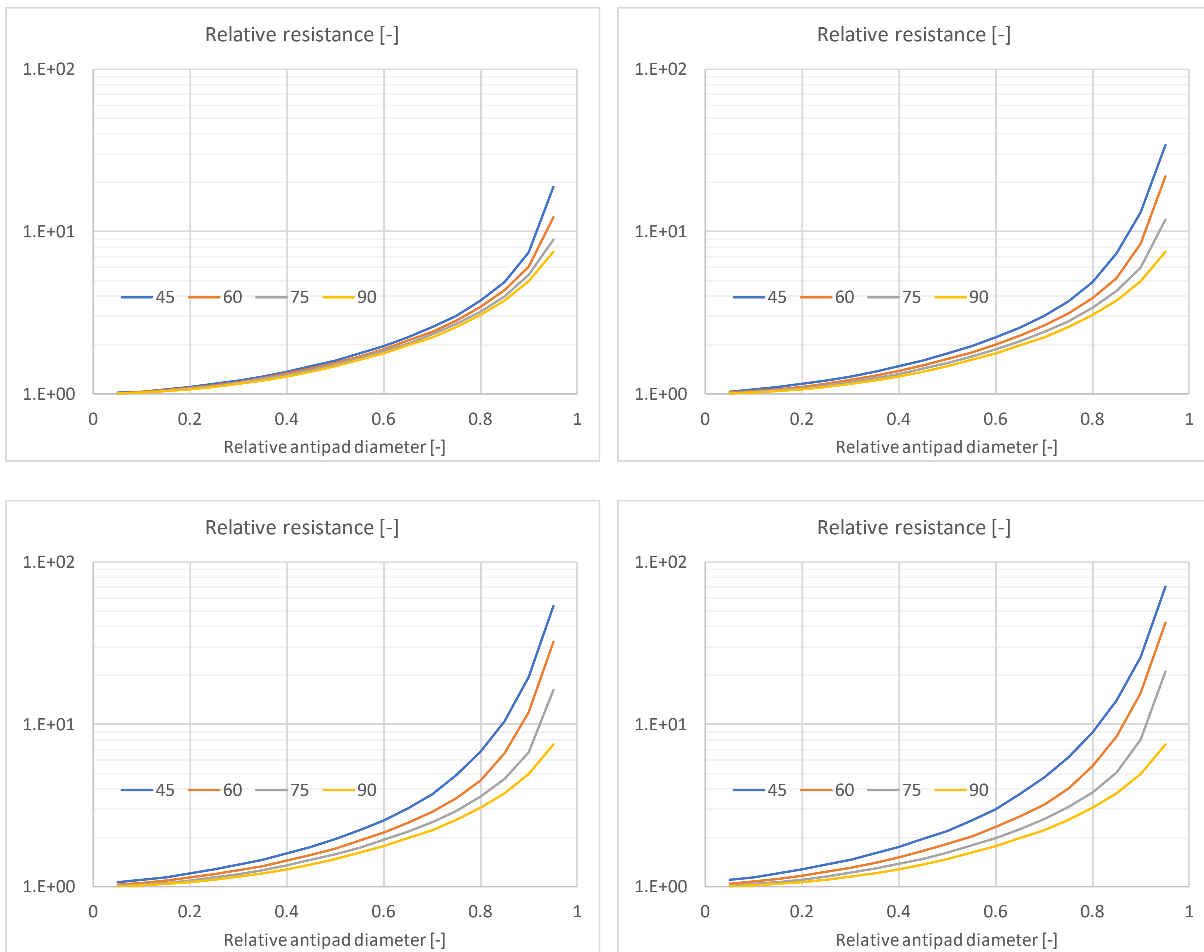


Figure V.4.2.: *Relative increase of resistance of a unit cell in an array of 9x9 cells with respect to the sheet resistance of the same sheet with no antipad. The sheet thickness for the upper left and right and lower left and right plots were 0.05, 0.1, 0.15 and 0.2 cm, respectively.*

The square was connected to high-conductivity strips with no cutouts. The high conductivity of non-perforated strips did not add to the simulated resistance, but ensured convergence of the tool in the extreme cases when the slanted side wall would cut into the bounding areas of the unit cells. The resistance of the cell in the middle was extracted and the values are plotted in *Figure V.4.2*. The sheet thickness for the upper left and right and lower left and right plots were 0.05, 0.1, 0.15 and 0.2 cm, respectively.

If we scale the results to a 40-mil (1 mm) antipad pitch with 28 mil antipad size, the resistance increase from 90-degree to 60-degree sidewall angle will be 8%, 18%, 29% and 44% for 50, 100, 150 and 200 um copper thicknesses, respectively, essentially the same we got for a single unit cell with equipotential entry and exit surfaces. This tells us that even though the unit cell simulation with equipotential ports does not ensure uniform current density through the entry and exit surfaces, it correctly represents the behavior in a real application, in the middle of a larger array.

Summary and conclusions

In this paper we looked at the SI and PI impacts of etch factor, the non-vertical sidewalls of etched copper on printed circuit boards. In real applications its impact shows up convoluted through a lot of other geometry and material-constant parameters. We have chosen a number of permutations of copper thickness, etch-factor angle and antipad pitch/size values that may represent some of the worst cases. In SI simulations the first-order impact is on the characteristic impedance, which has been documented earlier. Impact along previously not published parameter combinations have also been looked at and it was found that a distant second output parameter is loss: though counter-intuitively, in the skin-loss limited frequency region the relative per-unit-length series resistance increases less than how much the perimeter shrinks due to the slanted trace walls.

In SI simulations it was also found that routing a trace through an array of antipads with slanted side walls has little impact on trace characteristics beyond the previously documented effects of periodic discontinuities. Note that for practical reasons this study did not include correlations to measurements, since a number of parameters in the study are due to statistical manufacturing variations and would not be easy to control unless scaled models were used. For similar reasons all simulations ignored surface roughness of conductors and non-homogeneity and non-isotropic nature of materials.

As opposed to SI simulation results, the PI simulation runs showed noticeable difference due to etch factor values. It was found that with respect to antipad cutouts with vertical sidewalls, plane resistance will increase as the sidewall angle deviates from 90 degrees. It was found that with a 1-mm pitch and 28-mil antipad size the extra plane resistance through the perforated area increases by 8%, 18%, 29% and 44% for 50, 100, 150 and 200 um copper thicknesses, respectively.

References

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[2] Generic Standard on Printed Board Design, IPC-2221-1

[3] “Extracting Resistance from the DC Conduction Solution,” Q3D Extractor Help, Ansys.

[4] Ansys SiWave, Cadence PowerDC, Mentror Hyperlynx

[5] “Attenuation in PCB Traces Due to Periodical Discontinuities,” DesignCon 2006, Santa Clara Ca, February 6-9,2006

[6] “Losses Induced by Asymmetry in Differential Transmission Lines,” DesignCon 2007, Santa Clara Ca, January 29-31,2007