Case Studies Isolating Types of Power-Integrity Effects on Signal-Integrity, and Means of Mitigation

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Outline

- Background
- PDN effects on Buffer
- Return path PDN effects
- Test Case
“Power Aware Analysis”
“SI/PI Co-simulation”

PDN Impact on Buffers
SSO/SSN
External (VRM) Noise

PDN Impact On Signal Return
Impedance Discontinuity
Crosstalk
BUFFER EFFECTS
Buffer Effects > Background

- Traditional driver assumes ideal power supply
- Provide power equally well across all frequencies
• In reality, power is delivered to the driver through an imperfect Power Delivery Network (PDN)

• PDN might not be able to react fast enough to provide power to the driver equally well at all frequencies

• Signal quality can be affected
Buffer Effects > Modeling the PDN
Buffer Effects > Two methods of Analysis

**Frequency Domain**
- Ensure that impedance in Z-parameter is below requirement across all frequencies of interest.
- Easy to visualize and detect errors.
- Can be difficult to get frequency dependent impedance requirement.
- Does not correspond to Jedec’s timing requirements at DRAMs.

**Time Domain**
- Complete analysis including timing requirements at controller and DRAM.
- Noise visible on signals might not be easily separated from other sources of noise.
- Correctly generated Power-Aware IBIS models v5.0 (or equivalent) are required.
Simultaneously Switching Noise > Background

- Effect exacerbated when multiple signals demand power at the same time from the same PDN
- Simultaneously Switching Output (SSO) causes Simultaneously Switching Noise (SSN)
3 Cases
- No Capacitors anywhere
- Add only Pkg/Die Capacitances – helps higher frequencies
- Add all capacitors and DC source
SSN > Time Domain Setup

- Actual Board PDN
  - Without any Decoupling Capacitors
  - With only Pkg+Die Capacitors
  - With all Capacitors and DC source

- Signals directly terminated – no transmission line or other “irrelevant” effects
SSN > Time Domain Results – Vary Decoupling

- 8 bits toggling PRBS 15 at 2400MT/s
- Only Pkg+Die
  - Less than 1mV worse than best case
- No Decoupling
  - 88mV worse than best case
- Only Pkg/On-Die decoupling has real effect on SSN
SSN > Time Domain Results – Vary Number Bits

- All bits active vs. one bit active
- All bits active (rest held high) ➢ Decoupling impacts 88mV noise
- One bit active ➢ Decoupling impacts 2mV noise

**SSN is Bit-Pattern sensitive**

![Diagram showing SSN > Time Domain Results – Vary Number Bits](image-url)
- Same PDN as before
- VRM Assumed to have 1MHz 100mV p-p Sinusoidal noise
VRM Noise > Results

- 100mV p-p noise causes eye collapse by about 26mV (no decoupling)
- Good Decoupling opens up nearly all of it
Detection

- Frequency Domain gives quick feedback about potential issues
  - Impedance below target over all frequencies
  - Impedance flat (reduced resonances)

- Find difference in Time-Domain setup
  - With Power-Aware effects Enabled
  - With Power-Aware effects Disabled

- If difference is large, potential PDN related issue

- Can take long time to run with power-aware effects, especially at low frequencies
Mitigation

- Reduce inductance for Decoupling capacitors
  - Place close to load
  - Mount with low-inductance method
Why is DDR more susceptible to SSN?

Single Ended Signals

Asymmetric Signals

DDR Signals’ rising and falling edges not necessarily symmetric, and don’t always cross at midpoint.
RETURN PATH EFFECTS
Return Path Effects > Background

- Channel’s characteristics must take into account return path
- If return path is too far away, the inductive loop will adversely affect channel behavior
Return Path Effects > Signal Signal Setup

- Compare signal with nearby stitching via vs. distant stitching via
- Ground plane cutout to create some resonances as with many return planes
- Compare:
  - Signal via is ideal short
  - Nearby Stitching via
  - Distant Stitching via
Return Path Effects > Signal Signal FD Results

- Board edges are “visible” to channel if stitching via is far from signal via
- Nearby stitching via makes signal close to ideal
Return Path Effects > Signal Signal TD Results

- Nearby Stitching closes eye by about **20mV**
- Distant Stitching closes eye by about **450mV**

![Graph showing signal effects](image-url)
Return Path Effects > Crosstalk Setup

- One Stitching Via being shared by four signals
- 8 mil wide traces
- Outer two signals are separated by 50 mils
- Inner two signals are separated by 80 mils
Return Path Effects > Crosstalk FD Results

Purple = S25
Black = S23
Blue = S27

~20dB = 10% xtalk
Return Path Effects > Crosstalk TD Results

- Crosstalk closes eye by about **135mV**
Why is DDR More Susceptible?

- Single Ended Signals without dedicated return path structures
- Ground vias often not explicitly thought through during design
EFFECTS ON TEST CASE
Bringing it all together – Test case

- DDR4 2400 MT/s
- Lane 0 (DQ0) traverses layers 1 and 3
- Lane 7 (DQ56) traverses Layers 1 and 8
- x16 DRAM driving 2400MT/s DDR4 signal
Signal layout – DQ0 and DQ56

- DQ0 does not change reference layers
- DQ56 changes reference layers, but does not have nearby decoupling caps
### Return Path Effects - Single Signal

- **Baseline assumes signal via has ideal return path**
- **Single signal active – effect purely due to channel return path discontinuity**

<table>
<thead>
<tr>
<th></th>
<th>Eye Height with ideal return assumption</th>
<th>Eye Height with actual return path</th>
<th>Impact of imperfect return path</th>
</tr>
</thead>
<tbody>
<tr>
<td>DQ0</td>
<td>567mV</td>
<td>567mV</td>
<td>&lt; 1mV</td>
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<tr>
<td>DQ56</td>
<td>496mV</td>
<td>419mV</td>
<td>77mV</td>
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Effect of SSN

Baseline has 16 bits toggling and incorporates package xtalk

Both DQ0 and DQ56 have about 30mV SSN.
— Not dependent on layout

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<tbody>
<tr>
<td>DQ0</td>
<td>540mV</td>
<td>513mV</td>
<td>27mV</td>
</tr>
<tr>
<td>DQ56</td>
<td>484mV</td>
<td>454mV</td>
<td>30mV</td>
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Return Path Effect - Crosstalk

- Baseline has 16 bits toggling and incorporates package xtalk
- DQ0 is very nearly unaffected by shared return path crosstalk
- DQ56 is very affected by return path crosstalk

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<th>Eye Height with via-via crosstalk</th>
<th>Impact of via-via crosstalk</th>
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</thead>
<tbody>
<tr>
<td>DQ0</td>
<td>540mV</td>
<td>544</td>
<td>&lt;Negligible&gt;</td>
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<tr>
<td>DQ56</td>
<td>484mV</td>
<td>351</td>
<td>133mV</td>
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DQ0: SSN Disabled, Ideal Return, DQ0:15 active

DQ56: SSN Disabled, Ideal Return, DQ48:63 active
## All Effects combined

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<td>28mV</td>
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<tr>
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<td>484mV</td>
<td>340</td>
<td>144mV</td>
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- Baseline has 16 bits toggling and incorporates package xtalk
- DQ0 is primarily affected by SSN — Good return path layout
- DQ56 is primarily affected by return path crosstalk — Poor return path layout
**DDR5 Data rate – 4000MT/s**

- Baseline has 16 bits toggling and incorporates package xtalk
- Overclocking DDR4 IBIS at 4000MT/s
- Impact of both SSN and return path effects increase with increased data rates
- Only single signal return path effect *might* be offset by DFE
  — Crosstalk effects (SSN or return path) can’t

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<td>514mV</td>
<td>99mV</td>
</tr>
<tr>
<td>DQ56</td>
<td>542mV</td>
<td>345mV</td>
<td>197mV</td>
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THANK YOU

Q&A