How to Design Good PDN Filters

Istvan Novak, Samtec

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How to Design Good PDN Filters

Istvan Novak, (Samtec)
Istvan Novak is a Principle Signal and Power Integrity Engineer at Samtec, working on advanced signal and power integrity designs. Prior to 2018 he was a Distinguished Engineer at SUN Microsystems, later Oracle. He worked on new technology development, advanced power distribution and signal integrity design and validation methodologies for SUN’s successful workgroup server families. He introduced the industry’s first 25um power-ground laminates for large rigid computer boards, and worked with component vendors to create a series of low-inductance and controlled-ESR bypass capacitors. He also served as SUN’s representative on the Copper Cable and Connector Workgroup of InfiniBand, and was engaged in the methodologies, designs and characterization of power-distribution networks from silicon to DC-DC converters. He is a Life Fellow of the IEEE with twenty-five patents to his name, author of two books on power integrity, teaches signal and power integrity courses, and maintains a popular SI/PI website.
OUTLINE

* Introduction, scope
* Requirements
* Filter design procedure
* What can go wrong
  - Wrong layout
  - Bias dependence
* Simulations and correlations
* Demos
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What This Is and What This Is NOT

* This tutorial is NOT about all-parallel bypassing
* This tutorial is about PDN structures where series elements (whether intentionally placed or accidentally being in the circuit) matter for the performance
When We Need a Filter
To feed a sensitive low-current load

Primary supply side: 3.3V 10A, 200mVpp noise

Filtered secondary supply: 3.3V 0.1A, 2mVpp noise

It is easier to filter for a low-current rail than quiet a high-current rail.
When We Need a Filter
To keep noise spilling out from noisy loads

- Quieter primary supply side
- Noisy secondary supply

PDN filter

It is easier to contain noise at its source. Main stress parameter is capacitor ripple current.

DC DC
AC AC

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Typical Noise Source

* DC-DC converters are popular and needed for their high efficiency
* They tend to generate a lot of noise
DC-DC Converter Output Ripple Voltage

- The inductor ripple current flows through the output capacitor
- First-order mid-frequency capacitor model = ESR-only
- Output ripple voltage shape closely follows inductor ripple current

\[ \Delta v = ESR \times \Delta I \]

If \( C_{\text{load}} \times \text{ESR} \) pole is below \( F_{\text{sw}} \), the output ripple is:

\[ \Delta v = ESR \times \Delta I \]
DC-DC Converter Output Ripple Voltage

- The inductor ripple current flows through the output capacitor
- First-order mid-frequency capacitor model = ESR-only
- Output ripple voltage shape closely follows inductor ripple current
**DC-DC Converter Input**

* The input voltage is chopped by the switches
* Inductor current is continuous
* Input current has large jumps
**DC-DC Converter Ringing**

- The switching edges may have high-frequency transients
- Ringing frequency: 50 – 1000 MHz

Source:
- Mid-Frequency Noise Coupling between DC-DC Converters and High-Speed Signals, DesignCon 2016
- What is New in DC-DC Converters; An OEM’s Perspective, DesignCon 2012
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Analog Supply Noise Filter (1)

Typical noise to filter: DC-DC converter output ripple.
Analog Supply Noise Filter (2)

Possible functions and requirements:

* Low-pass filtering from main to secondary
* Low-pass filtering from secondary to primary
* Output impedance for the load (*)
* Input impedance for the source (*)

(*) Optional requirement

Passive filters may be physically symmetrical

Relevant transfer functions are mostly not symmetric

Watch DC voltage drops closely
Analog Supply Noise Filter (3)

Static and dynamic budget

Primary

Nominal

$V_{\text{min\_in}}$

↓

Static tolerance

↑

Dynamic noise

Dynamic noise

DC drop

Secondary

Nominal

$V_{\text{min\_out}}$

↓

Risk

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Analog Supply Noise Filter (4)

* Use low-Q inductors or ferrites, or

* Low Dropout Regulators

* DO NOT use Hi-Q filters
Transfer Functions

What transfer function matters?
- $Z_{21}$ or $S_{21}$?
- Something else?

$Z_{21} = \frac{V_{out}}{I_{in}}$

$S_{21} = \frac{\text{wave}_{out}}{\text{wave}_{in}}$
Transfer Functions

For filters from a high-current to a low-current rail we need the *unloaded voltage transfer function*: $\frac{V_{\text{out}}}{V_{\text{in}}}$
Impedances

What filter impedance function matters?

* $Z_{11}$, or $Z_{22}$?
* Something else?

For filters from a high-current to a low-current rail: Output impedance with shorted input and input impedance with open output
Filter Illustration

The good

\[ V(\text{output1}) \]

\[
\begin{align*}
C_{\text{out}} &= C_2 \\
100 \ \mu\text{F} & 0.003 \ \text{ohm} 5 \ \text{nH}
\end{align*}
\]
Filter Illustration
When more is less

Case 1  $C_{out}$
- 100 µF
- 0.003 ohm
- 5 nH

Case 2  $C_{out}$
- 100 µF
- 0.003 ohm
- 5 nH
- 0.1 µF
- 0.03 ohm
- 0.5 nH

Better at high frequencies, but we got a peak
Filter Illustration

The best

Identical capacitors in parallel
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The Filter Design Process

Collect input requirements
* Offending frequency components (frequency, magnitude) to filter
* Necessary attenuation
* Set design parameters:
* Filter cutoff frequency $f_c$ and $Q$

Design the inductance and bulk capacitance based on:

$$f_c = \frac{1}{2\pi\sqrt{LC}}, \quad Q = \sqrt{\frac{L}{CR_s}}$$

Or use a circuit simulator to quickly iterate component values…
Low-Current Filter Example (1)

Design requirements for low-current filter

- Cutoff frequency $f_c = 100 \text{ kHz}$ (DC-DC converter running at 1MHz)
- $Q = 0.5$

Assume $R_s = 1 \text{ Ohm}$

Calculated values:

- $L = 2.7 \mu\text{H}$
- $C = 10 \mu\text{F}$

Select:

- $L = 2.7 \mu\text{H} \ 0.1 \text{ Ohm}$
- $C = 10 \mu\text{F} \ + \ 0.91 \text{ Ohm}$
Low-Current Filter Example (2)

**Selected values:**
- \( L = 2.7 \mu H \) 0.1 Ohm
- \( C = 10 \mu F \) 4 mOhm 1 nH with series 0.91 Ohm
Low-Current Filter Example (3)

Selected components:
* Coilcraft 181PS-272 L = 2.7 μH 0.08 Ohm
* Kemet C0805C106K4PAC C = 10 μF 4 mOhm 1 nH
High-Current Filter Example (1)

Design requirements for high-current filter

* Cutoff frequency $f_c = 30$ kHz (DC-DC converter running at 300 kHz)
* $Q = 0.5$

Assume $R_s = 10$ mOhm

Calculated values:

* $L = 27$ nH
* $C = 1000 \ \mu F$

Select:

* $L = 27$ nH 1 mOhm
* $C = 1000 \ \mu F \ 9$ mOhm
High-Current Filter Example (2)

Selected values:
- \( L = 27 \text{ nH} \) 1 mOhm
- \( C = 1000 \, \mu \text{F} \) 9 mOhm 5 nH
High-Current Filter Example (3)

Selected values:
- \( L = 26 \, \text{nH} \quad 0.2 \, \text{mOhm} \)
- \( C(2x) = 470 \, \mu\text{F} \quad 18 \, \text{mOhm} \quad 4 \, \text{nH} \)
Selected components:

- FA2769-AL L = 26 nH 0.2 mOhm
- T520Y108M2R5ATE010 C = 1000 μF 10 mOhm 5 nH
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What Can Go Wrong

Layout issues

* In high-current filters (voltage drop matters)
  - DC issues around contact resistance
  - resistance increase in corners
  - uneven distribution of currents in via arrays

* In wide-band and high-attenuation filters
  - sneaky path around components
  - Sneaky path on the board

* Too much phase shift if the filter is inside a converter feedback loop (usually in unintentional filters)

* Stub resonance

[Image of filter and layout issues]

[Image of filter and layout issues]
Filter Geometry
A possible problem

We may not have room for filter capacitors near IC pins. But an extreme terminated trace resonates and amplifies noise.

Solution: need to series terminate the trace by
- Adding resistance in series to the trace, or
- Adding resistance in series to the capacitor

Primary | ferrite | Secondary
--- | --- | ---
C_{in} | | Zo, t_{pd}
--- | --- | ---
C_{out} | | C_{load}
Simulated
Before Fix

Filter transfer function [dB]

<table>
<thead>
<tr>
<th>Node</th>
<th>Transfer Function [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Node 3</td>
<td>-60 dB</td>
</tr>
<tr>
<td>Node 4</td>
<td>-50 dB</td>
</tr>
<tr>
<td>Node 5</td>
<td>-40 dB</td>
</tr>
</tbody>
</table>

Voltage transfer function of analog PDN filter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rdc</td>
<td>5</td>
</tr>
<tr>
<td>C1</td>
<td>4.70E-04</td>
</tr>
<tr>
<td>C2</td>
<td>1.00E-05</td>
</tr>
<tr>
<td>Fmin</td>
<td>1.00E+03</td>
</tr>
<tr>
<td>Lf</td>
<td>1.00E-06</td>
</tr>
<tr>
<td>R1</td>
<td>1.00E-02</td>
</tr>
<tr>
<td>R2</td>
<td>1.00E-02</td>
</tr>
<tr>
<td>Fmax</td>
<td>1.00E+10</td>
</tr>
<tr>
<td>Rf</td>
<td>1.00E-03</td>
</tr>
<tr>
<td>L1</td>
<td>5.00E-09</td>
</tr>
<tr>
<td>L2</td>
<td>5.00E-10</td>
</tr>
<tr>
<td>Fsteps</td>
<td>200</td>
</tr>
<tr>
<td>Rs</td>
<td>1.00E+00</td>
</tr>
<tr>
<td>Zo</td>
<td>2.50E+01</td>
</tr>
<tr>
<td>tpd</td>
<td>4.00E-10</td>
</tr>
<tr>
<td>Cl</td>
<td>1.00E-11</td>
</tr>
</tbody>
</table>
Simulated After Fix

Filter transfer function [dB]

Voltage transfer function of analog PDN filter

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Be Aware

* Sometime parasitic elements create non-negligible filtering

* All filter components may be impacted by bias stress
  - Capacitance loss due to voltage bias
  - Inductance loss due to current bias

* The filter has to pass DC current and therefore very low frequency noise can not be eliminated
  - Sub-harmonic converter ripple
  - Low frequency random noise

* Series resistive loss maintains second-order filtering; resistance in the parallel path approaches first-order filtering

* Check the DC-DC converter operating frequency before you switch to a different converter!
"Impact of Regulator Sense-point Location on PDN Response," Designcon 2015
Be Aware

Measured illustration of a DC-DC converter creating out-of-band low-frequency oscillation

* 6 kHz periodic disturbance in a narrow operating point range
* 500 kHz switching frequency
* Single-phase 12V to 0.9V regulator

Be Aware

- Random wander of current sharing
- 600 kHz switching frequency
- Six-phase 12V to 0.9V regulator

Current sharing among phases in the time domain
Spectrum of output voltage

Source: “Measuring current and current sharing of DC-DC converters,” DesignCon 2018
Be Aware: Distribution of Loss

Series resistive loss maintains second-order filtering; resistance in the parallel path approaches first-order filtering.
Be Aware: Q Amplification

Q times amplification of current

Peaky impedance: Q=3

No amplification of current

Q=1
Dissipation in capacitors:

\[ I_{\text{rms}}^2 \times \text{ESR} \]
Be Aware: Bias Effect

9dB peaking at 25 kHz!

37dB variation at 300 kHz!
Loss of Capacitance in MLCCs

<table>
<thead>
<tr>
<th>Percentage range [%]</th>
<th>Relative multiplier</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial tolerance</td>
<td>+0 -10</td>
</tr>
<tr>
<td>Temperature effect</td>
<td>+0 -15</td>
</tr>
<tr>
<td>DC bias effect</td>
<td>+0 -70</td>
</tr>
<tr>
<td>AC bias effect</td>
<td>+0 -30</td>
</tr>
<tr>
<td>Aging (over 3 years)</td>
<td>+0 -7.5</td>
</tr>
</tbody>
</table>

* For worst case, have to multiply all multipliers

* High CV ceramic capacitors can lose up to 85% of capacitance

* Highest impact is DC and AC bias voltage

Loss of Capacitance in MLCCs, Temperature

EIA Class II and Class III ceramics

First character:
Z: + 10C
Y: - 30C
X: - 55C

Second character:
2: + 45C
4: + 65C
5: + 85C
6: + 105C
7: + 125C
8: + 150C
9: + 200C

Third character:
F: +- 7.5%
P: +- 10%
R: +- 15%
S: +- 22%
T: + 22 / - 33%
U: + 22 / - 56%
V: + 22 / - 82%

The specification defines the bounding box only, not the shape of the curve
Loss of Capacitance in MLCCs, DC Bias

*Old assumptions are not valid any more!*

- In the past X7R capacitors were thought to lose less capacitance than X5R capacitors.
- Not true any more
- Last character on plot labels refers to X5R or X7R

Loss of Capacitance in MLCCs, AC Bias

* Vendors test with 0.5 or 1.0Vrms source voltage at 100/120Hz
* Most of the source voltage appears across the DUT
* Bypass applications call for mV or tens of mV noise across the capacitors
* In small signal applications we lose 20-30% capacitance

Other capacitor types show minimal or no DC or AC bias effect.
Loss of Inductance in Ferrite Beads

* High permeability materials can lose significant inductance
* Highest impact is DC current
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Simulation Models

* Ideal C (default model in some tools)

* C-R, frequency independent (used in DC-DC modeling)

* C-R-L, frequency independent (simple SPICE subcircuits)

* C-R-L, frequency dependent fitted models

* S-parameter models, series or parallel

* 2-D RLC grid

* 3-D RLC grid

* Dynamic models
Model Fitted to Measured Data

MODEL PARAMETERS:

- $C_{md} = 2.20 \times 10^{-5}$
- $R_{md} = 6.50 \times 10^{-1}$
- $L_{md} = 1.80 \times 10^{-8}$
2D Grid MLCC Model

Equivalent schematics:

Impedance magnitude [Ohm]

Dielectric current at parallel resonance [A]

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Modeling Capacitance and Inductance Variations

Source: “Needs and Capabilities for Modeling of Capacitor Derating,” DesignCon 2016, courtesy of Shoji Tsubota
Modeling Capacitance and Inductance Variations

Development of Dynamic Modeling

Source: “Needs and Capabilities for Modeling of Capacitor Derating,” DesignCon 2016, courtesy of Shoji Tsubota

0603/X5R/0.47uF/6.3V
Capacitance changes

Inductance does not change
No change in signature, only shift
Dynamic Models, Test Large-signal Nonlinearity

Charge balance:

\[ I \cdot dt = C \cdot dv \]

Dynamic Models

Capacitance at 100 Hz [F]

BW = 0.35/\(t_r\) = 0.35/4ms ~ 100Hz

Acknowledgement and Resources

Special thanks to

- Keysight and Picotest for providing demo equipment
  - https://www.picotest.com/products_BODE100.html
- Murata for assisting with dynamic models and samples

- Simulations were done with Analog Devices’ free LTSPICE
- Filter evaluation boards
  - https://www.sv1afn.com/rf-experimenter-s-pcb-panel.html

This presentation is based on the following training course materials

- https://www.cei.se/course-056-power-integrity-advanced-design-and-characterization-group.html
- https://www.conted.ox.ac.uk/courses/making-successful-power-distribution-designs
THANK YOU!

Any Questions?
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Test Board Construction, Build
DUT Circuit

C1, C2: 47uF 4V 0805 X5R MLCC

L1: 120 Ohm @ 100 MHz 0603 2A 50mOhm
Simulation Setup

```
.all 100 100 1E7
.include GRM21BR60J107ME15_LT.mod
.include BLM18PG121SN1.mod
.step param Vdc List 0,4
.step param Idc List 0,1
```

Note: Alternate SPICE solve engine may need to be selected!
Simulated Corners

Voltage transfer function

Input impedance

Bias:
0V 0A
4V 0A
0V 1A
4V 1A

Simulated with LTSPICE and Murata dynamic models.
Simulated Voltage Bias Effect

Simulated with LTSPICE and Murata dynamic models.

Idc = 0A

Vbias = 0...4V
Simulated Current Bias Effect

Simulated with LTSPICE and Murata dynamic models.

Idc = 0...1A

Vbias = 4V
Measurement Setup

**Frequency Response Analyzer**

- OUT
- CH1
- CH2

**Filter DUT**

- R
- L1
- C1: BLM18PG121SN1
- C2
- GRM21BR60J107ME15
- GRM21BR60J107ME15

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Options for Adding Bias

**Frequency Response Analyzer**

- OUT
- CH1
- CH2

Voltage bias from source

External voltage bias source

Filter DUT

- **Vin**
- **R**
- **L1**
- **C1** BLM18PG121SN1
- **C2**

Electronic load

Components:
- GRM21BR60J107ME15
- GRM21BR60J107ME15

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Bode 100 Setup

1) Omicron Bode 100
2) Laptop
3) DUT
4) DC voltage bias (battery)
5) DC current bias (electronic load)
Bode 100 Results

Voltage transfer function magnitude [dB]

-80  -60  -40  -20   0    20    40

Frequency [Hz]

0V, 0A
4V, 0A
4V, 1A

No-bias  V-bias  V-A-bias
E5061B Gain-Phase Setup
E5061B Gain-Phase Results

E5061B Network Analyzer

0dBm source
0 and 4V DC bias
0A current bias

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E5061B Gain-Phase Results

0dBm source
0 and 10V DC bias
0A current bias
E5061B Gain-Phase Results

E5061B
10dBm source
0 and 4V DC bias
0A current bias
E5061B Gain-Phase Results

0V and 10V DC bias
0A current bias

E5061B
10dBm source
E5061B S-parameter Setup
E5061B S-parameter Results

E5061B 0dBm source
No bias
Correlation with No Bias

- 0dBm source
- LTSPICE
- Bode100
- E5061B GP side
Correlation with Voltage Bias

- 0dBm source
- LTSPICE
- Bode100
- E5061B GP side
Correlation with Voltage and Current Bias

Voltage transfer function magnitude at 4V 1A bias [dB]

-70, -60, -50, -40, -30, -20, -10, 0, 10

Frequency [Hz]

0dBm source
- LTSPICE
- Bode100
- E5061B GP side
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