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## Impact of Power Plane Termination on System Noise

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## **Abstract**

To reduce power rail voltage fluctuations that could lead to noise emissions, it is critical to keep the power plane's impedance below a target and minimize impedance peaks over frequency. Previous studies have shown that RC power plane termination can reduce power plane impedance peaks including on an electrically dense production board where decoupling capacitors would not fit near critical memory components. In this study, we use measurements and simulations on a production board to show how RC termination impacts resonance distribution, the resonance Q-value, and voltage domain noise. We show how these translate into signal integrity performance and crosstalk.

RC power plane termination is a simple, low-cost technique using the least valuable PCB real estate at the edge of the power plane. We will show that this technique not only reduces power plane impedance peaks to improve voltage noise but can also improve the signal performance of nearby traces. In this way RC termination should not only be considered a last resort relegated to the EMC specialist but something that can be actively incorporated as a power integrity design strategy and something that should be considered to mitigate the influence of power plane resonances on signal integrity.

## Author(s) Biography

Ethan Koether earned his master's degree in Electrical Engineering and Computer Science in 2014 from the Massachusetts Institute of Technology and has spent the last seven years as a hardware engineer at Oracle. He recently began his new role as a Power Integrity Engineer with Amazon's Project Kuiper. His interests are in commercial power solutions and power distribution network design, measurement, and analysis.

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Istvan Novak is a Principal Signal and Power Integrity Engineer at Samtec, working on advanced signal and power integrity designs. Prior to 2018 he was a Distinguished Engineer at SUN Microsystems, later Oracle. He worked on new technology development, advanced power distribution, and signal integrity design and validation methodologies for SUN's successful workgroup server families. He introduced the industry's first 25  $\mu\text{m}$  power-ground laminates for large rigid computer boards and worked with component vendors to create a series of low inductance and controlled-ESR bypass capacitors. He also served as SUN's representative on the Copper Cable and Connector Workgroup of InfiniBand, and was engaged in the methodologies, designs and characterization of power-distribution networks from silicon to DC-DC converters. He is a Life Fellow of the IEEE with twenty-nine patents to his name, author of two books on power integrity, teaches signal and power integrity courses, and maintains a popular SI/PI website. Istvan was named Engineer of the Year at DesignCon 2020.

## Introduction

As printed circuit board (PCB) design continues to become more challenging with lower power plane target impedance requirements, higher system density and more power domains, system designers are continuously challenged to place enough decoupling capacitors to meet target impedances over a wide range of frequencies while avoiding issues related to resonances in the power delivery. Low frequency resonances can be dealt with through careful selection of capacitor values, placement, and connections [10] but power plane resonances can be more difficult to deal with, requiring the addition of a loss mechanism [9].

Adding RC power plane terminations is a simple, low-cost method of lowering power plane impedance peaks to reduce noise emissions and power resonances over a mid-range of frequencies, determined by the electrical spacing and parasitic inductance of termination components [1]. Furthermore, the RC termination components can be placed at the periphery of the power plane where component density is lowest. We have previously demonstrated the effectiveness of this technique for reducing power plane resonances in a high-current memory power rail in a large production board where the termination components replaced traditional decoupling capacitors [2]. In this study, we show the impact of the power plane terminations on the performance of signals in the same board area as the power net.

Previous studies have shown the impact of power net resonances on signal performance [3, 4, 7] and the impact of decoupling capacitor placement on power noise [6, 8]. In this study, we present measurements and simulations to show the impact of RC power plane termination on signal performance, showing how this simple technique can positively impact the entire system.

Our results show system designers a simple but powerful technique for reducing power plane impedance peaks to reduce noise emissions and present the impact of this technique on the performance of signals and power nets in a complex system. The solution has the added benefit of freeing up valuable real estate on the board in the highest-density areas.

## Impact of Termination on Power Plane Resonances

In this section we show the derivation of approximate termination values and measurement to simulation correlation of power plane impedance on a production motherboard with and without RC termination components.

### Calculation of RC Termination Values

The best termination value will match the impedance of the power plane, which can be approximated by the following formula, valid for single power-ground plane pairs

$$Z_{plane} \sim \frac{535}{\sqrt{\epsilon_r}} \cdot \frac{h}{P}$$

where  $h$  is the dielectric layer height between the power and ground layer in the PCB,  $P$  is the perimeter of the power shape, and  $\epsilon_r$  is the relative permittivity of the dielectric material [1,2].

The power net that we look at and terminate on this production board has shapes on multiple layers. We use the two largest plane shapes on this net from two layers to approximately calculate the impedance of the complex structure (Figure 1). Each power plane has an adjacent ground plane. The impedance of the plane structure can be modeled as three independent impedances in parallel.

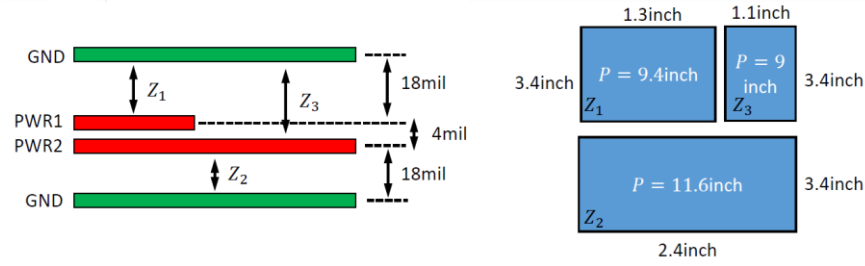


Figure 1. Power planes used for RC termination calculation showing the layer spacing and power plane perimeters. Figure from [2]

$$|Z_{eq}| = \frac{1}{\frac{1}{|Z_1|} + \frac{1}{|Z_2|} + \frac{1}{|Z_3|}} = 0.161\Omega$$

The number of termination elements around the power shape on top of the board ( $n = 22$ ) is selected to provide a convenient termination resistance when  $n$  is multiplied by  $Z_{eq}$ . This leads to a termination resistance value,  $R$ , of

$$|Z_{eq}| = \frac{R}{No. RC'S} = \frac{R}{22} \Rightarrow R \sim 3.3\Omega$$

Each termination resistor is placed in series with a capacitor to avoid DC power loss. The capacitance should be large enough that the RC cut-off frequency between the termination resistor and DC block capacitor is at least one order of magnitude below the first resonance peak of the power plane. As shown in the equation below, a capacitance of  $1\mu F$  was selected

$$f = \frac{1}{2\pi RC} < 50 kHz \Rightarrow C > 9.65 \times 10^{-7}$$

Additional high frequency capacitors can also be placed over the power plane to further suppress resonances by forcing a null in standing wave patterns at the connection point.

Note that while RC termination uniformly suppresses modal resonances where the effective series inductance of termination components is significantly lower than the equivalent inductance of the plane structure, placing the series resonance frequencies of bypass capacitors on plane-impedance peaks comes with the practical challenge that two relatively sharp resonances have to be matched in the frequency domain and the locations of components is more restrictive as well: it has to be adjusted to match the spatial resonance pattern.

## Measurement and Simulation of Power Plane Termination

Figure 2 shows the board layout and the locations of the 22 termination elements.

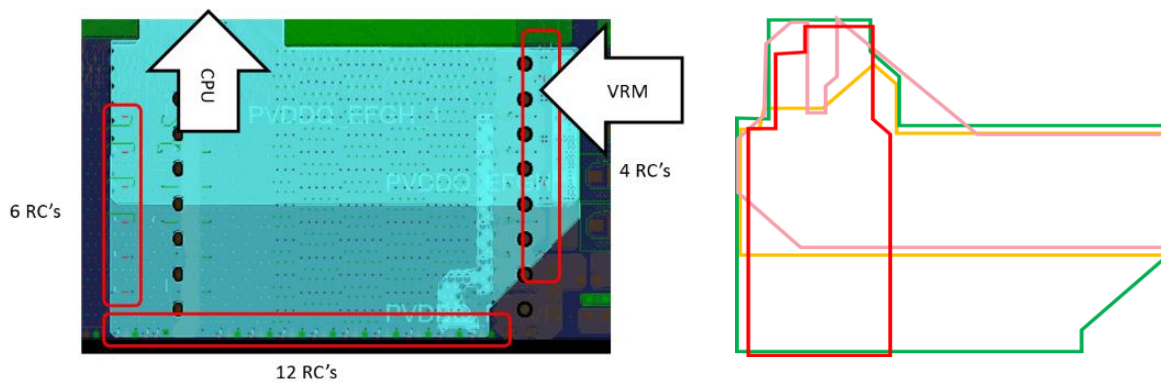


Figure 2. Left: Image of board file showing location of CPU, Voltage Regulator Module (VRM), and termination RC's. The power net has shapes located on multiple layers of the 16-layer board. Right: Outlines of the terminated power plane shapes on different layers of the board. Figure from [2].

We measured the power plane impedance on this production board with and without termination elements to determine the impact of these on suppressing power plane resonances. No other components were present on the board.

Figure 3 shows the orientation of probes used for the power plane impedance measurement. S21 was measured using a Performance Network Analyzer (PNA) [11] with wafer probes [12]. We performed a full two-port calibration before the measurement using a calibration substrate [13]. We then calculated the impedance from the measured S21 parameters [14].

We used an identical setup in a field solver [15] for correlation with the measurements. The probe locations shown in Figure 3 were chosen to match the measurement locations, and only the power and ground planes under investigation were included in the simulation.

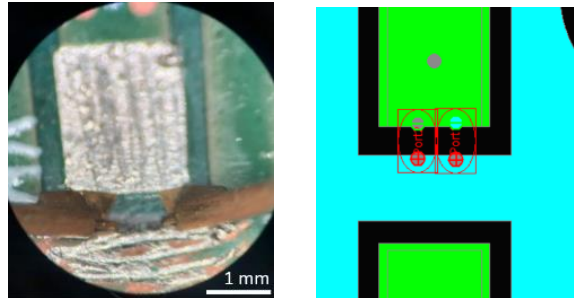


Figure 3. Left: Image through microscope of board showing wafer probes used for power plane impedance measurement. Right: Image of power plane (blue) in hybrid simulator tool showing location of probes relative to ground (green). Figure from [2].

For the analysis and correlation in this paper we chose a production board with multiple intertwined power rails. The measurement setup and connections presented multiple challenges. The density of the board would have not allowed us to add coaxial test ports even if we had known at the time of design that the board would be used for this analysis. As a result, wafer-probe connections were used, landing on exposed copper surfaces. Some landing points were on via pads, but in some cases there was no exposed ground nearby. In those cases the solder mask was scraped away and solder was applied to provide a soft landing surface for the probe tips. Creating a reliable connection to production printed circuit board without gold-plated surfaces requires higher-than-regular normal force when we land the probes. This limited the choice of probes to the VP-style adapter from GGB Industries. Even with the slightly higher normal force, the quick oxidization of the copper and tin surfaces presented further challenges: the very thin oxide layer can produce almost realistic looking, but still wrong results. To avoid this problem each measurement was performed multiple times with the probe tips and landing surfaces carefully cleaned in between.

The large dynamic range of PDN-related crosstalk signals required a careful selection of frequency range, cabling and DUT mounting. The lower end of measured frequencies was set to 1MHz, this ensured that there was no need to deal with the cable-braid loop error, which would have required the use of either common-mode chokes or an isolation amplifier, which in turn would have limited the upper frequency range. Two additional considerations we had to keep in mind: the proper polarity of connections and safely isolating the board from the probe-station metal frame. The proper polarity on a physically small, passive, unpowered DUT would not matter. This means that because we measure AC performance with the vector network analyzer, we don't necessarily have to connect the probe's ground blade to the DUT ground and the probe's center pin to the DUT power; reversing the connections would produce the same result. With our physically big DUT we did not have this flexibility: if we reversed the connection, the probe's center pin would have been connected to the large ground structure in the PCB, which would have created too much error through its stray capacitance to the environment. Even with proper polarity, we must provide sufficient isolation between the probe station's large metal frame and the DUT ground structure, otherwise the

common-mode noise picked up by the probe-station frame would introduce too much error. The isolation was provided by placing a one inch thick piece of plastic foam between the frame and board.

Figure 4 shows the measured and simulated power plane impedance magnitude versus frequency with and without termination elements. Two high Q resonances ( $Q_{3dB} = 22$  and  $Q_{3dB} = 27$ ) can be seen around 500MHz for the unterminated board. With the RC termination components, this Q value is drastically reduced:  $Q_{3dB} = 5.7$  for  $R=3.3\Omega$  and  $Q_{3dB} = 3.9$  for  $R=10\Omega$ .

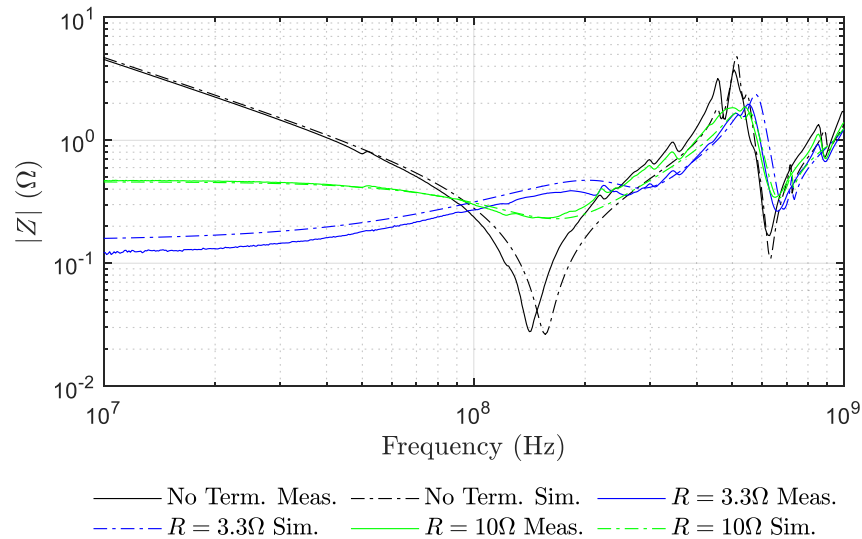


Figure 4. Impact of power plane termination measurement to simulation correlation. Measured power plane impedance magnitude versus frequency with no termination (black); 3.3Ω, 1μF RC terminations (blue); and 10Ω, 1μF RC terminations (green). Figure from [2].

The typical target impedance for a power plane in a system such as the one measured here is in the mΩ range. Despite the benefit that power plane termination provides in reducing mid-frequency plane resonances (Figure 4), we can see that it does not eliminate the need for low ESR bulk capacitors to reduce the low frequency impedance. We must further ensure that the low frequency bulk capacitors do not unintentionally resonate with the termination elements. Using the field solver, we see that the bulk capacitors do not resonate with the termination RC components between 1kHz and 1GHz (Figure 5). For the plane geometry of this board, the RC terminations help reduce impedance up to 1GHz and dampens the resonance between the board capacitance and bulk capacitor inductance at 250MHz. The dampening behavior is most obvious in Figure 6 where the impedance is plotted with a linear frequency scale. The added losses from the RC termination are helpful in the overall response of the PDN as they dampen impedance peaking arising from connecting the devices to the board. In addition, noise coupling from device to device is significantly attenuated by the strong low-pass filtering of component packages [16, 17].



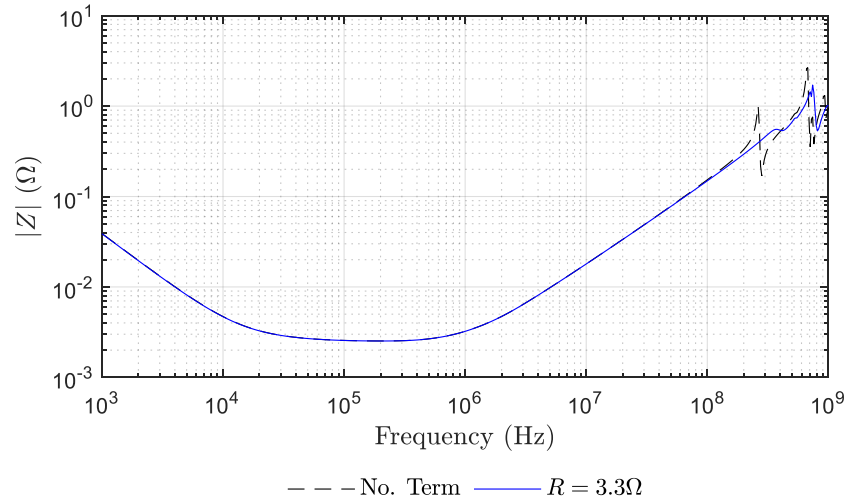


Figure 5. The simulated power plane populated with bulk capacitors with  $R=3.3\Omega$  and  $C=1\mu\text{F}$  termination elements (blue line) and without termination (dashed black line). Figure from [2].

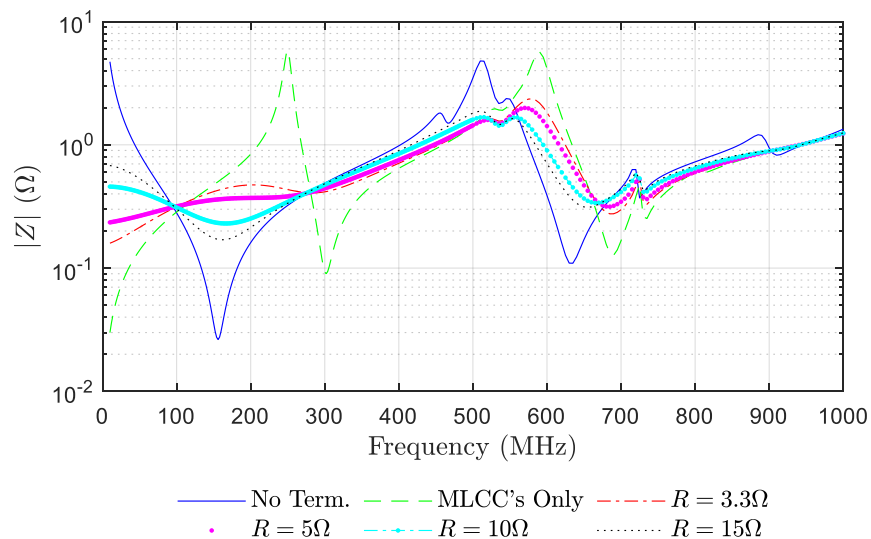


Figure 6. Simulated power plane impedance for a variety of  $R$  values to determine the optimal termination component value. Figure from [2].

The bare board impedance in Figure 6 shows a very high impedance at low frequency and the first major parallel resonance around 500MHz. If we were using only regular low-ESR capacitors to terminate the planes it would result in the green curve in the figure. As is well known, the capacitors provide a low impedance at the low frequency band at the expense of setting up a new parallel resonance between the inductance of the decoupling capacitors + mounting and the plane capacitance. As the plane and capacitors typically have very little loss this causes the high quality factor resonances at  $\sim 250\text{MHz}$ . In addition, by adding capacitors to the board, the first parallel board resonance has been pushed up by almost 100MHz, but with no significant  $Q$  reduction – the fundamental resonance energy balance

is not impacted from adding the capacitive termination in this case – but we do note that the three impedance peaks that existed around 500MHz have been reduced to just one using the capacitors.

Now, if we instead were to add RC termination of the planes, the loss from the resistors is expected to cause a reduction in Q for both the series and parallel resonances. From the simulations this is evident from the 600MHz resonance that exists in all C and RC terminated structures – the larger the resistance the lower the Q, and the added resistance causes the resonance to be pulled towards the lower frequencies. A resistance that is too high relative to the calculated value leads to a mismatch of the termination to the plane equivalent impedance, causing reflections and less reduction of resonance peaks.

## Upper Frequency of Termination Impact

To estimate the maximum frequency of effectiveness of the RC terminations, we calculate the frequency where the wavelength corresponds to the spacing between RC termination components. With an average spacing of 268 mils or 6.8 mm between RC terminations, we calculate a frequency of ~20GHz using the dielectric constant of FR-4. Since the spacing between the termination components should be much less than the wavelength of the maximum frequency of effectiveness, we divide by 10 to get 2 GHz. Since the power plane is only surrounded on three of the four sides with RC termination, we expect the termination's effectiveness to die out around 2GHz. Figure 7 shows the power plane impedance extraction to 10GHz. It shows that the termination doesn't impact results much beyond 1.5GHz.

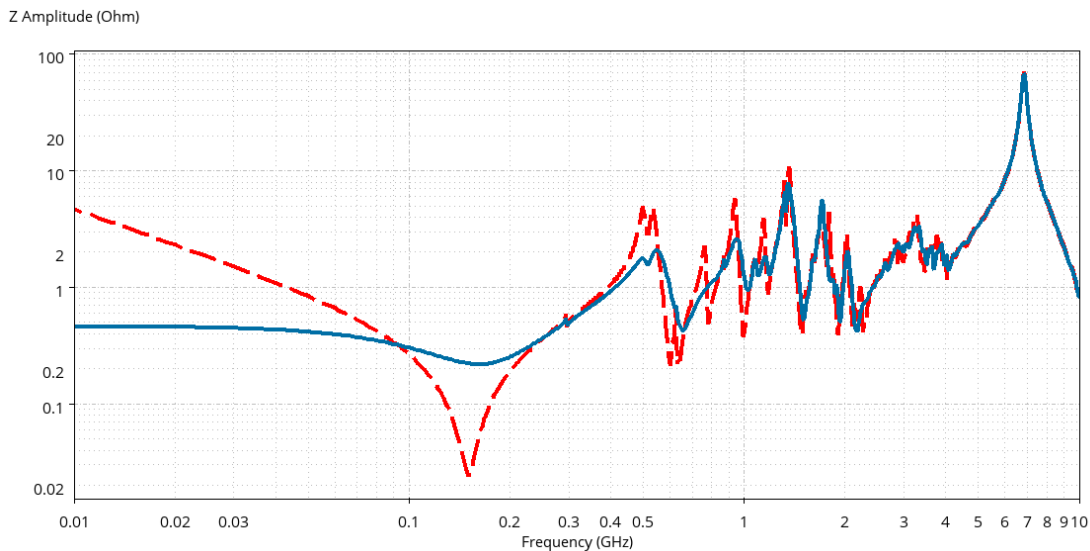


Figure 7. Simulated power plane impedance with (blue solid) and without RC (red dotted) termination to 10GHz.

To provide a sufficient number of termination components is a necessary condition, but it does not guarantee good results. It is also important that the termination elements have sufficiently low inductance. With small surface-mount components the effective inductance presented to the plane structure strongly depends on the layout. Layout details of surrounding elements, as well as assembly and layout restrictions may limit our ability to optimize the connection inductance. Figure 8 shows two instances of the termination elements, where the high density of surrounding components forced us to use traces instead of direct vertical via connections. The left image shows a compact geometry near the open edge of the plane. The right image shows an instance where the plane shape ended in the dense DIMM pin-field, necessitating the use of longer traces. The trace connecting the C and R elements could have been somewhat wider in this case to lower the inductive contribution. In the optimum layout, the power and ground connection vias should be connected with the widest possible traces and placed close to the components. But as Figure 8 shows, this can be really challenging in high-density areas.

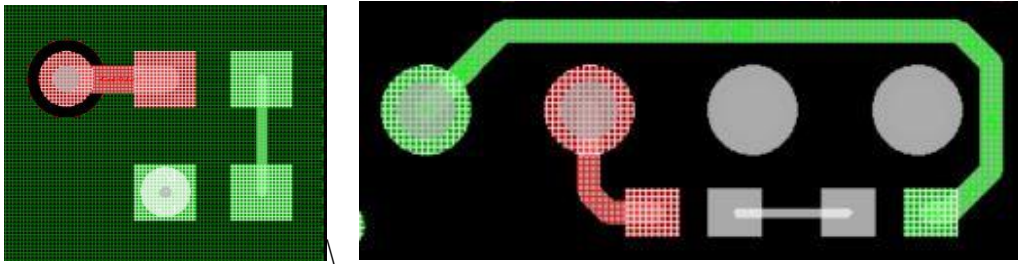


Figure 8. Sample RC termination connections. On the left a compact layout at the edge of the plane. The right image shows worst case RC routing in DIMM pin field.

We have shown that RC termination can lower power plane impedance and decrease the Q factor of resonances, making an individual power rail less susceptible to switching noise. In a complex motherboard system such as the one studied here, decreased power plane resonances on a single power rail can benefit the entire system since stray electromagnetic noise from one rail has very few barriers and can impact many other nets. In the following sections we will demonstrate the impact of RC termination on system coupling in the production motherboard.

## Impact of Termination on Power to Power Coupling

Since power nets often cover a large area of any given stack-up layer, a resonance on one power net can couple significantly to other nets. Looking at the coupling between the power net shown in Figure 2 and a nearby 5V power net, we saw a significant reduction in the magnitude of  $s_{21}$  with RC termination components present only on the VDD rail (Figure 9) at select frequencies. The impact of terminating multiple power nets simultaneously is left for future analysis and publications.

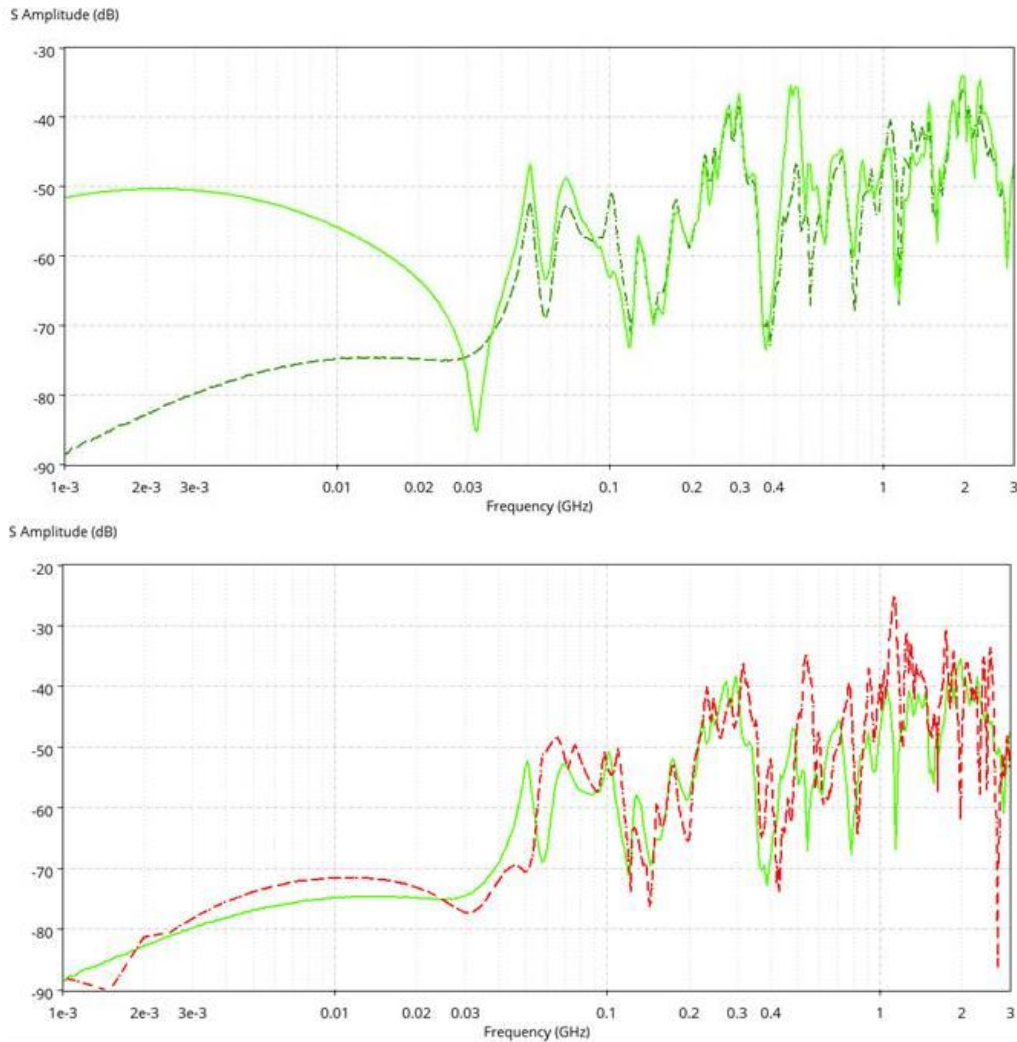


Figure 9. Top: Measurement of power to power coupling with (solid) and without (dashed) RC terminations. Bottom: Measurement (solid green) to simulation (dashed red) correlation of power to power coupling between VDD and P5V0 power rails with RC terminations.

From Figure 9, top, we see that with RC termination, coupling is reduced before the first series resonance at 35MHz, due to the better confinement of fields on the RC decoupled plane and then again around 60MHz (reduction ~4dB) and over 10dB around the 500MHz resonances. For other resonances you see only slight or no changes at all and then in some cases (e.g. around 1GHz) there is an increase in the coupling in the RC terminated case, which is expected to be due to the relatively high mounting inductance of the RC termination. Looking at the measurement to simulation correlation in the bottom of the same figure we see a general agreement between measurement and simulation up to 400MHz after which the trends in measurement and simulation agree.

We expect the reason for the RC termination only being effective for some of the resonance to be a question of which power cavities dominate a particular frequency. This was investigated by running a so-called spatial noise simulation in which a graphical

noise distribution overlay on the layout can be generated which will show what AC voltage is developing between overlapping planes in the design. An excitation was placed on the VDD rail and a voltage probe added at the measurement location of the victim 5V0 rail (lower right corner in Figure 10). It was found that when forcing 1A through the VDD plane, the peak voltage on the unterminated board was slightly below 3V (AC) at 500MHz. Figure 10 shows the spatial voltage noise distribution for the board between the pwr1 layer and the adjacent ground with and without RC termination at 500MHz. The entire pwr1 and pwr2 layers are dedicated to the different voltage supplies, and both exhibited the same behavior as discussed in the following.

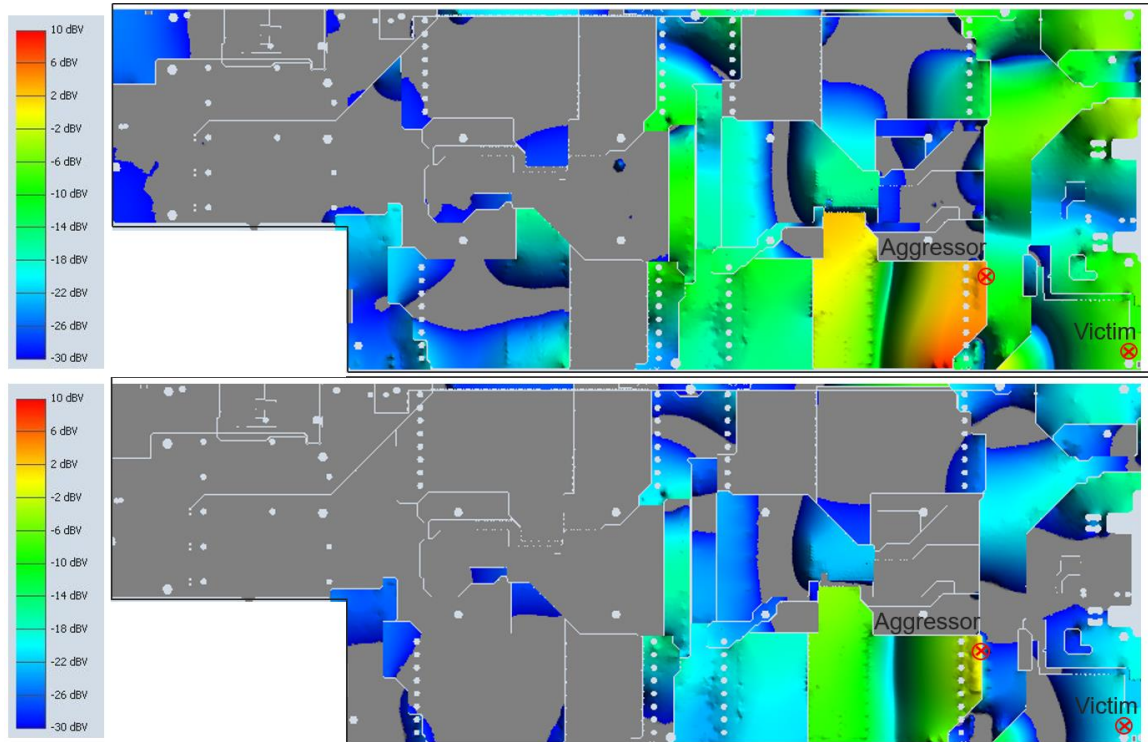


Figure 10. Spatial noise distribution for some voltage domains at 500MHz between the power plane layer and ground. Red 'x' depicts the locations of the aggressor and victim. Top: without RC termination. Bottom: with RC termination using  $C=1\mu\text{F}$ ,  $R=10\Omega$ . Grey area on the plot indicates that noise is lower than -40dB from the peak value.

As evident from above, the RC termination reduces the peak voltage level at 500MHz by 10dB, and another added value of the RC termination is that the noise cannot as easily leak out to other power planes through the power delivery network. This can be seen by noting that the area within the color scale is reduced, i.e. noise coupling is less than -40dBV in the grey areas. This is a very important aspect to point out as it demonstrates two things: (a) power plane cavities in a complex PCB are in a sense interwoven and it is not easy to contain energy within one cavity – in other words, if you try to isolate an analog power or ground domain from the noise digital domain, ferrite beads or other circuit filters on the power net may not necessarily give the desired isolation effects. Secondly, (b) it is common to think of local coupling paths when working on a system,



but for complex multi-layer boards it may not be enough especially if any planes are badly decoupled at critical system frequencies.

The effects described here will be subjected to a more thorough investigation in future work including discussions around the pros and cons of power plane adjacency.

## **Impact of Termination on Power to Signal Coupling**

In the previous sections, we showed that RC termination can be effective in lowering power plane impedance and power to power coupling. In this section, we demonstrate how RC termination lowers power to signal coupling on the production board used for this study.

To initially test our measurement to simulation setup, we performed a series of experiments on the measurement setup of the fully terminated board and compared these to our simulation results (Figure 11). For the measurement range below 10MHz, a common-mode choke was used to ensure the ground loop was not adding error to the measurement. For all three measurements, a full 2-port calibration was completed prior to the measurement. To achieve this level of correlation, it was necessary to do full-board simulations.

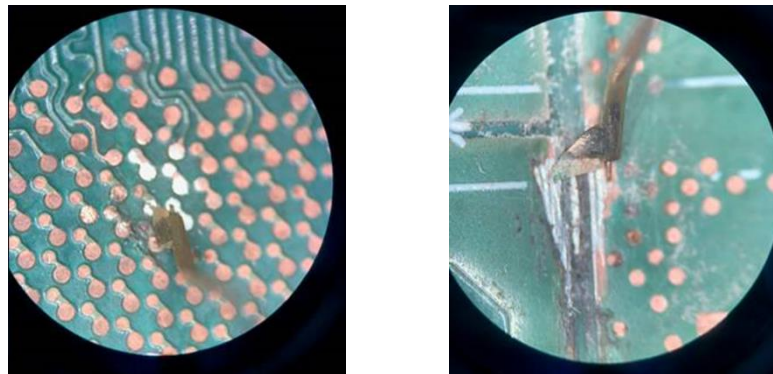


Figure 11.a. Wafer probe landings for measurements #1 (left) and #2 (right)

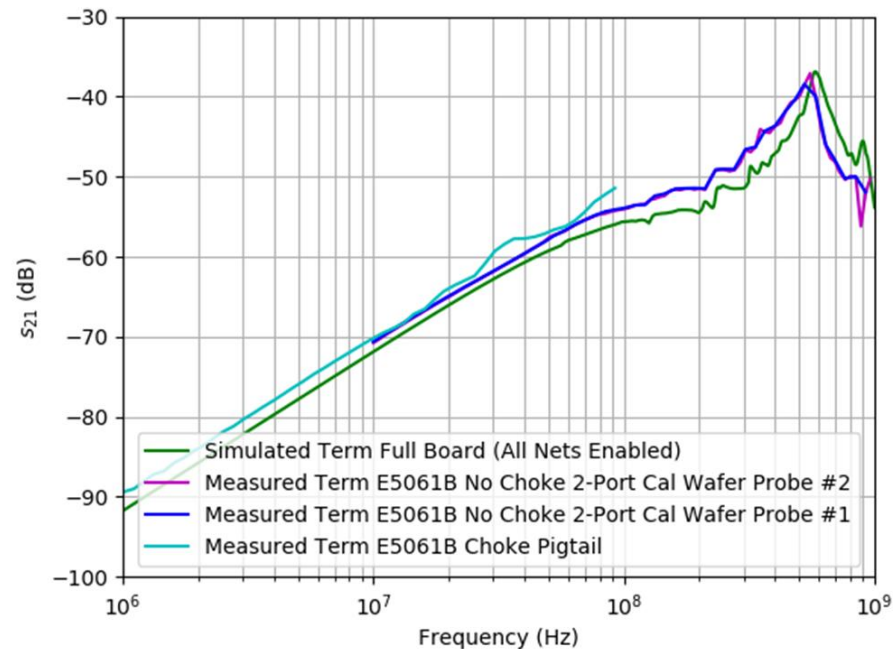


Figure 11.b. Measurement to simulation correlation of power to signal coupling with 10 $\Omega$  termination components. Above 10 MHz, two wafer probes were used to verify the measurement results (dark blue and magenta). Below 10 MHz, a common-mode choke and pigtail connections were used (light blue).

From the strong correlation results in Figure 11 we continued our measurements to determine the impact of RC termination on power to signal coupling. In Figure 12 we show measurements and simulation results of coupling from a power net to a clock enable net. The signal net travels from the ASIC to the DIMM socket through vias of the aggressor power net. The transmission line is sandwiched between two adjacent grounds, but any via transition through the power-ground cavities leaves the potential for noise coupling from the power domain cavities.

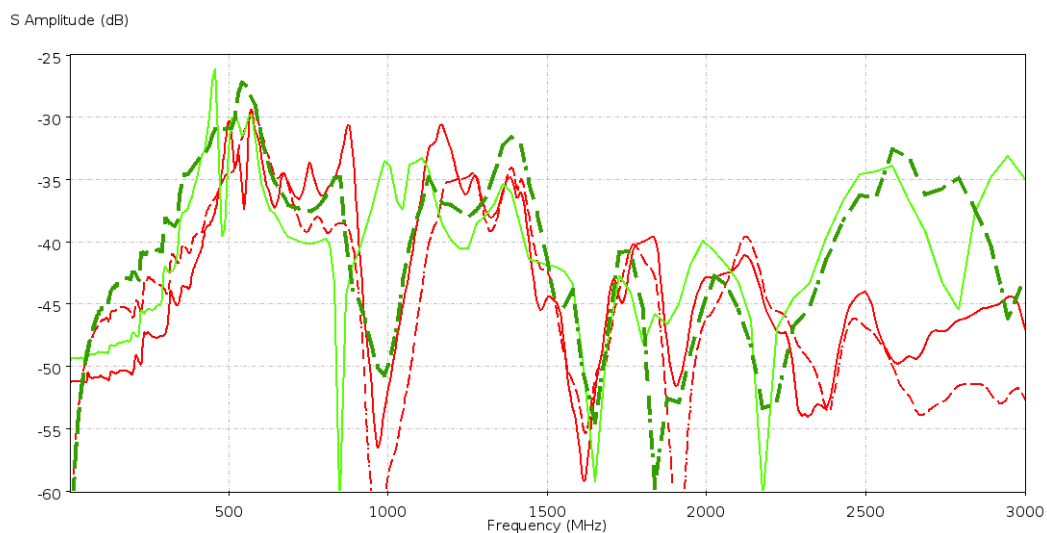


Figure 12. Power to signal coupling. Measurements without RC (solid green) and with RC (dashed green). Simulation results for same configurations (solid red – no RC; dotted red with RC).

From both curve sets in the above figure we see that adding the RC termination results in resonances being less significant (lower Q and more “smeared”) vs the bare board. There is scarcely any influence on the max coupling levels in this case and the RC terminated case shows higher peak coupling around 900MHz and 1400MHz in the measurement setup while from the simulation we were expecting more improvements. It is unclear whether this is due to measurement artefacts or some other aspects of the modeling setup, but the general comments around the challenges with the measurements still applies. Studying the simulation curves, we see the same trends as earlier. The RC decoupling is expected to lower the peak coupling values from power to signal, and like the power to power plane case, some frequencies see larger improvements than others. This is a point that will also be explored in future work and likely will be closely related to the observations made for the power to power coupling.

There is a noticeable difference between simulations and measurements at the low end of frequency range: the measurements appear to converge around -50dB, simulated values reach -60dB with a gradient. This will also be part of future explorations.

## **Impact of Termination on Signal to Signal Noise**

Lastly, we will be looking at the impact of RC termination on signal to signal coupling. FEXT and NEXT coupling was measured for two signal nets connecting between the ASIC and the DIMM. Both nets are located on the same layer but spaced far apart with 8 signal traces in between and trace to trace spacing between adjacent traces of roughly double the trace width. Under normal SI considerations there would be very little cross-talk between the two nets given that the nets are sandwiched between two adjacent ground planes. However, because the signals transition through the plane cavities of the interface power supply, they present good candidates for quantifying the amount of coupling between the nets and the impact of RC termination on these nets. Figure 13 shows FEXT and NEXT between the two signals



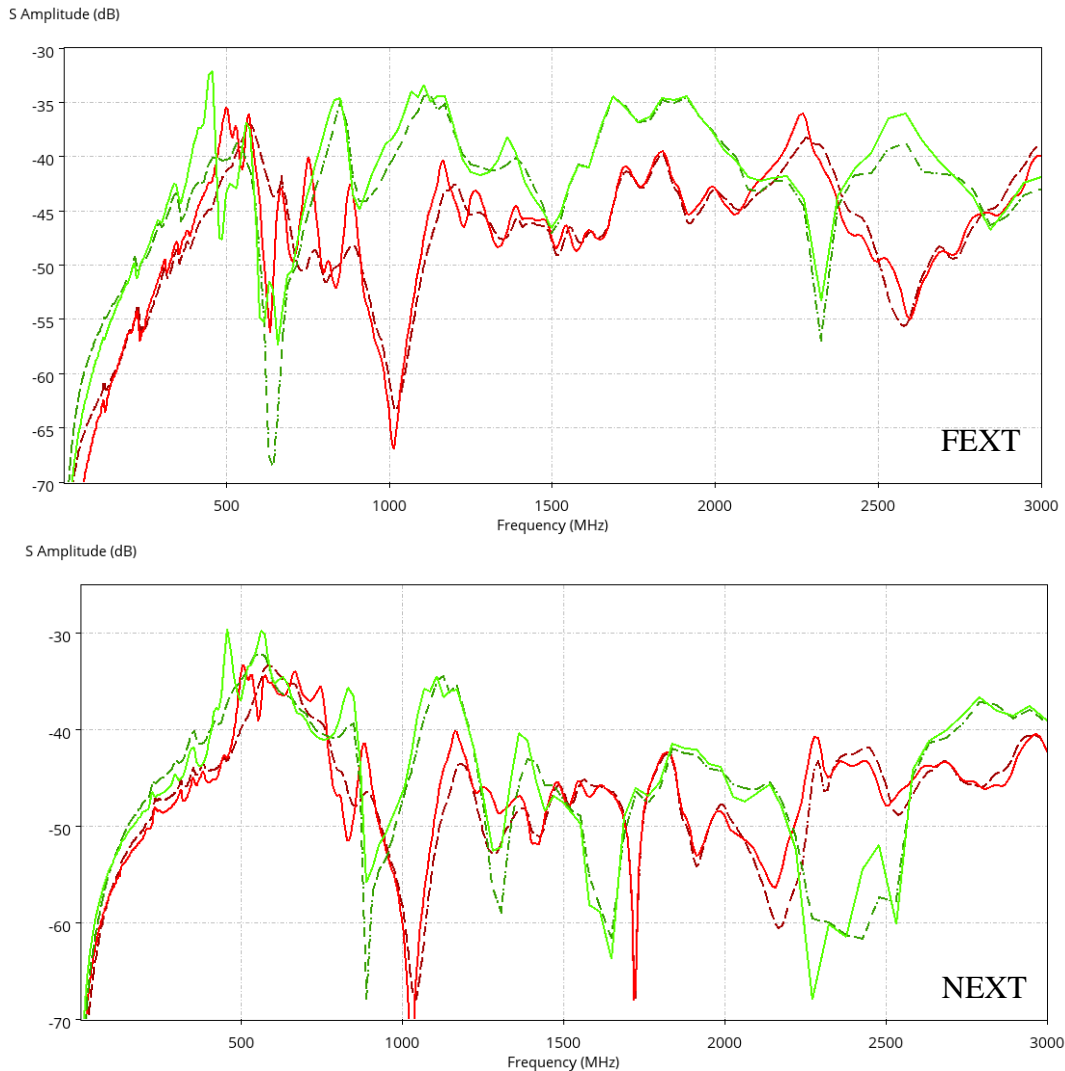


Figure 13. Signal to signal coupling. Measurement (green) vs simulation (red) with (dashed) and without (solid) RC termination components. Top: signal to signal FEXT. Bottom: NEXT.

As before the simulation predicts higher reduction with RC termination than the measurement. This can be attributed to losses not accounted for in the simulation and the fact that one of the via transitions for the signal traces is sitting in between the power and ground plane split. This is not well captured in the solver used and would need full 3D EM characterization. Another net could have been selected for this correlation, however because no test locations were pre-defined we are restricted in the measurements as to where we can probe. However, when looking at the curves it is clear that we are seeing peak reduction around 500MHz and again around 900MHz when using the RC termination. The reduction is fairly limited in the 500MHz range ~3-5 dB which we believe to be due to multiple resonances being closely spaced in the non-terminated case. Here the gain from adding the RC termination then is not so much the reduction in amplitude but the reduced Q and the smearing of the peaks. We see similar trends at

900MHz after which the improvement is negligible. It remains to be explained why we are seeing higher coupling predicted by the measurements at 1.1GHz.

## **Conclusions**

Our results show system designers a simple but powerful technique for reducing power plane impedance peaks that can reduce noise emissions, power-to-power crosstalk and signal-to-signal crosstalk of some traces.

We presented the impact of this technique on the performance of signals and power nets in a complex high-density production system board with multiple power domains. It was shown that twenty-two simple RC termination elements implemented with surface-mount components reduced the impedance peak by 10dB and also reduced the Q of the peak substantially. With the given geometry and layout, the termination gradually became ineffective above about 2GHz.

It was also shown that at their modal resonance frequencies the crosstalk between power nets with very minimal physical overlap can be substantial and terminating just one of the two power nets can reduce this resonance crosstalk. It was also shown that the reduced Q due to termination reduces the range of propagation of electromagnetic energy causing crosstalk between power nets and power and signal nets.

Finally, it was shown that signal-to-signal crosstalk is also reduced by terminating planes. Due to significant challenges that stress both simulations and measurements, further work is planned to achieve better correlation and to analyze several further options.

## **Acknowledgements**

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