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A Case Study in the Development of 112 Gbps-PAM4 Silicon and Connector Test Platform

Jean-Remy Bonnefoy (Samtec)

Ted Ballou, Istvan Novak, Gustavo Blando, Scott McMorrow (Samtec)
Raj Mahadevan (Alphawave IP)

SPEAKER

Jean-Remy Bonnefoy

Systems engineer, Samtec

jean-remy.bonnefoy@samtec.com

Jean-Remy Bonnefoy is a Systems Engineer for Samtec's Signal Integrity Group.

He is involved in the design of high-speed test systems, and he leads the hardware development of evaluation and demonstration platform for high data rate interconnects.

OUTLINE

- Optimizing a 112G test channel
- Power delivery network
- Channel performance
- Summary and conclusions

OUTLINE

- **Optimizing a 112G test channel**
- Power delivery network
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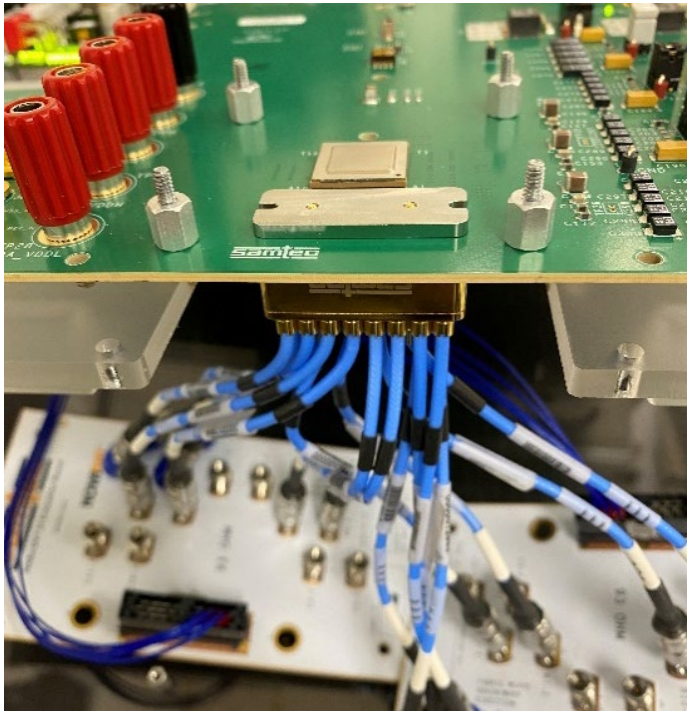
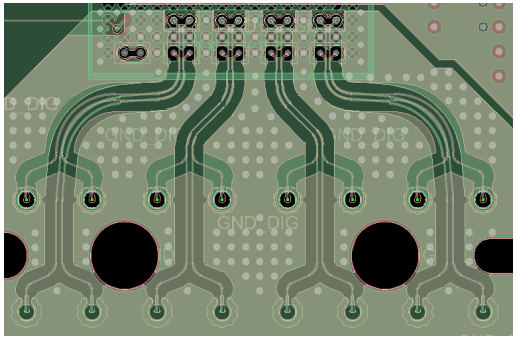
Optimizing a 112G-PAM4 test channel

- **Challenges and goals:**
  - Design an evaluation platform for 112G-PAM4 silicon and connector system
  - 3 dB total IL at 28 GHz for TX lanes
  - Use affordable, readily available material



PCB design

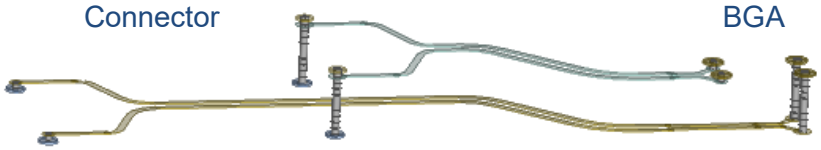
- **Stackup:**
  - I-Tera MT40
  - 1067 weave
- **Impedance:**
  - 90 Ohm package / 50 Ohm single ended coax cables
    - ➢ 92 Ohm BGA escape and open routing
- **Routing:**
  - Two routing layers (RX, TX)
  - Short TX traces, 11 mm
  - Board rotation to mitigate periodic fiber weave effects



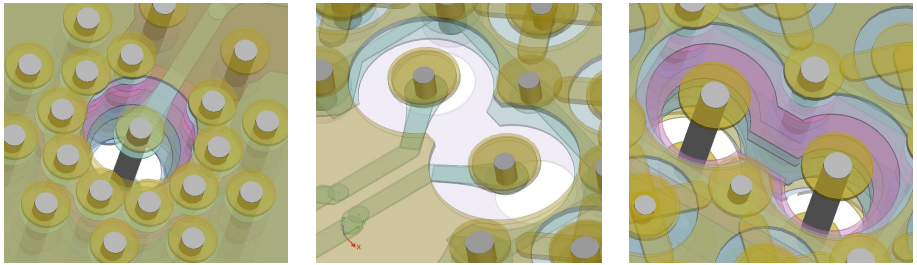
Layer	Calc Thickness	Primary Stack	Description	Dk / Df
	0.0010		Taiyo 4000-MP	3.60 / 0.0190
Layer - 1	0.0026		1/2oz Mix (Std Plt)	
	0.0050	0.0050 (2-1067)	I-Tera MT40	3.17 / 0.0023
Layer - 2	0.0006		1/2oz Sig	
	0.0052	1067 - 76% / 1067 - 76%	I-Tera MT40	3.08 / 0.0020
Layer - 3	0.0006		1/2oz P/G	
	0.0050	0.0050 (2-1067)	I-Tera MT40	3.17 / 0.0023
Layer - 4	0.0006		1/2oz Sig	
	0.0052	1067 - 76% / 1067 - 76%	I-Tera MT40	3.08 / 0.0020
Layer - 5	0.0006		1/2oz P/G	
	0.0140	0.0140 (2-2116/1-3313)	I-Tera MT40	3.56 / 0.0033
Layer - 6	0.0006		1/2oz P/G	
	0.0052	1067 - 76% / 1067 - 76%	I-Tera MT40	3.08 / 0.0020
Layer - 7	0.0006		1/2oz Sig	
	0.0050	0.0050 (2-1067)	I-Tera MT40	3.17 / 0.0023
Layer - 8	0.0006		1/2oz P/G	
	0.0052	1067 - 76% / 1067 - 76%	I-Tera MT40	3.08 / 0.0020
Layer - 9	0.0006		1/2oz Sig	
	0.0050	0.0050 (2-1067)	I-Tera MT40	3.17 / 0.0023
Layer - 10	0.0026		1/2oz Mix (Std Plt)	
	0.0010		Taiyo 4000-MP	3.60 / 0.0190

Via breakout optimization

- **Topology:**
  - Top-mounted BGA / Bottom-mounted connector
  - CDD and through vias, inherent minimal stubs



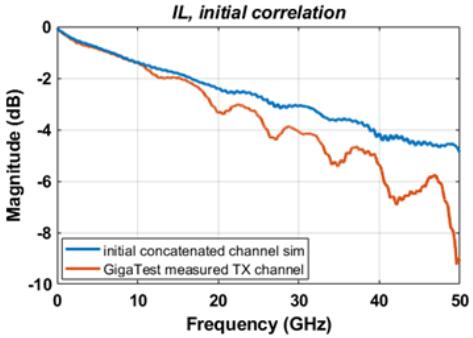
- **Impedance control:**
  - Auxiliary ground vias
  - Teardrops
  - Offset ground relief on lower reference plane

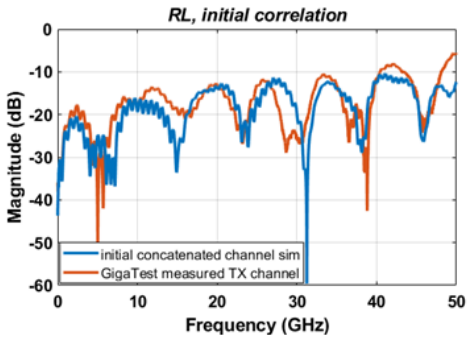


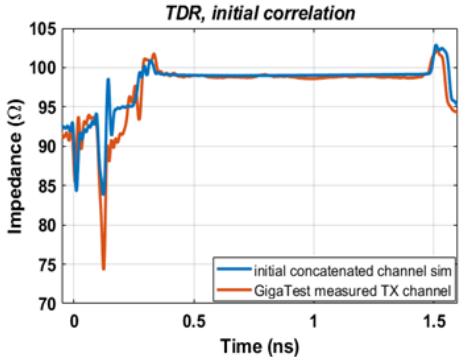
Connector via | CDD via | Thru via

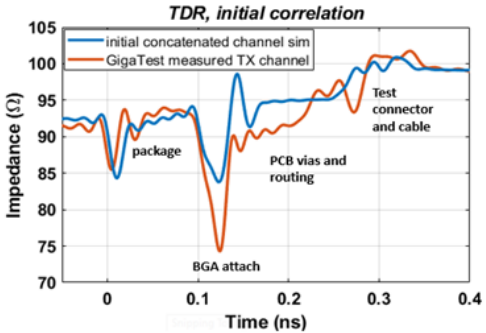
Initial simulations and measurements

- **Concatenated 4-port channel:**
  - Extracted package layout
  - Simulated GL102 dielectrics
  - Vias, PCB and cabling simulated separately
- **Measurements:**
  - Bare-die BGA package
- **Miscorrelation:**
  - Under-modeled impedance discontinuities
  - Missing resonances in the IL



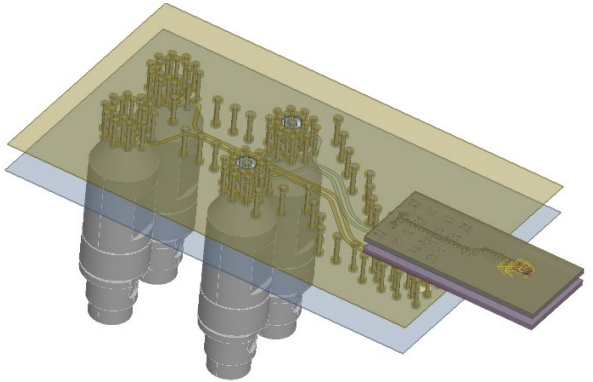




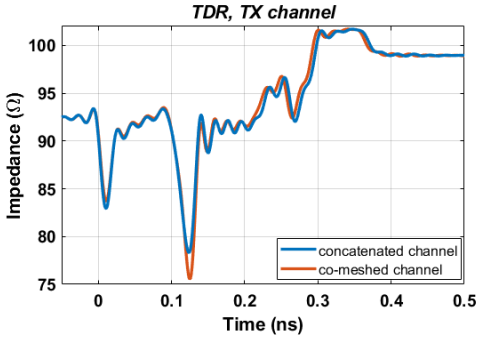


Examining root cause

- **Deep dive simulation review:**
  - Package vias
  - Package copper roughness
  - PCB thru vias
  - Connector model truncated
  - Co-meshed simulation



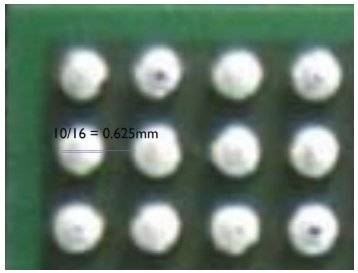
Combined co-meshed simulation model



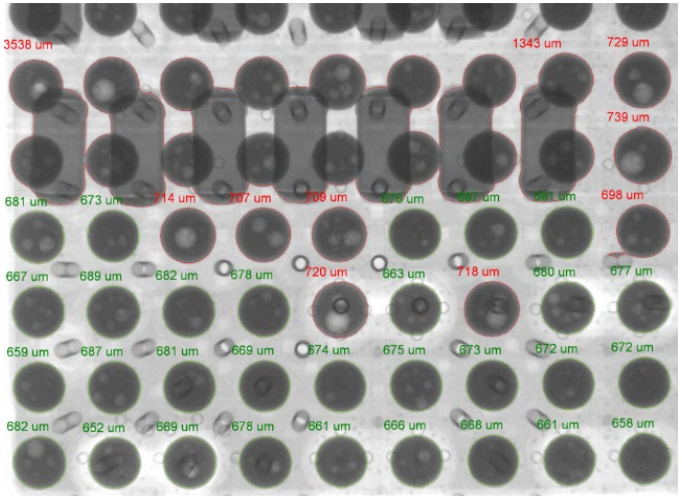
Key discontinuity = solder attach

- **BGA ball size impact on SI**
- **Reflowed ball shape predicts TDR discontinuities**

Real solder ball shapes



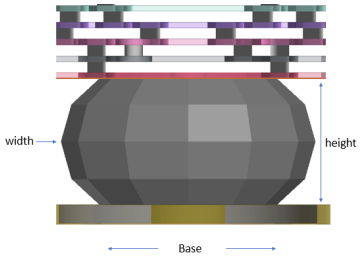
Pre-reflow solder ball



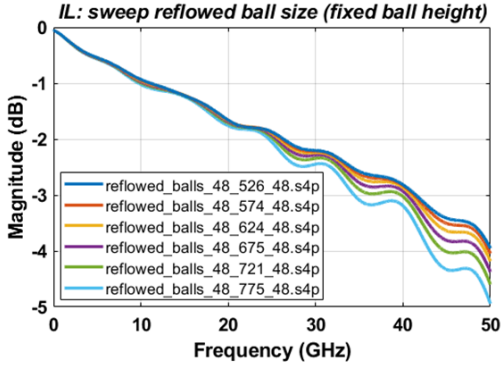
CT-scan of soldered BGA

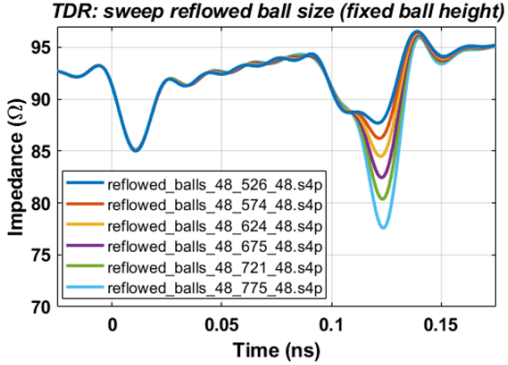
Solder ball model sweep

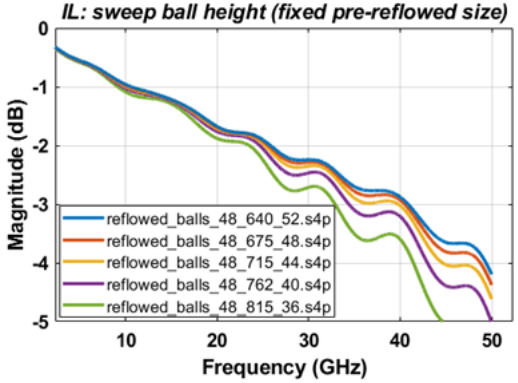
- **Reflowed ball size (width) sweep**

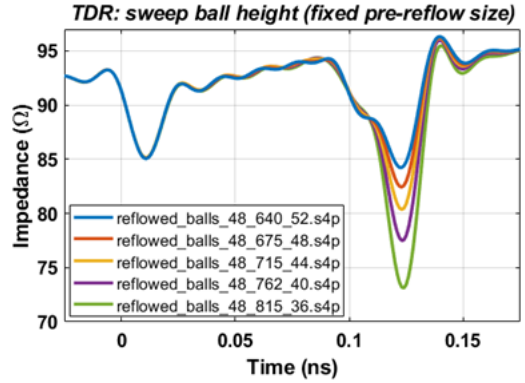


- **Ball shape (height) sweep**



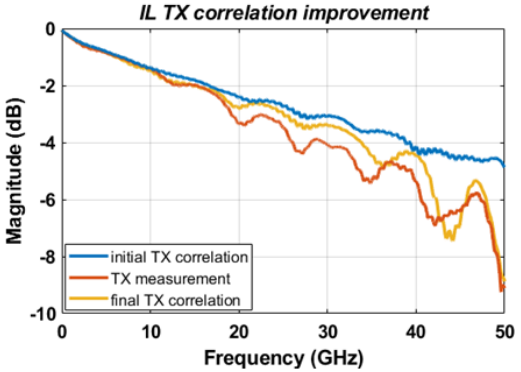


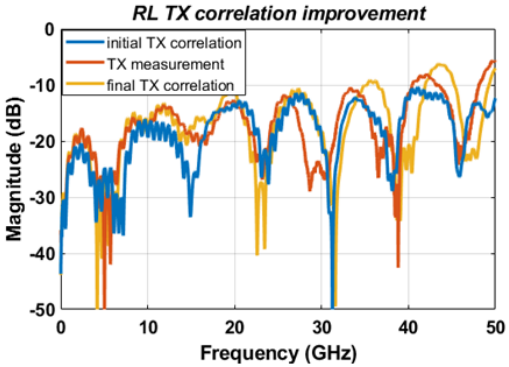


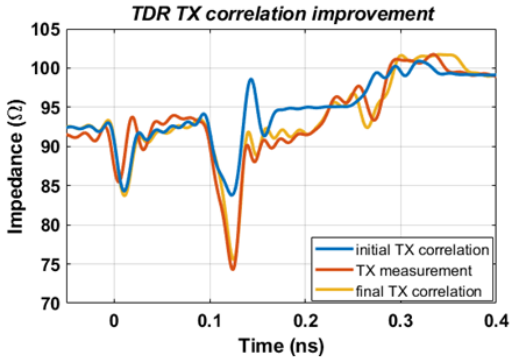


Improved correlation

- **Co-meshed simulation:**
  - Trace impedance updates
  - Improved reflowed solder ball model
- **Correlation:**
  - Still missing some IL resonance at higher frequencies
    - *Ball model approximation*
    - *Die probe calibration impact*
    - *Small uncertainty in VNA accuracy*







OUTLINE

- Optimizing a 112G test channel
- **Power delivery network**
- Channel performance
- Summary and conclusions

Power delivery

- **Goals:**
  - Power the board from single 5V supply
  - Provide option to feed each rail from its own supply
  - Neglect impact of noise on the board PDN

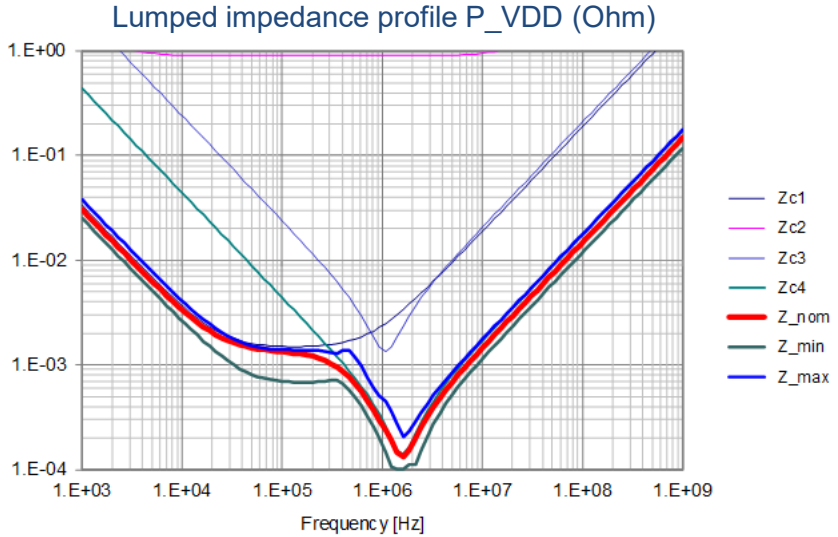
Net	DC voltage [V]	Max current [A]	Max transient current [A]	Allowed deviation [mV]	Target impedance [mOhm]
P_VDD	0.75	3	1.5	3	2
PA_VDDL	0.75	2	1	2	2
PA_VDDH	1.2	2	1	2	2
P_VDDH	1.8	1	0.5	1	2

- **Architecture:**
  - Relatively low current = cascaded linear regulators and jumper selectable supply options.

Capacitor selection

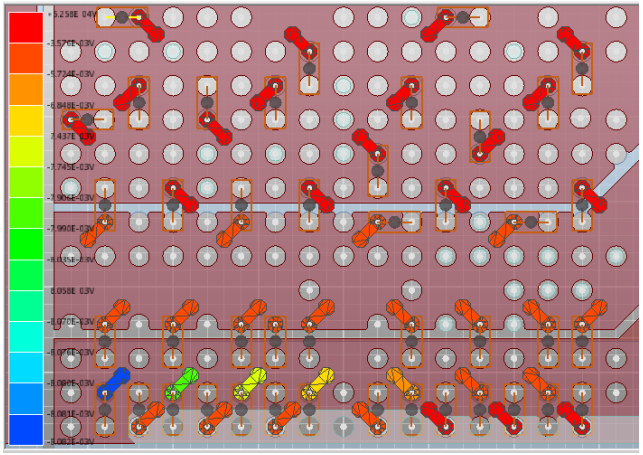
- **Big-V impedance profile:**
  - 10 uF 0402 ceramic on back of chip
    - *Single value*
    - *Directly on power/gnd pins*
  - 470 uF polymer bulk capacitors help regulator maintain low impedance
  - 22 uF ceramic at the output of the regulators for stability

Four parallel capacitor banks	C1	tol. [%]	C2	tol. [%]	C3	tol. [%]	C4	tol. [%]	
Capacitance C [F]:	4.70E-04	20	1.00E-04	20	2.20E-05	20	1.00E-05	20	Fmin[Hz]
		-20		-20		-20		-20	1.E+03
Ser. resistance ESR [ohms]:	0.015	0	0.9	0	0.004	20	0.005	20	Fmax[Hz]
		-50		-50		-20		-20	1.E+09
Ser. inductance ESL [H]:	3.00E-09	20	5.00E-09	20	1.00E-09	20	1.00E-09	20	
		-20		-20		-20		-20	Total:
Number of parts in bank:	10		1		3		36		50



PDN analysis

- **Optimize DC-drop**
  - 1 oz copper power layers
  - Hybrid solder iteration to optimize shape size



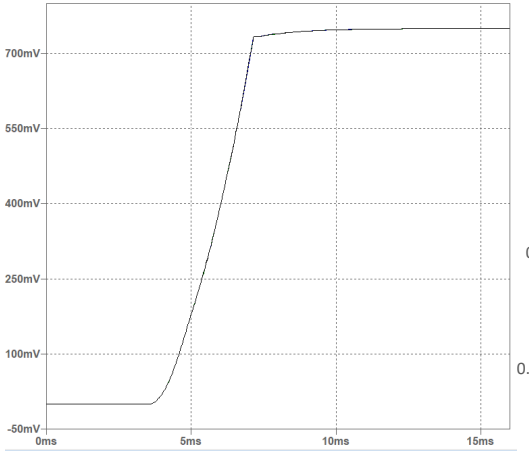
- **Minimize rail-to-rail crosstalk**
  - Avoid overlap between power planes of different nets.
  - Especially analog vs digital nets

Net	DC voltage [V]	Max current [A]	Max DC drop [mV]	Max rel. DC drop [%]
P_VDD	0.75	3	5.1	0.68
PA_VDDL	0.75	2	4.3	0.57
PA_VDDH	1.2	2	8.1	0.675
P_VDDH	1.8	1	0.53	0.03

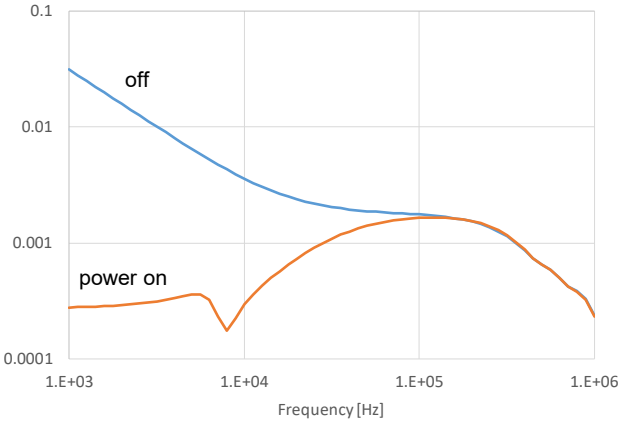
PDN analysis

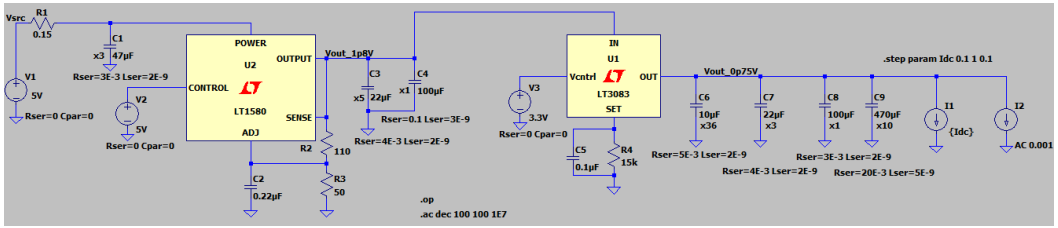
- **Spice simulations**
  - Vendor supplied models and simulator
  - Simulated startup behavior to ensure stability of cascaded regulators
  - Simulated output impedance with lumped external components

P_VDD startup (mV)



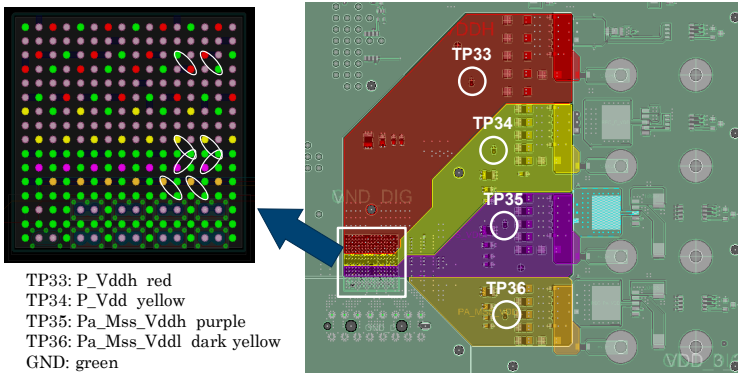
Impedance magnitude (Ohm)



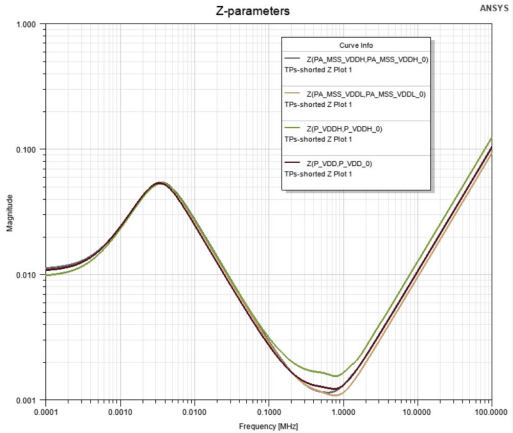


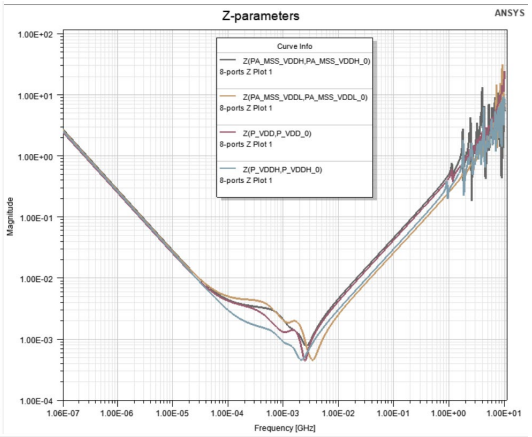
PDN analysis

- **AC impedance simulations**
  - Dedicated test points and chip's pin field location
  - Mimicking two-port shunt-through measurement
- **Two scenarios:**
  - Voltage regulator output open (right)
  - Series R-L element mimicking regulator output impedance (left)
    - *Equivalent inductance intentionally high to see bulk capacitance impedance*



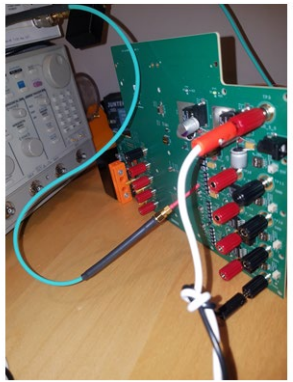
TP33: P_Vddh red
TP34: P_Vdd yellow
TP35: Pa_Mss_Vddh purple
TP36: Pa_Mss_Vddl dark yellow
GND: green



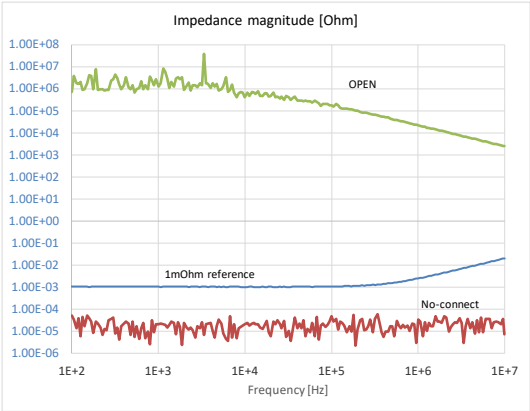


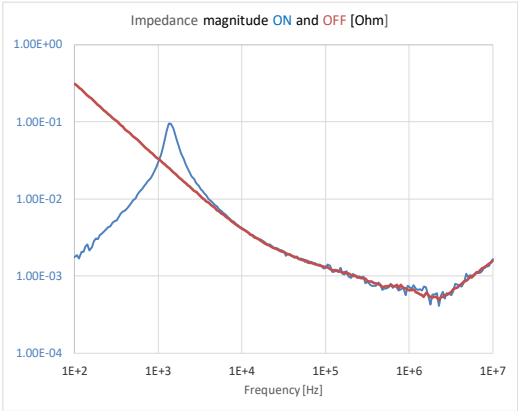
Measurements and correlation

- **Measurements:**
  - VNA with common-mode toroid suppresses cable-braid ground-loop error
  - Home-made semirigid probes
  - 100 Hz – 10 MHz measurements with and without power applied



- **Miscorrelation:**
  - DC resistance above 10 mOhm
    - *Selection jumpers simulated with zero resistance*
    - *Not shown – jumpers were shorted with solder*
  - Impedance peak at 12 kHz around 100 mOhm with minimum load current

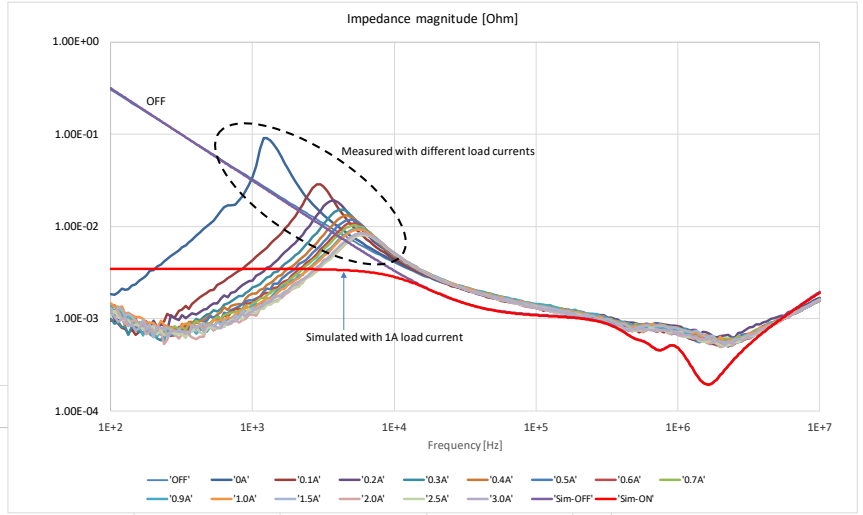


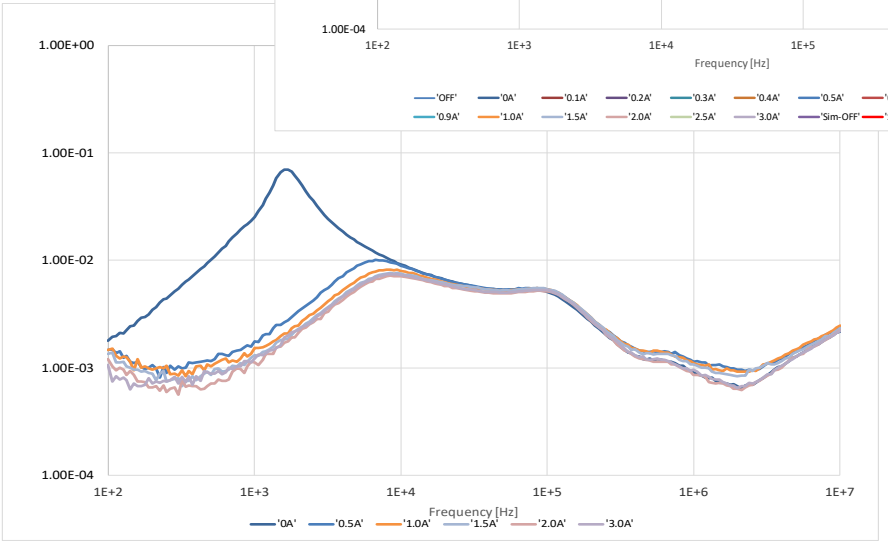


Root cause analysis

- **Investigation:**
  - Disabled upstream regulator
  - Added lossy bulk capacitors
  - Altered the regulator's feedback circuit
  - Measured evaluation board of regulator

- **Improvements:**
  - Updated regulator model's closed loop bandwidth
  - BOM change, higher ESR bulk capacitor





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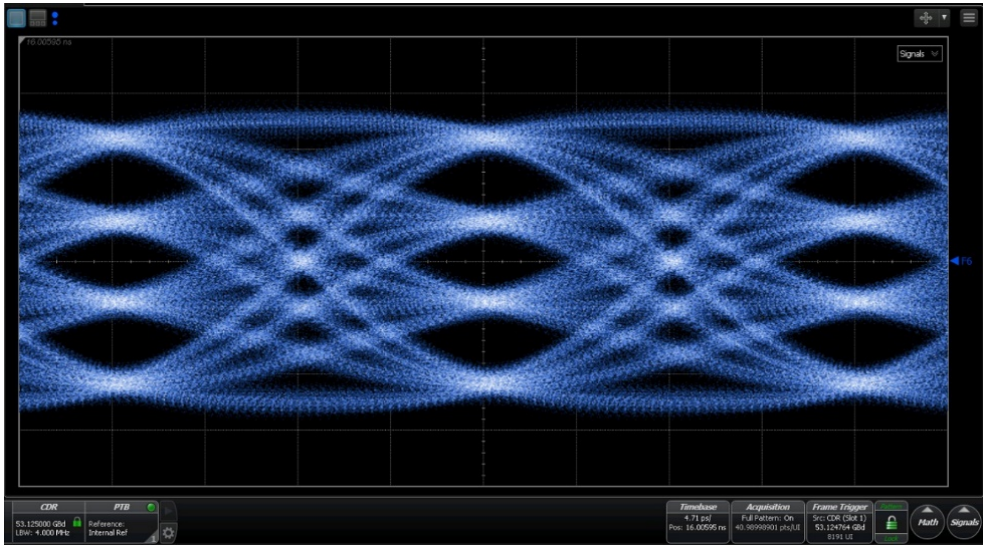
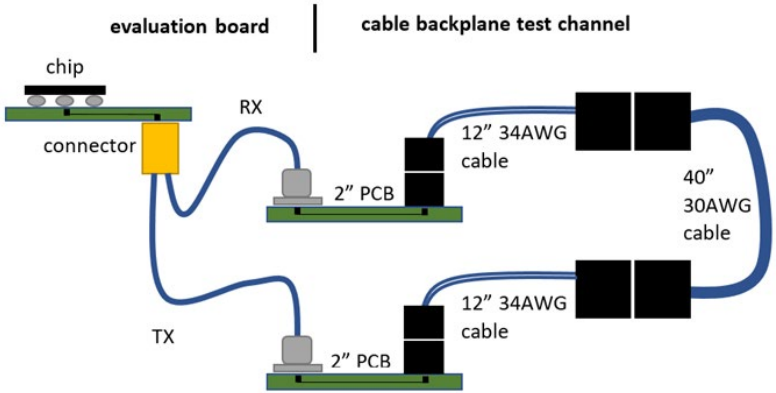
Channel performance

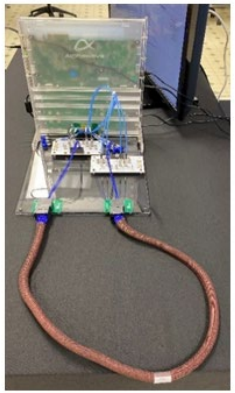
- Clean transmitter PAM4 eye diagram at 106.25Gbps
- Sampling scope with de-embedding tool

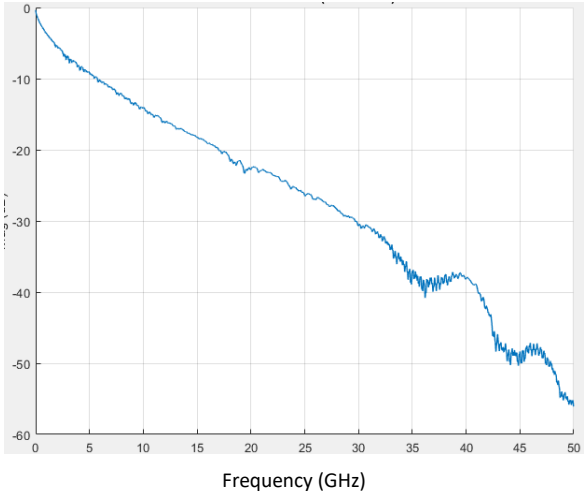


Channel performance

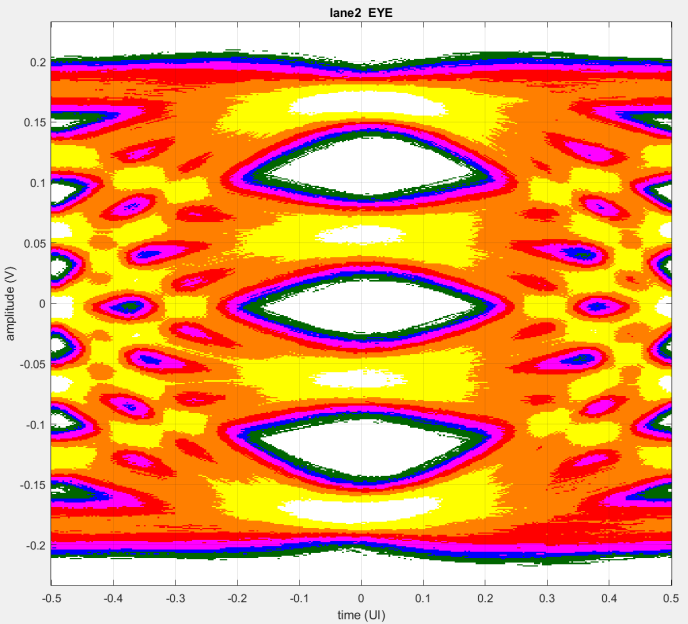
- **Cable backplane test channel**



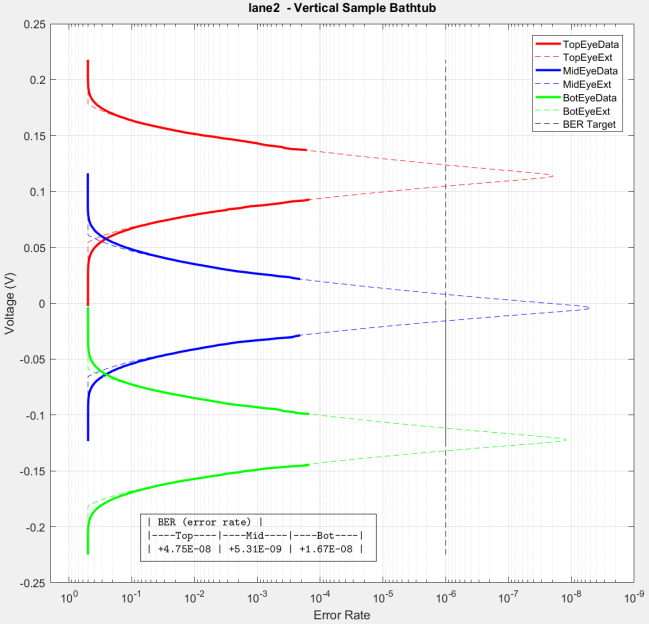




Channel performance



Receiver eye diagram



BER curve

- **Good margins**
- **BER << 1e-4**

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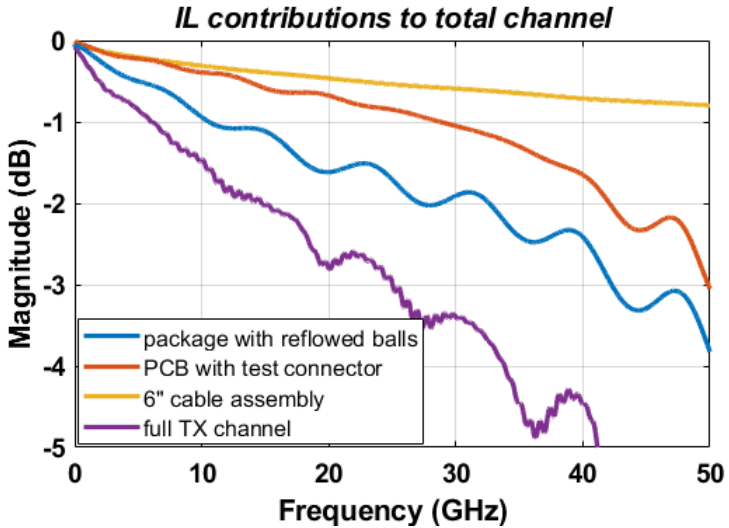
Summary and Conclusions

- **Successful design enabling 112G-PAM4 silicon evaluation**
  - Low insertion loss TX and RX design
  - Clean power distribution
  - Good channel performance
- **Important learnings**
  - Under-modeled loss contribution of the package
  - BGA package attach cannot be neglected for high data rates
  - Testing power converters prior to design



Thank you!

QUESTIONS?