DESIGNCON® 2022
WHERE THE CHIP MEETS THE BOARD

Long-Haul Inter-Domain Power Noise

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Abstract

The interaction of plane resonances in multi-layer, multiple power-domain board designs is explored for both a production as well as a test board. We will examine how the parameters of the plane cavities impact the noise coupling in consideration of both resonance frequency and Q-value. The effects will be examined in both frequency and time domains for a simple step response. Methods to reduce coupling will also be explored, including thin laminates.

Author(s) Biography

Ethan Koether earned his master's degree in Electrical Engineering and Computer Science in 2014 from the Massachusetts Institute of Technology and has spent the last seven years as a hardware engineer at Oracle. He recently began his new role as a Power Integrity Engineer with Amazon's Project Kuiper. His interests are in commercial power solutions and power distribution network design, measurement, and analysis.

Kristoffer Skytte is Senior Principal Application Engineer at Cadence focusing on chip, package, board and full system analysis. He is helping companies in Europe apply simulation tools to solve some of their toughest SI, PI and EMC related challenges in their design process. One of his interest is system level immunity/emissions and how these affect overall system performance. Kristoffer has a M.Sc.EE. degree from the Technical University of Denmark.

Joseph 'Abe' Hartman is a Principal Hardware Engineer focusing on system signal and power integrity at Oracle. Abe has worked as a signal integrity engineer at Amphenol TCS, Juniper Networks, and Enterasys. Abe also worked at General Motors. Abe holds a MS in Electrical Engineering from the University of Massachusetts-Lowell, a MS in Engineering Science from Rensselaer Polytechnic Institute, a BS in Mechanical Engineering and a BS in Electrical Engineering from Kettering University in Flint, MI.

Shirin Farrahi is a Senior Principal Software Engineer at Cadence working on SI and PI tools for automated PCB design. Prior to joining Cadence, she spent four years as a Hardware Engineer in the SPARC Microelectronics group at Oracle. She received her Ph.D. in Electrical Engineering from the Massachusetts Institute of Technology.

John Phillips is a principal application engineer with Cadence Design Systems. Prior to joining Cadence John worked at many different companies covering such diverse marketplaces as high end compute platforms and mil-aero. During his career he acquired a broad knowledge of SI, PI and EMC at chip, board and system level. John holds an MSc. Degree form Bolton University, UK. His current interests are SI/PI co-simulation and modelling for both serial and parallel interfaces.

Sammy Hindi is a Senior Principal Engineer at Ampere Computing. He has over 30 years of engineering experience, focusing on high-speed design, SerDes, Interconnect, Packaging, and forward error correction codes. Besides engineering, he enjoys reading in astrophysics and mathematics. He also enjoys biking, photography, and family life.

Mario Rotigni was born in Bergamo, Italy, in 1958 and received a diploma in Electrical Engineering in 1977. He was with the R&D Department of Magrini Galileo for 12 years working on design of process instrumentation operating in very hostile electromagnetic environments. After designing an Automatic Test Equipment for microcontrollers he joined STMicroelectronics, holding various position in the Engineering, Design, R&D in the Automotive Product Group. He is currently in charge of the EMC of Microcontroller and System on Chip for the automotive applications. He has co-authored 21 papers about EMC of Integrated Circuits for various Conferences.

Istvan Novak is a Principal Signal and Power Integrity Engineer at Samtec, working on advanced signal and power integrity designs. Prior to 2018 he was a Distinguished Engineer at SUN Microsystems, later Oracle. He worked on new technology development, advanced power distribution, and signal integrity design and validation methodologies for SUN's successful workgroup server families. He introduced the industry's first 25 μm power-ground laminates for large rigid computer boards and worked with component vendors to create a series of low inductance and controlled-ESR bypass capacitors. He also served as SUN's representative on the Copper Cable and Connector Workgroup of InfiniBand, and was engaged in the methodologies, designs and characterization of power-distribution networks from silicon to DC-DC converters. He is a Life Fellow of the IEEE with twenty-nine patents to his name, author of two books on power integrity, teaches signal and power integrity courses, and maintains a popular SI/PI website. Istvan was named Engineer of the Year at DesignCon 2020.

1. Introduction

Functional failures in a board design can often be very hard to root cause, resulting in significant time expenditure both in the lab debugging as well as potentially redesigning or modifying the design. Several papers deal with such reliability issues [1-6] which often can be traced back to either bad design practices or oversights in the power delivery network design review. Placement of switch nodes of power converters, via / plane interaction, sub-optimum component placement and selection, plane design and other noise coupling mechanisms are typically discussed in such context. In the paper [7] it was found that power domain to power domain coupling could be very significant even very far away from the aggressor point by way of multiple power cavity resonances on the board. This paper will study the power-to-power noise coupling in more detail and examine how the parameters of the plane cavities can impact the noise coupling between power domains and how frequency and Q of the resonances impact the coupling both in time and frequency domain.

After a brief summary of the structures used in this paper in section 2, section 3 examines the test instrumentations, probing and noise floor and simulation setup, section 4 looks at the noise coupling through power-structure resonances. Finally, section 5 considers the impact of stack-up and looks at some potential mitigation methods using thin laminates.

Throughout the paper, measurements, simulations and correlations will be shown on both a complex production board (from [7]) and a simple test board (from [6]) with several power-domain coupling features, like various edge coupling gap parameters and overlay-coupling scenarios.

2. Boards under test

Two boards will be used for investigating how noise can couple between power domains, a test board [6] and a large production server board [7]. The production board is a complex design where, due to placement constraints, RC termination was used to dampen resonances on the supply planes. The test board contains supply planes in different configurations allowing for both edge to edge coupling on same layer as well as adjacent power plane coupling.

In the production board, we previously found that noise couples between very distant parts of the board by way of the power domain cavities. Although the board in a populated state did not exhibit any functional issues, it spurred our interest in examining how far noise can actually spread over the board and how design decisions such as type of termination used (traditional bypass capacitors vs RC termination), number of layers, via design, plane spacing and other means of noise coupling mitigation will impact such spread. Figure 1 shows a noise distribution plot at 500MHz where the aggressor is in the lower right side of

the board. The graph shows the impact of RC termination of the power plane and is scaled such that the green areas are approximately 20dB down from the peak noise at the aggressor. Top and bottom plots are on the same scale.

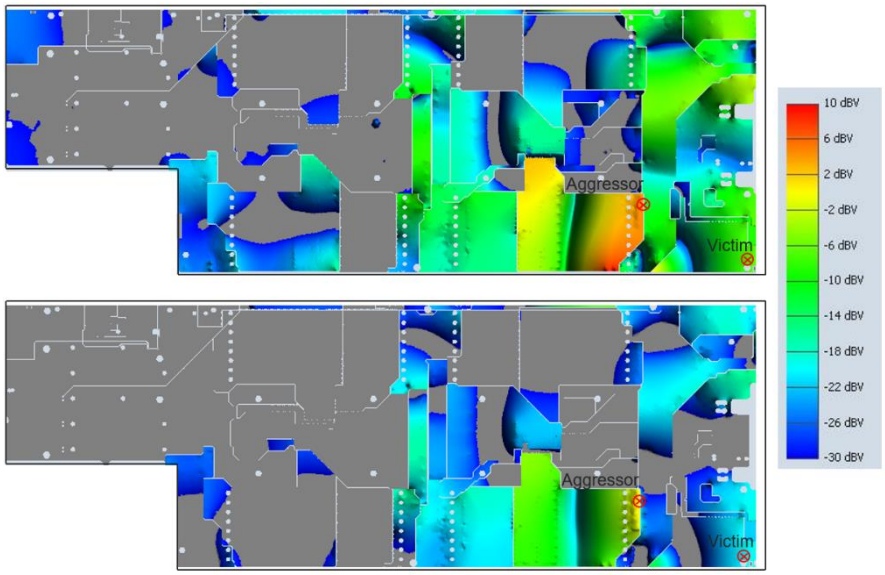

Figure 1 Spatial voltage distribution at 500MHz between power domain and neighboring ground. Any colored area is within 40dB from peak. Top image shows distribution without any decoupling on planes. Bottom image, same board but with RC termination placed on aggressor power domain. Notice how RC termination moves peak noise back to aggressor location, which is the desired behavior.

We see the noise distribution with (bottom) and without (top) RC terminations. With RC termination placed on the aggressor net, a significant reduction of coupling is seen although energy still escapes from the cavity to many of the adjacent nets. In the test all other planes were bare, i.e. no RC termination and no decoupling. If all planes on a design are well decoupled, power domain noise coupling can be reduced significantly at lower frequencies, but in the frequency range where typical-size planes exhibit modal resonances, discrete decoupling capacitors are much less effective. In very dense PCB designs with a significant number of unique voltage domains, ensuring good PDN design for all domains and under all operating circumstances is very challenging. Therefore, an appreciation of the potential design issues and ideas for avoiding them is key.

The production board will be used in this paper for showing that the long-haul coupling can exist, and we will show what impact the addition of RC terminations on the aggressor domain have on the coupling to other power domains. However, no layout variants are studied. This is where the simpler test board allows us to focus on the impact of the placement of planes, plane spacing, and how vertical overlap between them can be a source of increased coupling.

The test board is a 6-layer design on standard Eurocard dimensions of 160x100mm with 3 ground layers and 3 power layers. Two of the power planes (IN1 / IN4 – blue layers) are

split into three approximately equally sized planes, the third layer has 3 power domains with a separating ground plane between. On both sides of the board, there is an identical grid of decoupling capacitor sites and connectors. The details of the board are shown in Figure 2.

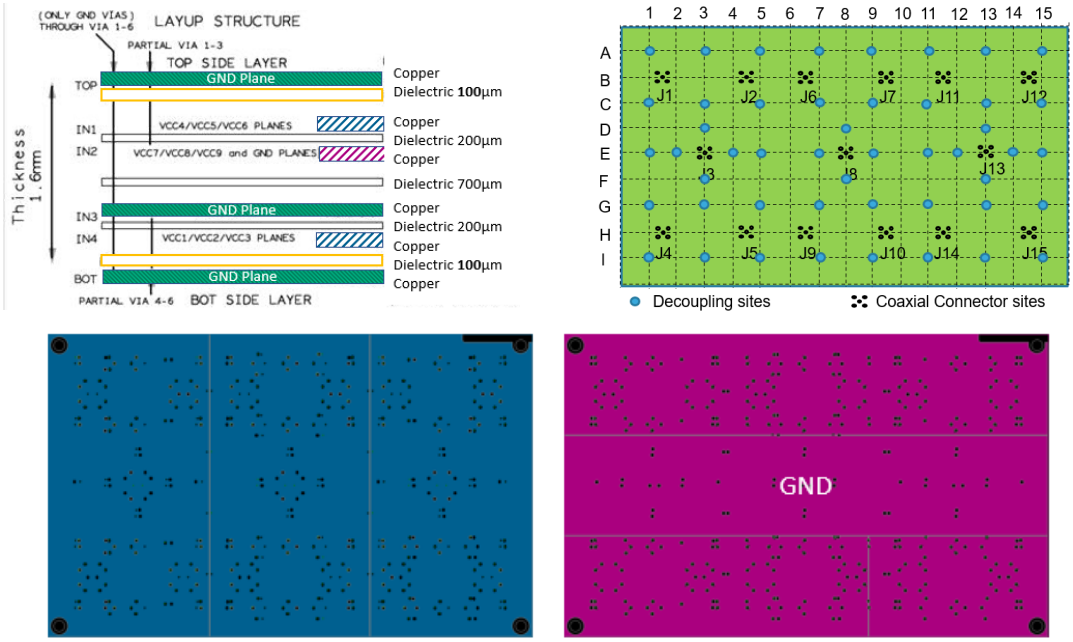

Figure 2 Stack-up construction (top left). Probing points J1-J15 and placement grid for capacitors (top right). Bottom left 3 planes as placed on IN1 and IN4 layers (bottom left) and IN2 layer (bottom right)

The bottom half of the PCB allows us to study the coupling between power domains, where coupling is between cavities and horizontal gaps between planes. The upper half is used to study what happens if planes of similar dimensions are coupled directly to other planes through vertical plane-to-plane capacitance.

Several variants of this board have been produced with different laminate thickness between top and IN1 and IN4 and bottom (marked in yellow). The nominal board has 100 µm dielectrics. The other variants use thin laminate stack-ups, often referred to as "embedded capacitance", with thicknesses of 12, 8, 6 and 3 µm from Oak-Mitsui Technologies (FaradFlex series).

3. Test instrumentation and setup

Several instruments where used for this work. For the frequency domain measurements, both logarithmic and linear frequency sweeps were used: the logarithmic sweep proved to be more useful to identify wide-band low-frequency signatures, whereas the linear sweep was useful in accurately capturing the modal resonances. To maximize the dynamic range

of the measurements, the VNA source power was set to +10 dBm and the IFBW was lowered to a value that still produced reasonable sweep speed. The first VNA [12] was used with 10 Hz IF BW, 100 kHz – 100 MHz 201-point logarithmic sweep and 2 MHz to 3000 MHz 1500-point linear sweep. The calibration was carried out using a mechanical calibration kit.

In addition, we used [14] and [15] network analyzers using 100Hz IFBW and linear sweep up to 10 GHz. [14] was calibrated with an electronic calibration kit.

3.1 Connections to the DUTs

The test boards have surface-mount SMA connector footprints connected with blind vias to specific plane shapes. There are fifteen connector sites on the top vertically lined up with fifteen connector sites on the bottom. The J1-J15 reference designators, shown in Figure 3, are used to identify the simulation and measurement locations. To reduce assembly complexity, each flavor of the test board had multiple copies and each copy had connectors populated only on one side. This was OK to do, because the top and bottom halves of the stack-up were independent. Figure 3 and Figure 4 show typical instrumentation setups used for the paper. The test board connector site allowed coaxial calibrations up to the end of the coaxial cables, which still leaves the female connector piece on the board for de-embedding. The connection was verified to be stable and producing repeatable results.

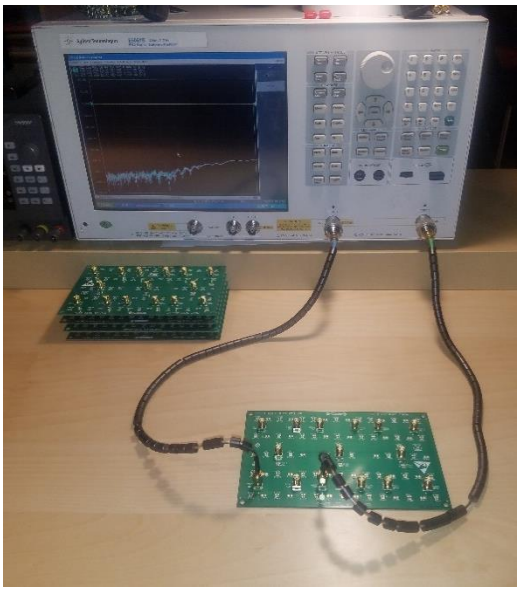

Figure 3 One of the measurement setups used for the test board.

It was more challenging to make proper connections to the production board, as it has no coaxial connectors at the chosen test locations. Measurement point selection was optimized in simulations for worst-case highest interactions. Connections to the production board were carried out in two different ways: landing on the selected locations with wafer probes

([7]) and using short open-pigtail SMA coaxial receptacles (this work). The hand-soldered coax connection is shown in Figure 5.

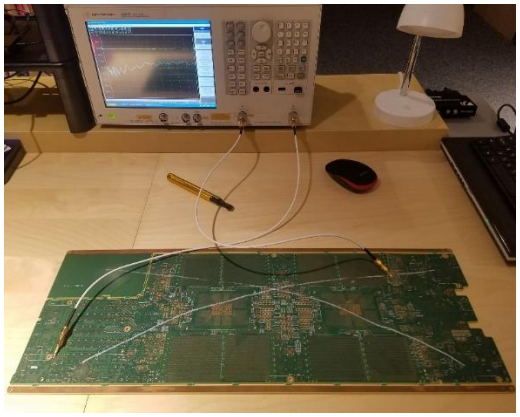

Figure 4 Production board instrumentation setup

Figure 5 Open-pigtail coax receptacle

3.2 Connector

Figure 6 shows an approximate 3D rendering of the SMA female connector that was soldered on the test board. On the right of the figure, the connector footprint is shown, which has two blind vias to the center pad and two vias each for the four ground posts.

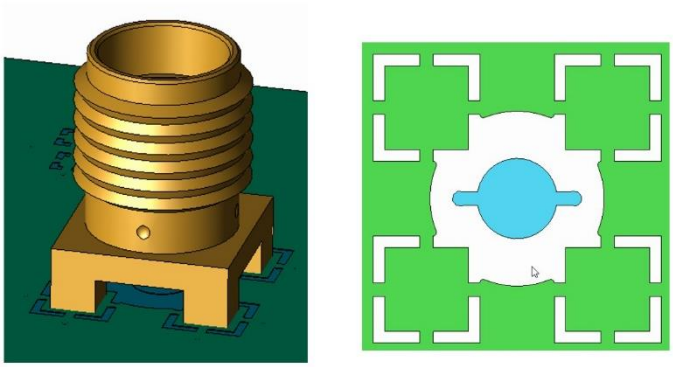

Figure 6 Connector 3D view and its footprint on the board

Although physically short, the connector model will have a significant influence on the measured results, which will be evident in some of the correlation between measurement and simulation shown later. The TDR response of the connector is shown below highlighting the mostly inductive nature of this transition on the board side.

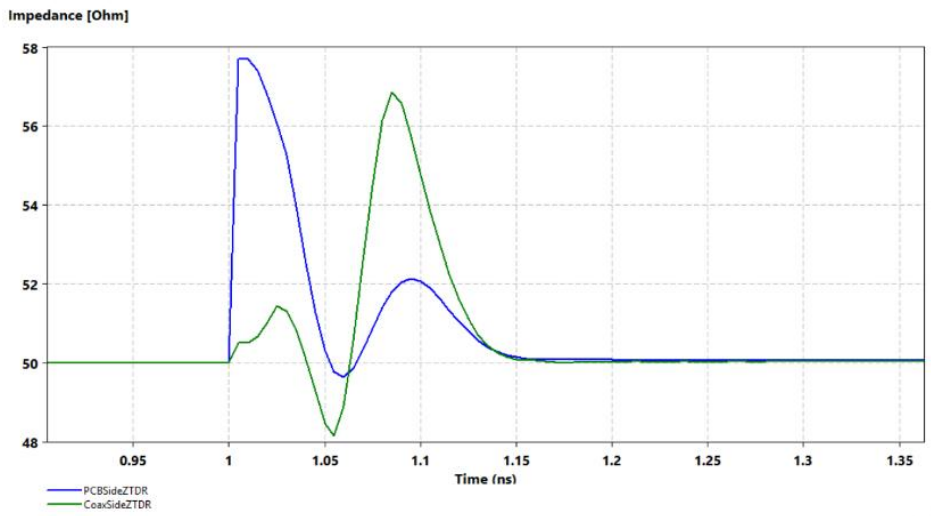

Figure 7 Simulated TDR response of the SMA receptacle with 30ps rise time. Blue is TDR at PCB launch site and green the TDR from the coax side at the mating interface.

3.3 Noise floor

The dynamic range with the VNA [12] is shown in
Figure 8. Note that the IF BW and the sweep parameters are different on the left channel, which is set to sweep up to 3 GHz and the right channel, which is set to sweep only to 100MHz.

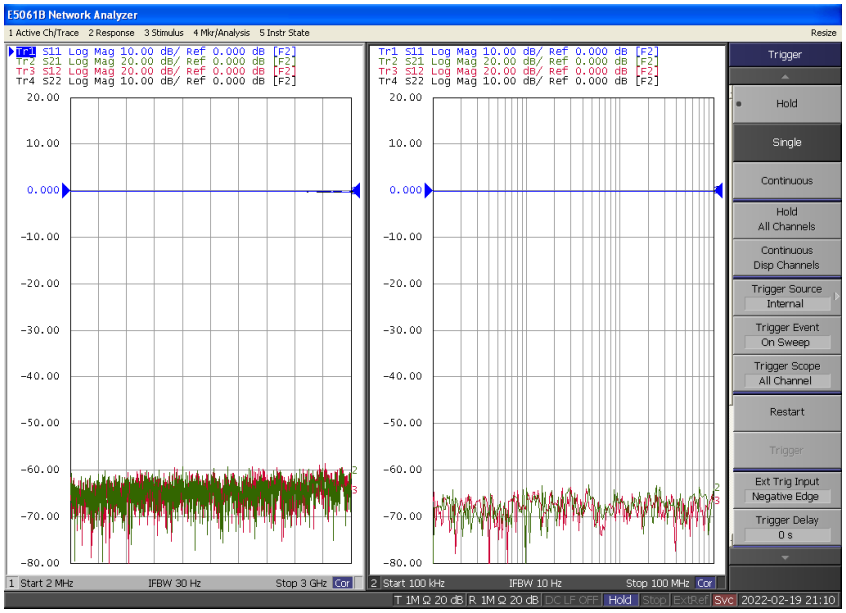

Figure 8 Noise floor with the E5061B VNA. On the left the noise floor with 3GHz sweep range and right-hand side with 100MHz sweep range.

3.4 Simulation setup and tools

Simulations were mostly performed using a hybrid electromagnetic solver dedicated to full board extractions [15]. This was used to both extract s-parameters as well as visualize the modal distributions vs frequency. To support some of the detailed design feature analysis related to the gaps in the test board and connector launch, a full 3D EM simulator was used [16]. For combining connector models onto the test board, performing TDR and for combining and comparing results, a circuit-level simulator was used [17].

4. Impact of Power Cavity Resonance on Noise Coupling in a Production Board

To investigate the potential for long haul power domain coupling on the production board, we identified two coupling scenarios. Both are between power domains not immediately adjacent to one another. In other words, coupling goes through multiple power domains before reaching the victim domain. The points identified align with the main resonance at 500 MHz on a PVDDQ domain [7]. We used the spatial noise distributions as shown in Figure 1 to identify appropriate locations for measurements considering the probing limitations with respect to pitch and accessibility. We ended up with the access points shown below.

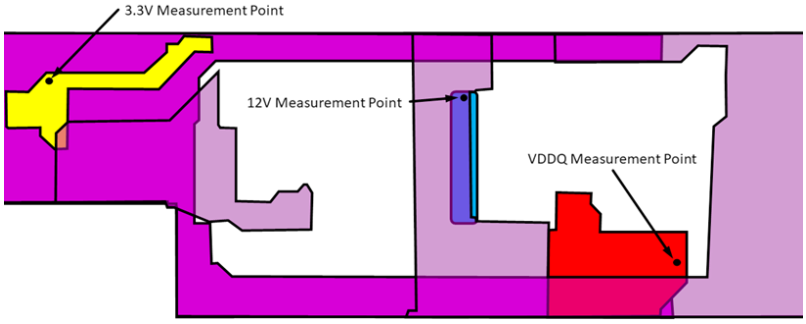

Figure 9 Illustration of production board power nets. The power net PVDDQ (red) couples to both 12V (blue) and 3V3 (yellow) through the purple multi-layer power nets. Board was used in previous studies to investigate the impact of RC termination on system noise [7].

The coupling from PVDDQ to the 12 V domain is shown in Figure 10, below.

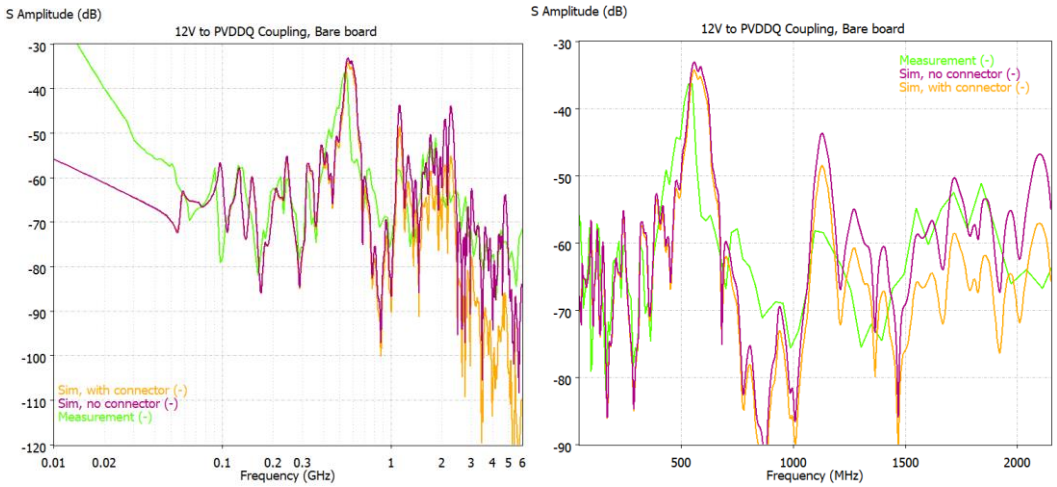

Figure 10 Measured (green) vs simulated parameter results with (yellow) and without (purple) pigtail model of connector used for measurement. Left picture is in log scale on the frequency axis and right in linear scale zoomed in around the peaks.

Considering the complexity of the board and the difficulty in obtaining precise electrical parameters for simulation, agreement is quite good in terms of resonance frequency location and peak values. In the low frequency end, we see some discrepancy for which we do not yet have a full explanation, but as the pigtail was hand soldered it is plausible that it's connectivity is causing the low frequency behavior to deviate from the expected capacitive slope. At higher frequencies trends are quite similar however we see a large variation in terms of exact resonance location and coupling levels between measurements and simulation of bare board vs simulation with a pigtail (connector) model. With the pigtail probe we expect to get good measurements to 200 – 400 MHz with gradually increasing error at higher frequencies due to the series parasitics that cannot be removed by calibration. Beyond a few GHz a more reliable probing method is required for accurate measurements. The simulation results tell us that modeling the connector launch is incredibly important for accurately capturing coupling levels at higher frequencies and coupling levels with small magnitude. In these simulations the pigtail connection is modeled/approximated as a simple coaxial line with a series inductance and contact resistance and that model itself will be bandwidth limited.

With above correlation in mind we will now switch to showing the impact of the RC termination on coupling between the domains. Only simulation results with the pigtail model are included.

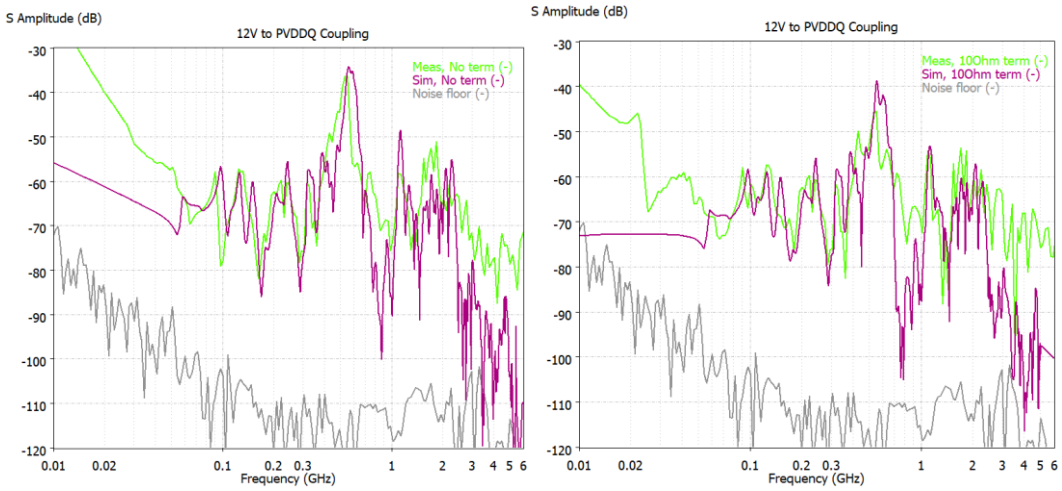

Figure 11 Measurement to simulation correlation of 12V to PVDDQ S21 coupling without (left) and with (right) RC termination components. Simulation curves include embedded SPICE model of pigtail components used for measurements. S21 measurement noise floor included.

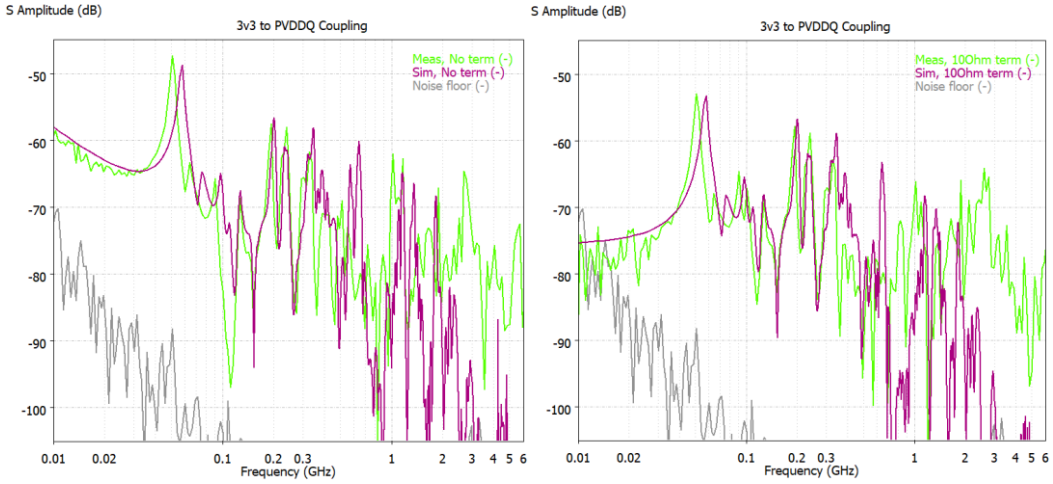

Figure 12 Measurement to simulation correlation of 3.3V to PVDDQ S21 coupling without (left) and with (right) termination components. Simulation curves include embedded SPICE model of pigtail components used for measurements. S21 measurement noise floor included.

The coupling, as in the initial results presented, shows reasonable trend correlation (again except PVDDQ to 12v for low frequency). The main peaks for both the 12V plane and the 3V3 domain are seen to be reduced by the RC termination – around 10dB for the 540 MHz resonance existing on the PVDDQ domain (see detail in Figure 13). Other resonances are generally shifted slightly in frequency having lower amplitude with RC termination than without. Some of the lower amplitude coupling peaks are significantly above those without RC termination, indicating that the RC termination is slightly shifting the exact mixing ratio of the modes on the board. Figure 13 below shows the improvement on the 12V to PVDDQ coupling by adding the RC termination – the red curve shows the reduction of the coupling using RC vs no termination (negative values means lower coupling). The peaks in the bare board case having lower coupling are highlighted to emphasize that this difference generally occurs when the coupling is lower compared to the main peaks. The reduction in coupling with RC termination is lower up to approximately 2GHz.

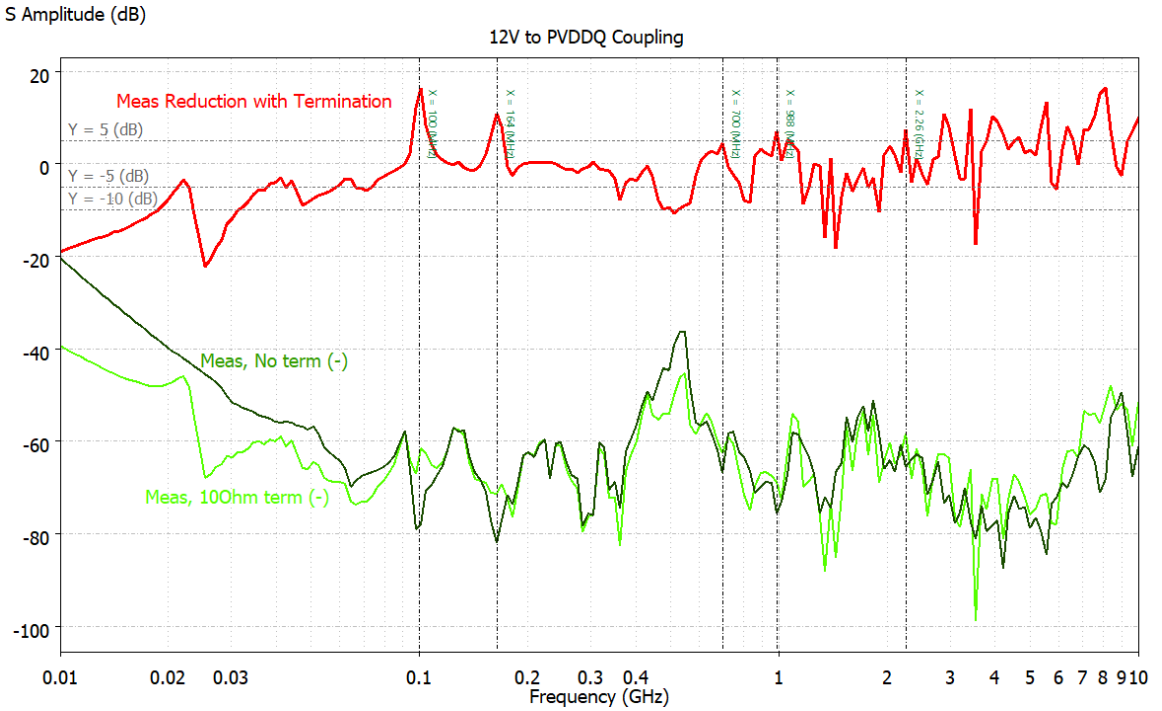

Figure 13 Comparison of measured coupling (S21) between 12V and PVDDQ domain with and without termination. The reduction in coupling by using RC termination is given by the red curve. Negative values correspond to RC termination having lower coupling.

Previously we looked at coupling from the RC terminated plane (PVDDQ) to other planes, but can the RC termination benefit plane to plane coupling on which the RC termination is not placed? In Figure 14 below we show the simulated coupling from the 12V to the 3V3 plane as well as the reduction with RC termination on PVDDQ. As is evident from this plot, the RC termination provides some reduction of coupling between planes that are far away – 4-5 dB around some of the peaks for the case examined.

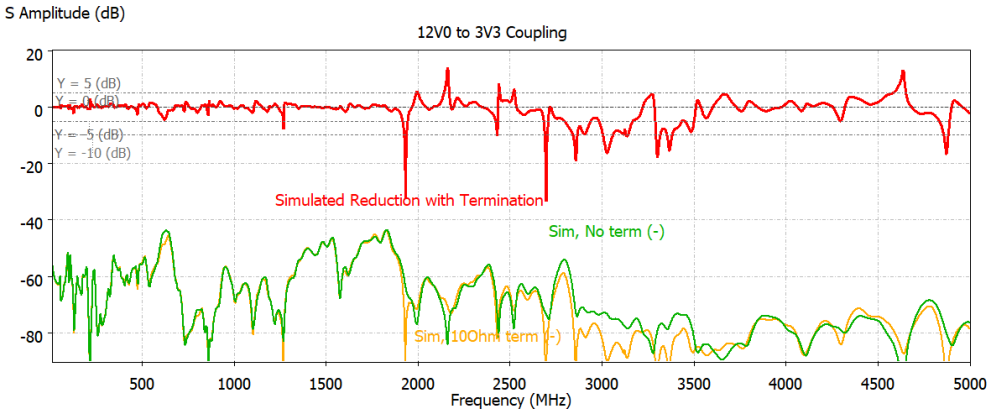

Figure 14 Coupling between domains without termination. RC termination is placed on the PVDDQ domain. Negative values correspond to RC termination having lower coupling.

The last results for the production board explore what happens if instead of RC terminations, we added only capacitors on the PVDDQ plane. Figure 15 shows in

simulation the significant improvement in low frequency noise coupling between power domains due to the addition of an RC termination.

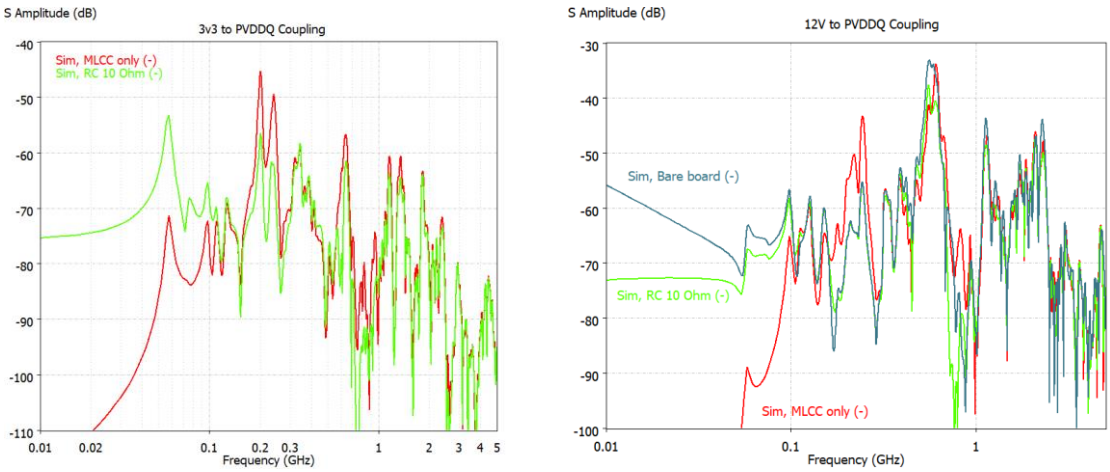

Figure 15 Simulation results showing the impact of MLCC termination vs RC termination on coupling between the 3v3 and VDDQ rails (left) and the 12V and VDDQ rails which includes also bare board behavior as reference (right).

From these plots it is clear that if the objective is mid frequency coupling reduction, using optimized RC termination can help reduce the impact of resonance peaks relative to using traditional MLCC based decoupling. In this case the RC termination reduces coupling by more than 10dB for some of the main mid frequency peaks. From approximately 2 GHz the performance of RC and MLCCs become more or less identical. We believe, that the limiting factor in terms of the bandwidth in this case is that the RC termination couldn't be placed optimally meaning that relatively high amounts of inductance is in the connection both between the R and C elements as well as to the planes. RC termination will increase coupling in the very low frequency end, and in the case of the 3V3 plane, even significantly increases the coupling around 30MHz. Improving the mounting of the RC termination [7] could help avoid such peaking with the caveat that a high mounting inductance in the RC termination can lead to increased coupling as well. Notice also that placing MLCC capacitors can actually increase mid-frequency coupling compared to no decoupling at all! This is due to the MLCC resonating with the planes due to the relatively low loss of the MLCCs.

In the cases described above we are not showing the coupling between the 12V and 3V3 planes as there was hardly any noticeable difference between decoupling using MLCCs and using RC termination.

5. Inter-domain PDN Coupling in Test Board

5.1 Expectations related to stack-up variations

Before analyzing in-depth the inter-domain PDN coupling for the test board, we start off by setting some expectations concerning one of the main aspects investigated in this paper – changing substrate heights and the impact of thin laminates on noise coupling. We will

examine the topic first for coupling between points on the same power domain. Figure 16 shows the impact of laminate thickness on coupling between the center and edge of the same power plane. The results shown are for the bottom half of the test board where we only have power planes on a single layer and ground on both sides.

Overall, we see nice agreement in the predicted amplitudes and resonance frequencies with some remaining discrepancy likely caused by the lack of full stack-up details (εr and height) for all the boards. We see almost 40 dB reduction in the coupling amplitude in the capacitive region when reducing outer layer laminate thickness from 100 µm to 3 µm. The thinner laminates both give rise to increased capacitance as well as reduced board inductance, causing a significant shift in the first modal resonance dominating the coupling from center to edge (f20: m=2,n=0). We also see a significant decrease in the peak impedance at resonances including f20 and an overall decreased Q.

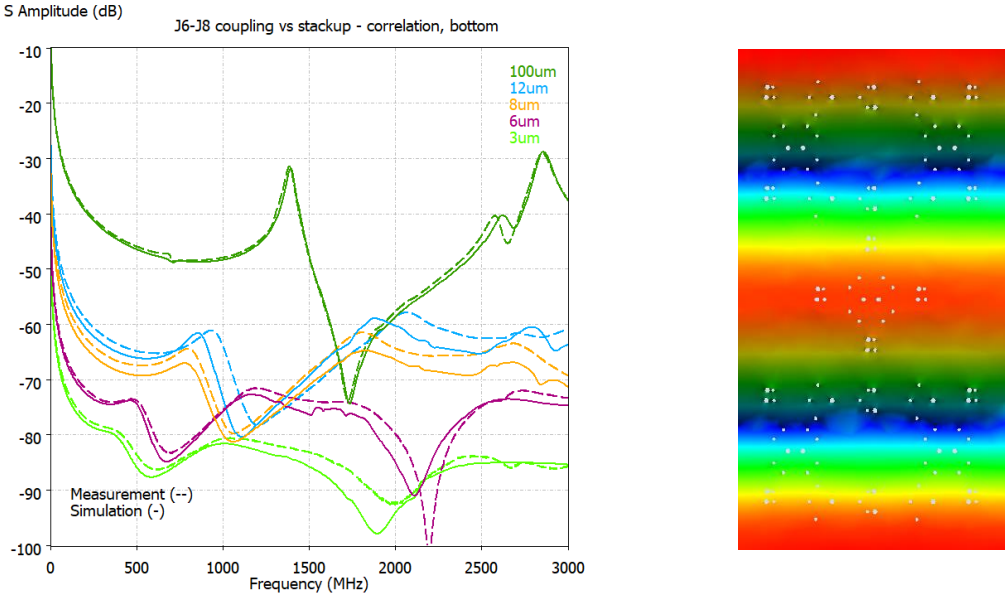

Figure 16 Impact of laminate thickness on coupling and correlation with measurements (left), the first modal resonance, f20, dominating the coupling around 1400MHz for the 100µm setup (right)

The reduction in Q of the peaks can be attributed to the thinner dielectric. This is evident when reviewing the loss components of a cavity resonator [8, 9]

$$\frac{1}{Q_t} = \frac{1}{Q_{rad}} + \frac{1}{Q_{sw}} + \frac{1}{Q_c} + \frac{1}{Q_d}$$

The total Q is thus a function of loss from radiation, Q_{rad}, surface wave modes, Q_{sw}, conductor losses, Q_c, and the dielectric losses, Q_d. Neglecting radiation and surface wave modes, valid when plane distance is $h<<\lambda$ [10, 11], we have the conductor and dielectric losses remaining. The Q associated with the dielectric loss is given as

$$Q_d = 1/\tan\delta$$

And the Q related to conductor losses being the ratio of dielectric height to skin depth

$$Q_c = h/\delta = h\sqrt{\pi f \mu \sigma}$$

We see that the reduced peaks are directly related to the reduced distance between the planes. The decreased losses in the dielectrics when going to thinner layers leads to quite large increase in the dielectric Q which means that it will be the conductor related losses that will dominate the total Q.

Stackup [um]	Material	εr	tanδ	Qd	Qc	Qt	f20 MHz (J6-J8)
100	FR-4	4.5	0.02	50	84	31	1390
12	FaradFlex MC12TM 12um	10	0.015	67	10	9	932
8	FaradFlex MC8TM 8um	10.5	0.02	50	7	6	910
6	FaradFlex MC6TM 6um	21.7	0.008	125	5	5	633
3	FaradFlex MC3TM 3um	21.7	0.008	125	3	2	633

Table 1 Stack-ups investigated for the test board with electrical properties, calculated Q values at 3GHz and predicted f20 resonance frequency from the 100 µm stack-up.

As Qc is frequency dependent, the above table values are given for the highest frequency of interest in this investigation (3 GHz). Reducing frequency would increase skin-depth and thus lower Qc which would in turn reducing the total Qt. The values quoted are for pure annealed copper. A lower conductivity would result in slightly reduced Qt from that expressed above. If you were to extract the Q values from the above graphs you would find that the Q value from simulation and measurements are actually below what is predicted from purely considering Qc and Qd terms, e.g. Q for 100µm stack-up at f20 ~15 and for 12µm Q ~4. The difference between predicted and actual Q is not yet fully understood, but there may be a couple of reasons including a) the Q_c term is derived for pure rectangular cavity b) the non-idealities of the planes and the loading of the neighboring planes loads the cavity and adds more loss.

The coupling change between the stack-ups at low frequencies is due to the embedded capacitance increase which is proportional to εr and inversely proportional to the thickness. The inductance reduction of the planes is directly proportional to h, so the change in resonance frequency of the peaks will scale as

$$\frac{f_1}{f_2} \propto \sqrt{\frac{\varepsilon_2}{\varepsilon_1}}$$

The table above shows the predicted f20 frequencies based on the measured f20 peak from the 100 µm stack-up. The predicted f20 resonance frequencies are in good agreement with the observed results. The same scaling applies to all other resonance frequencies giving a quick way of estimating the impact of changing the dielectric material and dielectric heights for both Q and change in resonance frequency.

5.2 Coupling between adjacent power nets

The three planes in the bottom part of the test board allows us to investigate coupling between planes as a function of horizontal spacing of planes on the same layer. This was extensively investigated in [6] and it will only quickly be recapped here for reference. The two planes on layer IN4 are separated with the production min spacing of 125µm and the last domain is separated by a gap of 10x min spacing.

A general routing guideline is to increase gap between planes for isolation purposes, this experiment helps quantify that. The Figure 17 below shows the coupling between the connectors placed on the center of the planes through the narrow gap, through the wide gap and also between non-adjacent power planes

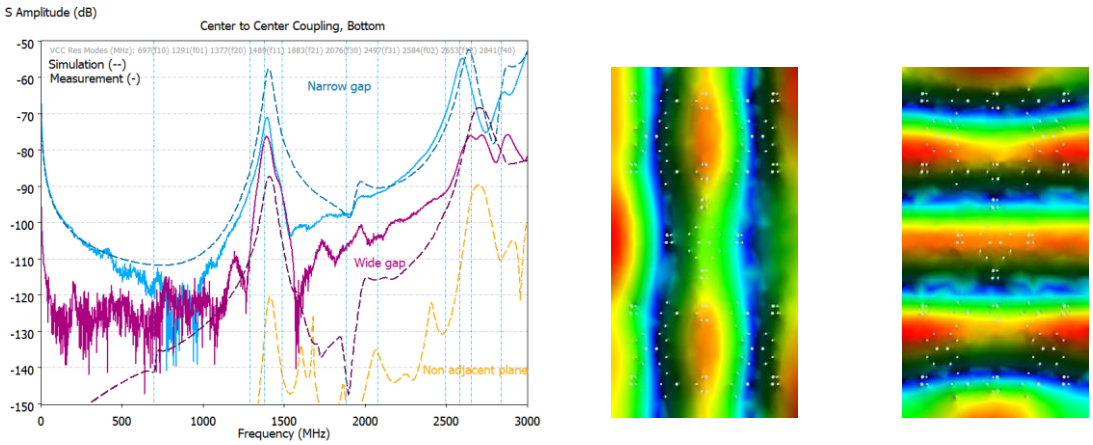

Figure 17 Coupling between connectors on center of planes on bottom side. The vertical lines represented the resonance modes from the unloaded single plane resonance. Results for nominal 100µm stack-up. Three modes dominate coupling f20, shown earlier, and f02 (mid) and f40 (right).

As expected, increasing the gap lowers the coupling and non-adjacent power planes have even less coupling. The coupling between the connectors increases around resonances. The unloaded cavity resonances for a single VDD plane are shown with vertical dotted lines. We see that the loaded resonance frequencies are slightly shifted upward. Finally, in the frequency band of interest, there are 3 modes that have peak at or near the center point on the planes, f20, f02 and f40. f20 was shown earlier while f02 and f40 are shown in above. The modes correspond to peak coupling values.

We see quite some discrepancy in the predicted coupling levels while resonance frequencies are in good agreement, even on some of the non-dominant modes. Measurements shows 5dB coupling difference between narrow and wide gap for the f20 mode, while simulations show much more sensitivity to changes in gap size. The exact geometry and material properties are believed to have a major impact here. Some sensitivity studies where done indicating this, but further work is required if better measurement to simulation correspondence is required.

However, the interesting thing to note here is if very narrow spacing between planes are used in a design, it becomes very sensitive to a host of production related variations, making coupling around resonances potentially vary unpredictably. To minimize sensitivity to such variation it is recommended to ensure good spacing (gap) between adjacent planes whether those are used for grounding or not.

5.3 Broadside coupling on the test board

The plane configuration investigated above appear on layer IN1 as well. In this case the plane separation is 125 µm, i.e. minimum gap spacing. The spacing to the ground above IN1 is 100µm (nominally), and IN2 has another power layer 200 µm away. The two power planes are thus facing each other which is not an uncommon stack-up configuration, as used in the production board we discussed earlier. What is the influence of having such adjacent non-decoupled power planes on coupling? Figure 18 below shows two configurations, from one edge of a supply plane to the edge of another supply plane as well as from center to center of different supply planes

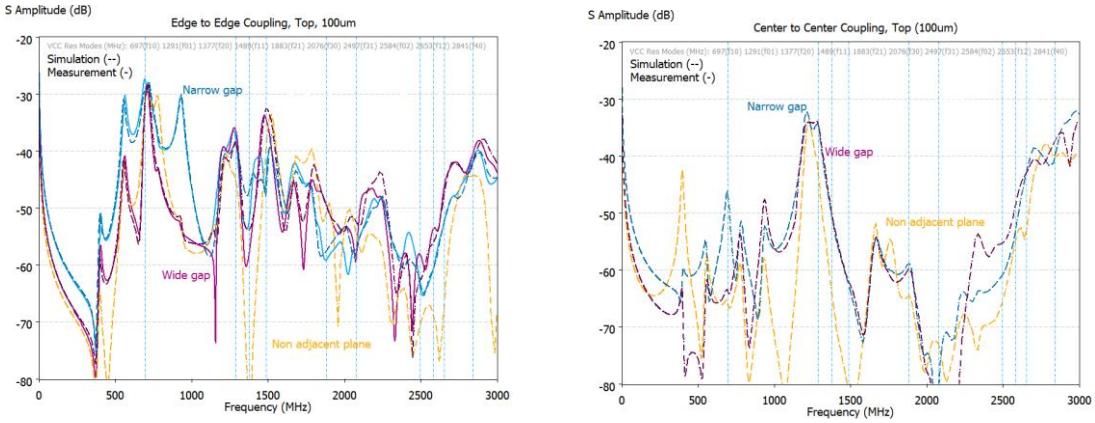

Figure 18 Top side coupling for 100µm stack-up for a wide and narrow gap and coupling between non-adjacent planes. Left edge to edge connector coupling. Right center to center coupling

As is evident from above, without decoupling on adjacent planes, the coupling level increases significantly over having adjacent ground planes. Also, we see very little difference between wide and narrow coupling at the peaks indicating that the gap coupling is not dominating, rather it's the direct plane to plane coupling which determines the overall coupling level. In other words, the sensitivities that we saw earlier due to gap modeling can be ignored for broad side coupling scenario and agreement between measurement and simulation is very good. As we will see next, sensitivity due to gap coupling could re-appear as we decrease stack-up thickness but because we are only changing stack-up thickness, the gap size relative to plane spacing becomes gradually less important as the planes couple tighter to their reference. Along with this the lower Q will help eliminate the impact of resonances altogether.

Note also, that at several frequencies, noise jumps between multiple power domains and the level of coupling at some frequencies is actually higher than adjacent plane pairs. This is highly dependent on the mode energy distributions on the different planes in the cavities. For instance, the peak in the center to center coupling around 400 MHz is due to a mode on the adjacent power layer. Another aspect to be aware of, is that the modes appearing in the impedance plots are in part the loaded resonance of the single planes, but also at times where the entire power plane behaves as if one big plane. For instance, the resonance at 1182 MHz is the f20 mode of the entire board.

Figure 19 below shows the center to center coupling with decreased stack-up thickness along with the coupling between non-adjacent planes. As is evident, decreasing the stack-up height is a very effective way to lower coupling between both adjacent and non-adjacent power planes. The achieved reduction for most frequencies going from a 100 µm stack-up to 12 µm is in excess of 30 dB. Further stack-up height reduction lowers the coupling even further. Note the reduced Q and resonance frequencies. The reduction in Q comes directly from the stack-up height reduction while the shifted resonances are due to the different εr of the materials.

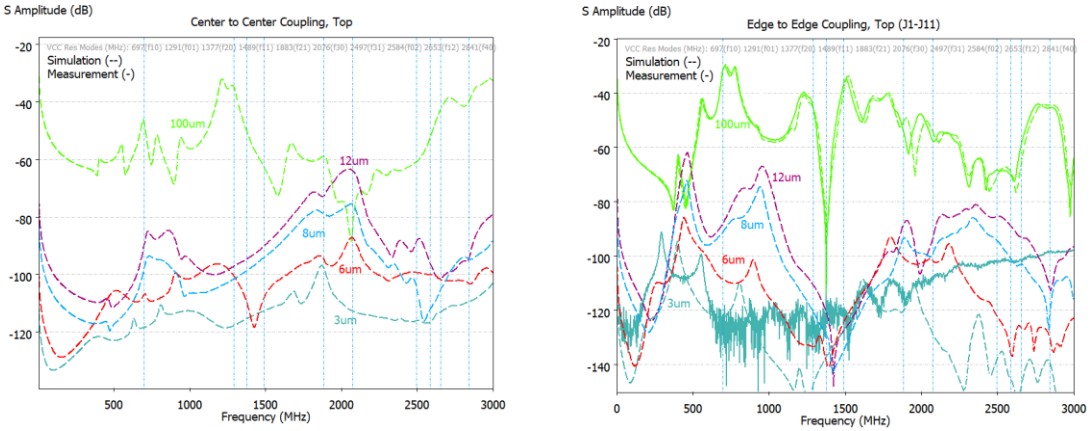

Figure 19 Center to center coupling (J3-J8) vs stack-up. Only sim results available (left). Right edge to edge coupling between non-adjacent power domains (J1-J11).

5.4 Long haul coupling on the test board

The final aspect we will investigate on the board is that of long haul / coupling between non-adjacent planes. We saw previously that coupling can spread between distant planes, and that plane resonances occur that cannot be predicted by looking at the shape of the individual planes. Instead, the entire layer appears as one plane – the example brought forward was the case of the resonance at 1182 MHz (100 µm stack-up) which is actually the f20 resonance of the entire board. This mode is shown below in Figure 20 where we are plotting the normalized energy distribution between IN1 and its corresponding GND (top side), between IN2 and its ground and finally between the two adjacent power planes.

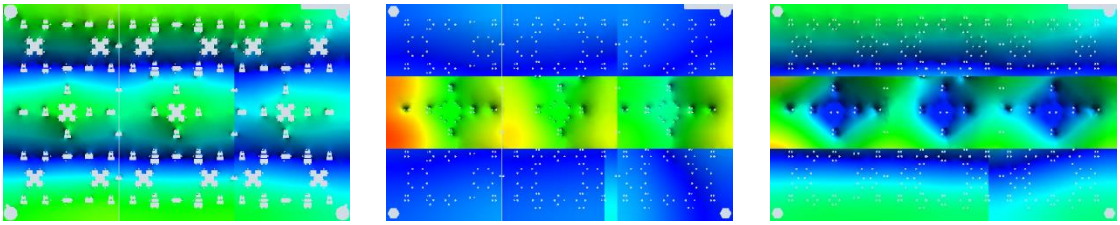

Figure 20 Normalized energy distribution between plane cavities on top side of test board for 100µm stack-up @ 1182MHz. GND on top layer to IN1 (left), power to power IN1 to IN2 (mid), IN2 to inner GND layer (right). Red color corresponds to peak energy, green roughly ½ peak power and blue 0 energy.

It's is clear that the f20 mode exists on both power domain planes and that the GND routing on layer IN2 is actually playing an important part in this resonance due to its non-ideal stitching to the other grounds. The GND defect was added on purpose here because it is a very common trait of designs – stitching vias may be missing or placed in a regular pattern but with insufficient spacing.

A very common practice to get noise isolation is to place sensitive power domains very far away from the noisy power domains. The above has shown that this may not be enough – even with well decoupled planes, as resonances at higher frequencies, can spread out between multiple domains across the system. The GND on IN2 again is a good example. The points where the normalized noise is close to zero represents an ideal decoupling scenario. Wherever decoupling is present, plane noise is minimized, but placement of decoupling doesn't guarantee resonances to be completely suppressed.

The key points to keep in mind here are

1. Spacing planes far apart is not enough to guarantee isolation, full plane cavity resonances can cause a very drastic increase in coupling
2. Ground planes can be a vehicle of noise coupling just like any other plane. Appropriate stitching is required to the ground to behave as such and to minimize cavity resonances
3. As with point #2 the same applies for power planes except "stitching" here means decoupling / RC termination

6. Conclusions

It has been demonstrated on the two boards examined, that cavity resonances can cause significant coupling across multiple power domains, whether those planes are on the same layer or adjacent layers in the stack-up. We have demonstrated that RC termination can be used to quiet down a supply plane. RC termination improves not only the plane to which it is connected, but also can lower coupling from the terminated plane to other domains as well as between domains that do not necessarily have RC termination themselves. Along the same lines, coupling a power plane more tightly to its neighboring ground makes the design less susceptible to noise induced from the other planes whether those are placed on the same layer or an adjacent layer in the stack-up.

A key indicator to the risk of excessive coupling is expressed by the Q of the cavity. As shown, thin laminates not only have the benefit of higher capacitance and lower inductance, generally very good traits for a PDN design, but can also lower cavity Q and reduce noise coupling in the PDN. Opting for a thin laminate must include consideration of the design's dielectric breakdown requirements, manufacturing, and production costs for the final PCB. As shown in this paper, the use of thin laminates is a potentially very useful tool to lower coupling both within the same power domain as well as to lower coupling across multiple power domains – even when the decoupling design may be less than optimal. It is interesting to keep the aspect of lower coupling within a given power domain in mind, because it implies that thinner layers not only help improve isolation between different power domains but also allows multiple power domains to be combined into one domain while still achieving isolation requirements. This in itself could be an important driver for reducing overall system cost and implementation complexity.

Further work is required in the area of PDN quality factor, multi-cavity resonances and understanding the impact in time domain to help quantify how this impacts a full system.

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