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Santa Clara Convention Center

Long-Haul Inter-Domain Power Noise

Ethan Koether, (Amazon – Project Kuiper)

Kristoffer Skytte (Cadence), Abe Hartman (Oracle Corporation)
Shirin Farrahi (Cadence), John Phillips (Cadence),
Sammy Hindi (Ampere Computing Inc.),
Mario Rotigni (STMicroelectronics),
Istvan Novak (Samtec)

Authors

Ethan Koether

Power Integrity Engineer, Amazon – Project Kuiper

koether@amazon.com

Ethan Koether earned his master's degree in Electrical Engineering and Computer Science in 2014 from the Massachusetts Institute of Technology and has spent the last seven years as a hardware engineer at Oracle. He recently began his new role as a Power Integrity Engineer with Amazon's Project Kuiper. His interests are in commercial power solutions and power distribution network design, measurement, and analysis.

Kristoffer Skytte

Senior Principal Application Engineer, Cadence

kskytte@cadence.com

Kristoffer Skytte is Senior Principal Application Engineer at Cadence focusing on chip, package, board and full system analysis. He is helping companies in Europe apply simulation tools to solve some of their toughest SI, PI and EMC related challenges in their design process. One of his interest is system level immunity/emissions and how these affect overall system performance. Kristoffer has a M.Sc.EE. degree from the Technical University of Denmark.

Authors

Abe Hartman

Principal Hardware Engineer, Oracle Corporation

abe.hartman@oracle.com

Joseph 'Abe' Hartman is a Principal Hardware Engineer focusing on system signal and power integrity at Oracle. Abe has worked as a signal integrity engineer at Amphenol TCS, Juniper Networks, and Enterasys. Abe also worked at General Motors. Abe holds a MS in Electrical Engineering from the University of Massachusetts-Lowell, a MS in Engineering Science from Rensselaer Polytechnic Institute, a BS in Mechanical Engineering and a BS in Electrical Engineering from Kettering University in Flint, MI.

Shirin Farrahi

Senior Principal Software Engineer, Cadence

shirinf@cadence.com

Shirin Farrahi is a Senior Principal Software Engineer at Cadence working on SI and PI tools for automated PCB design. Prior to joining Cadence, she spent four years as a Hardware Engineer in the SPARC Microelectronics group at Oracle. She received her Ph.D. in Electrical Engineering from the Massachusetts Institute of Technology.

Authors

John Phillips

Principle Application Engineer, Cadence

phillips@cadence.com

John Phillips is a principal application engineer with Cadence Design Systems. Prior to joining Cadence John worked at many different companies covering such diverse marketplaces as high end compute platforms and mil-aero. During his career he acquired a broad knowledge of SI, PI and EMC at chip, board and system level. John holds an MSc. Degree form Bolton University, UK. His current interests are SI/PI co-simulation and modelling for both serial and parallel interfaces.

Sammy Hindi

Senior Principal Engineer, Ampere Computing Inc.

sammy@amperecomputing.com

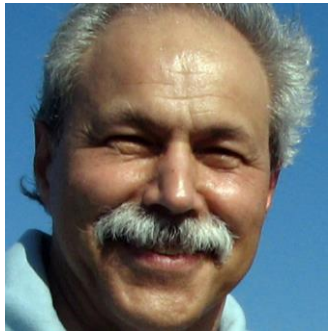
Sammy Hindi is a Senior Principal Engineer at Ampere Computing. He has over 30 years of engineering experience, focusing on high-speed design, SerDes, Interconnect, Packaging, and forward error correction codes. Besides engineering, he enjoys reading in astrophysics and mathematics. He also enjoys biking, photography, and family life.

Authors

Mario Rotigni

SoC EMC Manager, STMicroelectronics
mario.rotigni@st.com

Mario Rotigni was born in Bergamo, Italy, in 1958 and received a diploma in Electrical Engineering in 1977. He was with the R&D Department of Magrini Galileo for 12 years working on design of process instrumentation operating in very hostile electromagnetic environments. After designing an Automatic Test Equipment for microcontrollers he joined STMicroelectronics, holding various position in the Engineering, Design, R&D in the Automotive Product Group. He is currently in charge of the EMC of Microcontroller and System on Chip for the automotive applications. He has co-authored 21 papers about EMC of Integrated Circuits for various Conferences.



Istvan Novak

Principal Signal and Power Integrity Engineer, Samtec
istvan.novak@samtec.com

Istvan Novak is a Principal Signal and Power Integrity Engineer at Samtec, working on advanced signal and power integrity designs. Prior to 2018 he was a Distinguished Engineer at SUN Microsystems, later Oracle. He worked on new technology development, advanced power distribution, and signal integrity design and validation methodologies for SUN's successful workgroup server families. He introduced the industry's first 25 µm power-ground laminates for large rigid computer boards and worked with component vendors to create a series of low inductance and controlled-ESR bypass capacitors. He also served as SUN's representative on the Copper Cable and Connector Workgroup of InfiniBand, and was engaged in the methodologies, designs and characterization of power-distribution networks from silicon to DC-DC converters. He is a Life Fellow of the IEEE with twenty-nine patents to his name, author of two books on power integrity, teaches signal and power integrity courses, and maintains a popular SI/PI website. Istvan was named Engineer of the Year at DesignCon 2020.

Outline

- Power Plane Resonances
- Plane Termination
- Production Board Power Plane Coupling
- Test Board Investigation
- Conclusion

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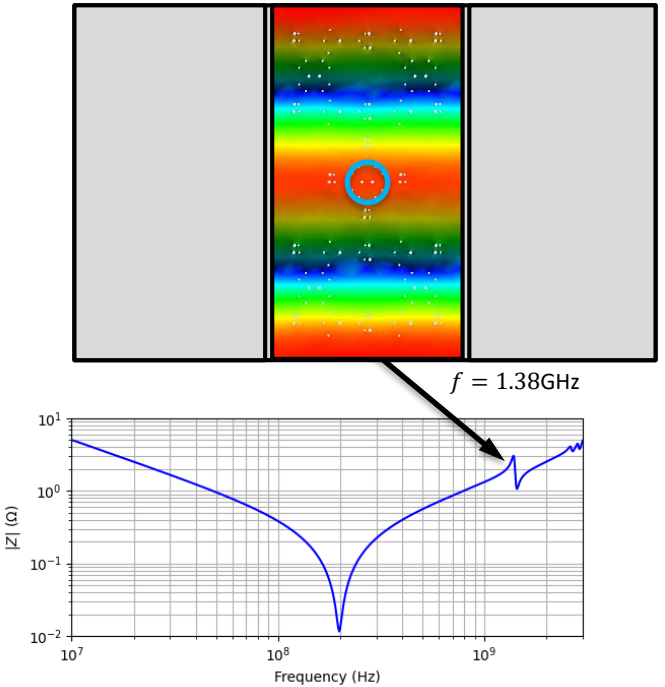
Power Plane Resonances

- Spatially motivated resonances occur when the wavelength of excitation approaches same order of magnitude as dimensions of power plane
- Power plane resonant modes in modern system boards often in 10 MHz – 10 GHz range.
  - Midfrequency noise from signals, power converters, clocks can excite power plane resonances
- Often power plane decoupling establish boundary conditions such that resonances are moved around frequency
- Impact on system integrity at resonant frequency of power plane:
  - Power-to-signal coupling – *increases*
  - Signal-to-signal coupling – *increases*
  - Power-to-power coupling – *increases*



Simulated impedance seen from connector (blue circle) at center of cavity composed of power and gnd planes with corresponding resonant modes' spatial plots.

Outline

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- **Plane Termination**
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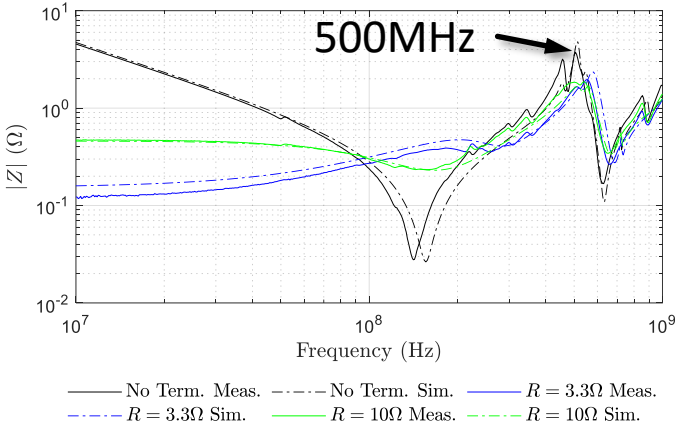
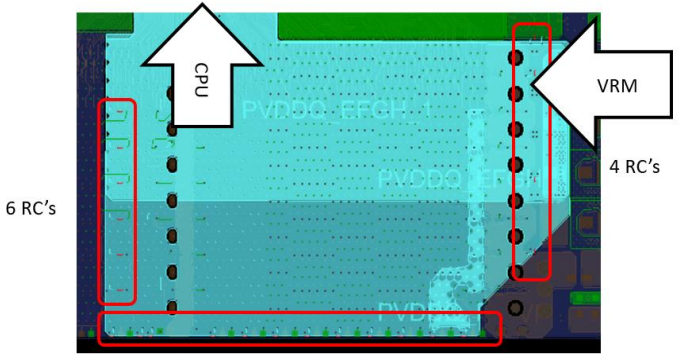
Power Plane Termination

- Terminating power plane (like transmission line) with RC series elements to change boundary conditions such that resonance cannot be sustained and cavity energy dissipated
  - Series capacitor prevents DC power loss
- On example production board 22 RC termination elements lined perimeter of otherwise bare power plane
  - Termination reduced self-impedance Q's significantly
- Often termination deemed unnecessary in designs leaving open the question of to what extent does a power plane resonance impact a system?





Bare power plane terminated on 3 sides by 22 termination R-C elements to mitigate power plane resonances.

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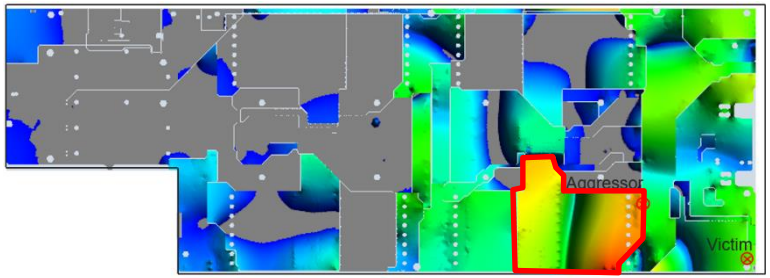
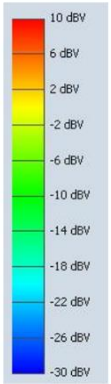
Power-to-Power Coupling: Production Board

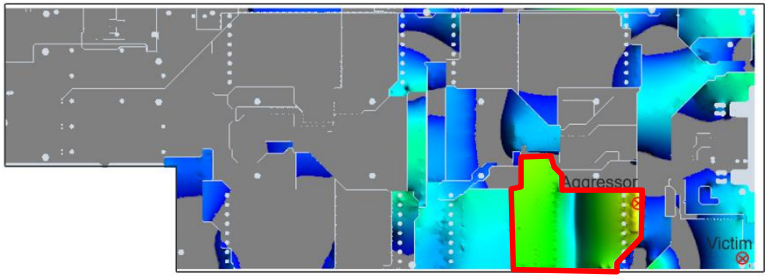
- Power planes can couple to other planes when overlapping (capacitive coupling), or through via-to-via coupling (inductive coupling)
- In production board, coupled noise seen to carry from aggressor across neighboring plane to victim power plane on other side of layer

Unterminated Aggressor Plane





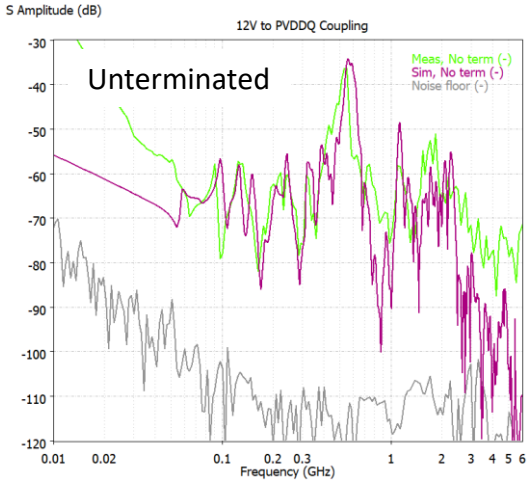
Terminated Aggressor Plane

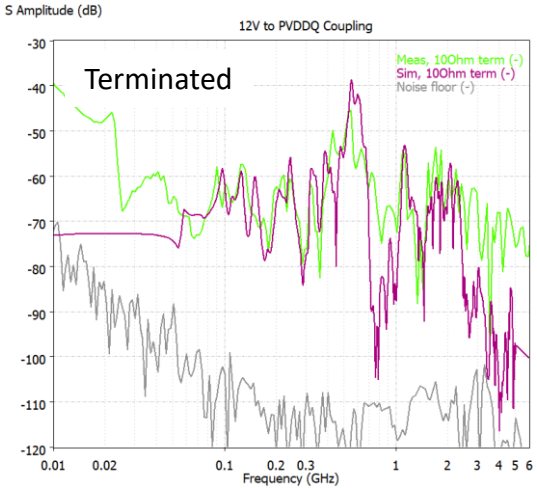


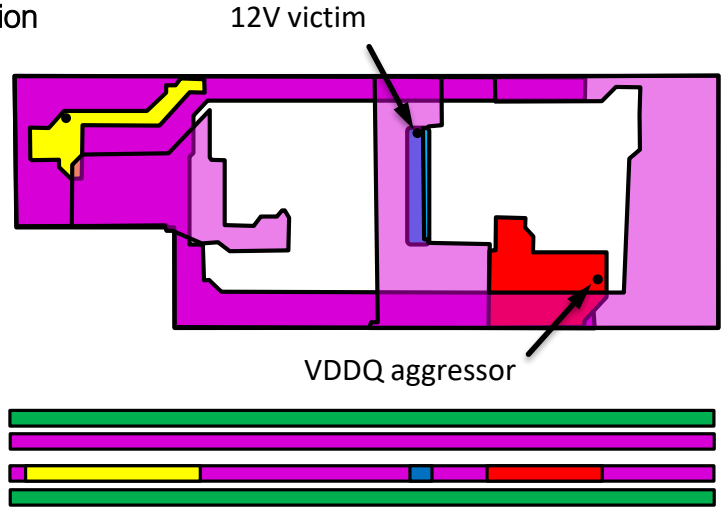
Voltage noise distribution across single power layer of production board. Aggressor plane is highlighted in red and loaded with 1A at 500MHz. In unterminated case the noise sprawl appears across the board at resonant frequency. In the unterminated case the noise sprawl is comparatively limited.

Power-to-Power Coupling: Nearby Victim

- Production board carrier plane (purple) dynamically filled open space on power layers during layout forming primarily capacitive coupling path from aggressor domain (red) to nearby victim domain (blue)
- S21 measurement and simulation between aggressor and victim domains show peak crosstalk at 500MHz, resonant frequency of aggressor power plane in unterminated and terminated cases
- Termination reduces crosstalk by ~10dB in measurement and ~5dB in simulation



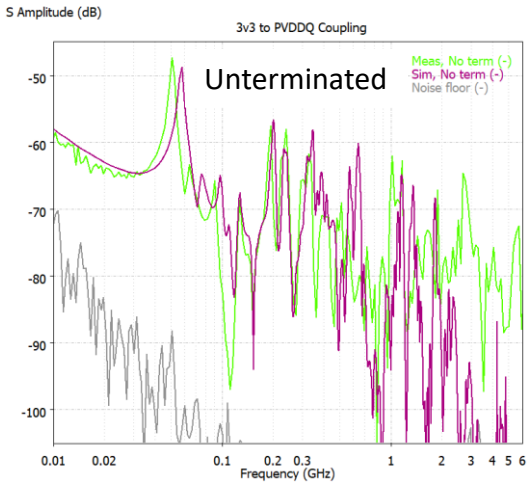


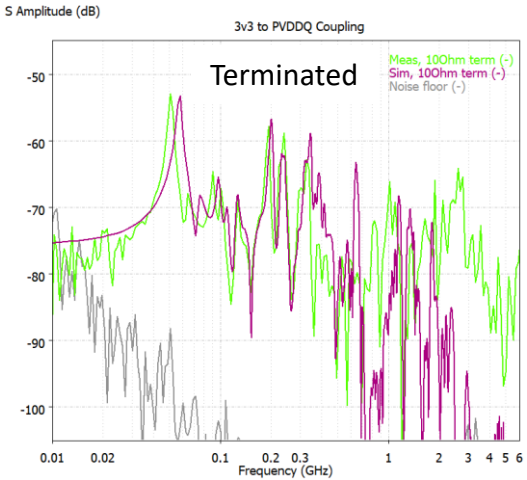


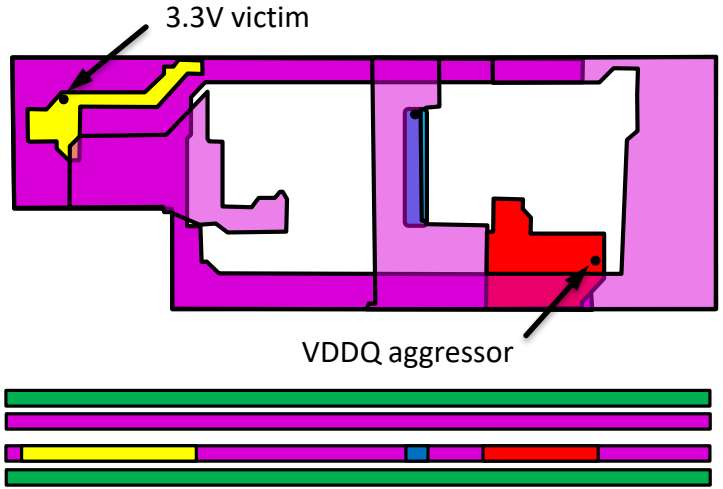
Vertical cross section of stackup around power planes of interest.

Power-to-Power Coupling: Far Away Victim

- Second capacitive coupling path analyzed from aggressor domain (red) to far away victim domain (yellow)
- S21 measurement and simulation between aggressor and victim domains again show peak crosstalk at 500MHz, resonant frequency of aggressor power plane in unterminated and terminated cases
- Termination reduces crosstalk by ~8dB in measurement but does not impact crosstalk simulation



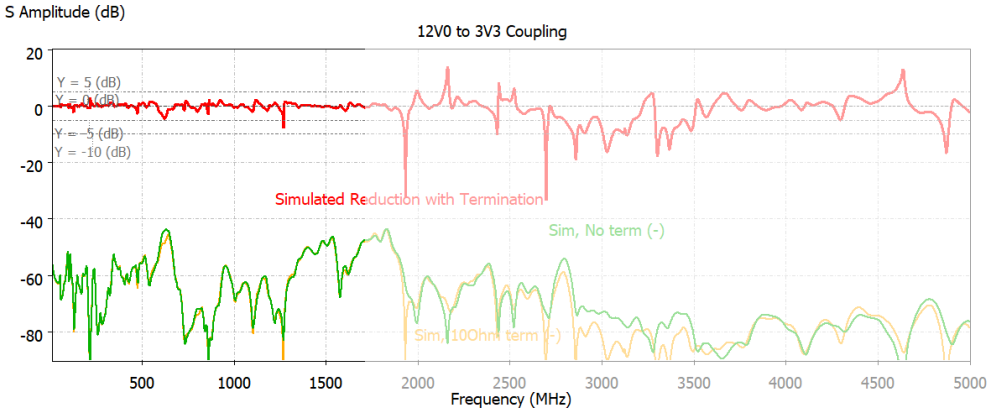


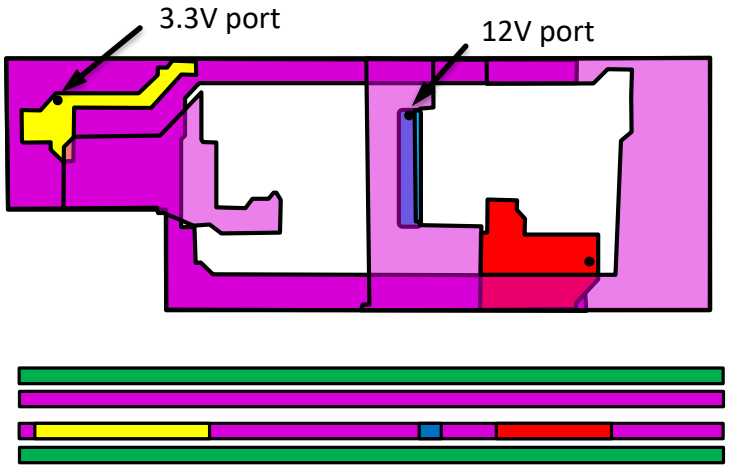


Vertical cross section of stackup around power planes of interest.

Power-to-Power Coupling: Victim-to-Victim

- 3.3V (yellow) –to– 12V (blue) power domain coupling simulated to see if termination of aggressor plane reduces crosstalk between unterminated planes
- Termination of aggressor plane reduces crosstalk between unterminated planes by 4-5dB in frequency range of interest

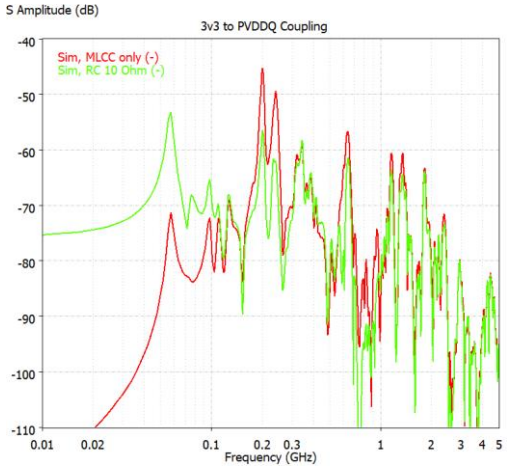


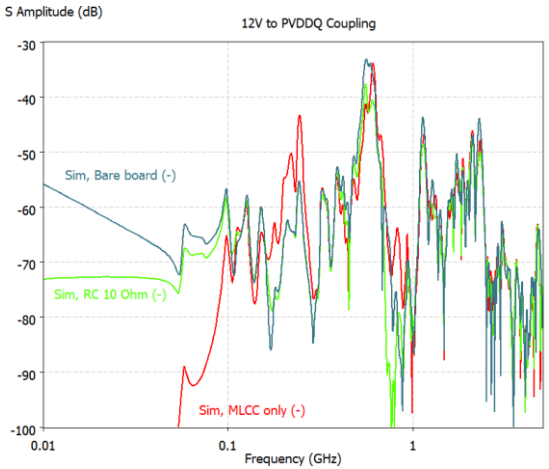


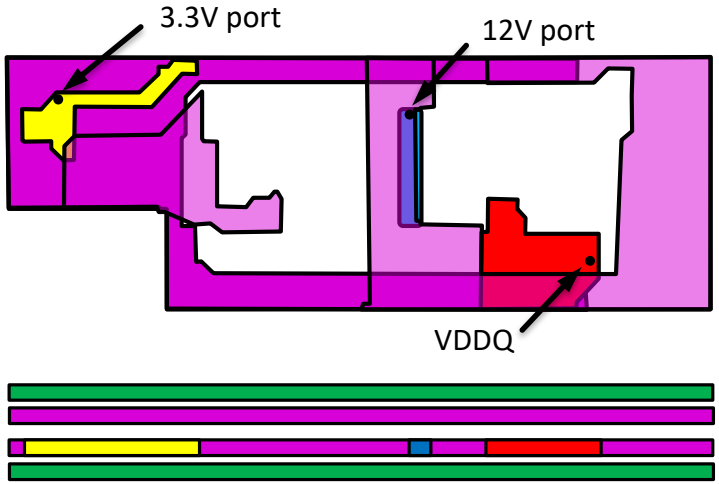
Vertical cross section of stackup around power planes of interest.

Power-to-Power Coupling: MLCC Termination

- In simulation aggressor VDDQ power plane (red) terminated with only MLCCs to compare effect on crosstalk with that of RC termination
- Low frequency crosstalk reduced significantly compared to RC terminated case
- At resonant frequency of aggressor plane midfrequency crosstalk reduced more in RC terminated case







Vertical cross section of stackup around power planes of interest.

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- **Test Board Investigation**
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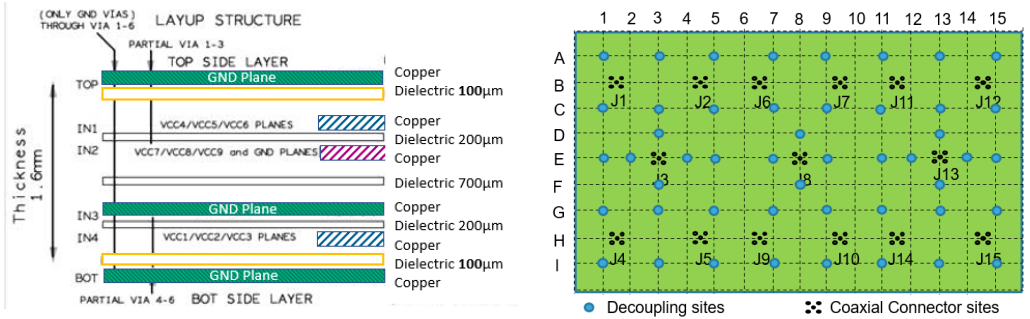
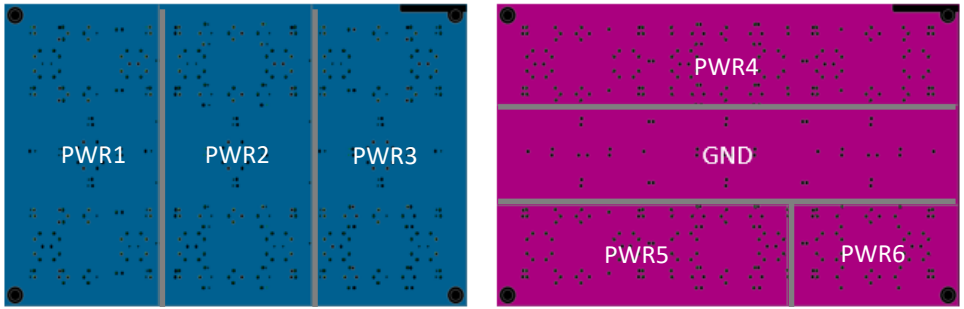
Test Boards

- Test boards developed to study:
  - Power domain coupling mechanisms:
    - Placement of planes
    - Plane spacing
    - Vertical overlap
  - Impact of thin laminates on power domain coupling
- Test board design:
  - 6-layer (3 GND + 3 PWR)
  - Stackup designed to analyze vertical and horizontal coupling
- Several iterations of board constructed with varying dielectric thickness between TOP/IN1 and IN4/BOT
  - 100um, 12um, 8um, 6um, and 3um (from Oak-Mitsui)



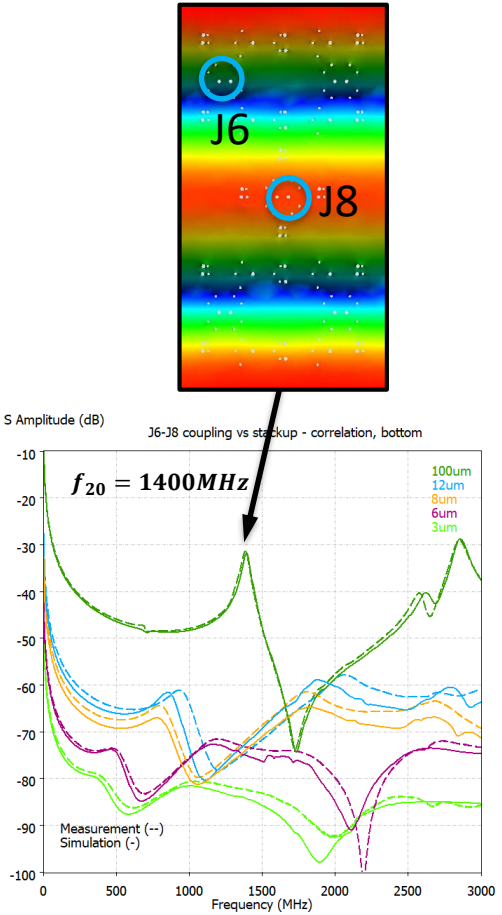
Test board stackup (left) and probing point/decoupling site mapping (right).



Test board plane layouts of IN1 and IN4 (left) and layout of IN2 (right)

Test Boards: Self Coupling

- Goal to study self coupling of power plane from center of plane to edge
- First resonance with 100um laminate seen at $f_{20} = 1400MHz$
- 40dB reduction in coupling amplitude when reducing laminate thickness from 100um to 3um
- Significant decrease in peak Q coupling amplitude with decrease in laminate thickness
- Lower frequency resonance: $\frac{f_1}{f_2} \propto \sqrt{\frac{\epsilon_2}{\epsilon_1}}$
  - Capacitance change proportional to the dielectric constant and inversely proportional to cavity height
  - Inductance change proportional to laminate thickness

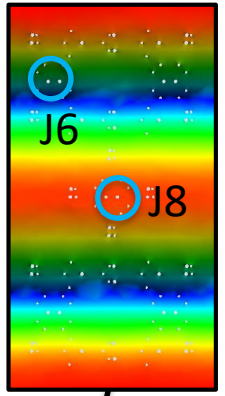


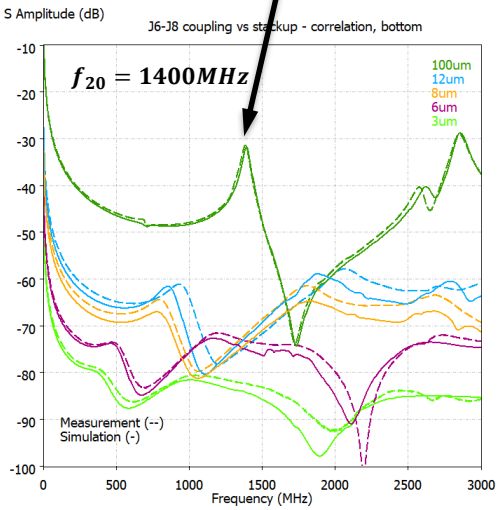
Test Boards: Self Coupling

- $\frac{1}{Q_{total}} = \frac{1}{Q_{rad}} + \frac{1}{Q_{sw}} + \frac{1}{Q_c} + \frac{1}{Q_d}$
  - Loss due to radiation and surface wave modes negligible because $h \ll \lambda$
  - Dielectric loss: $Q_d = \frac{1}{\tan\delta}$
  - Conductor loss: $Q_c = \frac{h}{\delta} = h\sqrt{\pi f \mu \sigma}$
    - Conductor Q increases linearly with laminate thickness
- Loss dominated by conductor related losses

Stackup [um]	Material	εr	tanδ	Qd	Qc	Qt	f20 MHz (J6-J8)
100	FR-4	4.5	0.02	50	84	31	1390
12	FaradFlex MC12TM 12um	10	0.015	67	10	9	932
8	FaradFlex MC8TM 8um	10.5	0.02	50	7	6	910
6	FaradFlex MC6TM 6um	21.7	0.008	125	5	5	633
3	FaradFlex MC3TM 3um	21.7	0.008	125	3	2	633

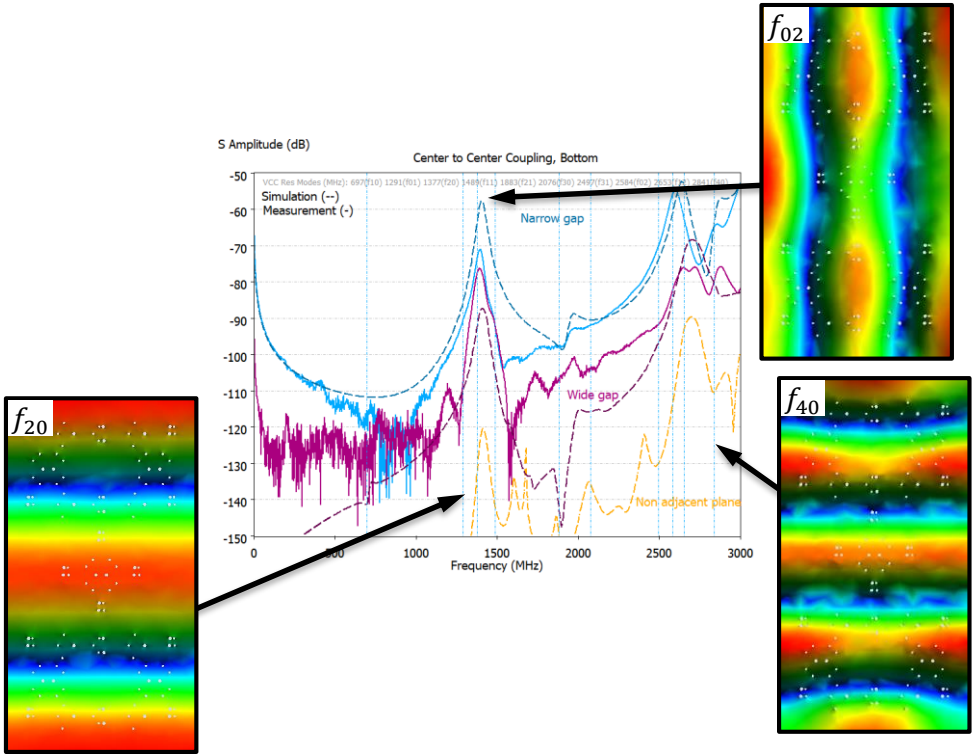
- Simulated Q less than calculated Q
  - $Q_{total,f20}(h = 100\mu m) \sim 15; Q_{total,f20}(h = 12\mu m) \sim 4$





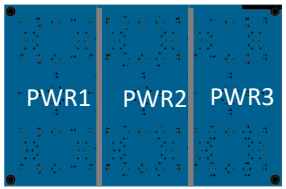
Test Boards: Adjacent Power Nets

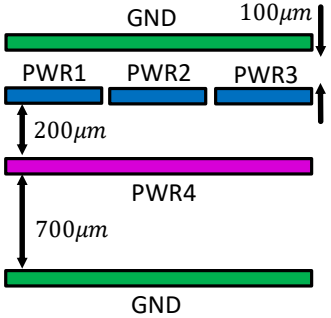
- Test board layer IN4 has planes spaced by 127um and 1.3mm (just over 10x min spacing)
- f20, f02, and f40 have resonance peaks at center of planes
- Measurements show 5dB coupling difference between narrow and wide gap for f20 mode whereas simulations show much more sensitivity to changes in gap size
- Increasing gap reduces coupling
  - Minimum gaps between planes highly susceptible to production variability leading resonances to potentially vary unpredictably

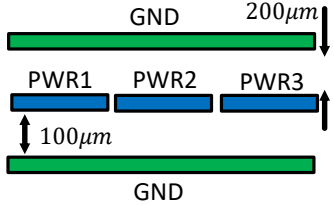


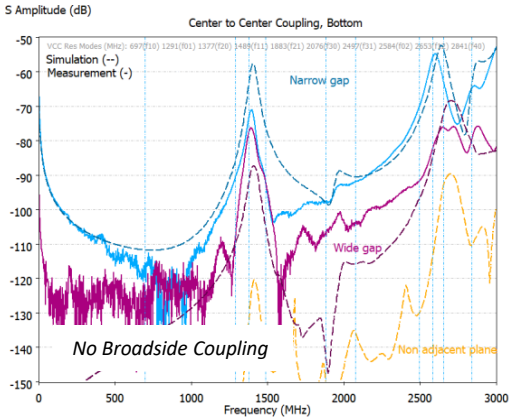
Test Boards: Broadside Coupling

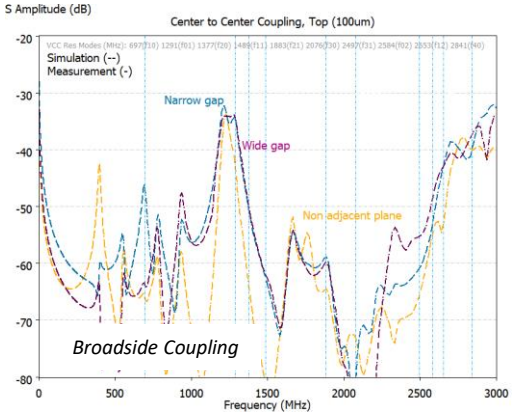
- Test board layer IN1 has planes with minimum gap spacing of 127um and 1.3mm (just over 10x min spacing)
- IN2 has PWR/GND plane 200um distance from IN1 power plane
- Coupling level increases significantly over having adjacent GND planes
- Little difference between wide and narrow plane gaps indicating broadside coupling is dominant coupling path
  - In some cases non-adjacent plane coupling greater than or equal to adjacent plane coupling





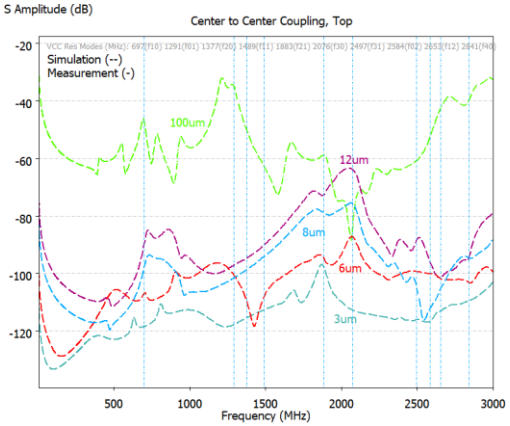


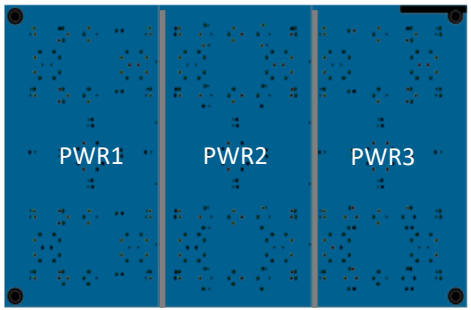


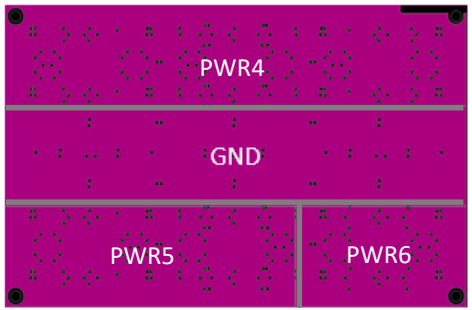


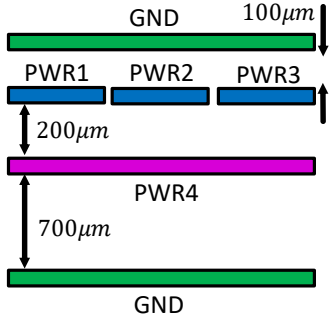
Test Boards: Broadside Coupling

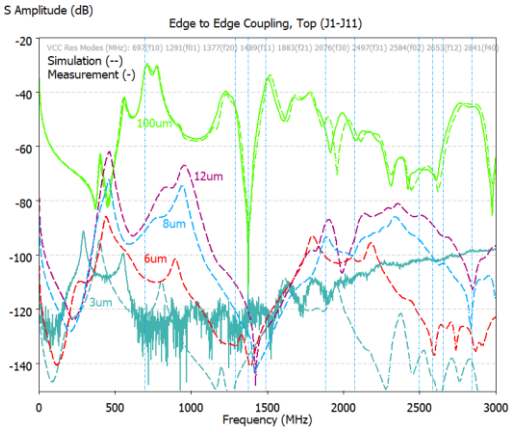
- Plane coupling between different planes due to adjacent plane coupling or broadside plane coupling decreases with decreasing laminate thickness
  - 30dB reduction in coupling when reducing laminate thickness from 100um to 12um
- Reduction in Q due to reduced laminate thickness
- Reduction in resonant frequencies due to higher dielectric constant of thinner laminates





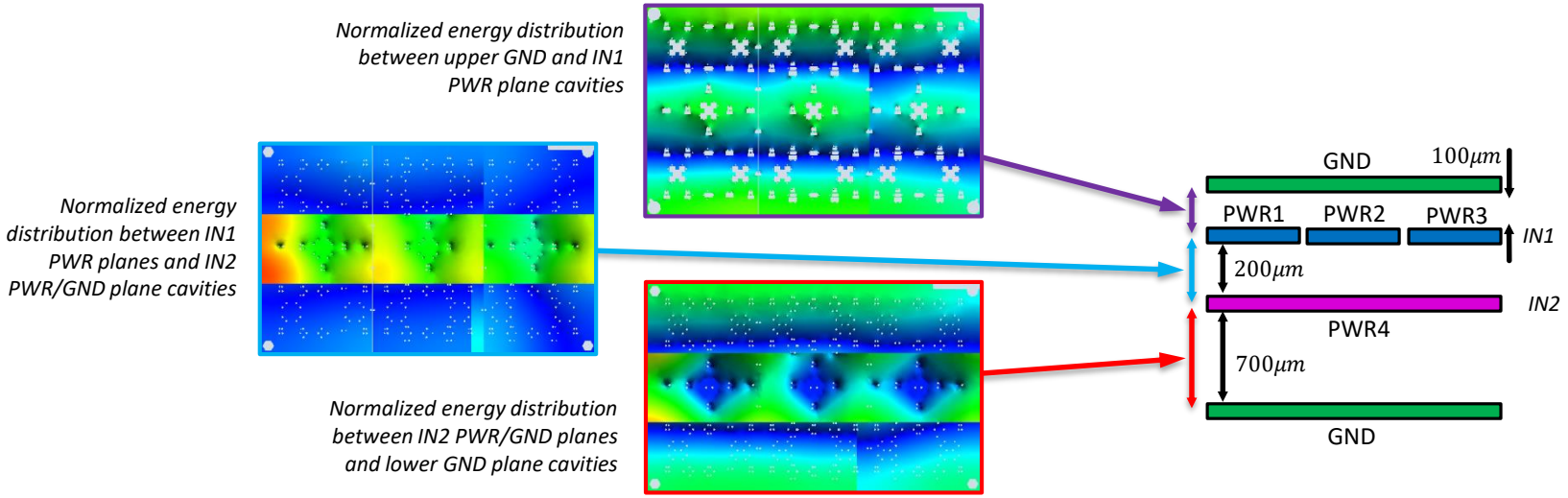






Test Boards: Long-Haul Coupling

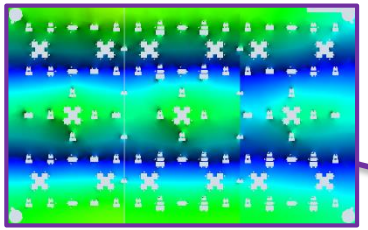
- Power plane resonances couple across distinct power planes, therefore entire power layer needs to be considered
  - Considering power planes independently of one another insufficient to predict sustainable resonant modes seen on power planes
- Test board IN1 and IN2 (200um separation) see 1.182GHz as f20 resonant mode across entire layer
- GND plane on IN2 plays important role as bridge of 1.182GHz resonant mode across board



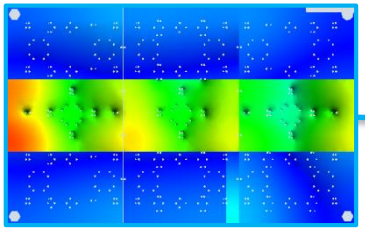
Test Boards: Long-Haul Coupling

- GND plane on IN2 plays important role as carrier of 1.182GHz resonant mode across board
- GND connection defect intentionally added to emulate common behaviors when laying out via stitching:
  - Missing vias
  - Regular stitching patter with insufficient spacing

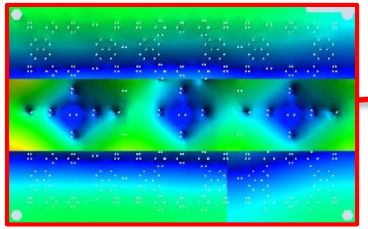
Normalized energy distribution between upper GND and IN1 PWR plane cavities

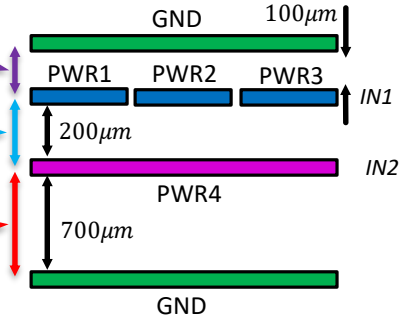


Normalized energy distribution between IN1 PWR planes and IN2 PWR/GND plane cavities



Normalized energy distribution between IN2 PWR/GND planes and lower GND plane cavities





Outline

- Power Plane Resonances
- Plane Termination
- Production Board Power Plane Coupling
- Test Board Investigation
- **Conclusion**

Conclusion

- **RC termination can be used to quite power plane resonances and inter-plane coupling**
- **RC termination of planes can reduce coupling between unterminated planes**
- **Thinner laminates can be used to dampen power plane Q and build immunity to inter-plane coupling**
- **Spacing planes far apart from one another not sufficient for isolation as full cavity resonances can drastically increase coupling**
- **Power planes can be vehicle for coupling between domains**
  - Sufficient decoupling, RC termination, and thinner laminates can be used to build resonance immunity and noise immunity from other power domains
- **GND planes can be vehicle for coupling between domains**
  - Sufficient via stitching necessary to ensure good reference plane behavior and mitigate multi-cavity resonances

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Thank you!

QUESTIONS?