

Welcome to

3th ANNIVERSARY

DESIGNCON[®] 2025
WHERE THE CHIP MEETS THE BOARD

Conference

January 28–30, 2025
Santa Clara Convention Center

Expo

January 29–30, 2025

DESIGNCON[®] 2025
WHERE THE CHIP MEETS THE BOARD

Information Classification: General



JAN. 28–30, 2025

#DesignCon

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 **informa** markets

Determining the Requirements, Die vs. Package vs. Board: Multi-level Power Distribution Network Design

Ethan Koether (Amazon)

John Phillips (Cadence), Shirin Farrahi (Cadence), Kristoffer Skytte (Cadence), Joseph Hartman (Oracle), Mario Rotigni (retired), Istvan Novak (Samtec)



SPEAKERS



Ethan Koether

Sr. Signal and Power Integrity Engineer, Amazon Project Kuiper
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Ethan Koether earned his master's degree in EECS in 2014 from MIT then spent seven years as a hardware engineer at Oracle. He then joined Amazon's Project Kuiper as a Sr SIPI engineer. His interests are in commercial power solutions and power distribution network design, measurement, and analysis.



SPEAKERS



Kristoffer Skytte

Application Engineer Architect, Cadence
kskytte@cadence.com

Kristoffer Skytte has 20 years experience working on chip, package, board and full system analysis including SI, PI, thermal, and EMC challenges. His recent efforts are on examining differences between measurement and simulation. He holds an M.Sc.EE. degree from the Technical University of Denmark.



Shirin Farrahi

Sr. Principal Software Engineer, Cadence
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Shirin Farrahi is working on SI and PI tools for automated PCB design. Prior to joining Cadence, she spent four years as a Hardware Engineer in the SPARC Microelectronics group at Oracle. She received her Ph.D. in Electrical Engineering from the Massachusetts Institute of Technology.



John Phillips

Sr. Principal Application Engineer, Cadence
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John has 30+ years experience working on SI, PI, and EMC challenges at the chip, board, and system level in applications including high-end computing and mil-aero. He holds an MSc. from Bolton University, UK. His current interests are SI/PI co-simulation and modelling for high-speed interfaces.



Abe Hartman

Principal Hardware Engineer, Oracle
abe.hartman@oracle.com

Abe works on system SI/PI at Oracle and has worked at Amphenol TCS, Juniper Networks, Enterasys, and GM. Abe holds a MS in EE from UMass-Lowell, a MS in Engineering Science from Rensselaer Polytechnic Institute, and a BS in both ME and EE from Kettering University in Flint, MI.



SPEAKERS

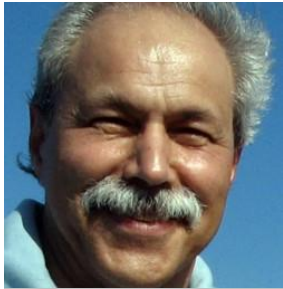


Mario Rotigni

Retired

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Mario retired after a 45-year career in R&D working on micro-controllers and EMC for automotive applications. He has co-authored 22 papers about EMC of Integrated Circuits and is a member of the IEEE & IEEE EMC Society.



Istvan Novak

Principal SI/PI Engineer, Samtec

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Istvan works on advanced SI/PI designs at Samtec and was previously a Distinguished Engineer at SUN later Oracle. He introduced the first 25 μ m power-ground laminates for large rigid PCBs and worked to create a series of low inductance, controlled-ESR capacitors. He is a Life Fellow of the IEEE with 25 patents, author of two books on PI, teaches SI/PI courses, and maintains a popular SI/PI website. He was named Engineer of the Year at DesignCon 2020.



GOALS

- Updated target impedance methodology with frequency and spatial position
- POL (Point of Load) vs parallel loads on PDN – what's the difference
- Correlate BW changes with major PDN components from the DC source to the silicon
- Guidelines to avoid over-designing PDNs & understand considerations for complex multi-load power deliveries

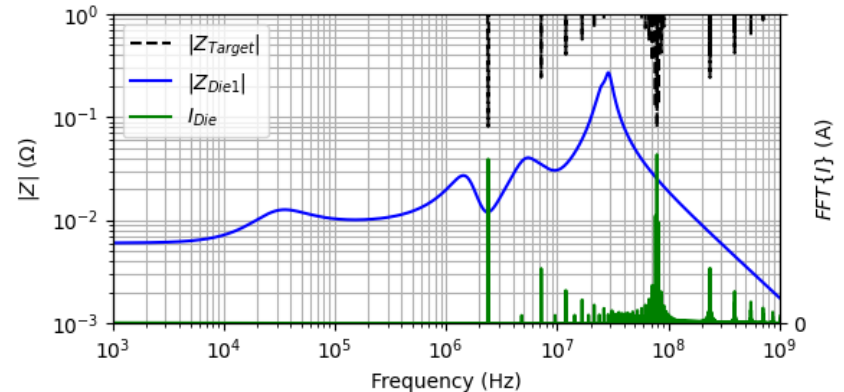
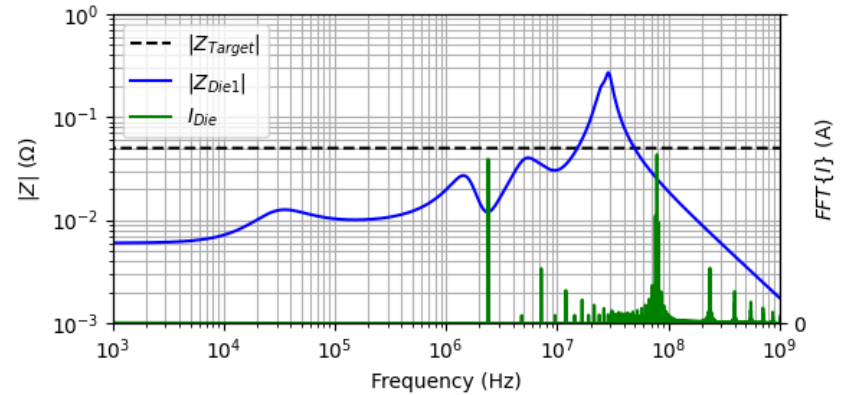


TARGET IMPEDANCE

- PI design target for systems:

$$|Z_{PDN}| \leq \Delta V_{tol} / \Delta I_{max} \text{ for } 0 \leq f \leq f_{max}$$

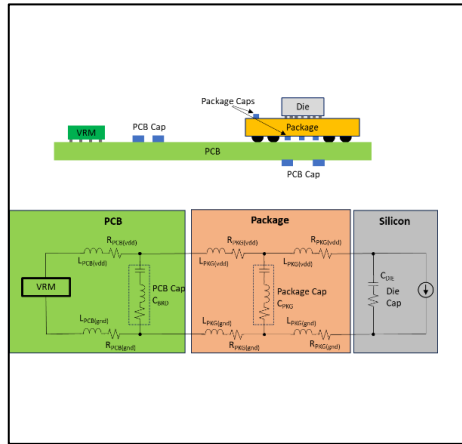
- Different flavors of “target impedance” metric
- Assumes minimum-phase, LTI system
- Can meet target impedance but see voltage fluctuation generated outside of spec.
- Not clearly extendable for multi-load or multi-power domain PDN
- Can be unrealistic target to meet over entire frequency range



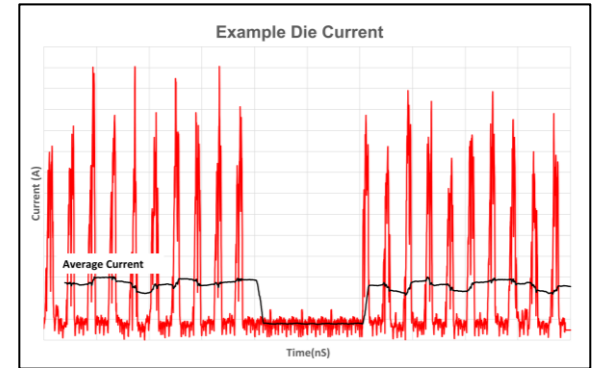
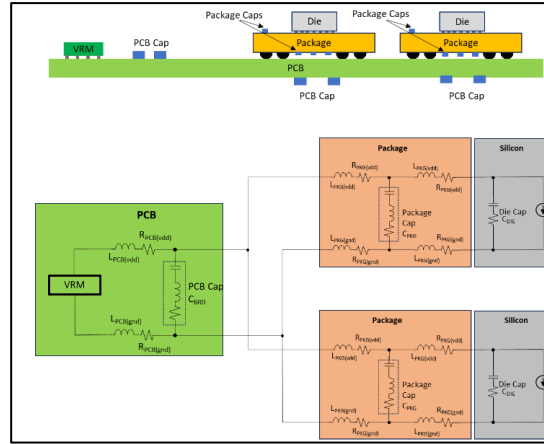
POL and Multi-Load PDN Ladder Models

- POL PDN and two-load PDN
- Transient current at die-level of PDN is filtered by die-package resonances and PCB impedance before appearing on the board or at neighboring die

POL (Single-Load PDN)

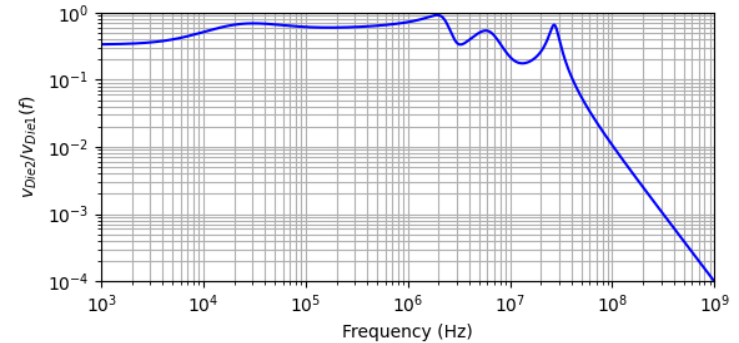
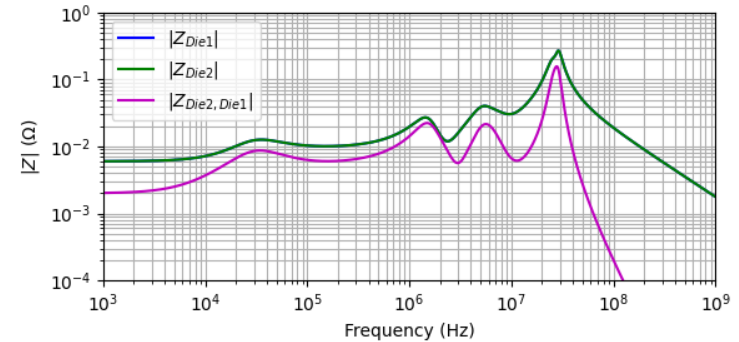


Multi-Load PDN

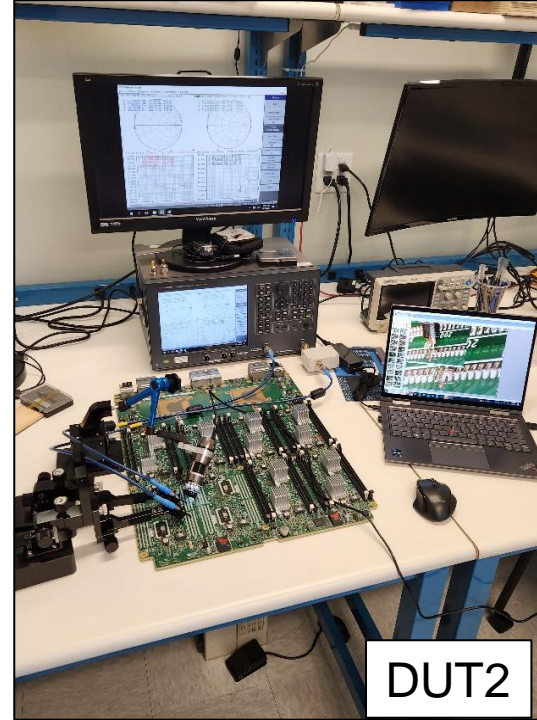
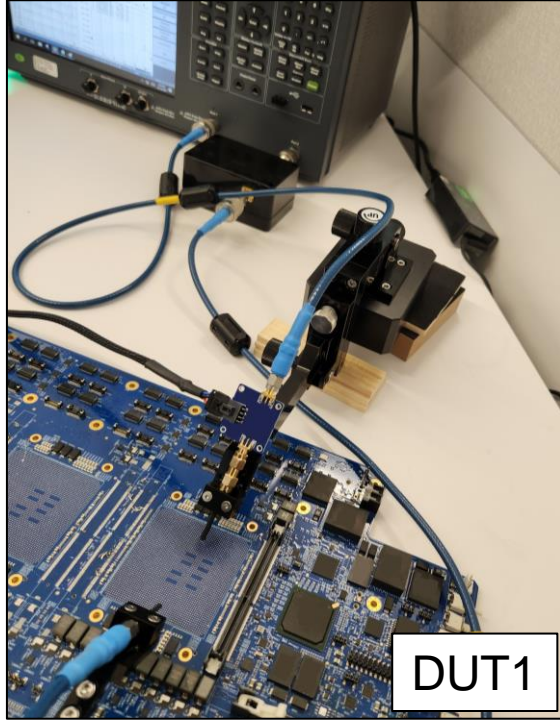


FILTERING BETWEEN DIES IN MULTI-LOAD PDN

- Noise between dies attenuated due to low-pass filtering
- Noise coupled between dies:
 - Content above package-die resonance highly attenuated
 - Content in package-dominated PDN frequency range less attenuated
 - Content in frequency ranges where PDN is pcb-dominated or VR-dominated sees little attenuation



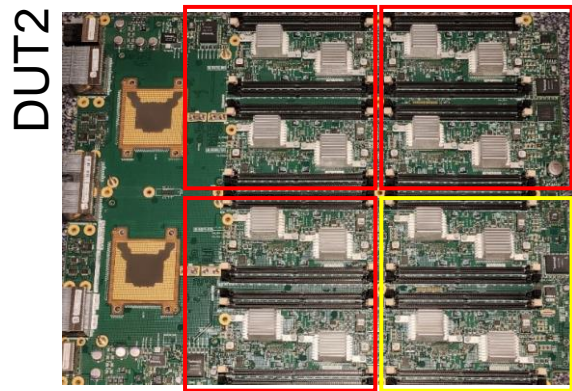
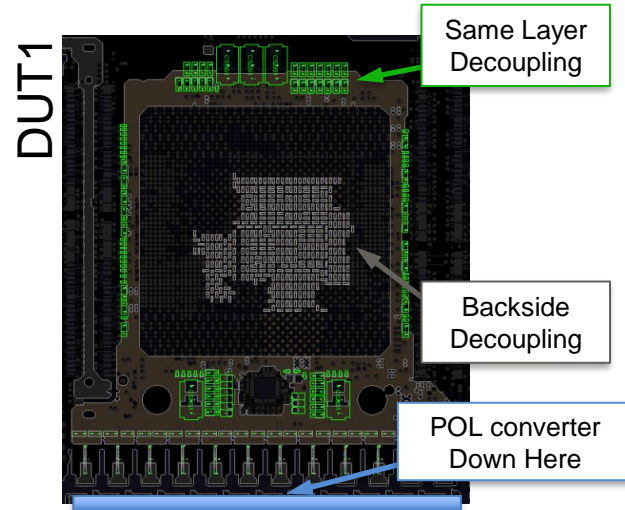
DUTs AND SETUP OVERVIEW



DUTs

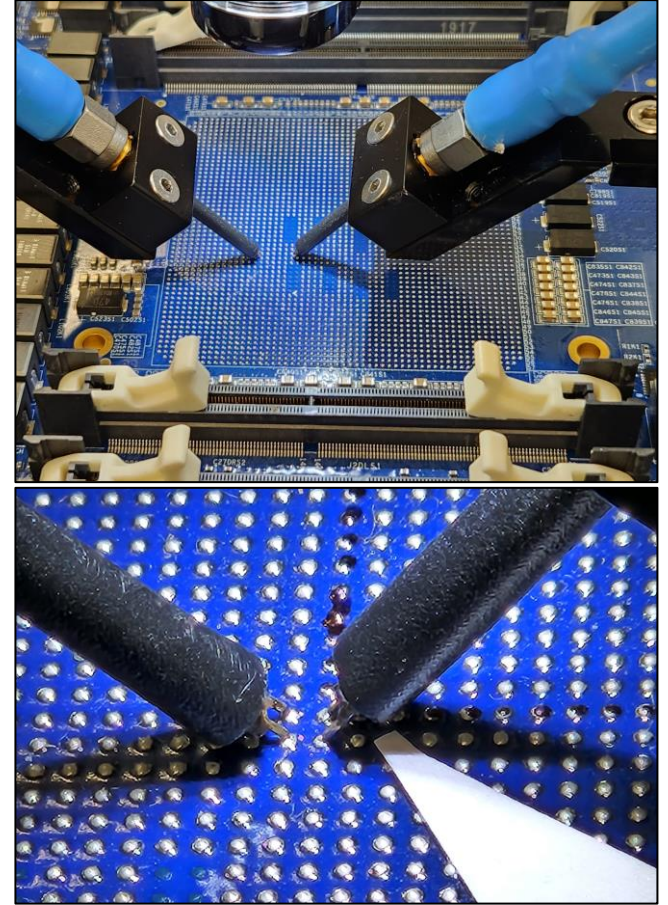
- DUT1: POL, 250A AI application
 - 30-layer stackup, 3 power layers, half of layers GND
 - BGA: 430 pwr pins, 1400 GND pins
 - 500 decoupling caps, 5 different values
 - $<0.25\text{nH}$ net inductance seen by IC
 - $<1\text{m}\Omega$ impedance 10kHz - 3MHz (seen looking into pcb BGA)
- DUT2: Multi-load, high-computing application
 - 32 DIMM sockets driven by 16 memory modules, split into 4 power planes, each with 80A DCDC converter
 - 28layer stackup multiple 2oz power layers
 - 8x 1000uF, 27x 330uF by VR
 - 40x 47uF near DIMM sockets
 - 238x 4.7uF near memory controllers

	VRM	Decoupling	ASICs
DUT1	Mounted, not powered	Mounted	Not mounted
DUT2	Mounted, not powered	Mounted	Mounted



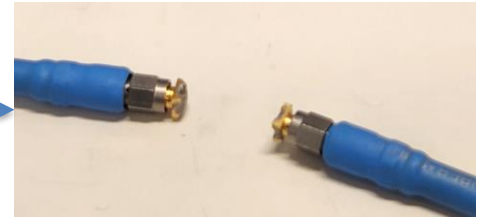
MEASUREMENT SETUP

- Keysight E5061B VNA
- Packetmicro RP-GR-121510 probes and positioner
- Microscope
- Common mode choke toroid for use up to 10MHz
- SOLT calibration (including Isolation) to end of cables.
- Landing probes not de-embedded
 - +/-40pH - 50pH mutual probe-tip loop inductance @1MHz @1mm
 - Negligible phase rotation from probes in this frequency range
- 5Hz IFBW
- 10dBm source power



NOISE FLOOR INVESTIGATION

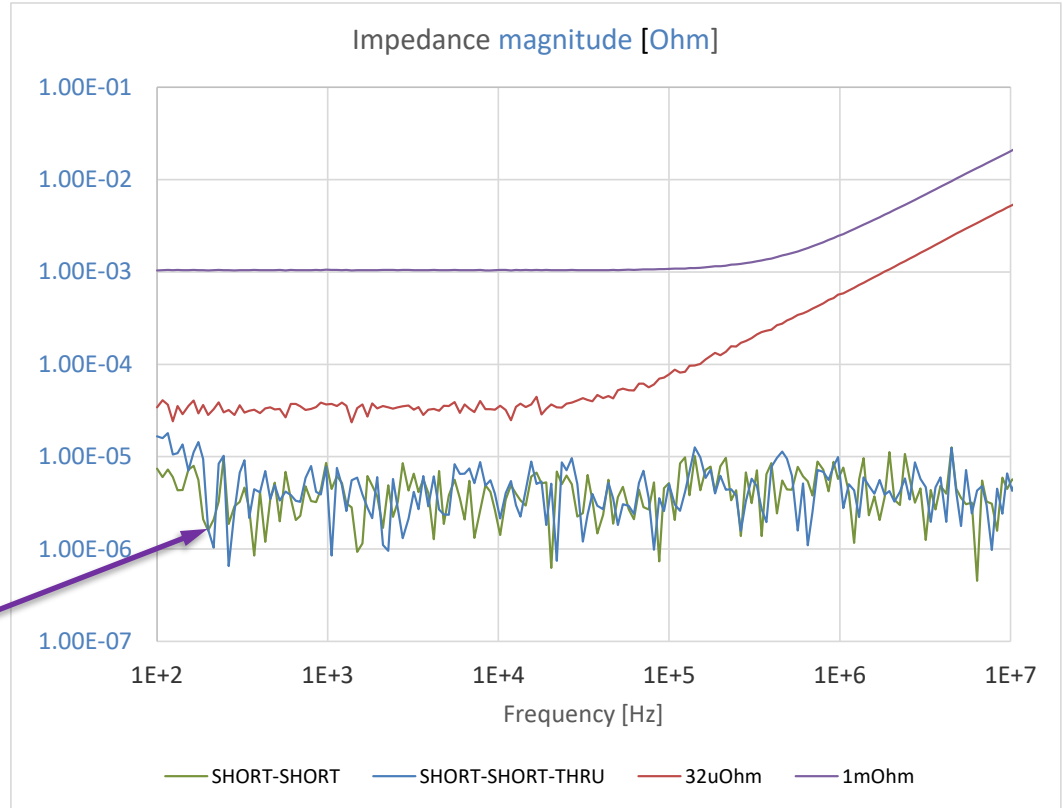
- Aimed to see how far noise floor could be reduced using E5061B VNA
- SOLT calibration (including Isolation) to end of coax cables
- Some of the reference pieces
 - SMA-SMA SHORT
 - SMA-SMA SHORT-THRU
 - 32uOhm
 - 1mOhm
- Setup variations
 - No external active device
 - 20dB low-noise preamplifier on Port2
 - 20dBm power booster on Port1
 - 20dBm power booster on Port1 and 20dB low-noise preamplifier on Port2



NOISE FLOOR INVESTIGATION

- 5Hz IFBW
- 10dBm source power
- No averaging
- SOLT calibration (including Isolation)
- No external active device
- DUT data shown in this paper used this setup

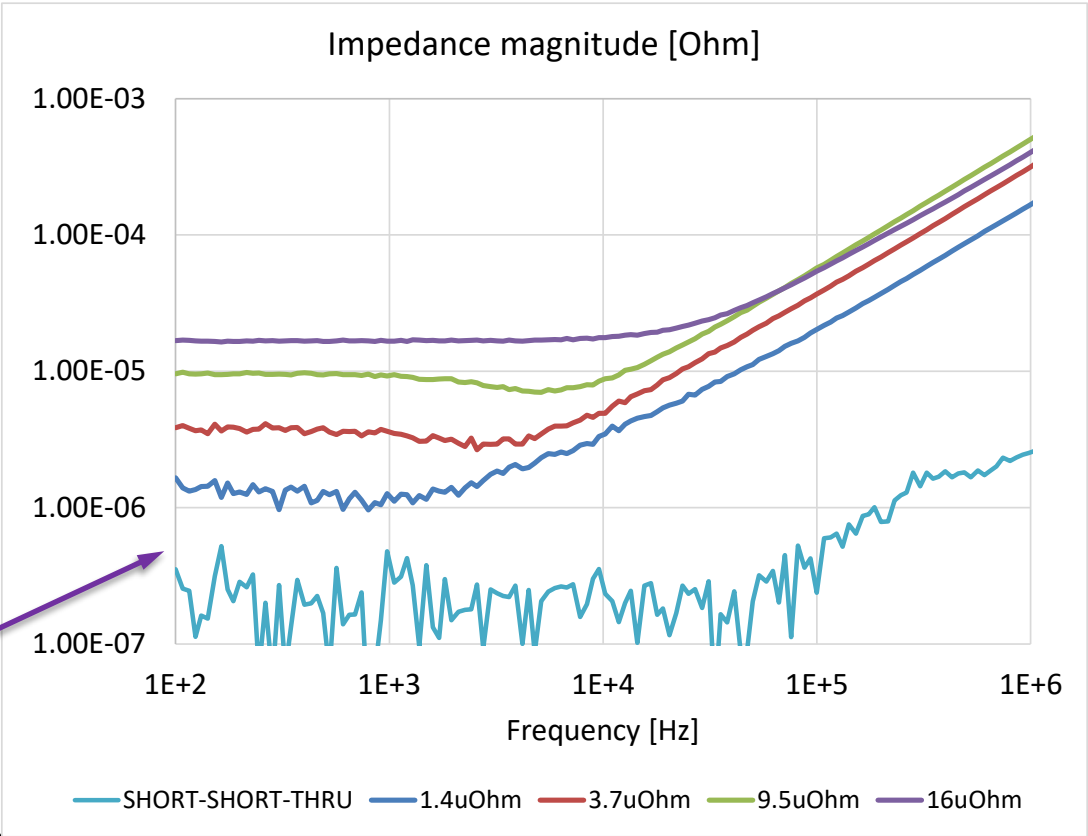
< 10 $\mu\Omega$ noise floor



NOISE FLOOR INVESTIGATION

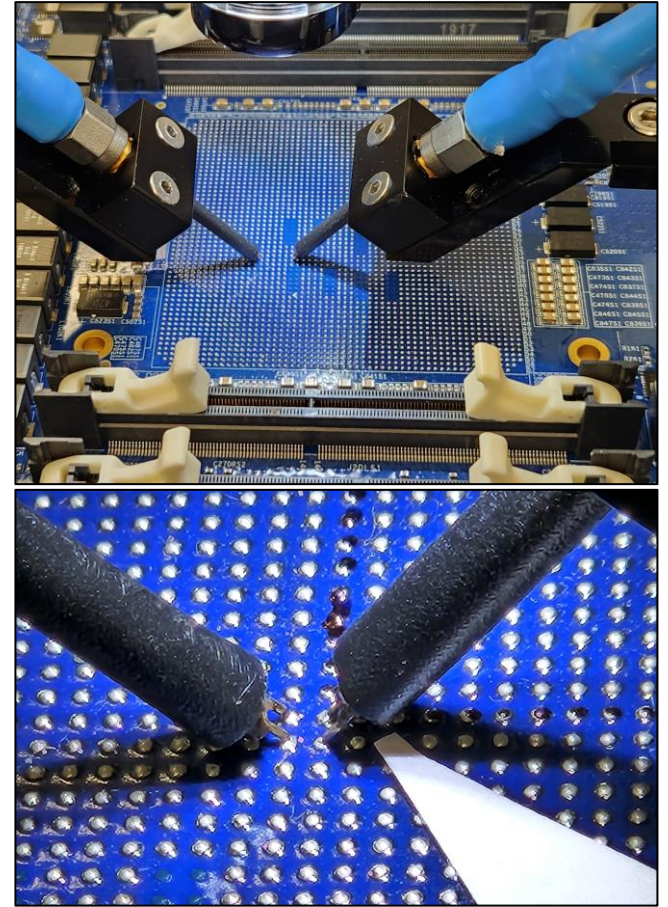
- 1Hz IFBW
- 0dBm source power
- No averaging
- SOLT calibration (including Isolation)
- 20dB 20dBm power booster on Port1
- 20dB low-noise preamplifier on Port2

< 1 $\mu\Omega$ noise floor



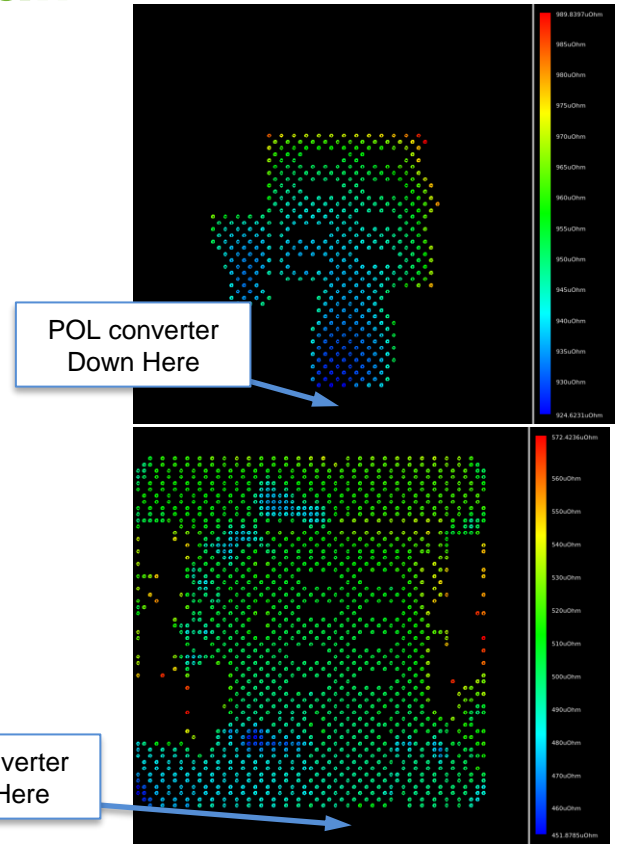
SIMULATION SETUP

- Hybrid solver
 - Wanted to see what quality correlation achievable with this faster simulator versus full 3D simulator.
- DUT1 Simulation Setup:
 - Capacitors modeled with SPICE or s-parameter model for corresponding vendor or like vendor where possible
- DUT2 Simulation Setup:
 - Capacitor R-L-C models used where satisfactory vendor s-parameter models were not available



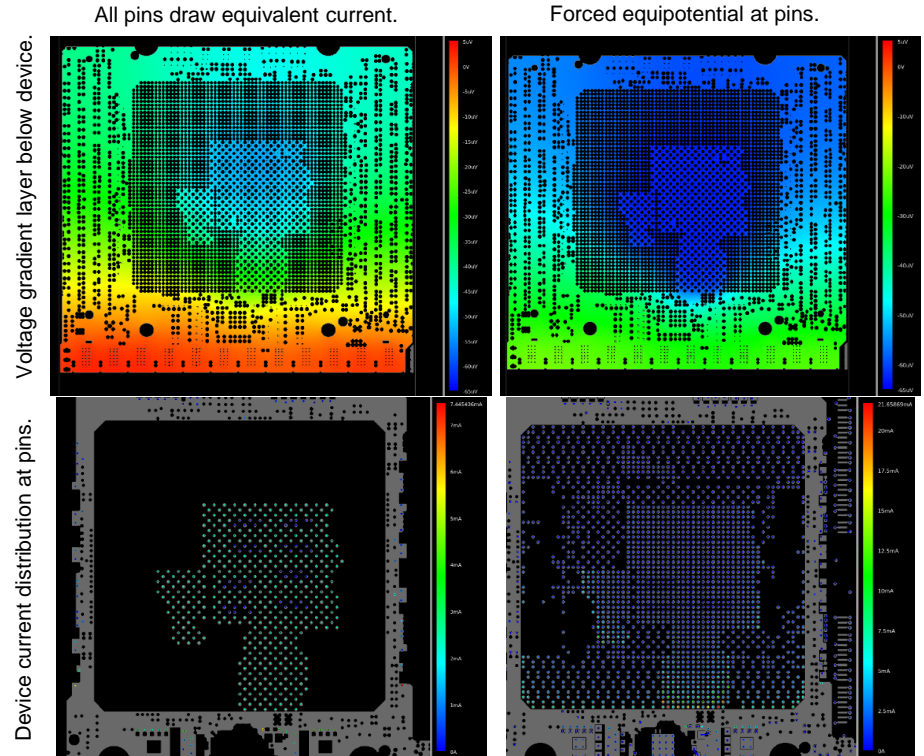
DUT1: DC Conductivity per Pin Pair

- DUT1: POL, 250A AI application
 - 30 layer stackup, 3layers power, half of layers GND
 - BGA: 430 pwr pins, 1400 GND pins
 - 500 decoupling caps, 5 different values
 - $<0.25\text{nH}$ net inductance seen by IC
 - $<1\text{mOhm}$ impedance 10kHz - 3MHz (seen looking into pcb BGA)
- DC Test 1: DC Resistance seen by pins
 - Top plot: Power domain pins see variable resistance path to POL due to variation in geometric distance to POL ranging from $920\mu\Omega$ (blue) - $955\mu\Omega$ (green) - $990\mu\Omega$ (red)
 - Bottom plot: GND BGA pins' resistances vary similarly from $450\mu\Omega$ (blue) - $515\mu\Omega$ (green) - $570\mu\Omega$ (red)



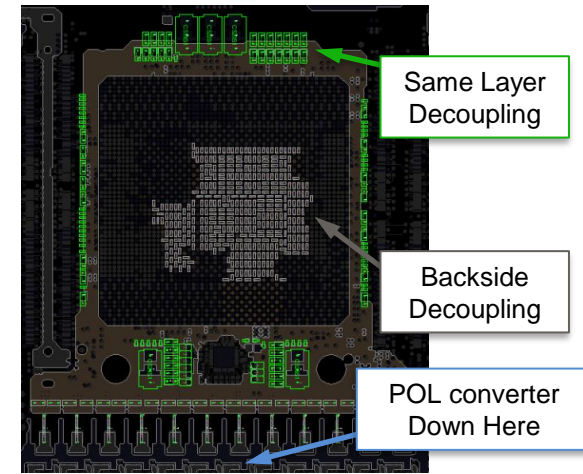
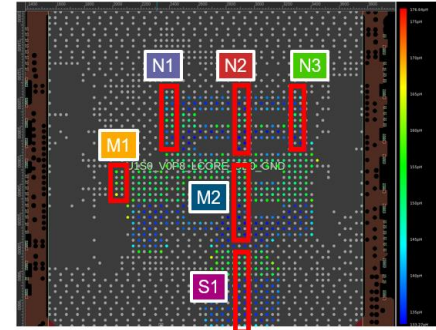
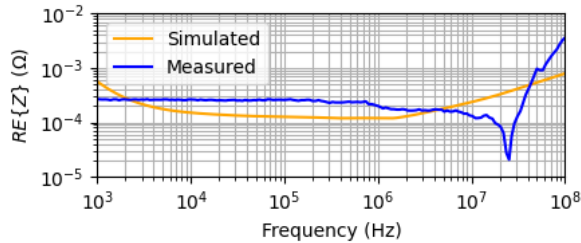
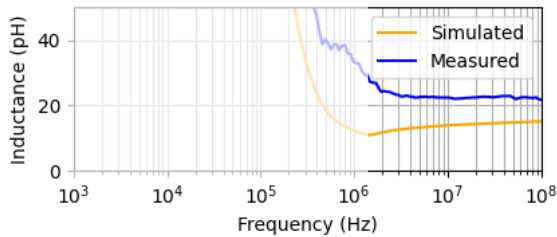
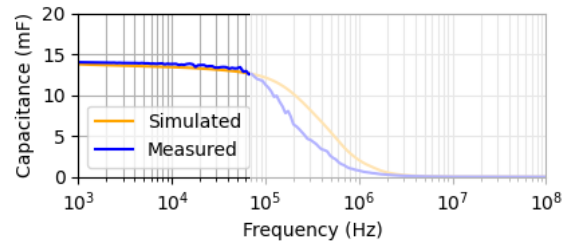
DUT1: DC Equipotential Load vs. Equivalent Current Distribution

- DC Test 2: DC Equipotential Load vs. Equivalent Current Distribution
 - All power pins draw equivalent amount of current
 - Ideal forced equipotential on BGA power pins
 - Uniform voltage supplied at BGA
 - Current is purely function of path resistance
 - 3x increase in max current per pin nearest POL



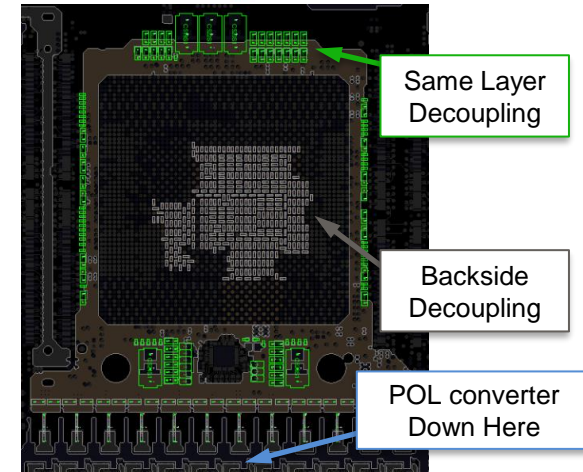
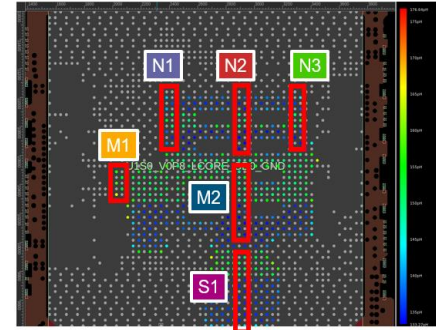
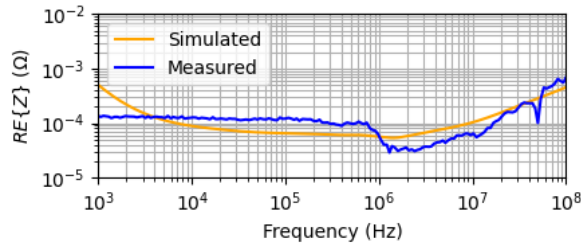
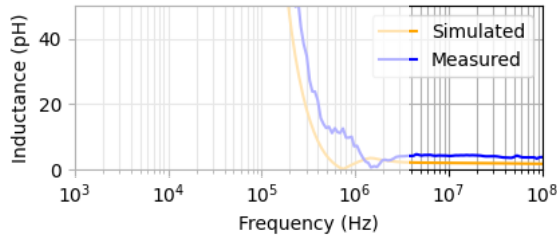
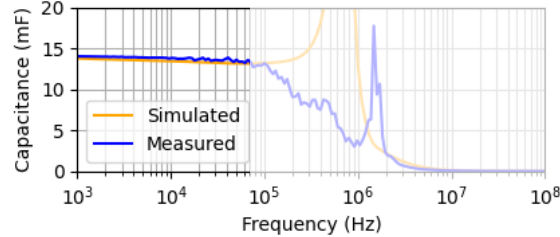
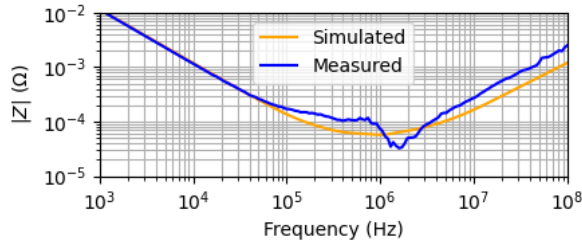
DUT1: AC Simulation and Measurements

- BGA power domain pins grouped into 6 regions
- Self-impedance simulations and measurements taken many places
- Example: N2 region self-impedance plots



DUT1: AC Simulation and Measurements

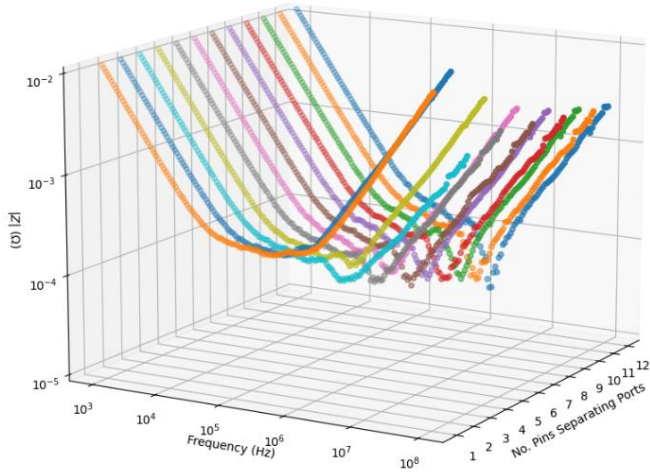
- BGA power domain pins grouped into 6 regions
- Transfer-impedance simulation and measurements taken many places
- Example: N2 region transfer-impedance plots



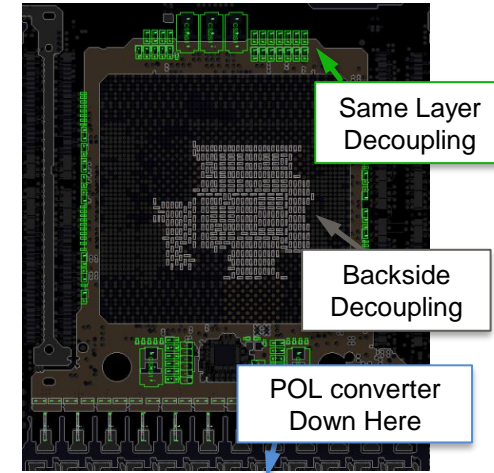
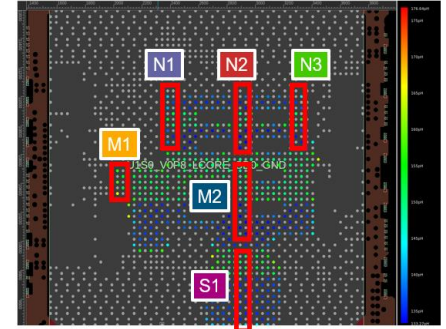
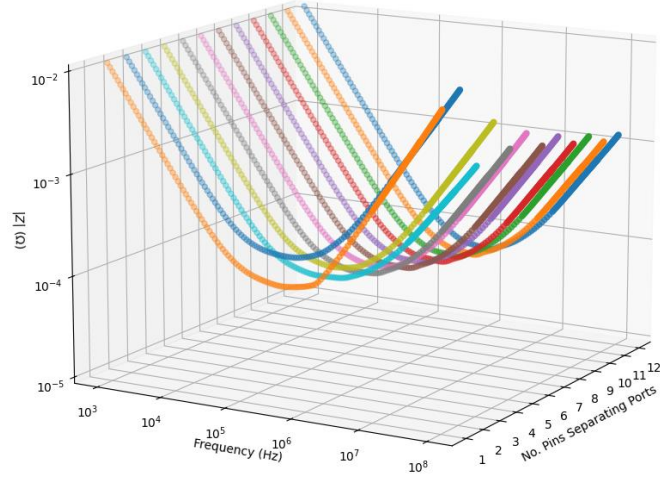
DUT1: AC Simulation and Measurements

- Self-impedance – to – transfer impedance
- N2 region simulations and measurements a pin spacing between probe landings is increased
- As probes separate: Capacitance (no change), resistance (\downarrow), inductance (\downarrow)

Measured Data:

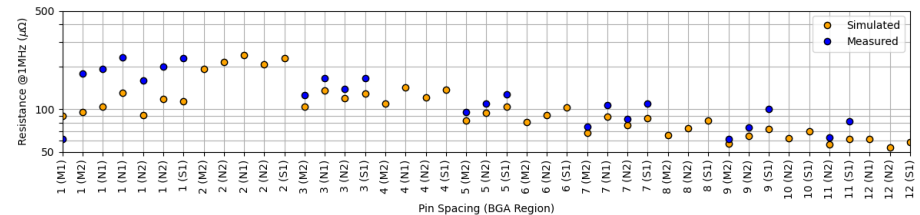
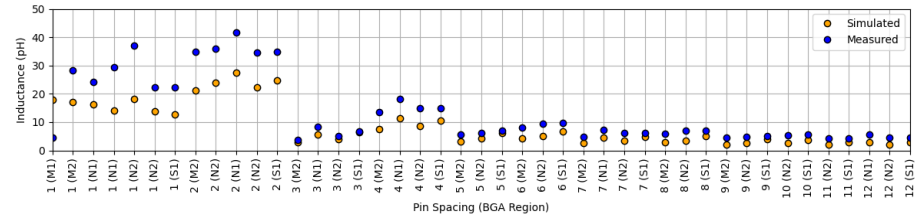
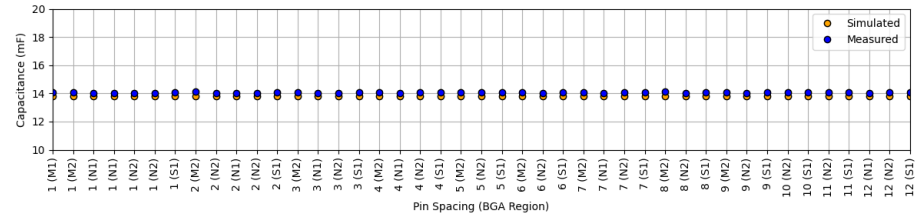


Simulated Data:



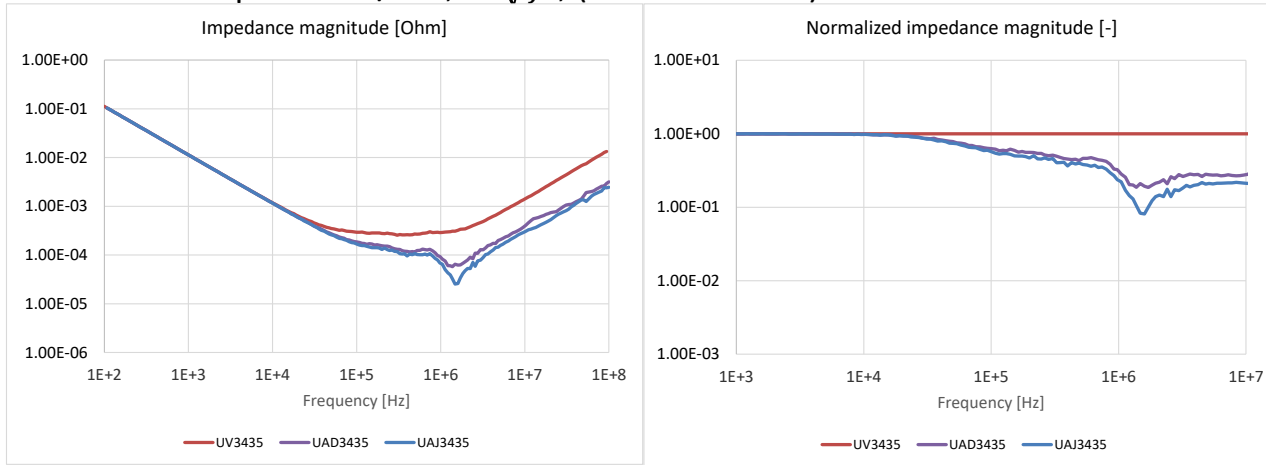
DUT1: AC Simulation and Measurements

- Capacitance: consistent between all datasets
 - No variation expected or seen due to variation of observer
- Inductance:
 - Highest in self-impedance cases
 - Larger disagreement between simulated and measured data due to probe tip coupling
 - Probe tip coupling falls off as probes separate
 - Little difference between the different self-impedance cases, likely due to decoupling on the opposite side of the BGA
- Resistance:
 - Highest in self-impedance cases
 - Trends lower as probe landings separate



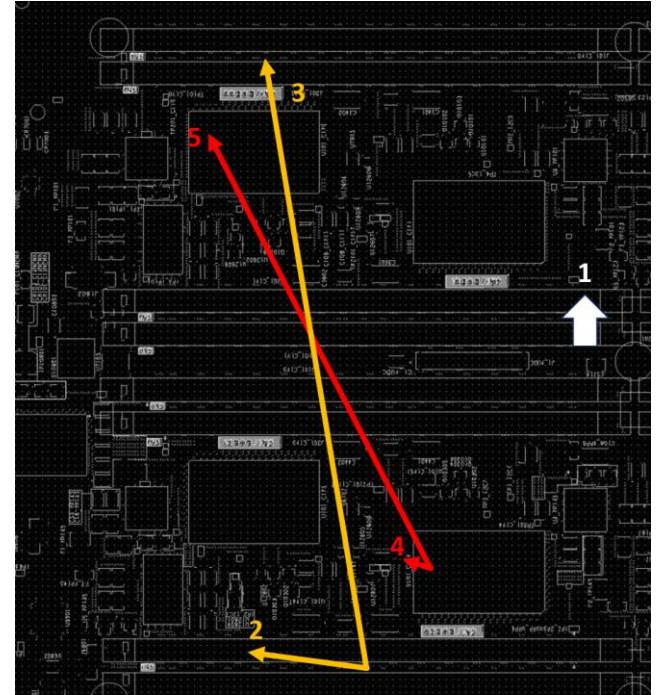
DUT1: Filtering Effect

- Normalized transfer-impedance to self-impedance in order to estimate filtering transfer function: $\frac{Z_{21}}{Z_{11}} \sim \left(\frac{v_2}{i_1}\right)$.
- $\left(\frac{i_1}{v_1}\right) = \frac{v_2}{v_1}$
- Cutoff frequency $\sim 30\text{kHz}$ for both BGA regions
 - $< 30\text{kHz}$: little deviation showing effective “lumped” region. Filtering here due to DC resistance of planes
 - $30\text{kHz} - 800\text{kHz}$: RC filtering region due to plane’s DC and ‘skin’ resistances and net capacitance on plane
 - Transfer function slope $\sim 10\text{dB/dec}$, $\propto \sqrt{f}$, (skin resistance)



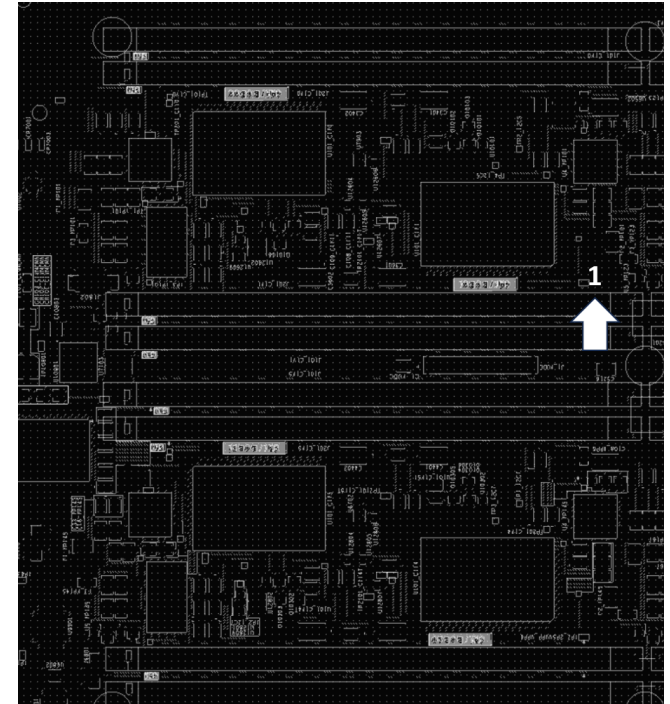
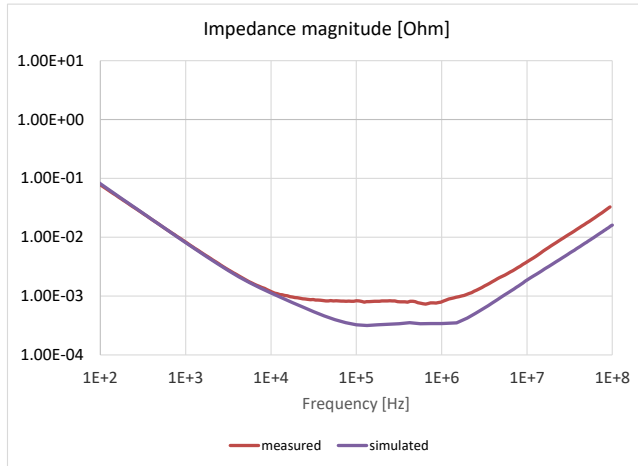
DUT2: AC Simulation and Measurements

- DUT2: Multi-load, high-computing application
 - 32 DIMM sockets driven by 16 memory modules, split into 4 power planes, each with 80A DCDC converter
 - 28layer stackup multiple 2oz power layers
 - 8x 1000uF, 27x 330uF by VR
 - 40x 47uF near DIMM sockets
 - 238x 4.7uF near memory controllers
- Measurement locations:
 1. Core vias for top-bottom self-impedance probing
 2. Top-side DIMM sites for “near” transfer-impedance probing
 3. Top-side DIMM sites for “far” transfer-impedance probing
 4. Bottom-side Memory Driver sites for “near” transfer-impedance probing.
 5. Bottom-side Memory Driver sites for “far” transfer-impedance probing.



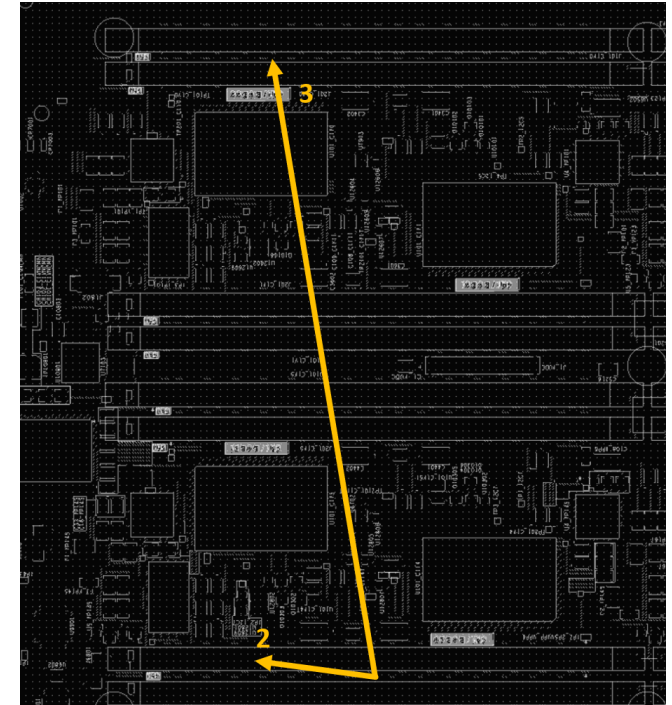
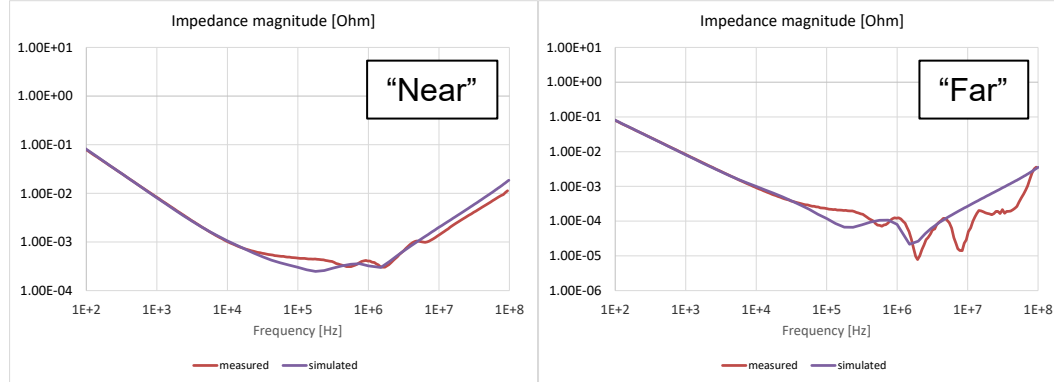
DUT2: AC Simulation and Measurements

- Site 1: self-impedance data
 - Capacitive region: good correlation
 - >10kHz: deviation between measurement and correlation (Hybrid solver)



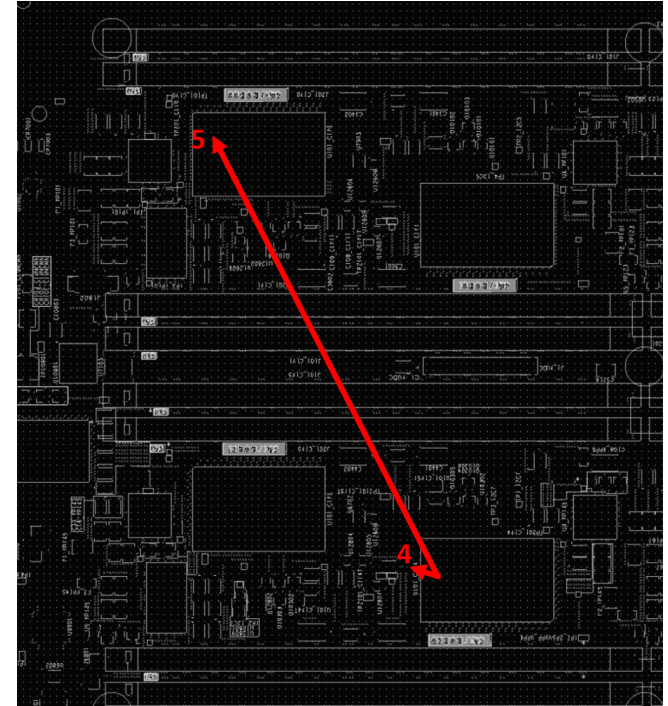
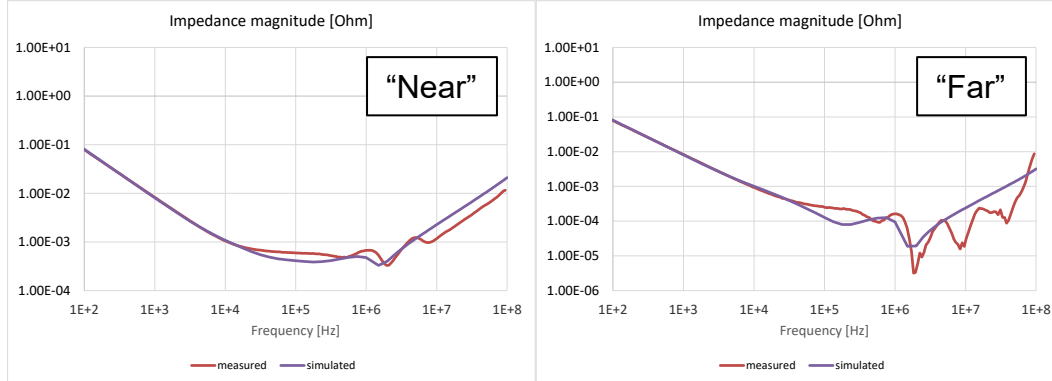
DUT2: AC Simulation and Measurements

- Site 2/3: DIMM sites' transfer-impedances
 - "Near" transfer-impedance
 - stays $>0.2\text{m}\Omega$
 - "Far" transfer-impedance
 - bottoms out around $0.1\text{m}\Omega$
 - Dips to 10s of $\mu\Omega$ at SRF of MLCCs
 - Correlation good given simulation used RLC models
 - Measurement's 8MHz dip believed to be due to Memory Drivers' on-package decoupling (not modeled in simulation)



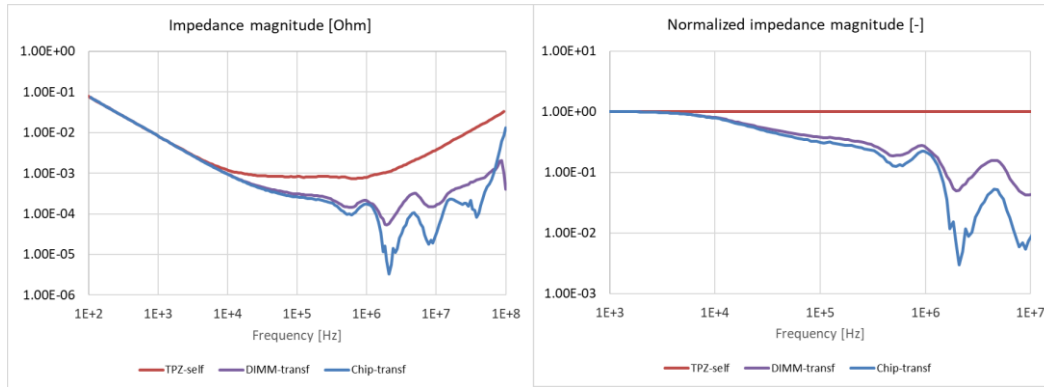
DUT2: AC Simulation and Measurements

- Site 4/5: Memory Driver sites' transfer-impedances
 - “Near” transfer-impedance
 - stays $>0.2\text{m}\Omega$
 - “Far” transfer-impedance
 - bottoms out around $0.1\text{m}\Omega$
 - Dips to 10s of $\mu\Omega$ at SRF of MLCCs
 - Correlation good given simulation used RLC models
 - Measurement's 8MHz dip believed to be due to Memory Drivers' on-package decoupling (not modeled in simulation)



DUT2: Filtering Effect

- Normalized transfer-impedance to self-impedance in order to estimate filtering transfer function: $\frac{Z_{21}}{Z_{11}} \sim \left(\frac{v_2}{i_1}\right) \cdot \left(\frac{i_1}{v_1}\right) = \frac{v_2}{v_1}$
- Cutoff frequency ~10kHz for both DIMMs and Memory Drivers
 - <10kHz: little deviation showing effective “lumped” region. Filtering here due to DC resistance of planes
 - 10kHz – 1MHz: RC filtering region due to plane’s DC and ‘skin’ resistances and net capacitance on plane
 - Transfer function slope ~10dB/dec, $\propto \sqrt{f}$, (skin resistance)
 - SRF of 47uF and 4.7uF MLCCs visible



- Normalized transfer-impedance to self-impedance in order to estimate filtering transfer function: $\frac{Z_{21}}{Z_{11}} \sim \left(\frac{v_2}{i_1}\right) \cdot \left(\frac{i_1}{v_1}\right) = \frac{v_2}{v_1}$
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 - Transfer function slope ~10dB/dec, $\propto \sqrt{f}$, (skin resistance)
 - SRF of 47uF and 4.7uF MLCCs visible



CONCLUSIONS

- We were able to achieve decent simulation/measurement correlation for two different DUTs (DUT1: AI Application, DUT2: High Intensity Compute Application)
- VNA-base two port shunt-thru impedance measurement setup shown to achieve $10\mu\Omega$ noise floor when crosstalk calibration (isolation) step is used
 - **Noise floor shown to be reduceable to $1\mu\Omega$ with improved setup!**
- We considered the spatial filtering effects of the passive PDN and their physical roots
 - Low frequency RC cutoff due to net capacitance and plane resistance in $\sim 10\text{kHz}$ range
 - SRF of PCB AND package-level MLCCs appear in high frequency ranges of the self and transfer impedances seen from the PCB
- Target impedance methodology cannot be replaced but it can be adapted and optimized for our individual applications as we consider the different noise sources and filterings living in our PDN



Thank you!

QUESTIONS?

Ethan Koether

Sr. Signal and Power Integrity Engineer, Amazon Project Kuiper

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