Probes and Setup for Measuring Power-Plane Impedances with Vector Network Analyzer

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Abstract:
Power-distribution planes in multilayer printed-circuit boards of high-speed systems target for low impedances. While several methods have been developed to simulate the characteristics of parallel planes, verification by measurements is lagging behind, primarily because the probing and measurement setup for wide-band low impedances on a digital board is not trivial. Impedance analyzers and VNAs in one-port setup are loosing accuracy toward low impedances. The paper describes a probe arrangement and measurement setup based on HP8720D and 4396A VNAs to measure self and transfer impedances of power-distribution planes. The accuracy at low impedance values is improved by making two-port measurements for self-impedances as well, which places the uncertainty of connecting discontinuities in series to the system's 50 ohm impedance rather than in series to the low plane impedances to be measured. The measurement results were compared against simulated impedances of the same structures.

Authors/speakers:
Istvan Novak
Current activities
Istvan is signal-integrity staff engineer at SUN Microsystems, Inc. Besides of signal-integrity verification of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks, bypassing and decoupling of printed-circuit boards of workgroup servers. He creates and uses SPICE models, and develops measurement techniques for the power-distribution networks.

Istvan's background
Istvan has 25 years of experience with high-speed digital, RF, and analog circuit and system design as well as in teaching related subjects at university regular courses and industry short courses. He is Fellow of IEEE for his contribution to the signal-integrity and RF measurement and simulation methodologies. Istvan received his masters degree from the Technical University of Budapest, Budapest, Hungary, and his PhD from the Hungarian Academy of Sciences.

Slide 2:

Outline

- Introduction
- Z, Y, and S parameters
- Self and transfer impedances
- VNA
- One-port impedance measurement
- Two-port impedance measurement
- DUTs
- Measured self and transfer impedances
- Correlation to simulations
- Resources
- References

Slide 3:

Requirements in Power Distribution

In digital and mixed analog/digital systems:

- Core and signaling voltages drop
- Noise margin goes down
- Core and total I/O current go up
- Bandwidth goes up

Requirement:

Few milliohms over hundreds of MHz bandwidth.

Solution:

In multilayer boards, power and ground are distributed over (solid) planes.

For many years of digital electronic designs, a +5V supply voltage for TTL and CMOS logic, and /or a -5.2V supply for an ECL logic was common. With the submicron silicon feature sizes, however, the breakdown voltage of the structure limits the supply voltage at below 5V, both in the core and in the I/O area. At the same time, the constantly growing demand for higher data throughputs results in wider buses. To avoid the runaway of total current requirements of the wider buses, and to reduce the potential EMI risk, too, the signaling voltage drops steadily from generation to generation. Because in every new generation new functionality is added, the growth of the number of I/O lines usually outweighs the decrease of current in one I/O, therefore the net supply current demand is still on the rise. The lower signaling voltage calls for a lower value of tolerable noise on the supply rails, which together with the higher current consumption dramatically reduces the

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impedance that should be provided by the power-distribution network [1]. The faster bus signaling also comes with faster edges and transients, requiring a proportionally wider bandwidth in the power-distribution network. A high-end system with single-ended signaling today may have 10A total transient current in the signal-return paths of buses, and may require 50mV maximum ripple on the power-distribution network. This converts into 5 milliohms of power-distribution impedance. With a 0.6…0.3nsec signal transition time, the required bandwidth for the 5 milliohm power-distribution impedance is 500-1000MHz. In multilayer printed circuit boards, the wide-band low-impedance power distribution is typically provided by dedicated ground and power copper layers with an array of bulk and high-frequency bypass capacitors. This paper describes probes, instrumentation, and a measuring method which is suitable for measuring low impedance values over a wide frequency range.

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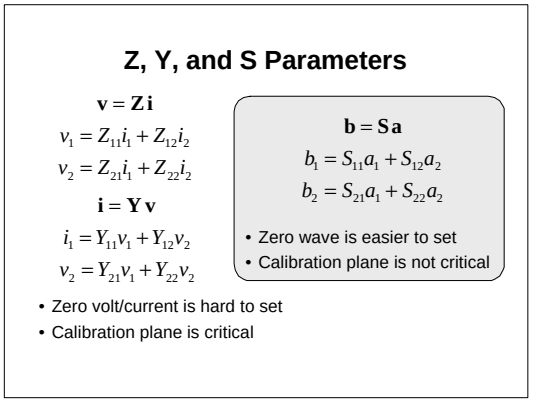

Before we decide what and how to measure, we need to look at the available options. We assume that the power-distribution network is linear, because it consists of power/ground planes and a set of capacitors. This network is later connected to the active devices at N nodes, and at every node the active device may inject a given amount noise current into the power-distribution network, and at every one of the N nodes we may want to calculate/measure the noise voltages as a result of these injected noise currents.

If we know the injected currents and one set of parameters of the power-distribution network, the voltages at the nodes can be calculated. We assume that we know the noise currents, and our goal here is to determine (by measurements) a suitable set of parameters for the power-distribution network.

A linear electrical network with N ports can be described by one of several sets of parameters. Here we consider three of these, the Z, Y, and S parameters. The Z and Y parameters relate voltages at the ports to currents. To obtain one of the Z or Y parameters, one has to measure the voltage or current at the respective port(s) while the other ports are left open or shorted, respectively. The slide also shows the network equations for two ports. We see from the equations of Z parameters, for instance, that when we set $i_2=0$, from the first equation we get $Z_{11}=v_1/i_1$ as the open-terminated input impedance at node1, and from the second equation we obtain $Z_{21}=v_2/i_1$ as the open-terminated transfer impedance from node1 to node2. In the rest of the paper we call all of the Z_{ii} parameters as self impedances (at node i) and all Z_{ji} parameters as transfer impedances (from node I to node j).

While this is a convenient way of measuring at low frequencies, providing short and open at hundreds of MHz frequencies is a difficult task. To overcome this problem, the S (scattering) parameters relate incident and reflected waves at the ports. To obtain one specific scattering parameter, the incident and reflected wave at the selected ports must be measured while the incident wave at the other ports should be zero. Zero incident wave at nonexcited ports can be achieved by connecting the reference impedance (usually 50 ohms) to those ports. Because wideband precision terminations are easier to make (and connect to the device under test) than open or short, high-frequency measurements almost exclusively use S parameters to describe networks.

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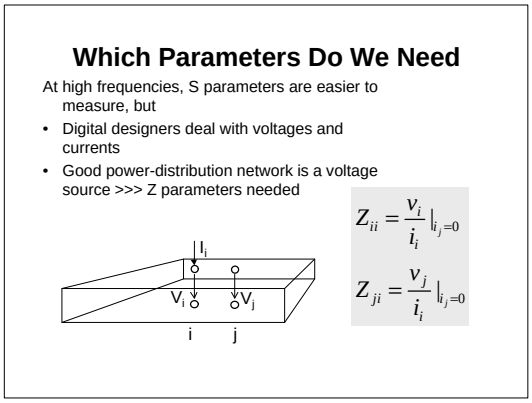

Even though scattering parameters are easier to measure, in digital designs, and especially in the power-distribution networks, the usual parameters are voltages and currents. Also, if the power-distribution network (the power and ground planes together with the array of bypass capacitor) works well, its impedance should be much lower than the impedances of the connected active devices. This means that for considering noise injection, the active devices act more like current sources, and when we calculate the resulting noise voltages, the active devices have much higher impedances than the power-distribution network, effectively leaving the nodes open terminated. This kind of current input and voltage output arrangement corresponds to the Z parameter description of networks. We understand that because of practical reasons, we will have to measure S parameters, but eventually we want to convert the result to Z parameters.

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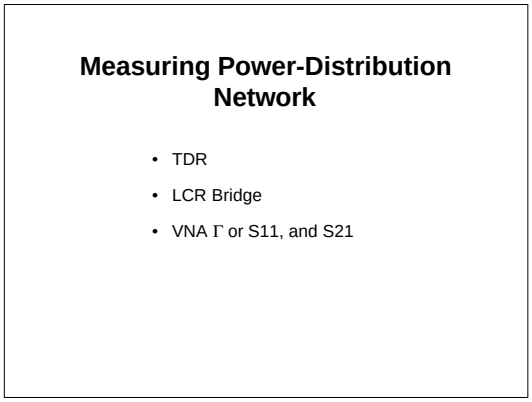

There are several options available to verify the power-distribution network impedances by measurements. Time-Domain Reflectometry (TDR) instruments launch a step wave into the device under test, and measure the composite waveform with a wideband oscilloscope. The noise and nonlinearity of the oscilloscope's front-end electronics and digitizer, however, limit the measurable impedances at a few tenth of an ohm. The Tektronix 11801 mainframe with an SD24 TDR plug-in would launch a 250mV step wave, and measure the waveform through an 8-bit digitizer, with an approximate noise floor of 0.5mV, which corresponds to an impedance magnitude of 0.1 ohms. RLC meters are also usually not suitable for measuring sub-ohm impedances at hundreds of MHz frequencies. Vector-Network Analyzers can be used to measure the scattering parameters of devices. As we will see, the higher dynamic range of the vector-network analyzers together with the suggested two-port self-impedance measurement setup is usable for wide-band low-impedance measurements. From the scattering parameters, the required self and transfer impedance values will be calculated.

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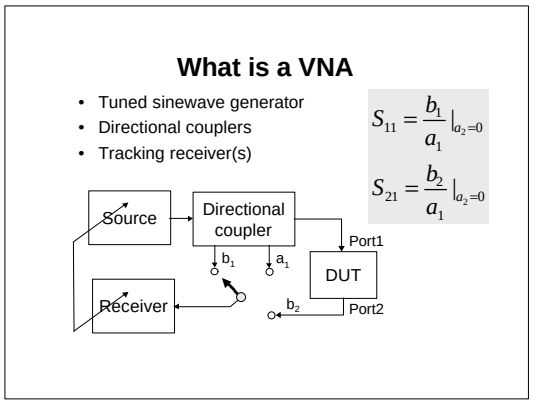

The vector-network analyzer is an instrument for measuring scattering parameters [2]. A synthesized tuned source with calibrated source impedance and calibrated source voltage generates the incident wave at the excited port. The signal is connected to Port1 of the device under test through a directional coupler which separates the a_1 and b_1 incident and reflected waves, respectively. Port2 of the device is terminated in the reference impedance, and the wave appearing at that port is b_2. A selective

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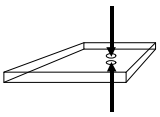
receiver is used to measure the incident and reflected waves at the ports. If the network to be measured has more than two ports, we can excite one by one all of the ports.

Because the frequency of the test signal is exactly known, the sensitivity and accuracy of the measurement is readily improved by locking the receive frequency to the transmit frequency, and/or by using averaging.

Slide 8:

One-Port Self-Impedance Measurement



$$S_{11} = \frac{Z_{in} - 50}{Z_{in} + 50}$$

$$Z_{11} = Z_{in} = 50\frac{1 + S_{11}}{1 - S_{11}}$$

The impedance is measured between the ground and power planes at the selected point

At the selected location of the power-distribution network, the calibrated Port 1 of the vector-network analyzer is connected between the planes, and the voltage-reflection coefficient reading (S_{11}) is taken. The traditional one-port impedance measurement with a vector-network analyzer uses then the inverted formula of the voltage-reflection coefficient to calculate the impedance.

Slide 9:

Errors of One-Port Self-Impedance Measurement

- VNA accuracy is lower at high reflections
- Connecting discontinuity is in series of low-Z DUT

The one-port impedance measurement with vector-network analyzers suffers from two fundamental drawbacks when low impedance values are measured. The low impedance creates an almost full reflection, therefore the incident and reflected wave magnitudes are similar. The low impedance value must be resolved from the difference of the two waves with almost equal magnitude, therefore the measurement errors increase very sharply with low impedance values. Similarly, any discontinuity between the calibrated VNA port and device under test appears in series to the low-value measured impedance.

Slide 10:

VNA Error in S11 Measurement

- |S11| uncertainty of HP8720D is 1.5% at |Γ|~1 in the 50-2000MHz range
- Impedance uncertainty is 0.375 ohms
- For low measurement errors, Z_{DUT} must be in the ohms range

But we want to measure fractions of an ohm

The measurement uncertainty of the Hewlett Packard 8720D vector-network analyzer in one-port impedance measurements depends on the frequency and measured value of voltage reflection coefficients. In the 50-2000MHz frequency range, the uncertainty is 0.004 near zero reflection coefficient, and it rises to 0.015 at full reflection. The 1.5% error near full reflection means that when measuring low impedances, the uncertainty is 50*0.015/2 = 0.375 ohm. This makes it impossible to measure impedances in the hundred milliohm range or lower; only impedances in the ohm range and above can be measured with reasonable accuracy.

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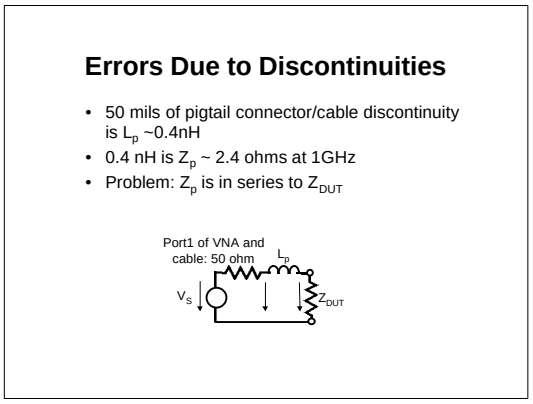
Slide 11:

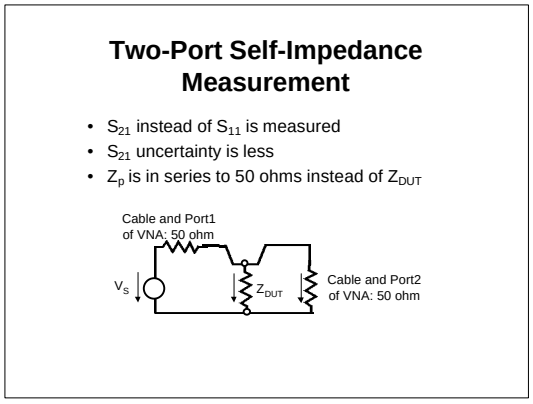


Another source of errors in one-port impedance measurements is the discontinuity between the device under test and the calibrated vector-network analyzer port. With an estimated 50 milliinches length of inductive discontinutiy, the corresponding 0.4nH inductance amounts to about 2.4 ohms at 1 GHz. The discontinuity is in series to the low impedance of the device under test, and without a deembedding procedure we can only measure the series equivalent of the impedances of the DUT and discontinuity. The result is that at higher frequencies the impedance reading will be higher than the true impedance to be measured. With a resistive DUT and inductive discontinuity impedance, the cutoff frequency above which the measured reading departs from the DUT impedance is given by:

$$f_c = \frac{R_{DUT}}{2pL}$$

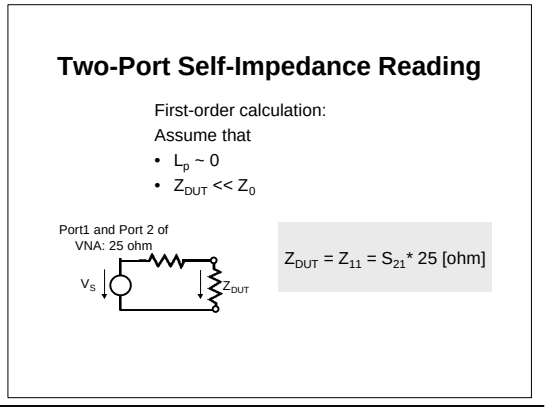
The corner frequency is lower for lower DUT impedances. With 0.4nH inductance and 0.1 ohms DUT resistance the corner frequency is approximately 40MHz, which is more than a decade lower than the estimated measurement bandwidth requirement.

Slide 12:



To achieve reasonable accuracy for low DUT impedance values, the two-port self-impedance measurement makes use of both ports of the vector-network analyzer, and its operating principle is similar to the four-wire measurements of very low resistances. Rather than sending the test signal and sensing the receive signal on the same port of instrument, in the two-port measurement Port1 is used only to launch a current through the unknown impedance, while Port2 is used to measure the voltage drop across the unknown impedance. This way we take the S_{21} transfer parameter reading from the VNA instead of S_{11}. We need to remember though that in this particular connection arrangement the S_{21} transfer parameter refers to one single node on the DUT, since both Port1 and Port2 of the VNA are connected to the same point on the DUT. With low impedances, the uncertainty of S_{21} measurements is much less than that of the corresponding S_{11} readings, and the connecting discontinuity is now in series to the 50-ohm VNA impedance rather than the low unkown impedance.

Slide 13:



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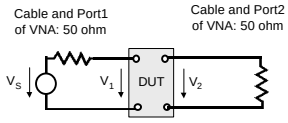
In a first-order approximation, we may neglect the discontinuity which is now in series to 50 ohms, and we also assume that the impedance to be measured is much less than 50 ohms. With these assumptions, the equivalent circuit of the setup is a voltage divider between the two times 50 ohms port impedances of the VNA in parallel and the unkown impedance of device under test. If we calibrate and set the S_{21} reading of VNA without the DUT to zero dB, the unknown impedance is simply $Z_{DUT} = S_{21}*25$. Here both Z_{DUT} and S_{21} may be complex values, and S_{21} is the dimensionless ratio of the output and input waves. If the magnitude of S_{21} is obtained on a dB scale from the VNA, it can be converted into its dimensionless equivalent by using:

$$S_{21} = 10^{\frac{S_{21}[dB]}{20}}$$

Slide 14:

Transfer Impedance Measurement



In the transfer-impedance measurement setup, Port1 of the VNA is used to launch a current at a selected input point of the DUT, while Port2 is used to measure the voltage at another point of the DUT. This time the S_{21} transfer parameter reading from the VNA is a true transfer parameter since the VNA ports are connected to different points on the DUT. With two selected connection points on the DUT, the transfer-impedance measurement can be taken either in one or the other direction. However, with just RLC elements in the bypass-capacitor bank and with commonly used printed-circuit-board planes, the power-distribution network is reciprocal. The reciprocity means that transfer parameters are the same regardless of the direction we look at them, therefore we know that for all i and j: $Z_{ij}=Z_{ji}$.

Slide 15:

Transfer Impedance Reading

First-order calculation:
Assume that
- $L_p \sim 0$
- $Z_{11} << Z_0$
- $Z_{22} << Z_0$
- $Z_{21} << Z_0$

$Z_{21} = Z_{12} = S_{21}* 25$ [ohm]

As a first-order approximation, the transfer-impedance value from the measured parameters can be calculated as follows. With no DUT, the through calibration is done and the S_{21} reading is set to 0dB (ratio=1). There is a 2:1 voltage divider formed by the two 50-ohm impedances of the VNA, therefore this corresponds to $V_s=2$, and $V_1=V_2=1$ voltages. We further assume that all DUT impedances are much smaller than the 50-ohm VNA impedance, so that the i_1 input current is simply the shunt current of the source: $i_1=2/50$. The measured $v_2 = Z_{21}*i_1$ output voltage is equal to the S_{21} reading, therefore $Z_{21}=25*S_{21}$. Note that this is the same expression that we had for the two-port self-impedance reading.

Slide 16:

S21 Uncertainty

- $|S_{21}|$ uncertainty of HP8720D:
  <1dB in the $|S_{21}|$ > -60dB range
  <3dB in the $|S_{21}|$ > -70dB range
- Impedance uncertainty:
  1dB (10%) for Z_{DUT} > 25milliohms
  3dB (40%) for Z_{DUT} > 8milliohms

The uncertainty of S_{21} reading is a function of frequency and S_{21} magnitude. The uncertainty gets bigger at lower frequencies and lower readings. For the Hewlett Packard 8720D vector-network analyzer, the uncertainty is less than 1dB and 3dB at any frequencies between

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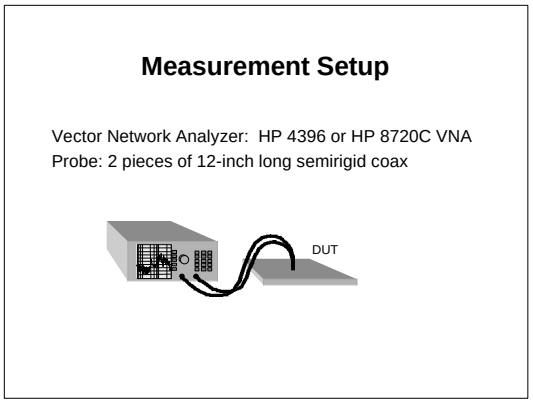
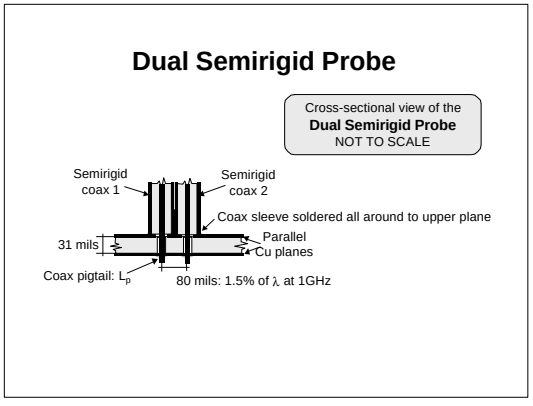
50MHz and 20GHz as long as the S_{21} reading is above -60dB and -70dB, respectively. This corresponds to a 1dB and 3dB impedance-reading uncertainty of 25 milliohms or higher and 8 milliohms or higher, respectively.

Slide 17:



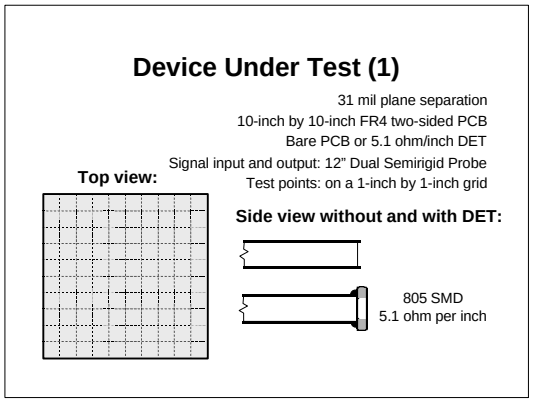
To measure the impedances of power-distribution networks, two Hewlett Packard vector-network analyzers were used. The model HP4396A covers the frequency range of 100kHz to 1.8GHz, while the HP8720D model covers the frequency range of 50MHz to 20GHz. The power-distribution network was connected to the VNAs through two pieces of 12-inch long semirigid 50-ohm coax cables.

Slide 18:



The probe connection to the DUT was selected to match the conditions on digital multilayer printed-circuit boards. Even though repeatable measurements and easy calibration would call for snap-on or screw-on type coaxial connectors, on digital production boards one could hardly find the room for those. Instead, a direct soldered open pigtail connection was selected. The DUT had through holes at the selected test points to accommodate the center pins of the semirigid coax cable. For self-impedance measurements, at every test points the DUT had two through holes with an approximately 80 mils separation, so that the 80-mil semirigid coax cables could be connected to the DUT right next to each other. In one DUT, the sleeves of the semirigid cables were soldered to the corresponding copper plane all around the sleeve. In another DUT the connection to the sleeve was done by two copper wires on the opposite sides of the semirigid sleeve, going and soldered to through holes in the DUT. Up to 1GHz frequency, there was no noticeable difference in the impedance reading with the two methods of coax-sleeve connection.

Slide 19:



Several different DUTs were built to verify the measurement method. One set of boards were made of 31-mil FR4 cores, where the two copper layers on the opposite sides were directly accessible to hook up the probes. The size of the boards was 10 inches by 10 inches. The appropriate through holes were drilled on a one-inch grid. Some of these test boards were totally bare and unpopulated, while some had Dissipative Edge Termination resistors [3] connected to the boards. The Dissipative Edge Termination (DET) was implemented by 5.1-ohm 805 size resistors at every inch of the board periphery.

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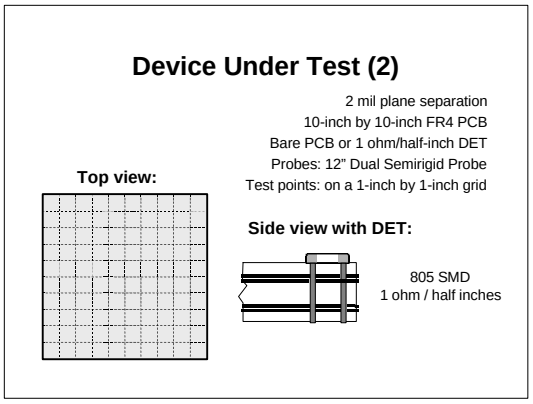
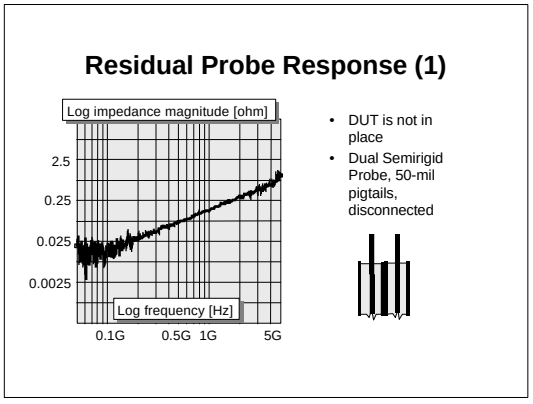
Slide 20:



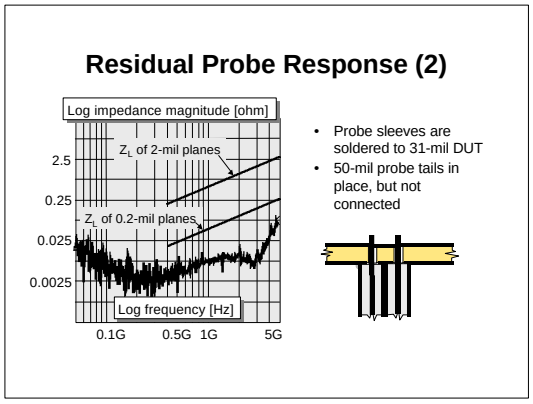
A second set of DUTs used 2-mil ZBC2000 cores in the stackup. For symmetry reasons, two 2-mil cores were used, each starting at about 8 milliinches below the surface of the board. The center was filled so that the total thickness of the board was around 90 mils. The size of the boards was 10 inches by 10 inches. The appropriate plated through holes for the test points were on a one-inch grid. Some of these test boards were totally bare and unpopulated, while some had DET. The Dissipative Edge Termination was implemented by 1-ohm (or 1-ohm in series to 100nF) 805 size components at every half inches along the board periphery. Note on the side view of the DUT that all test points and DET components were connected only one of the 2-mil cores. Since on this test board the power-ground planes (similarly to a real multilayer board) were not directly on the surface, to minimize the effect of the via inductance, at every connection points multiple plated through holes were used.

Slide 21:



To measure the self impedances of DUT, the two probes should ideally be connected to the same points on the DUT. In the actual connection, the open pigtails of the semirigid cables were 80 mils apart, which distance is determined by the cable diameter. The pigtail wires are then close enough that the direct feedthrough between the open wire portions should be looked at. To characterize the residual feedthrough of the self-impedance measurements with the two closely-spaced semirigid probes, first the reading was taken with the probes only, no DUT in place. The vertical impedance scale on the graph was converted from the S_{21} readings with the $Z=25*S_{21}$ approximative formula. Note that up to 1GHz, the residual reading is below 0.15 ohms. This residual reading, which comes mostly from the capacitive feedthrough between the open pigtails, would not allow us to measure power-distribution impedances in the milliohm range. However, as we see on the next slide, the presence of the DUT significantly reduces this error.

Slide 22:



Next, the residual feedthrough reading of the dual semirigid probe was taken with the 31-mil DUT. On one side, the semirigid sleeves were soldered to the copper plane. The pigtails were in the through holes, but were not soldered to the other copper plane. The vertical impedance scale on the graph was again converted from the S_{21} readings with the $Z=25*S_{21}$ approximative formula. Note that up to 3 GHz, the residual reading is below 25 milliohm, and in the 100MHz to 1GHz frequency range it is below about 10 milliohms. The residual feedthrough is reduced by the DUT itself: while the higher dielectric constant of the FR4 material increases

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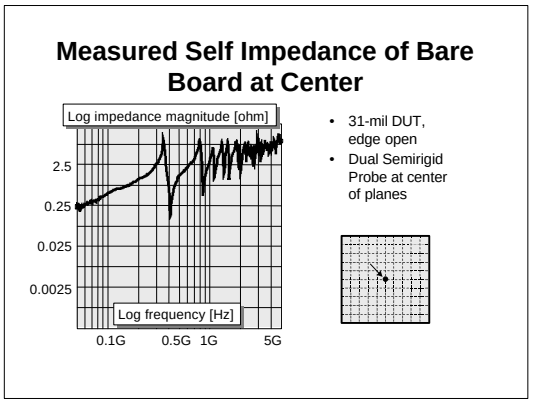
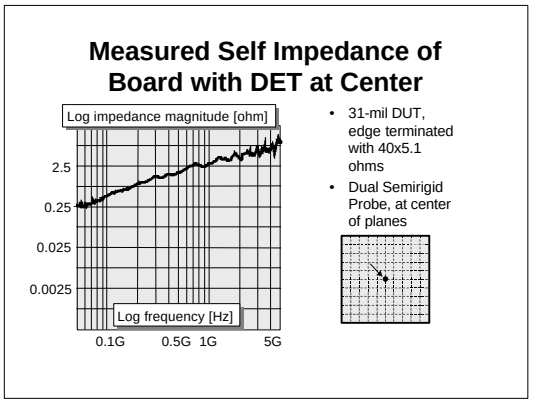
the capacitive coupling between the pigtails, the copper-plane parts connected to the grounded sleeves counterbalances this effect. For comparison purposes, the chart also shows the approximate impedance of the inductance of a pair of power/ground planes with 2 mil and 0.2 mil separation. We see that the residual reading of the dual-probe measurement arrangement is sufficiently low that it will not seriously degrade the self-impedance measurement of the presently used printed-circuit board planes.

Slide 23:



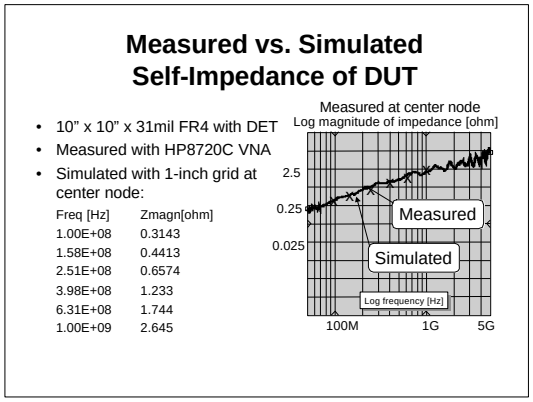
The slide shows the self-impedance of the 31-mil bare DUT measured at the center. The instrumentation was the Hewlett Packard HP8720D VNA with the 12-inch dual semirigid probe described above. The graph clearly shows the resonances of the planes due to the open edges.

Slide 24:



The Dissipative Edge Termination [3] was used to reduce the reflections from the open edges of the planes, and to create a smooth impedance profile. The vertical impedance scale on the graph was converted from the S_{21} readings with the $Z=25*S_{21}$ approximative formula.

Slide 25:



To verify the measuring method and the expression to convert the S_{21} readings into self-impedance values, the self and transfer impedance profiles of the 31-mil FR4 DUT with DET were simulated and compared against the measured values. The simulation was based on the commonly used transmission-line grid equivalent circuit [4], [5]. The simulation used lossless Tline elements with a one-inch grid. Simulations were done with ideal current source and infinite sensing impedance to obtain true Z_{11} values, and also with the 50-ohm VNA source and load impedance as well as the estimated pigtail discontinuity taken into account. It was found that up to 1GHz the 50-ohm VNA impedance and the pigtail discontinuity had very little effect on the simulated self impedance values. The vertical impedance scale on the graph was converted from the S_{21} readings with the $Z=25*S_{21}$ approximative formula. The measured results are shown as a continuous trace, while the simulated impedance values are shown by crosses, and also listed in tabular form.

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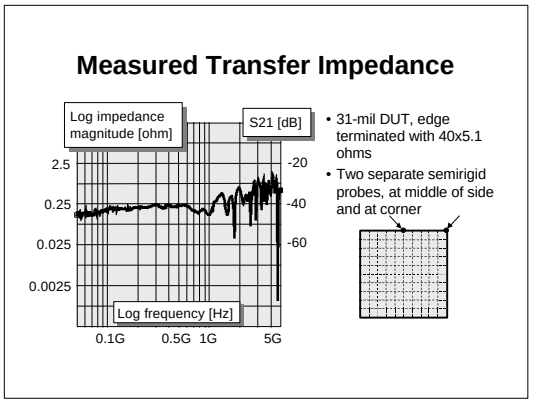
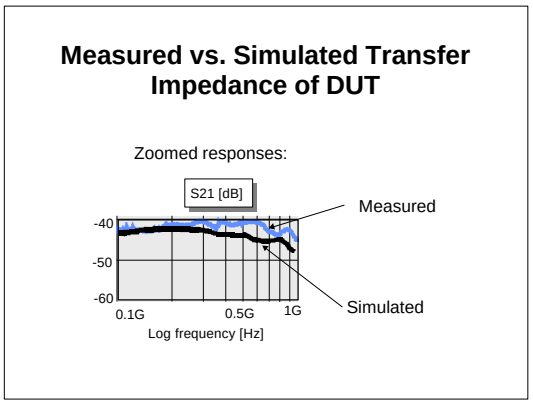
Slide 26:



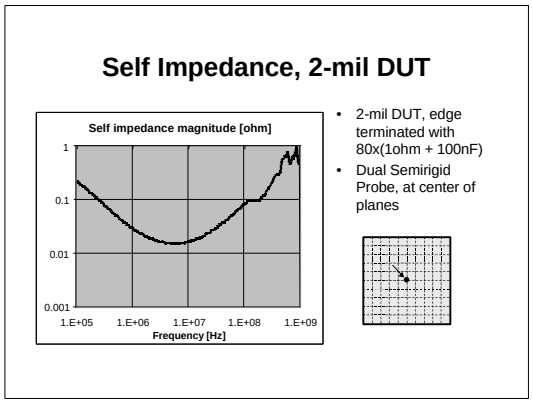
The transfer impedances were also measured between different test points. The slide shows the transfer impedance from the middle of one side of the square to the nearest corner. The DUT had 31-mil plane separation, and the same 5.1 ohm per inch DET as for the earlier measurements. Here too, the vertical impedance scale on the graph was converted from the S_{21} readings with the $Z=25*S_{21}$ approximative formula. On the right side, the graph includes the original dB scale for the S_{21} readings.

Slide 27:



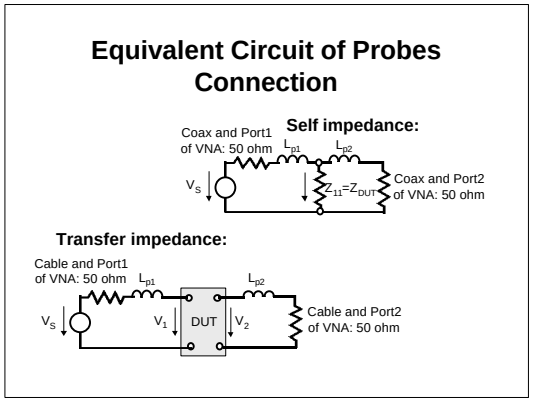
To verify the measuring method and the expression to convert the S_{21} readings into transfer-impedance values, the measured transfer-impedance profile was compared against simulated values. The SPICE model for the planes was the same as for the self-impedance simulation. Two different simulations were done: one with an ideal current source and infinite sensing impedance to obtain true Z_{21} values, and another with the 50-ohm VNA source and load impedance as well as the estimated pigtail discontinuity taken into account. It was found that for the transfer impedance simulations the VNA impedance and the pigtail discontinuity made a noticeable difference, therefore instead of using the approximate $Z=25*S_{21}$ formula for the conversion, the simulation used the VNA and pigtail impedances and computed the S_{21} -like parameter in SPICE. On the slide, a zoomed portion of the comparison chart is shown in the 0.1 to 1GHz frequency range.

Slide 28:



The second set of DUTs with 2-mil ZBC2000 cores were measured with both the HP8720D and HP4396A vector-network analyzers. The slide shows the self-impedance profile of the 10-inch by 10-inch DUT measured at the center with the dual semirigid probe and HP4396A VNA. The DUT had 1-ohm and 100nF RC dissipative edge termination at every half inches.

Slide 29:



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To further analyze the error introduced by the discontinuity between the semirigid probe and the DUT, as well as to provide a more accurate transformation from the measured S_{21} readings to the self and transfer impedances, the equivalent circuits shown on the slides were created [6]. The equivalent circuits assume that the interconnection discontinuity is lumped and inductive within our entire frequency range of interest. In general, the discontinuities on the two connections may be different L_{p1} and L_{p2} inductances are assumed on side 1 and side 2, respectively.

Slide 30:

S_{21} Conversion to Self Impedance

$$Z_{ii} = S_{21}\frac{Z_1}{2}\frac{1}{1-S_{21}\frac{Z_1+Z_2}{2Z_2}} \approx S_{21}*25*\frac{1+jwt_p}{1-S_{21}}$$

Where $Z_1 = 50+j\omega L_{p1}$

$Z_2 = 50+j\omega L_{p2}$

$\tau_p = L_p/50$

By solving the Z-parameter circuit equations, the Z_{ii} self-impedance parameter can be expressed in terms of the measured S_{21} transfer ratio. For the self-impedance expression the result depends only on the self impedance of DUT at the measured point, and the transfer-impedance parameters have no effect on this reading. The expression can be simplified if we assume that the two discontinuities are equal: $L_{p1}=L_{p2}$. This yields the expression on the right, which contains the $25*S_{21}$ main term, which was used in the approximate calculations, multiplied by an error term. The nominator of the error term describes the frequency dependent error due to the inductive discontinuity. Its corner frequency is determined by the $L_p/50$ time constant. Assuming a 0.4nH inductance, the corner frequency is around 20GHz. The denominator of the error term depends on the S_{21} reading. This error is smaller when we measure lower values of impedances. When the measured impedance is 0.2 ohms or less, the denominator yields a less then 1% error.

Slide 31:

S_{21} Conversion to Transfer Impedance

$$Z_{ji} = S_{21}\frac{Z_1}{2}\frac{\left(1+\frac{Z_{11}}{Z_1}\right)\left(1+\frac{Z_{22}}{Z_2}\right)}{1+\frac{S_{21}Z_{21}}{2}\frac{Z_1}{Z_2}} \approx$$

$$S_{21}*25*\frac{1+jwt_p}{1+50*\left(\frac{S_{21}}{2}\right)^2}*\left(1+\frac{Z_{11}}{Z_1}\right)\left(1+\frac{Z_{22}}{Z_2}\right)$$

Where $Z_1 = 50+j\omega L_{p1}$

$Z_2 = 50+j\omega L_{p2}$

$\tau_p = L_p/50$

The Z-parameter equations can also be solved to obtain the Z_{ji} transfer-impedance parameter. If we assume that the two discontinuities are equal: $L_{p1}=L_{p2}$, the expression can be simplified to have the same $25*S_{21}$ main term, which was used in the approximate calculations, multiplied by an error term. The error term now is more complex, because the transfer parameter depends on the self impedances at both connection points as well. The nominator contains the frequency dependent error due to the inductive discontinuity, the same term we have in the self-impedance expression. The denominator now varies with the square of the S_{21} reading, this means that this error term diminishes even faster as we measure lower values of impedances. The other two multiplicative error terms depend on the self impedances at the two connection nodes, and their error values linearly go down as the self impedances of the DUT gets lower.

Slides 32:

Recommended Resources

Hewlett Packard Vector Network Analyzers:

- HP 8720 VNA
- HP4396 VNA

Circuit simulator software:

- Avant! HSPICE

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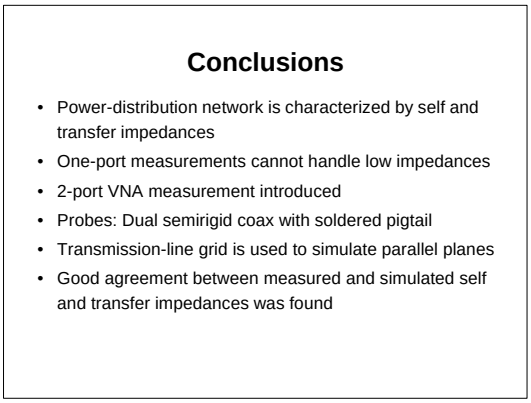
Slide 33:



References:

[1] Dale Becker, Larry Smith, "Power Distribution Design for High Performance Systems," Short course at the 1998 Topical Meeting on Electrical Performance of Electronic Packaging, October 26-28, 1998, West Point, NY

[2] Understanding the Fundamental Principles of Vector Network Analysis, Hewlett Packard Application Note 1287-1.

[3] I. Novak, "Reducing Simultaneous Switching Noise and EMI on Ground/Power Planes by Dissipative Edge Termination," Proceedings of the 1998 Topical Meeting on Electrical Performance of Electronic Packaging, October 26-28, 1998, West Point, NY, pp.181-184.

[4] E. Leroux, Peter Bajor, "Modeling of Power Planes for Electrical Simulations," Proceedings of the 1996 Wroclaw EMC Symposium, June 25-28, 1996.

[5] Henry Wu, Jeffrey Meyer, Ken Lee, Alan Barber, "Accurate Power Supply and Ground Plane Pair Models," Proceedings of the 1998 Topical Meeting on Electrical Performance of Electronic Packaging, October 26-28, 1998, West Point, NY, pp.163-166.

[6] Personal communications with Rich Hoft, Hewlett Packard, Burlington, MA.

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