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Transient Load Tester for Time Domain PDN Analysis

Ethan Koether (Oracle)
Istvan Novak (Oracle)

Speakers

Ethan Koether
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He is currently focusing on system power-distribution network design, measurement, and analysis. He received his master's degree in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology.

Istvan Novak
Senior Principal Engineer, Oracle
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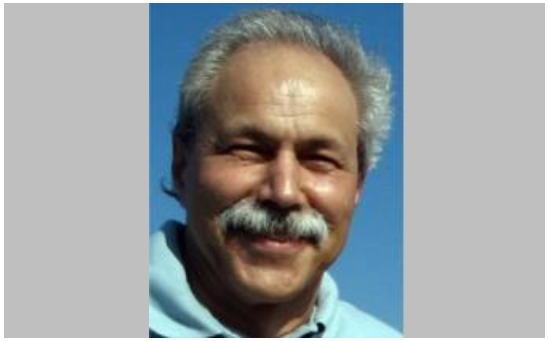
Besides signal integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is a Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies.



Outline

- Motivation for Time Domain PDN Validation
- Transient Load Tester Circuit Design
- The GaN FET
- Transient Load Tester Implementation and Performance
- Conclusion

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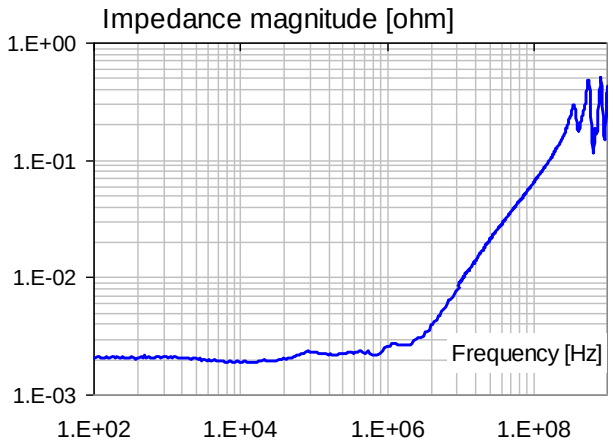
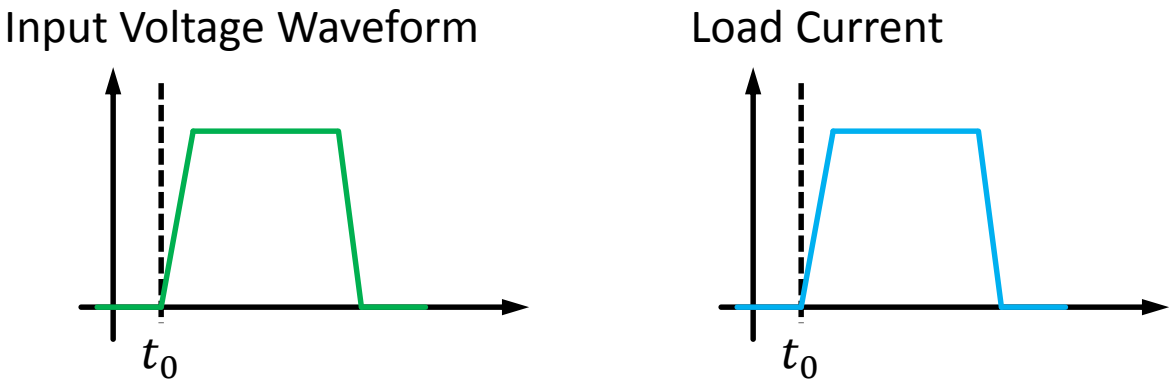
Target Impedance Methodology

- Estimates upper bound for rail's impedance
  - Voltage fluctuation on rail: ΔV
  - Maximum current step: ΔI
  - Target Impedance: $Z_{Target} = \Delta V / \Delta I$
- Valid for linear and time-invariant PDN
- Approximation unless impedance strictly resistive



Time Domain PDN Validation

- Load device under test (DUT) with current who's waveform follows input voltage waveform.



- For PDN design, can load DUT with worst case current in worst case time to analyze simulated behavior in live system.

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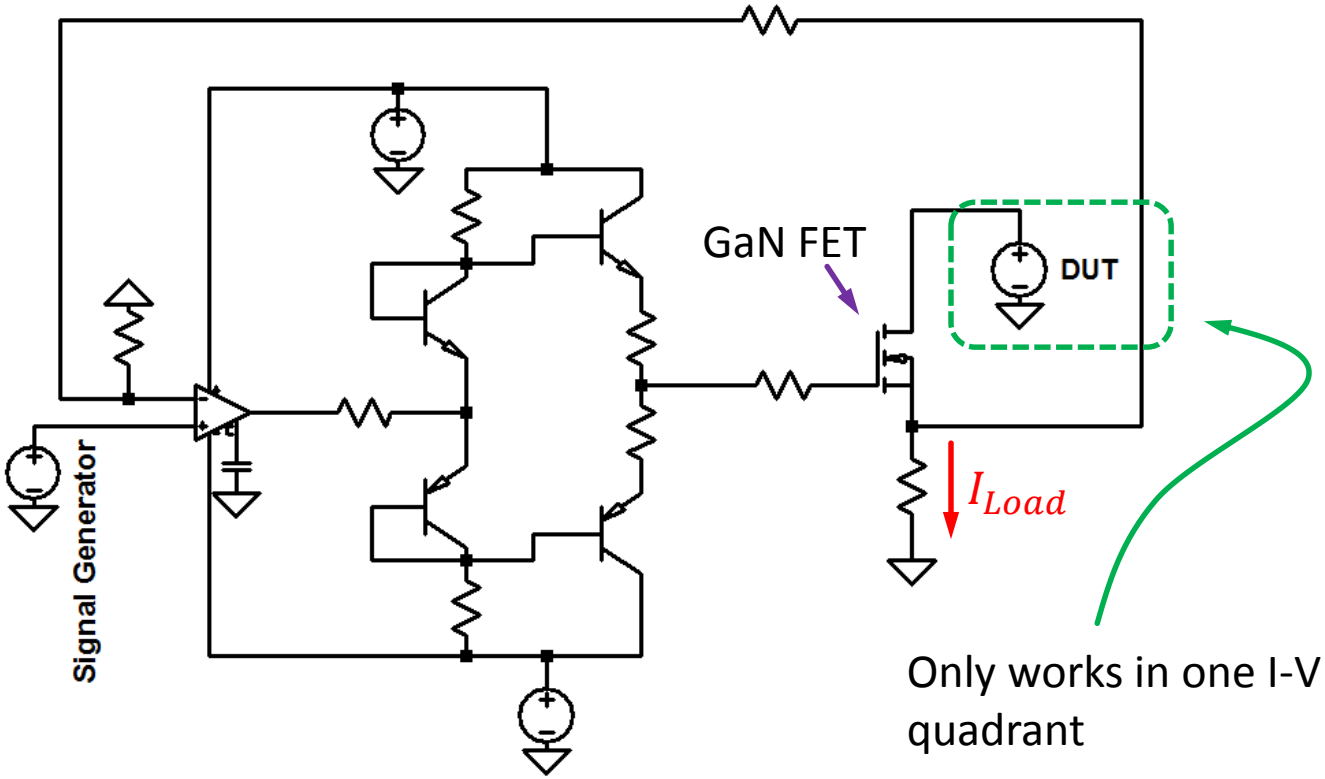
Transient Load Tester (TLT) Circuit Design



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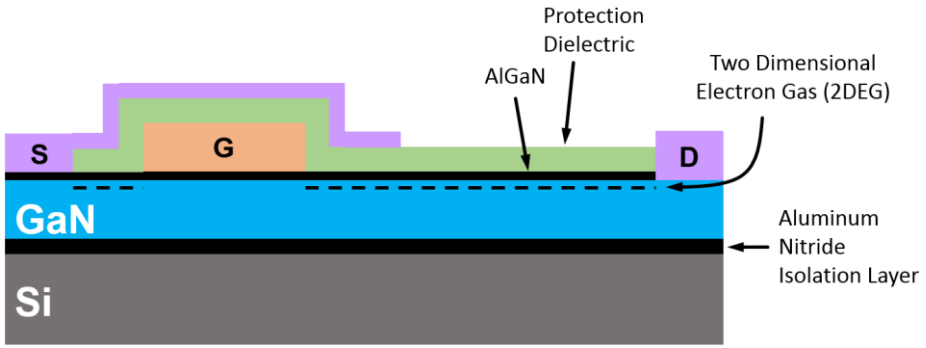
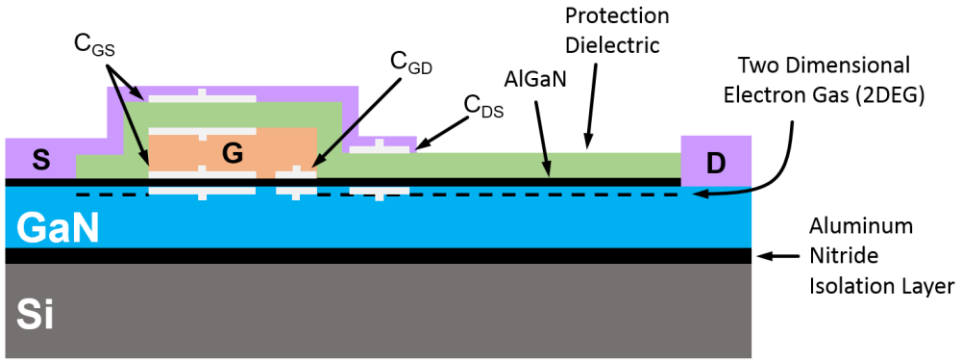
The Gallium Nitride FET (GaN FET)

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage (Continuous)	40	V
	Drain-to-Source Voltage (up to 10,000 5ms pulses at 150°C)	48	
I_D	Continuous (T_A = 25°C, $R_{\theta JA}$ = 6°C/W)	53	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	235	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	



The Gallium Nitride FET (GaN FET)

- The enhancement mode GaN FET used compared to silicon MOSFETs with similar electrical characteristics:
  - Faster switching speeds and shorter delay time
    - C_{GD} is exceptionally small in value
    - C_{GS} is relatively small in value
    - Lower threshold voltage
    - Lower package inductance
  - Lower $R_{DS(ON)}$



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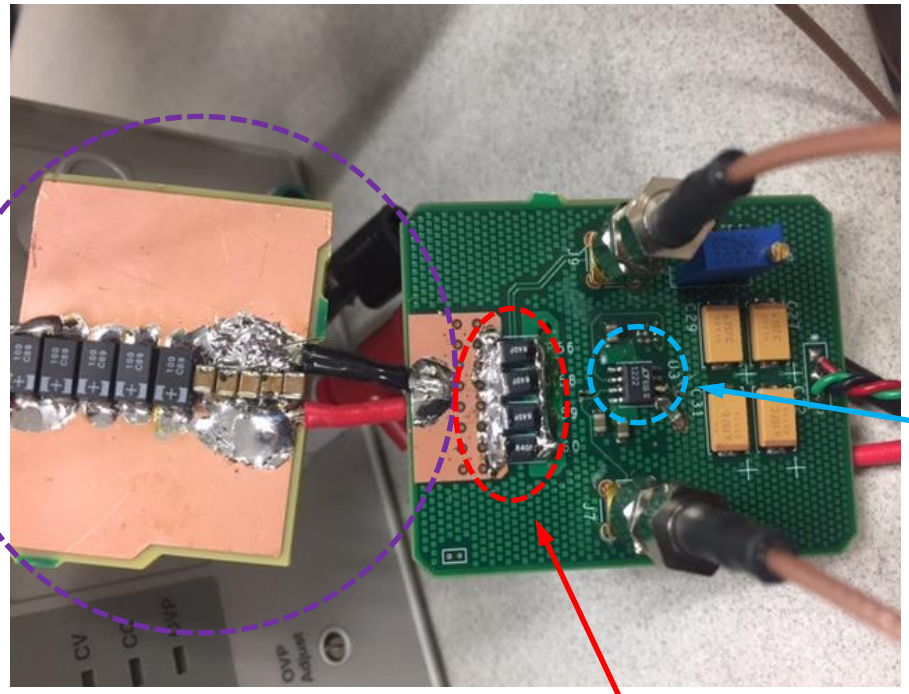
TLT Circuit Breadboard Implementation



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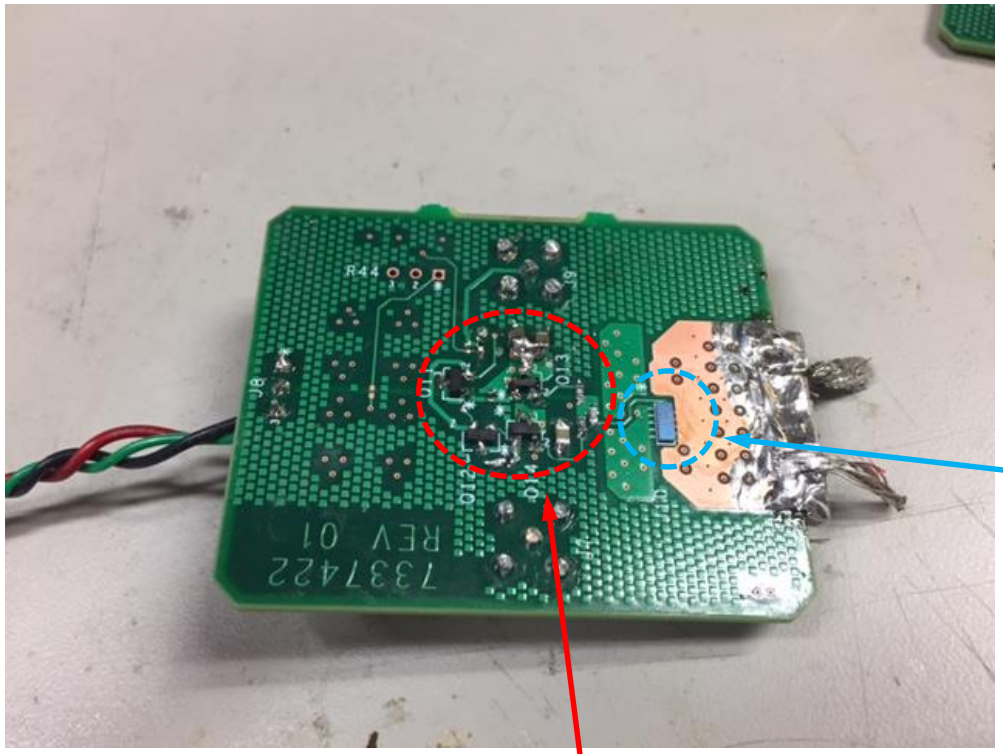
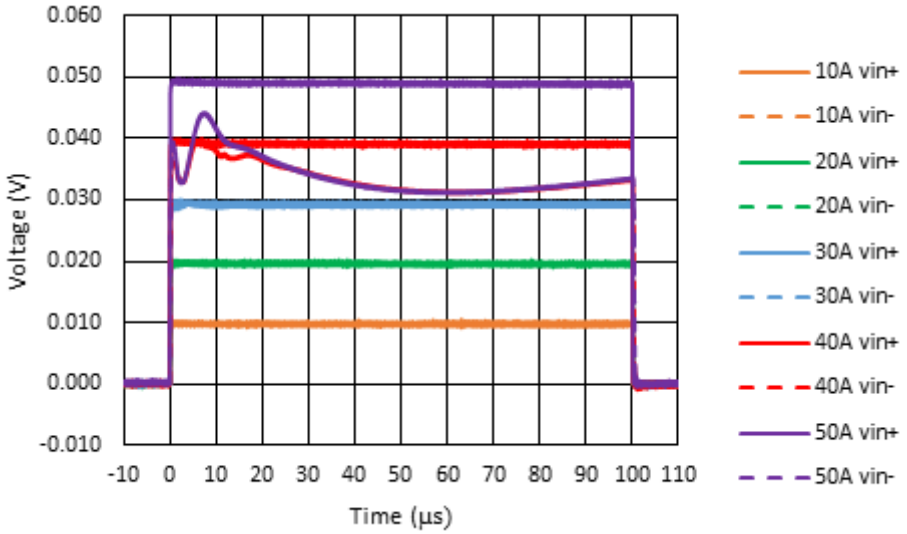


TLT Implementation and Test Results

- TLT voltages measured at inverting and non-inverting inputs of op amp
- For figure below: DUT voltage of 1V, rise/fall times of 100ns



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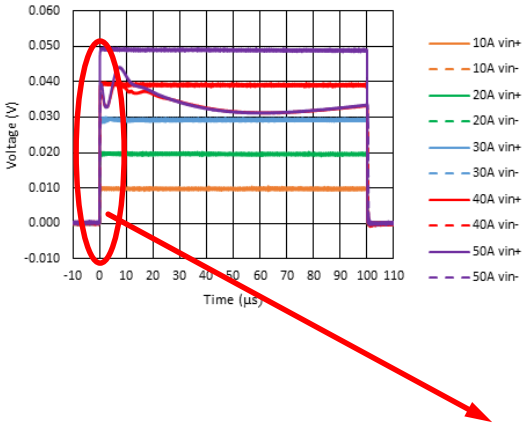
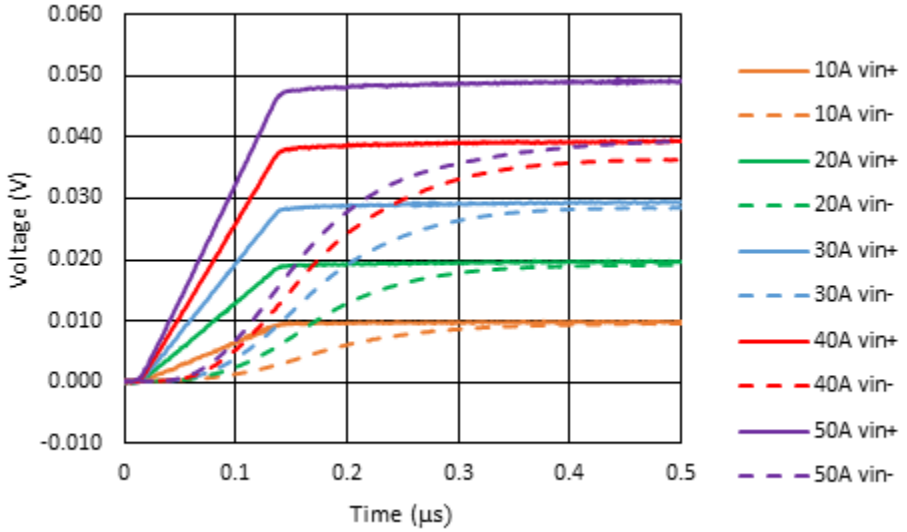
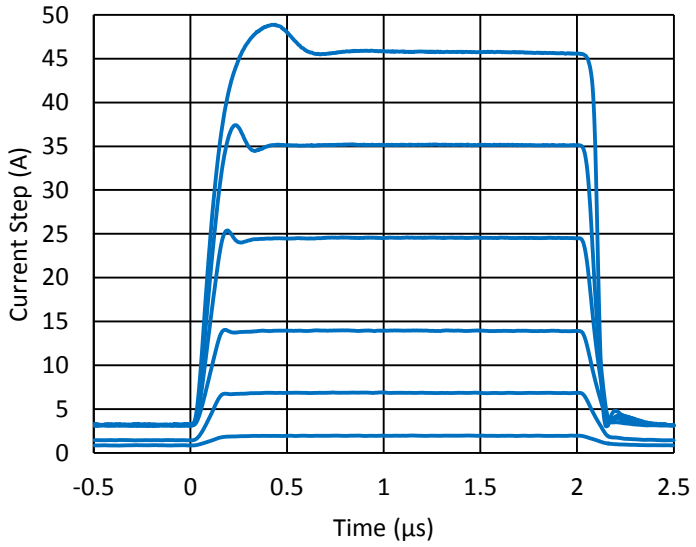




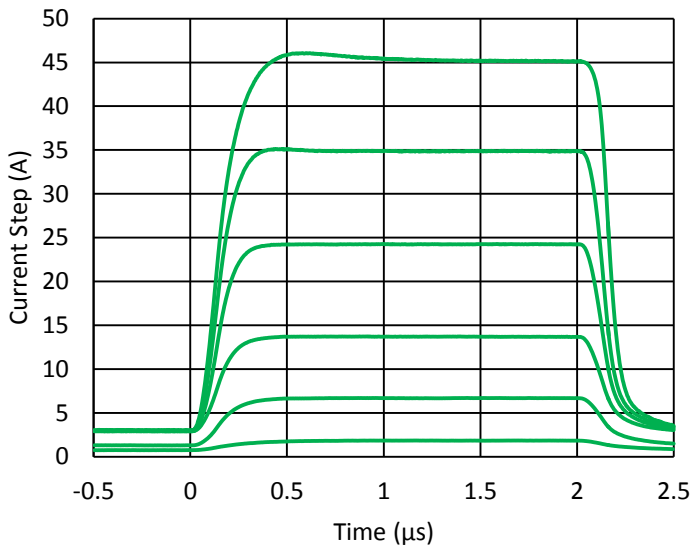
TLT Implementation and Test Results

- Limitation of max operating current of individual circuit can be overcome by operating circuits in parallel
- The measurements below were captured from boards operating alone with 100ns rise/fall time on a DUT supplying 1V

TLT board #1

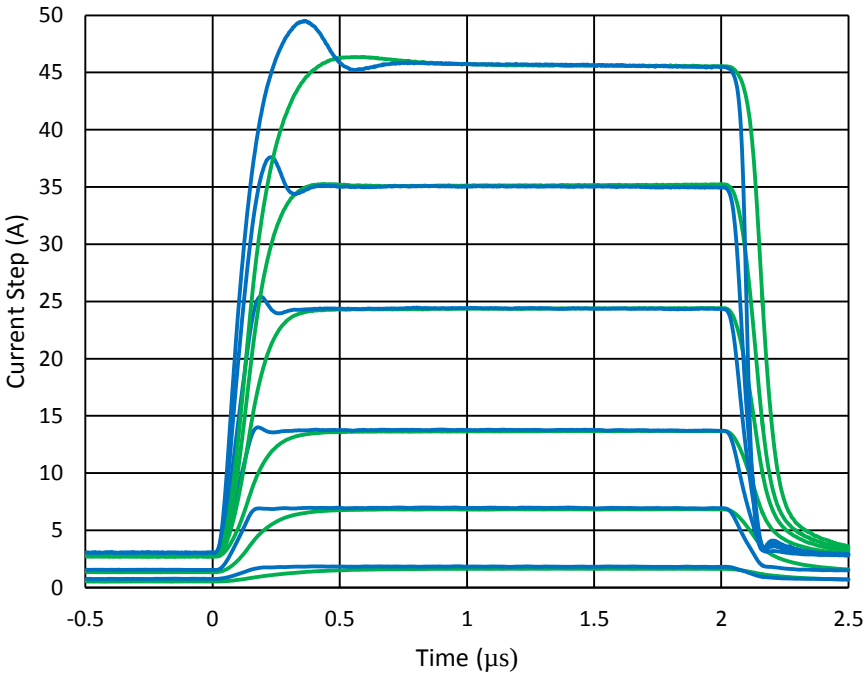


TLT board #2



TLT Implementation and Test Results

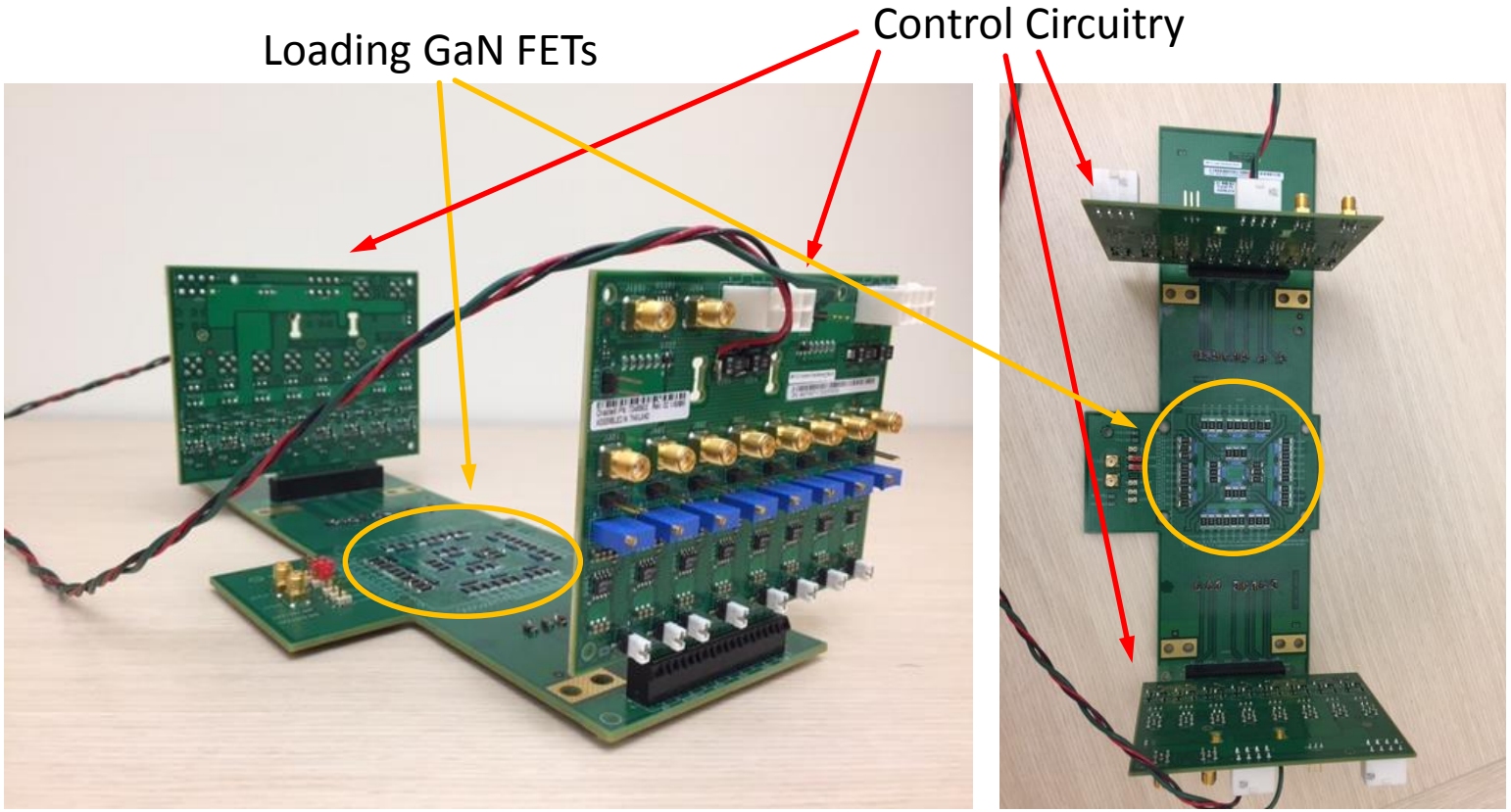
- The measurements below were captured from TLT boards #1 and #2 operating in parallel with 100ns rise/fall time on a DUT supplying 1V



- Parallel operation does not affect operational behavior of TLT circuit

TLT Full PCB Implementation

- Side and top views of 16 TLT circuits implemented in CPU BGA plug-in PCB for parallel operation



TLT Usage for DC-DC Converter and its PDN's Time Domain Performance Testing

- Verify PDN can supply necessary current to devices
- DUT can be tested with complex waveforms using arbitrary waveform generator
- TLT validation uses current pulse train with magnitude equal to max current step PDN must support
  - Can vary frequency and duty cycle to explore exacerbations from resonances

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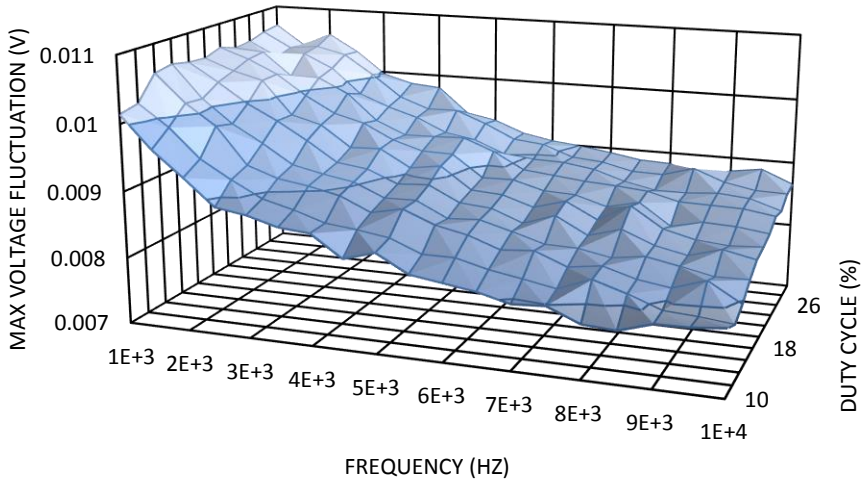

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Conclusion

- Time domain validation of PDNs important for thorough PDN design and analysis
- The GaN FET offers faster turn on speeds and relatively low threshold voltage compared to silicon MOSFETs with similar electrical characteristics
- Implementation of GaN FET with TLT circuit topology along with parallel operation of TLT circuits delivers fast slew of current at 100ns rise/fall time with virtually unlimited current magnitude
- TLT allows for simulation of worst case loading conditions on a PDN in system within a lab setting for thorough PDN validation.

Acknowledgements

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More Information

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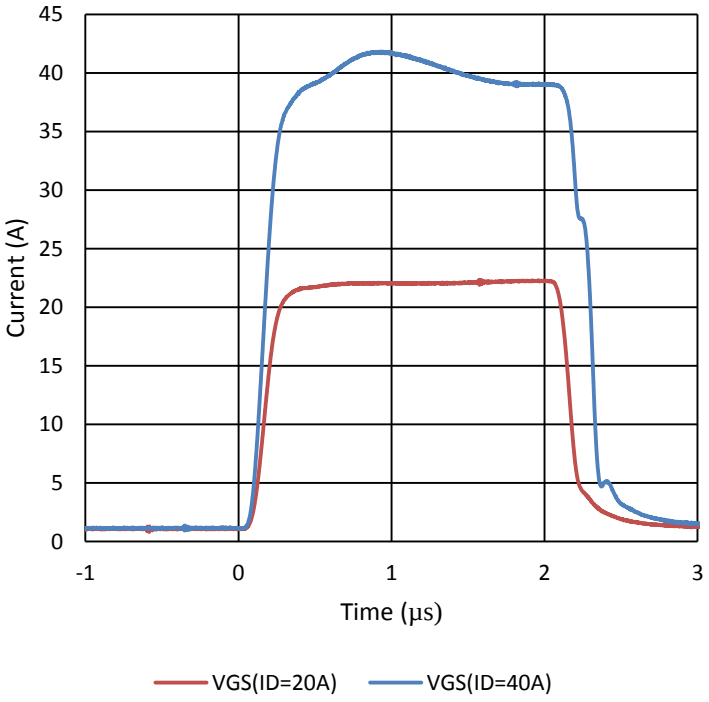
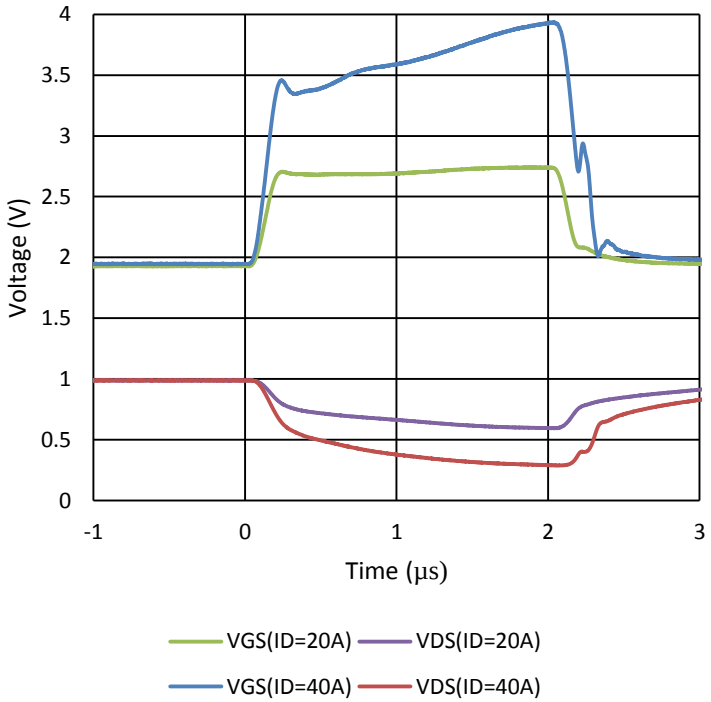
Thank You!

QUESTSIONS?

TLT Implementation and Test Results

- Inherent fight between V_{GS} and V_{DS}, convergence of which determines operational behavior of TLT
- Figures below captured with DUT supplying 1V, show V_{DS}, V_{GS}, and resulting load current at steps of 20A and 40A with 100ns rise and fall times





TLT Implementation and Test Results

- PCB implementation of TLT circuits operating in parallel demands loading FETs be in close proximity to one another
- Little thermal dependence of TLT operational behavior
- Data below captured with TLT operating at 100ns rise/fall time connected to DUT supplying 1V