ARIES: Using Annular-Ring Embedded Resistors to Set Capacitor ESR in Power Distribution Networks

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ABSTRACT

Power-distribution networks need to provide flat low impedance over a wide band. Bypass capacitors with different values, and capacitors and planes create resonance peaks, unless the capacitor parameters are selected properly. Distributed Matched Bypassing is used to create a smooth impedance profile. The ESR of ceramic capacitors is increased by adding embedded annular resistors in series to the capacitors.

Introduction

There has been considerable interest in recent years to improve the power-distribution network of high-end computer and networking equipment. At the module level, on printed-circuit boards, full-area conductive layers over thin laminates provide embedded capacitance for high-frequency decoupling [1], complemented by sometimes several thousands of capacitors for mid and lower frequency bypassing and decoupling [2]. Conductive plane pairs in printed-circuit boards (PCB) exhibit multiple resonances [3], which should be suppressed by proper damping of the structure [4], [5].

Bypass capacitors with different values connected to the conductive planes also may exhibit resonances either between different capacitor banks [6] or between capacitors and planes. One universal approach to reduce these resonance peaks is to minimize the inductance connecting the parts. With discrete surface-mount capacitors the loop inductance is several hundred pH, and usually the dimensions of PCB and capacitor do not allow us to lower it below 70-80 pH, which value is still too high in some applications to avoid resonance peaks. The ESR of bypass capacitors could also be selected to provide a flat impedance response, however, the ESR parameter for today's capacitors is not user defined. ESR of tantalum and electrolytic capacitors is usually in the order of ohm range, whereas ESR of multi-layer ceramic capacitors is usually in the milliohm range.

This paper describes a bypass-capacitor selection process with a possible way to set (increase) the ESR of ceramic bypass capacitors by using embedded printed resistors.

Distributed Matched Bypassing

The cumulative impedance of all bypass capacitors connected to the PCB planes should be a basin-shape impedance profile. For a lumped-equivalent model, it is shown in Fig. 1. The total capacitance value is determined by the VRM's equivalent inductance and the mid-frequency impedance requirement. At very high frequencies, the required cumulative inductance (which may be the result of detailed simulations of planes and capacitors together) of bypass capacitors will determine the number of capacitors. For instance, if we find that the capacitors altogether should provide an inductance of 10pH, and the PCB stackup, layout and capacitor dimensions allow a minimum of 500pH inductance for each bypass capacitor, we need 500pH/10pH=50 pieces of high-frequency capacitors. With today's technology, 1uF capacitance is conveniently available in two-terminal 0805 sizes, and 4x1uF is available in low-inductance eight-terminal 1206 sizes. Each capacitor may have an ESR of 5-10 milliohms. If we connect 50 such capacitors in parallel, the total capacitance is 50 to 200 uF, and the expected ESR is 0.1 to 0.2 milliohms. For applications, where the mid-frequency impedance requirement may be 1-100 milliohms, it would be very convenient to have capacitors with user-definable ESR, such as ESR=50 to 5000 milliohms for the above example.

By matching the mid-frequency impedance requirement to the inherent plane impedance, the Distributed Matched Bypassing can not only eliminate inter-capacitance resonance peaks, but at the same time can also suppress plane resonances.

The Distributed Matched Bypassing methodology uses a few simple steps: a) determine the number of high-frequency capacitors from the required total inductance, b) select the highest available capacitance in the given size, c) calculate the required ESR of each capacitor. If the total capacitance of high-frequency bypass capacitors and the achievable connecting inductance of VRM would still create a resonance peak, additional (lower-frequency) capacitor banks are selected, similar to the process described in [6]. Optionally, if suppression of plane resonances is also required, the inherent plane dimensions should be selected to match the mid-frequency impedance requirement.

By following the above procedure, the possibility of inter-capacitor and plane-to-capacitor resonances can be minimized. For ceramic bypass capacitors, one possible way to achieve the user-defined ESR is shown below.

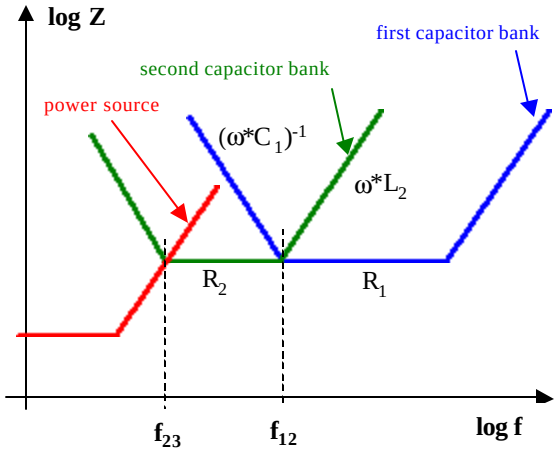

Figure 1.: Distributed Matched Bypassing

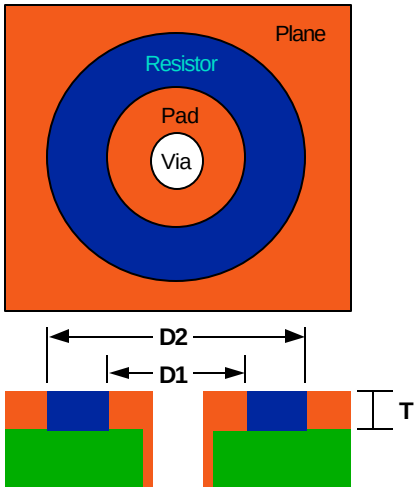

Figure 2.: ***A***nnular ***B***uried ***R***esistor

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The ARIES solution (***A***nnular ***R***esistive ***I***nterstitial ***E***lement, ***S***creened-in) is based on the ABR (***A***nnular ***B***uried ***R***esistor, Fig. 2) process [7], where the ESR of a ceramic capacitor is increased by adding a series resistor element, created in an annular void between a conductive pad and its surrounding antipad. In bypassing applications, one terminal of the resistor should be on one of the planes, conveniently eliminating the need for an antipad ring connection, thus maximizing the available density. To minimize the required footprint and the loop inductance, as shown in Figure 3, the ARIES solution uses eight-terminal capacitors with blind vias connecting to the PCB planes. The capacitor sits on the outermost (L1) metal layer, and four of the capacitor's terminals are connected to the second (L2) ground plane. Four other blind vias connect the remaining terminals of the capacitor to the third (power) layer (L3). Having the ground layer outside, and putting the embedded resis tors (Figure 4) on the power plane allows us to maximize the density of the structure and thus minimize its loop inductance.

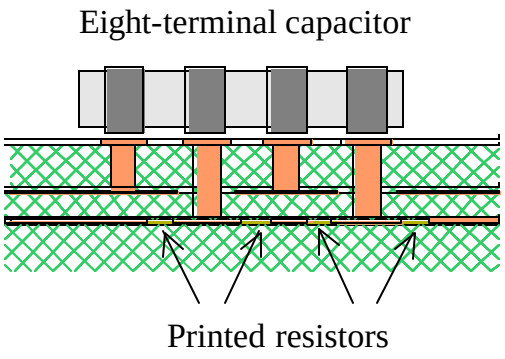

Figure 3.: ARIES construction

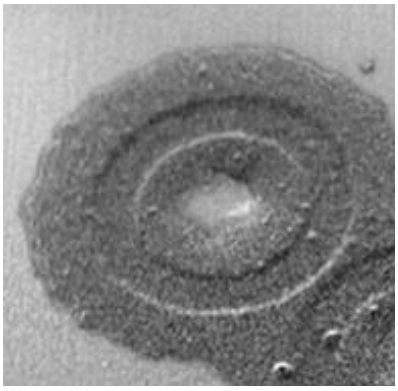

Figure 4.: Embedded resistor on inner layer.

Test board structure

10"x5" test boards with embedded-capacitance layers [7] were designed and built. The boards had two one-inch grids 0.5" offset with respect to each other. On the grid points of one of the grids surface pads for the 1206 eight-terminal capacitors with the appropriate blind vias and embedded resistors [8] were placed. On the second grid test through-holes were placed to allow the measurement of the impedance profile.

First, the bare board was characterized by detailed SPICE-grid simulations and measurements. The mechanical and electrical parameters of the test boards were measured and/or derived, and the parameters of the capacitor pad/via set were extracted. Figure 5 shows the simulated and measured self-impedance of the bare test board. From the self-impedance profile with one capacitor-pad set shorted, the extracted values for the pads and vias were found to be 50pH and 1.5 milliohms.

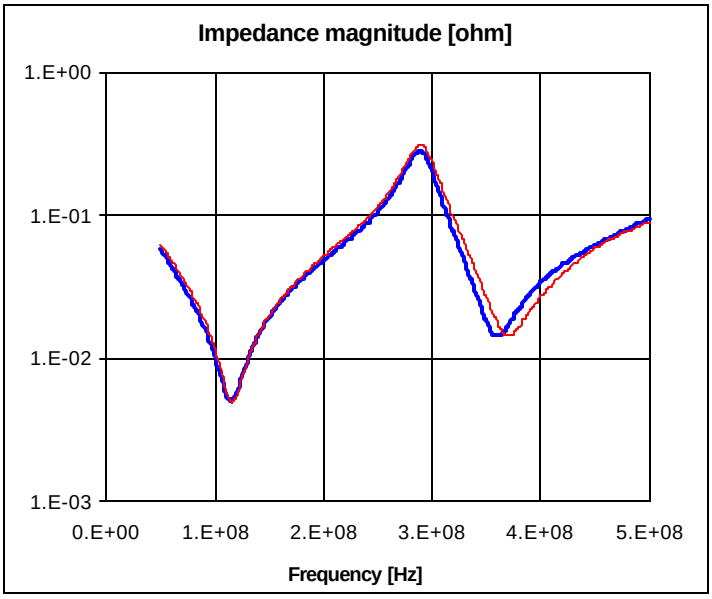

Figure 5.: Self impedance magnitude of 10"x5" test board, 2 inches from the corner, along the edge. Laminate: 2-mil FR4 plane pairs. Thick line: simulated, thin line: measured.

Measurement results

Figure 4 shows the photograph of an embedded resistor on an inner layer of the test board. Its measured self impedance profile with twenty six 1206-size eight-terminal capacitors and embedded resistors are shown in Figure 6. Figure 7 illustrates the savings in component count and board area on a module.

Conclusions

The Distributed Matched Bypassing design methodology inherently avoids resonance peaks in the impedance profiles of power-distribution networks. It was shown that embedded resistors can be used to set (increase) the ESR of capacitors.

References

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[5] "System and method for edge termination of parallel conductive planes in an electrical interconnecting apparatus," US Patent 6,104,258, August 15, 2000.

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[7] "Capacitor laminate for use in capacitive printed circuit boards and methods of manufacture," US Patent 5,079,069.
[8] "Annular circuit components coupled with printed-circuit board through-hole," US Patent 5,708,569

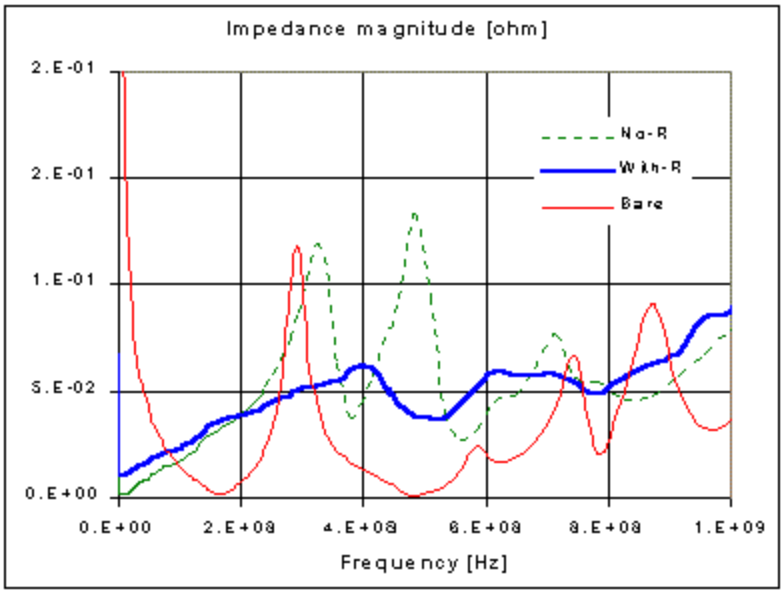
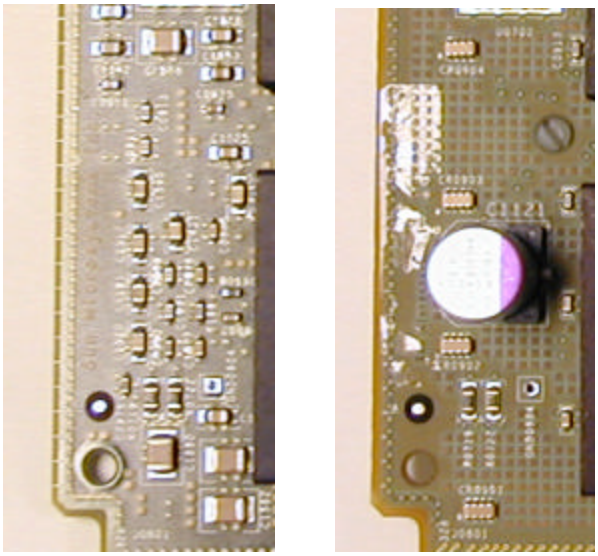


Figure 6.: Self-impedance measured on the 10"x5" test board with 26 pieces of IDC capacitors with and without the embedded resistors. The three traces: a) thin continuous line: impedance of the bare board (for reference), b) dashed line: impedance of the same board without embedded resistors, and c) solid heavy line: impedance with embedded resistors. The graph above shows that by adding the embedded resistors, the impedance at 324 MHz is reduced from 0.119 ohms to 0.052 ohms, and at 480MHz the impedance peak is reduced from 0.133 ohms to 0.038 ohms.



a., b.,

Figure 7.: Illustration of savings in component count and board area: a) board detail of module with more than 250 pieces of mid-frequency bypass capacitors, and b) same module with 50 Distributed Matched Bypassing capacitors.