

# Design Considerations and Modeling Accuracy of Lossy Power Distribution Networks

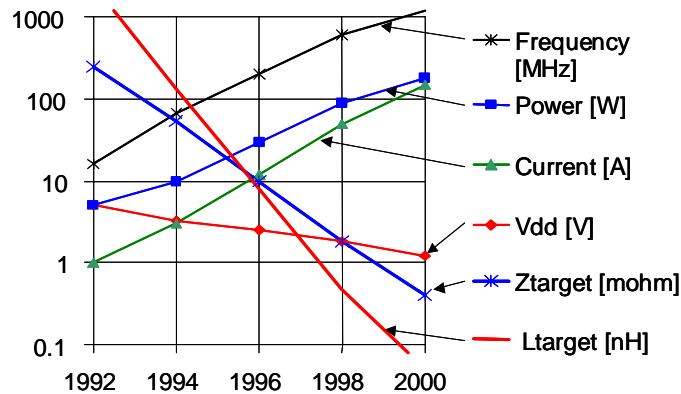
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## Abstract

The modeling errors of the analytical plane-impedance expressions and lossy transmission-line grid plane models are compared. The lossy transmission-line grid model is used to simulate power-ground plane pairs with thin dielectric and thin conductive layers. Thin dielectric layers in power distribution provide good suppression of plane resonances. When combined with thin conductive layers, a resistor-like flat impedance profile can be created. Simulated and measured impedances are compared on test structures with plane separation of 1.6 and 0.3 mils.

## I. Introduction

With increasing clock speeds and decreasing supply voltages in computing devices, the correct design and measurement verification of power-distribution networks (PDN) become more challenging. As shown in Figure 1, the required target impedance may reach the sub milliohm range, while the bandwidth of transients moves into the GHz range [1].



**Figure 1.:** Trend of power-distribution parameter requirements. Note the very steep drop of the equivalent inductance of PDN.

At the same time, systems may have large printed-circuit boards (PCB) with board dimensions in excess of 0.5 meters. It is also typical that the DC sources are located on the same PCB in the form of DC-DC converters. The power is then distributed on one or more power/ground planes of the PCB. These conductive planes form the basis of the PDN. The wideband low impedance is achieved by the combination of properly designed DC-DC converters, bulk capacitors, medium- and high-frequency signal-integrity (SI) capacitors. The power-ground planes of PCB interconnect these elements, but due to the fact that the PCB size is not negligible compared to the wavelength of the highest frequency of interest, the

transmission-line effects of the planes must also be considered, and eventually the planes become an integral part of the PDN.

At the low end of the spectrum, the PDN in high-end systems must carry large currents, sometimes exceeding one hundred Amperes. The DC resistance of a square of a one-ounce copper plane is approximately 0.7 milliohms. To achieve sufficiently low DC drop, several conductive planes in parallel may be required. An often overlooked requirement of PCB PDNs is that isolation is required among the electronic subsystems attached to the PCB. With physically separate subsystems, such as plug-in cards, the isolation partly comes naturally from the connectors and wires. At high frequencies, the equivalent characteristic impedance of connectors and wires is usually much higher than the impedance of the power-distribution network, and therefore these can be considered as decoupling inductances. On the printed-circuit boards, however, we may need closely spaced power/ground planes to achieve the low impedance at high frequencies. Combined with the typical epoxy-resin-fiberglass (e.g., FR4) dielectric materials, the power-ground planes form a two-dimensional transmission line with fairly low attenuations up to a couple of GHz.

If not designed properly, the power/ground planes in the PDN may exhibit resonances in the frequency domain [2], and at specific resonance frequencies the transfer impedance at remote points may be even higher than the self-impedance at the location of the noise source. To avoid the resonances in the PDN, there are several options. In conventional designs, many bypass capacitors may be attached to the PDN planes. These capacitors eventually create a capacitively loaded transmission structure, and it can suppress plane resonances while creating low-pass function as well. The limitation of this approach stems from the difference between the mounted inductance of bypass capacitors (several hundred pH, see e.g., [3]) and the few times ten pH equivalent inductance of closely-spaced power/ground planes. Another possibility of suppressing plane resonances is to increase the losses of the dielectric material between the power/ground planes. [4] suggests a lossy conductive layer in the dielectric material. This technique requires an extra step in PCB manufacturing is needed, and we have to make sure that the signal vias are not affected by the losses. Resistive termination at the plane edges can also be used [5], [6]. The resistive termination reduces the resonance peaks in the impedance and radiation profile, but it does not in itself provide a low-pass transfer function. Yet another possibility (as it is shown later in this paper) to reduce plane resonances, and at the same time to provide low-pass filter transfer function is to rely on the inherent conductive losses of the PCB planes. This is of particular interest in light of recent efforts to embed bypass capacitors into the PCB ([13], [14]).

Using any methodology to design the PDN, the accurate and efficient simulation of the two-dimensional transmission-line planes becomes a necessity. This paper summarizes some accuracy considerations for two of the simulation approaches: the transmission-line grid method and the analytical plane-impedance method. The measurement methodology for very low wideband impedances was covered elsewhere [7], [8].

## **II. Simulation of power/ground planes in PDNs**

### **II. 1 Analytical plane model**

One useful alternative to the bedspring equivalent circuit is the analytical impedance expression of the power/ground planes, which was originally derived for microwave resonators and patch antennas ([9] through [12]). Not limited by a fixed grid of components, the analytical expression can be solved for any set of arbitrary points on the planes. The expressions yield the self and/or transfer impedances, and the computation may be very efficient [10].

The generic impedance between any two ports on the planes (assuming negligibly small port dimensions) is given by:

$$Z_{ij}(\omega) = j\omega\mu h \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \frac{\chi_{mn}^2}{w_x w_y (k_n^2 - k^2)} \cos\left(\frac{2m\pi x_i}{2w_x}\right) \cos\left(\frac{2n\pi y_i}{2w_y}\right) \cos\left(\frac{2m\pi x_j}{2w_x}\right) \cos\left(\frac{2n\pi y_j}{2w_y}\right)$$

where  $\omega=2\pi f$  is the angular frequency

$\mu$  is the permeability of dielectric ( $\mu=\mu_0=4\pi 10^{-7}$ )

$c$  is the speed of light, and for lossless structures,

$$\chi_{mn} = 1 \text{ for } m = 0 \text{ and } n = 0; \sqrt{2} \text{ for } m = 0 \text{ or } n = 0; 2 \text{ for } m \neq 0, n \neq 0$$

$$k = \omega \sqrt{\varepsilon\mu} = \omega \sqrt{\varepsilon_r \varepsilon_0 \mu_0} = \sqrt{\varepsilon_r} \frac{\omega}{c}$$

$$k_n^2 = \left(\frac{m\pi}{w_x}\right)^2 + \left(\frac{n\pi}{w_y}\right)^2$$

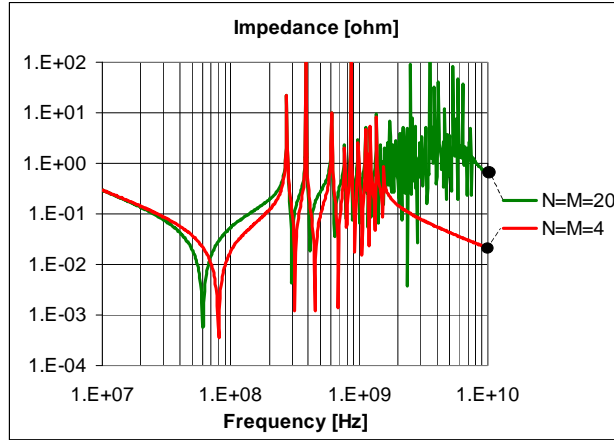
For structures with light losses, the imaginary part of  $k$  may represent the lossy nature:  $k = k' - jk''$ , where  $k' = k$  above.

Though not limited by finite spatial granularity, there are two fundamental limitations to consider when we apply this formula to PDNs. First, the initial assumptions limit the validity of the expression to low-loss cases. Second, the analytical expression has a double infinite series, which for practical calculations must be truncated, so that instead of being infinite, we have to use finite  $n_{\max} = N$ , and  $m_{\max} = M$  limits.

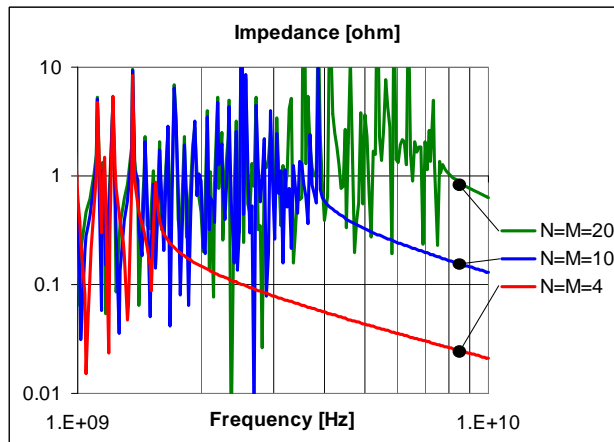
The plane-impedance expression contains a double series of second-order terms. These terms accurately describe the poles (peaks) in the impedance profile, and the frequencies of the peaks do not change as we add or remove terms. The minima of the impedance profile, however, do change as more terms are added to the series. More importantly, beyond the frequency of the last pole of the truncated series, as opposed to the inductive upslope of the plane impedance at high frequencies, the truncated series yields an impedance of capacitive down slope. Also for this reason, the high-frequency spreading inductance of planes can be obtained from the expression only with large summation limits.

To show these effects, a pair of 10-inch square planes with 2-mil separation was simulated. Figure 2 shows the simulated self impedance at the corner of planes with two different  $N=M$  summation limits, Figure 3 illustrates the high-end capacitive down slope of impedance profile.

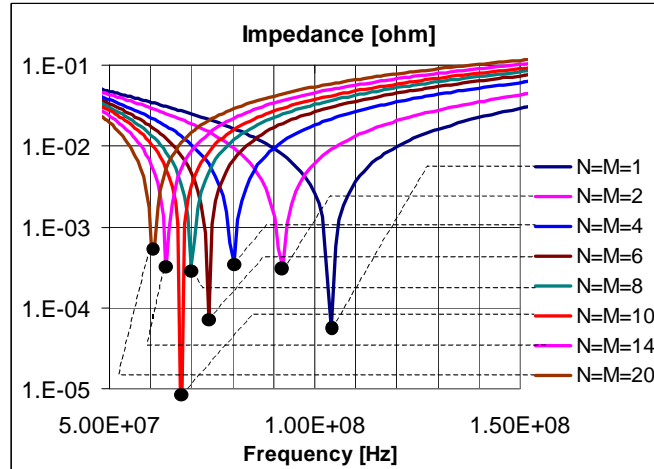
While the simulated impedance peaks line up for all values of  $N=M$ , the frequencies of minima vary with the summation limit. Figures 4 and 5 show that the frequency of the first minimum shifts in a range of almost 2:1.



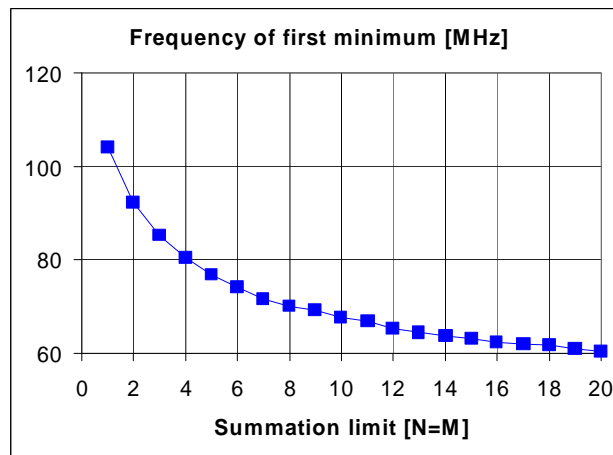
**Figure 2.:** Self impedance of a 10-inch by 10-inch pair of planes, with 2-mil plane separation and FR4 dielectrics (dielectric constant of 4.7). Impedance is simulated by the analytical plane expression, at the corner of the planes. Full span of impedance with two different summation limits are shown,  $N = M = 4$ , and  $N = M = 20$ .



**Figure 3.:** Self impedance of a 10-inch by 10-inch pair of planes, with 2-mil plane separation and FR4 dielectrics. Impedance is simulated by the analytical plane expression, at the corner of the planes. High-end range of impedance with three different summation limits are shown,  $N = M = 4$ ,  $N = M = 10$ , and  $N = M = 20$ .



**Figure 4.:** Self impedance of a 10-inch by 10-inch pair of planes, with 2-mil plane separation and FR4 dielectrics. Impedance is simulated by the analytical plane expression, at the corner of the planes. The frequency range close to the first minimum is shown with a wide range of summation limits.



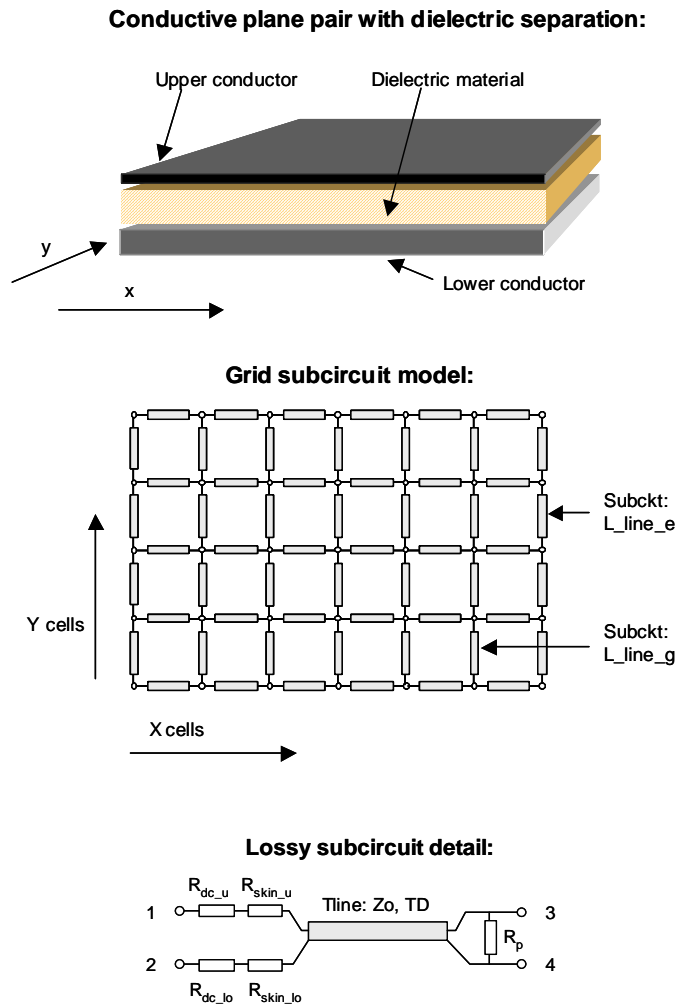
**Figure 5.:** Frequency of first minimum readings from Figure 4 as a function of summation limit.

## II.2. Lossy transmission-line grid model

To consider the time-of-flight and resonance effects of planes, a grid of transmission lines is used (see e.g., [11] and [12]). Figure 6 shows the transmission-line grid model used for the simulations in this paper. The equivalent circuit uses a grid of subcircuits, each of which contains a lossless transmission line, a DC and AC resistance separately for the upper and lower conductive planes, and a parallel resistor describing the dielectric losses. The AC series resistance is scaled with the square root of frequency, while the parallel loss scales linearly with frequency. The input parameters and the derived HSPICE parameters for the subcircuits are shown in Figure 7. Note that Figure 6 contains two different subcircuits: T\_line\_g is the lossy transmission line subcircuit for all of the internal paths of the grid, whereas T-Line\_e is the subcircuit only for the edges. The T-Line\_e parameters are adjusted by a factor of two, to take into account the fact that they have no neighboring planes. Note that in this grid representation the grid cells correspond to squares on the planes, and if the x and y dimensions of the planes are not the same, the number of cells along the two axes will reflect the different dimensions. Note also that the grid is ‘floating’, the reference

side of the Tlines are not hardwired to SPICE node0, thus allowing – if necessary – a combination of various grid layers.

A series of simulations were done first to see the effect of the number of cells. Obviously, with fixed physical plane dimensions, the frequency range of validity of the plane model is improved as the number of cells increases. From Figure 8 we can see that the runtime is manageable up to a grid size of 30x30, which still runs under three minutes.



**Figure 6:** Lossy transmission-line grid model for power-ground plane simulations.

```

* Constants *
.param PI= 3.14159265
.param eps_nul= 0.00000000000885
.param mu_nul= '4*PI*0.0000001'

* Input data *
.param unit_length=0.0254 $ unit length in meters
.param x_cells=20 $ number of grid cells in x direction [-]
.param y_cells=20 $ number of grid cells in y direction [-]
.param grid_size='10/20' $ size of one grid cell [selected unit]
.param plane_sep=0.005 $ separation of planes [selected unit]
.param eps_rel=4 $ relative dielectric constant [-]
.param tan_delta=0.002 $ loss tangent of dielectrics [-]
.param u_cond_th=0.0012 $ thickness of upper conductor [selected unit]
.param u_sigma=5.8E7 $ conductivity of upper conductor [S/m]
.param lo_cond_th=0.0012 $ thickness of lower conductor [selected unit]
.param lo_sigma=5.8E7 $ conductivity of lower conductor [S/m]

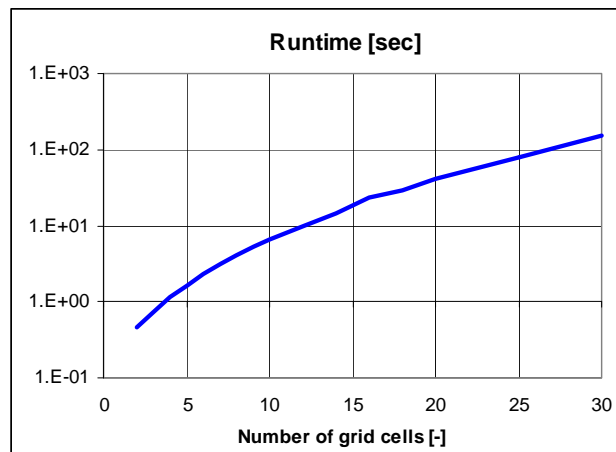
* Derived data *
.param L_u= 'mu_nul*plane_sep*unit_length'
.param C_u= 'eps_nul*eps_rel*grid_size/plane_sep*grid_size*unit_length'
.param Zo_grid= 'sqrt(L_u/C_u)*sqrt(2)'
.param tpd_sq= 'sqrt(L_u*C_u)/sqrt(2)'
.param Rdc_u_grid = '1/(u_sigma * u_cond_th)'
.param Rs_u_grid = 'sqrt(PI*mu_nul/u_sigma)'
.param Rdc_lo_grid = '1/(lo_sigma*lo_cond_th)'
.param Rs_lo_grid = 'sqrt(PI*mu_nul/lo_sigma)'
.param cond_grid = '2*PI*tan_delta*tpd_sq/Zo_grid'

.subckt L_line_g 1 2 3 4
  Rdc_u 1 5 Rdc_u_grid
  Rskin_u 5 6 'Rs_u_grid*sqrt(hertz)'
  Rdc_lo 2 7 Rdc_lo_grid
  Rskin_lo 7 8 'Rs_lo_grid*sqrt(hertz)'
  Tline 6 8 3 4 Z0=Zo_grid TD=tpd_sq
  Rp_g 3 4 '1/cond_grid/hertz'
  Rdummyg 2 4 1E6
.ends L_line_g

.subckt L_line_e 1 2 3 4
  Rdc_u 1 5 '2*Rdc_u_grid'
  Rskin_u 5 6 '2*Rs_u_grid*sqrt(hertz)'
  Rdc_lo 2 7 '2*Rdc_lo_grid'
  Rskin_lo 7 8 '2*Rs_lo_grid*sqrt(hertz)'
  Tline 6 8 3 4 Z0='2*Zo_grid' TD=tpd_sq
  Rp_e 3 4 '2/cond_grid/hertz'
  Rdummye 2 4 1E6
.ends L_line_e

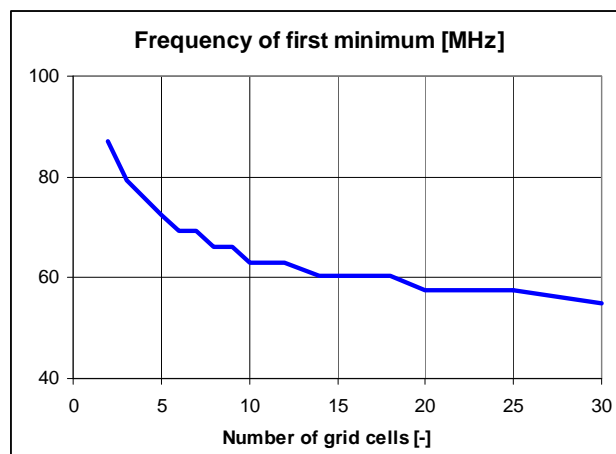
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**Figure 7.:** User input and derived parameters for the HSPICE lossy transmission-line grid model.



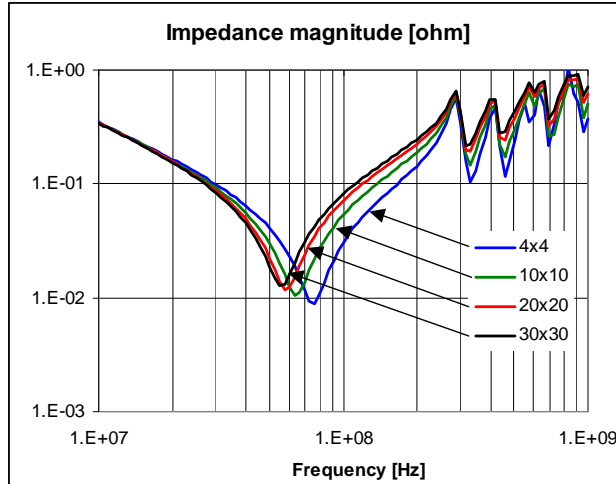
**Figure 8.:** Runtime of the lossy transmission line grid model with 300 points in the frequency domain, on a UltraSparc60 machine. Square planes were assumed with the same number of cells along both axes.

To see the effect of grid granularity on the simulated poles and zeros, the frequency shift of the first minimum frequency of a pair of 10" by 10" pair of planes with 2 mils of dielectrics were simulated with the lossy grid model. The dielectric constant was 4, and the minima of the self-impedance magnitudes at one of the corners were recorded. It was found that both with the analytical plane model and with the lossy transmission-line grid, the frequency of the first minimum showed noticeable variation, while the second and third minima had successively lower sensitivity. Note that the lossy transmission line grid model results in almost the same 2:1 frequency variation of the first minimum as what we see with the analytical plane model. Figure 9 illustrates the shift of the first minimum frequency, Figure 10 shows the self impedance profile at the corner of a pair of 10" by 10" pair of planes with 2 mils of dielectrics, dielectric constant of 4. The square planes were modeled by a lossy transmission line grid of Figures 6 and 7, with 4x4, 10x10, 20x20, and 30x30 cells.



**Figure 9.:** Frequency shift of the first minimum frequency of a pair of 10" by 10" pair of planes with 2 mils of dielectrics, dielectric constant of 4. The minima of the self-impedance magnitudes at one of the corners were recorded.

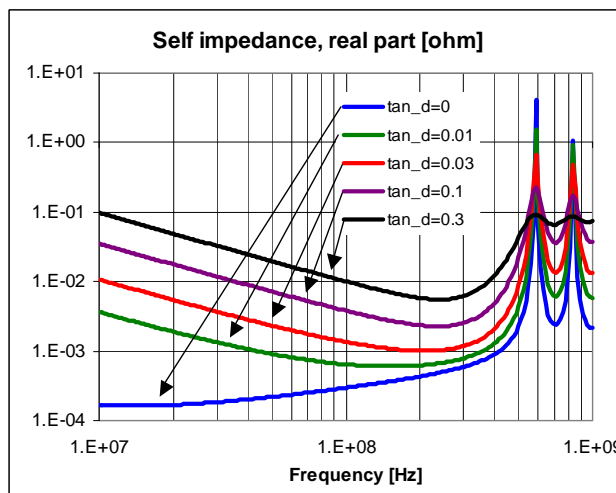




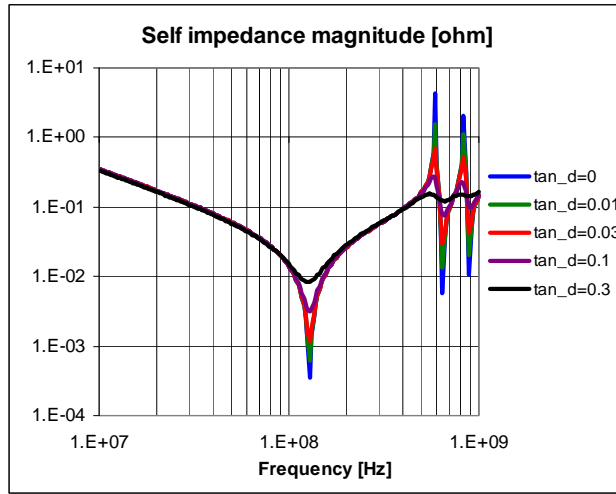
**Figure 10.:** Self impedance profile at the corner of a pair of 10" by 10" pair of planes with 2 mils of dielectrics, dielectric constant of 4. The square planes were modeled by a lossy transmission line grid with 4x4, 10x10, 20x20, and 30x30 cells.

### II. 3. Effect of dielectric losses on the plane impedance

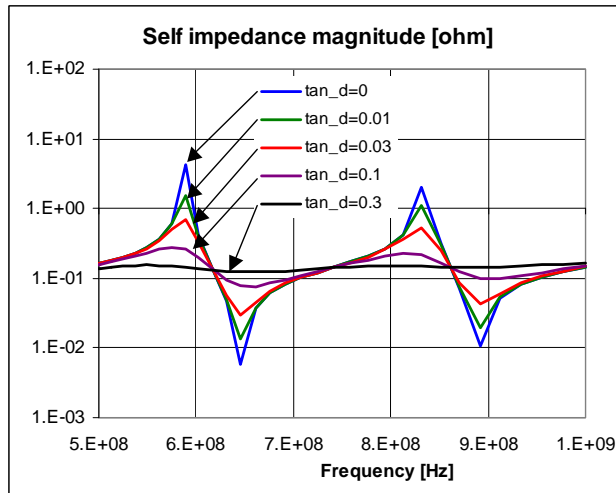
The typical PCB materials have been optimized for low-loss signal transmission, and because of this, they do not provide sufficient suppression of plane resonances. If used only between the power/ground planes, intentionally high dielectric losses may be used. Figure 11 contains the real part of the simulated self impedance at the center of a pair of 10" by 10" planes with 2 mils separation. Figure 12 shows the impedance magnitude for the same circuit. Figure 13 is the zoomed version of Figure 12. In Figure 12 the individual traces are on top of each other, suggesting that the dielectric loss itself does no noticeable shift the resonance frequencies. From the curves of Figure 13 we can conclude that a dielectric loss tangent of 0.3 or higher is sufficient to suppress almost completely the plane resonances.



**Figure 11.:** Effect of dielectric losses on the real part of self impedance at the center of a pair of 10" by 10" pair of planes with 2 mils plane separation, dielectric constant 4, one ounce copper .



**Figure 12.:** Effect of dielectric losses on the magnitude of self impedance at the center of a pair of 10" by 10" pair of planes with 2 mils plane separation, dielectric constant 4, one ounce copper.



**Figure 13.:** Effect of dielectric losses on the magnitude of self impedance at the center of a pair of 10" by 10" pair of planes with 2 mils plane separation, dielectric constant 4, one ounce copper. Zoomed frequency scale shows the first two peaks.

#### **II. 4. Effect of dielectric thickness on the plane impedance with regular copper thickness**

It is known that the series conductor losses of a transmission line increase the attenuation, which under matched conditions can be expressed as:

$$A^{dB} = 4.35 \left( \frac{R_s}{Z_o} + G_d Z_o \right)$$

where

A is the attenuation of the matched-terminated trace in dB,

$R_s$  is the series attenuation at the required frequency

Gd is the parallel conductance of the dielectrics at the required frequency

$Z_0$  is the characteristic impedance of trace

$R_s$  is the total series resistance of the conductor at the frequency of interest, determined by the cross section and conductivity of the conductor. At higher frequencies, the resistance of conductor increases, because current tends to flow on the surface, leaving for current conduction only an effective channel of depth, which is proportional to the inverse square root of frequency. This effective depth is called the skin depth, and at a first approximation it is expressed as:

$$\delta = \sqrt{\frac{1}{\pi f \sigma \mu}}$$

where

$\delta$  is the skin depth

f is the frequency of interest

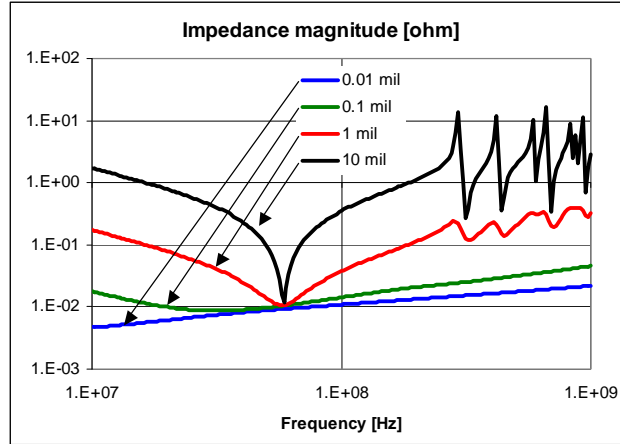
$\sigma$  is the conductivity of conductor

$\mu$  is the permeability of conductor

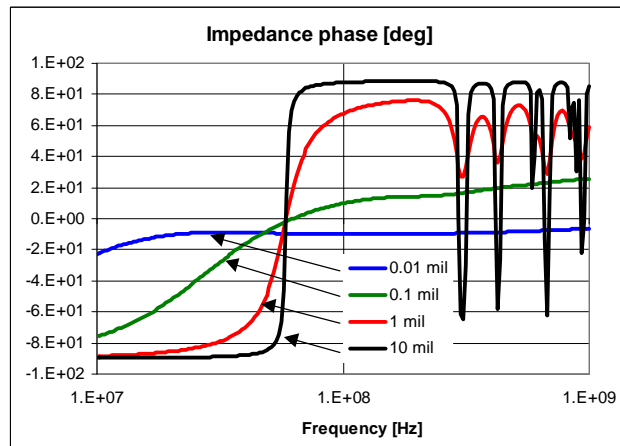
The above expressions suggest that the same series resistance produces higher attenuation if the characteristic impedance is lower. This also suggests that in case of parallel conductive planes, if the planes are put sufficiently close (in order to reduce the equivalent characteristic impedance of the planes), without any change in the material properties, the series resistance eventually provides enough attenuation to suppress plane resonances.

The lossy grid model of Figures 6 and 7 were applied to simulate a pair of 10" by 10" parallel planes with one ounce copper on either side, but with variable thickness of dielectric separation. The dielectric constant was assumed to be 4. The grid size was 20x20, providing at least 1GHz of useful upper limit for the model.

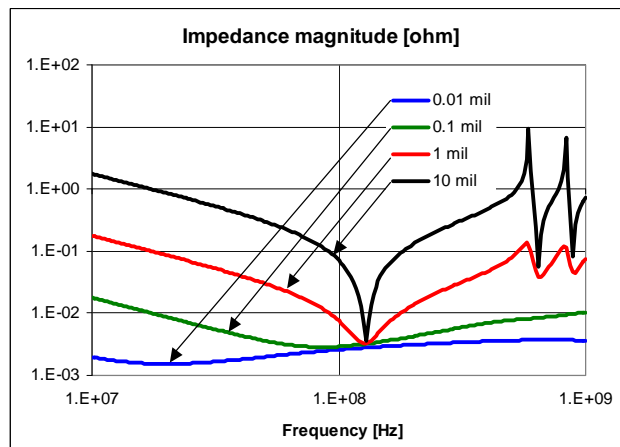
Figures 14 and 15 show the magnitude and phase of self impedance at the corner, Figures 16 and 17 include the same parameters at the center. As the dielectric thickness is reduced, the impedance profile becomes more smooth at high frequencies. There is another obvious advantage: the low-frequency impedance is also reduced inversely proportional to the dielectric thickness due to the increase of static capacitance. This helps to reduce the need for low-frequency bulk capacitors, but the real advantage is the complete suppression of plane resonances. It is also shown on the phase figures: with thin dielectrics, the phase of the self impedance becomes more resistive. Note also the slant of the self-impedance magnitude at high frequencies: this is due to the increase of skin resistance with the square root of frequency. Figure 18 proves our assumption that increasing series losses create a low-pass transfer function: while dielectric thickness above about one milli-inch yields a transfer function with noticeable peaks at high frequencies, a thickness of 0.1 mils creates a flat response, and even thinner dielectric separation provides a monotonic low-pass function. The series losses also increase the upper frequency limit of the model by reducing the reflections, and effectively creating a resistor rather than transmission line grid at high frequencies.



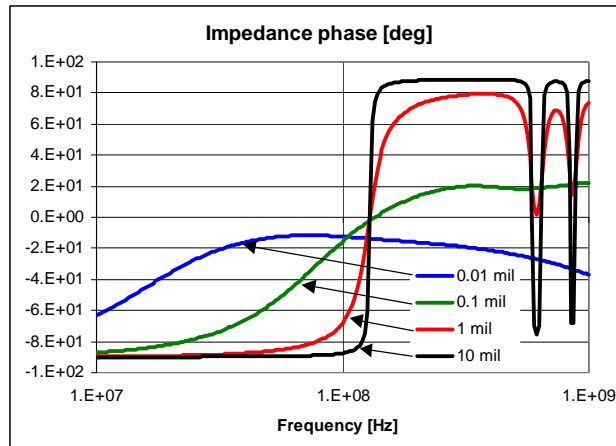
**Figure 14.:** Effect of dielectric thickness on the self impedance of a pair of 10'' by 10'' planes, with one ounce copper. The self impedance magnitude is shown at the corner. The parameter on the graph is the dielectric thickness.



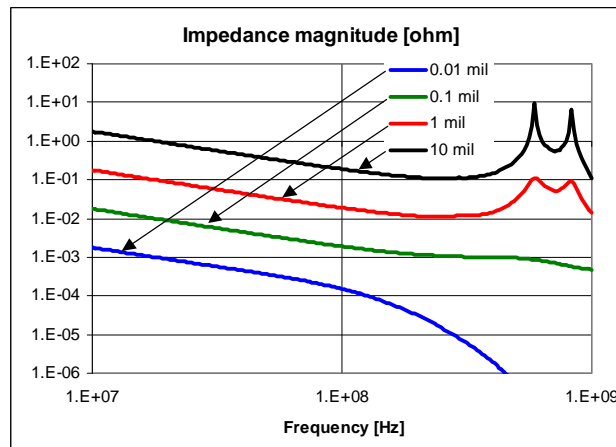
**Figure 15.:** Effect of dielectric thickness on the self impedance of a pair of 10'' by 10'' planes, with one ounce copper. The phase of the self impedance is shown at the corner. The parameter on the graph is the dielectric thickness.



**Figure 16.:** Effect of dielectric thickness on the self impedance of a pair of 10'' by 10'' planes, with one ounce copper. Self impedance magnitude is shown at the center of planes. Parameter: dielectric thickness.



*Figure 17.: Effect of dielectric thickness on the self impedance of a pair of 10" by 10" planes, with one ounce copper. The phase of the self impedance is shown at the center. The parameter on the graph is the dielectric thickness.*



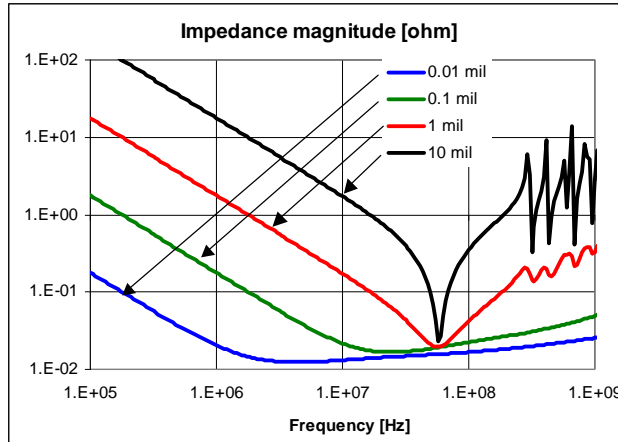
*Figure 18.: Effect of dielectric thickness on the self impedance of a pair of 10" by 10" planes, with one ounce copper. The magnitude of the transfer impedance is shown between the center and one of the corners. The parameter on the graph is the dielectric thickness.*

## **II. 5. Effect of dielectric thickness on the plane impedance with thin conductor**

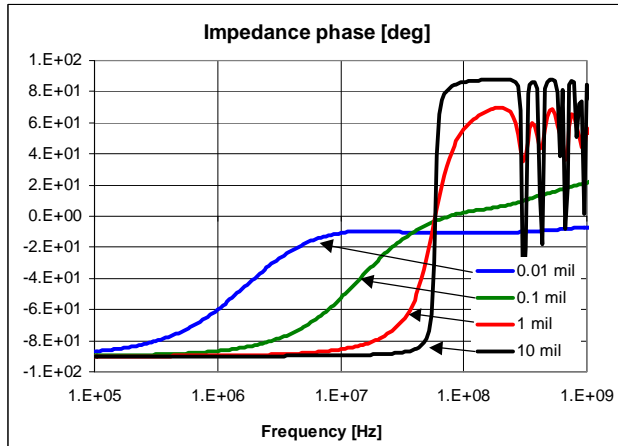
While the advantages of thin dielectrics are clear from the simulations results of Figures 14-18, it is unfortunately not practical to manufacture and handle a dielectric layer of a few micrometer or less thickness with the usual several micrometer or more copper layers. With a 0.01 mil dielectric layer the copper would be about hundred times thicker.

To look at the other extreme, Figures 19 through 23 show the same structure under the same assumptions as Figures 14 through 18, except the conductive layer on both sides is assumed to be 0.01-mil copper. Note that the skin depth in copper at 1GHz is approximately 2 micrometers, which is about eight times higher than the selected 0.01-mil (0.25 micrometers) copper thickness. Due to this fact the series loss resistance is less dependent on frequency. By comparing Figures 14-18 and Figures 19-23, we can see that the high-

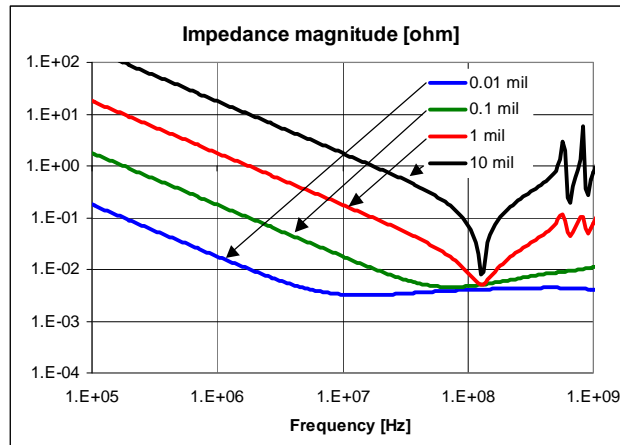
frequency impedance does not drop inversely proportional to the plane separation, as one would expect based on the equivalent inductance between the planes, because the impedance is limited by the series resistance. With the 0.01-mil copper conductors, the self-impedance profile is almost totally flat at the center of the planes as soon as at about 10MHz the impedance of the static capacitance intercepts the series resistance. The higher series resistance also creates a stronger low-pass filtering.



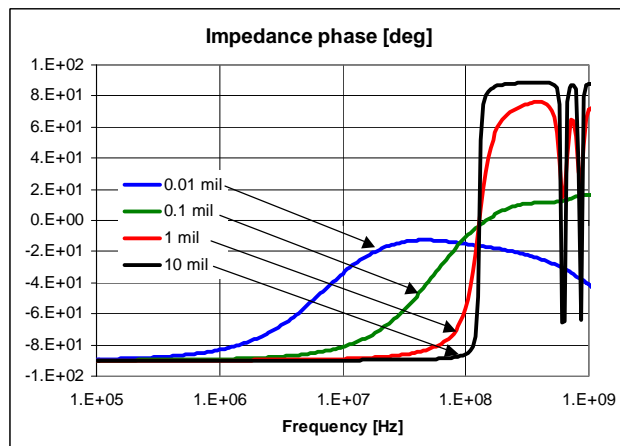
**Figure 19.:** Effect of dielectric thickness on the self impedance of a pair of 10" by 10" planes, with 0.01 mil copper. The self impedance magnitude is shown at the corner. The parameter on the graph is the dielectric thickness.



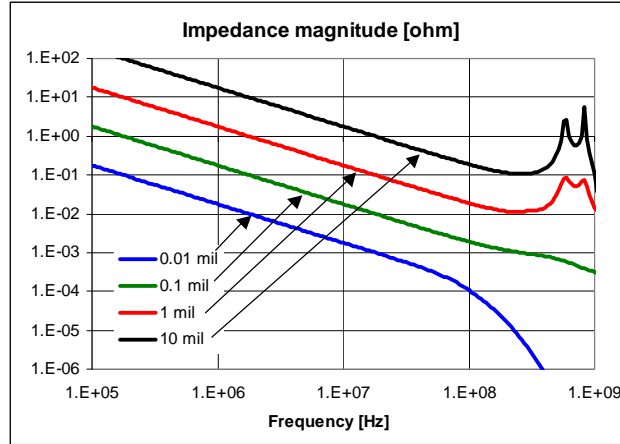
**Figure 20.:** Effect of dielectric thickness on the self impedance of a pair of 10" by 10" planes, with 0.01 mil copper. The phase of self impedance is shown at the corner. The parameter on the graph is the dielectric thickness.



**Figure 21.:** Effect of dielectric thickness on the self impedance of a pair of 10" by 10" planes, with 0.01 mil copper. The self impedance magnitude is shown at the center. The parameter on the graph is the dielectric thickness.



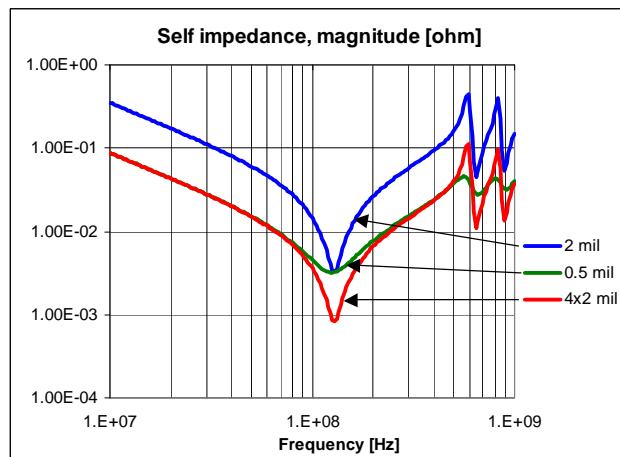
**Figure 22.:** Effect of dielectric thickness on the self impedance of a pair of 10" by 10" planes, with 0.01 mil copper. The phase of self impedance is shown at the center. The parameter on the graph is the dielectric thickness.



**Figure 23.:** Effect of dielectric thickness on the self impedance of a pair of 10" by 10" planes, with 0.01 mil copper. The magnitude of the transfer impedance is shown between the center and one of the corners. The parameter on the graph is the dielectric thickness.

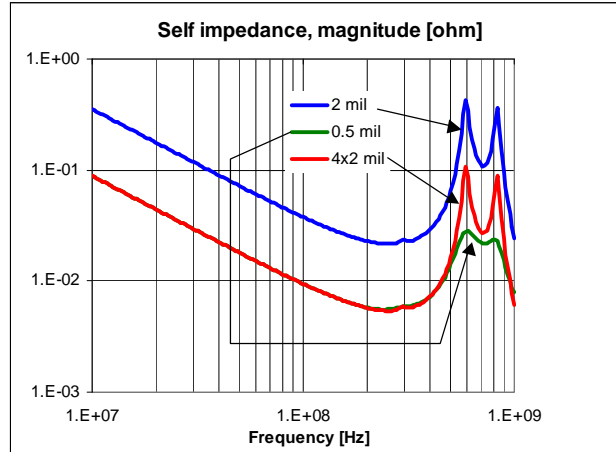
On the other hand, using very thin conductive layers alone is not practical either, because the copper weight is needed to handle the large DC currents in the systems. By using both thin dielectric and thin conductive layers, we can provide the necessary copper weight by stacking up several of these thin layers. This at the same time will further reduce the impedance. A typical 2-mil dielectric separation with one ounce (1.2-mil) copper has a total thickness of 4.4 mils. If we used the 4.4-mil total thickness and we stacked up 220 pairs of 0.01-mil dielectrics with 0.01-mil copper, we would end up with the same total thickness, 2.2-mil of total copper on either side, and (neglecting the connecting impedance between the stacked layers) an approximately 25 micro ohm flat resistive impedance in the 10-1000MHz frequency range.

It is also clear that stacking power-ground plane pairs in parallel has its advantages if we already reach the resistive bottom of the impedance profile with thin dielectrics. It is illustrated in Figures 24 and 25 that in the unsaturated range of the curves it is better to use one plane pair with thinner dielectrics as opposed to stack up several of them.



**Figure 24.:** Self impedance magnitude at the center of 10" by 10" parallel planes with three different configurations: a) standalone pair with 2-mil plane separation, standalone pair with 0.5-mil plane separation, and four pairs of plane pairs with 2-mil each plane separation.



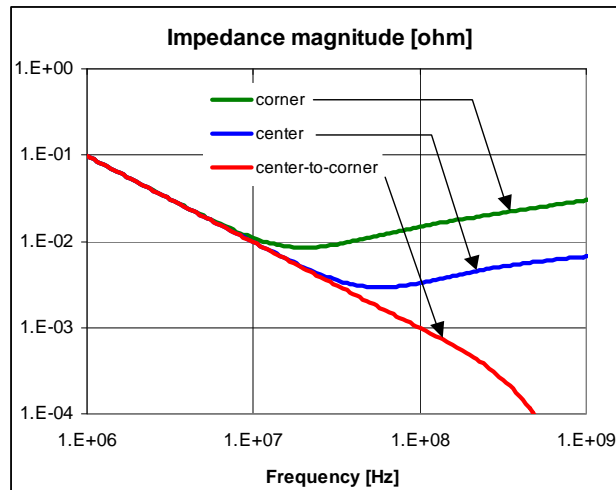


**Figure 25.:** Transfer impedance magnitude from the center to one of the corners of 10” by 10” parallel planes with three different configurations: a) standalone pair with 2-mil plane separation, standalone pair with 0.5-mil plane separation, and four pairs of plane pairs with 2-mil each plane separation.

### III. Simulated and measured results of test structures

#### III. 1. Thin dielectric and thin conductive layer

Thin dielectric and conductive layers can be manufactured by various thin-film processes ([17], [18]). A structure assuming a 4” by 4” size, one ounce copper base, 0.2 micrometer thin silica dielectric layer and 0.5 micrometer aluminum layer on top was included in the simulations with a grid of 20x20. The simulated self and transfer impedance magnitudes as well as the phase of the self impedances are shown in Figures 26 and 27, respectively. Note that the self impedance shows a square root of frequency increase at high frequencies because of the copper base, which is much thicker than the skin depth at 1GHz. The transfer impedance has a monotonic low-pass nature.



**Figure 26:** Simulated impedances of a 0.2 micrometer silica layer on a one-ounce copper base, with 0.5 micrometer aluminium metallisation on the top. The assumed dimensions are: 4” by 4” square. Three impedance magnitudes are shown: self-impedance at the corner, self-impedance at the center, and transfer impedance between the center and one of the corners.

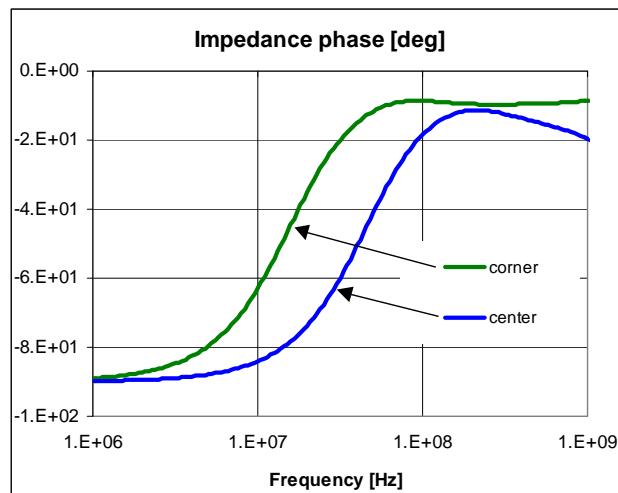


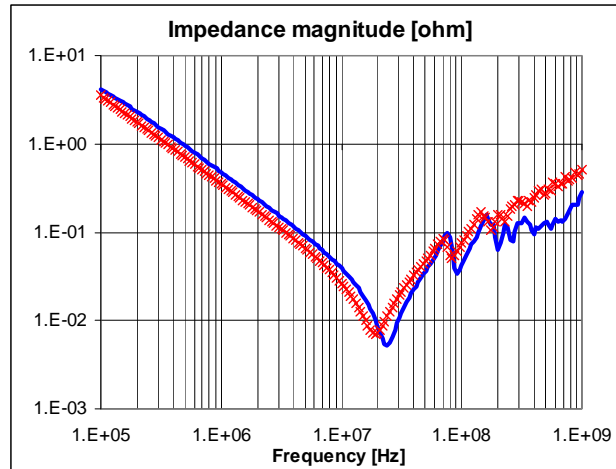
Figure 27.: Phase of impedances for the self-impedance curves on Figure 26.

### **III. 2. 1.6-mil and 0.3 mil dielectric layers with a dielectric constant of 16.**

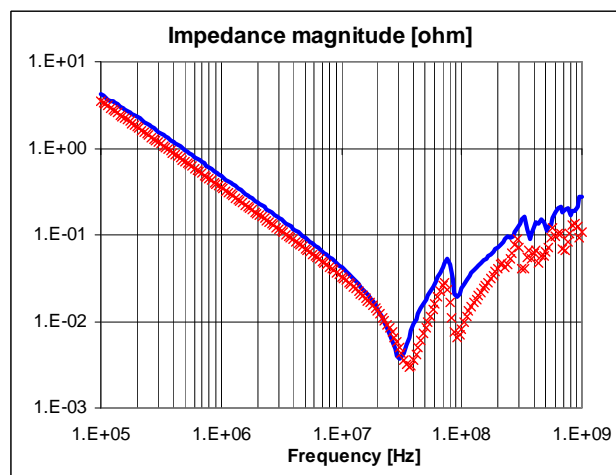
Figures 28 and 29 include the simulated and measured impedances on a test board with dimensions of 20" by 10". The board had six layers, four of those were arranged as power/ground plane pairs, located approximately 8 mils below the PCB surface. To allow the measurement of self and transfer impedances in various combinations, at every inch interval, a set of vias were connected separately to each plane. One set of test boards were fabricated with the two plane pairs of having 1.6 mil separation each, and a dielectric constant of approximately 16 ([15], [16]).

The simulation of the test boards were performed with a 20x10 lossy transmission-line grid. The measurements were done with the instrumentation and set up described in [7] and [8].

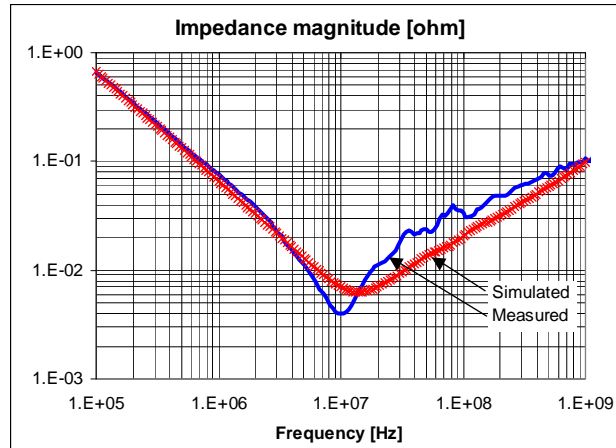
A standalone 0.3-mil sheet of copper-clad dielectric layer was also measured and simulated. The size of sheet was 20" by 10" with one ounce copper, and the self impedance was measured and simulated at one of the corners. Due to the difficulties of the probe connection to the standalone sheet, the measured and simulated impedances (shown in Figure 30) differ more at high frequencies.



**Figure 28.:** Measured and simulated self impedance at the corner of a 20" by 10" test board with 1.6mil dielectrics, dielectric constant 16. Solid line: measured, crosses: simulated.



**Figure 29.:** Measured and simulated self impedance of a 20" by 10" test board with 1.6mil dielectrics, dielectric constant 16. Solid line: measured, crosses: simulated. The probe point was five inches in each direction from the corner.



*Figure 30.: Simulated and measured self impedances at the corner of a 18" by 10" laminate with 0.3mil dielectric thickness and one ounce copper on each side.*

## Conclusions

It was shown that analytical plane-impedance expressions have a limitation due to the necessary truncation of the double infinite summation. Lossy transmission-line grid plane models can simulate power-ground planes with heavy losses. Thin dielectric layers in power distribution provide good suppression of plane resonances. When combined with thin conductive layers, a resistor-like flat impedance profile can be created.

## References:

- [1] Larry D. Smith, Istvan Novak, "Power-Distribution Challenges in the New Millennium," half-day public course at the 8<sup>th</sup> Topical Meeting on Electrical Performance of Electronic Packaging, October 24, 1999, San Diego, CA.
- [2] W. John, M. Vogt, U. Gierth, R. Remmert, "Methods for Parametrization of Transmission Line Structures on Printed Circuit Boards and other Dielectric Substrates," Proceedings of the 1994 EMC Symposium, May 16-20, 1994, Sendai, Japan, pp. 52-55.
- [3] Tanmoy Roy, Larry Smith, John Prymak, "ESR and ESL of Ceramic Capacitor Applied to Decoupling Applications," Proceedings of the 7<sup>th</sup> Topical Meeting on Electrical Performance of Electronic Packaging, October 26-28, 1998, West Point, NY, pp.213-216.
- [4] Sung-Jim Kim, Hai-Young Lee, Tatsuo Itoh, "Rejection of SSN Coupling in Multilayer PCB Using a Conductive Layer," Proceedings of the 7<sup>th</sup> Topical Meeting on Electrical Performance of Electronic Packaging, October 26-28, 1998, West Point, NY, pp.199-202..
- [5] T. Morris, "AC coupled termination of a printed circuit board power plane in its characteristic impedance," US Patent 5,708,400, Jan.13, 1998
- [6] I. Novak, "Reducing Simultaneous Switching Noise and EMI on Ground/Power Planes by Dissipative Edge Termination," in Proceedings of the 7<sup>th</sup> Topical Meeting on Electrical Performance of Electronic Packaging, October 26-28, 1998, pp.181-184.
- [7] I. Novak, "Probes and Setup for Measuring Power-Plane Impedances with Vector Network Analyzer," Proceedings of DesignCon99, High-Performance Systems Design Conference, Santa Clara, CA, Feb 1-4, 1999, pp. 201-215.
- [8] I. Novak, "Measuring Milliohms and PicoHenrys in Power Distribution Networks ," paper to be presented at DesignCon2000, Santa Clara, CA, February 1-4, 2000.

- [9] K. R. Carver, J. W. Mink, "Microstrip antenna technology," IEEE Transactions on Antennas and Propagation, AP-29, pp. 2-24, January 1981.
- [10] Nanju Na, Madhavan Swaminathan, "Modeling and transient Simulation of planes in Electronic Packages for the GHz Systems," , " Proceedings of the 87<sup>th</sup> Topical Meeting on Electrical Performance of Electronic Packaging, October 25-27, 1999, San Diego, CA, pp.149-152.
- [11] E. Leroux, P. Bajor, "Modeling of Power Planes for Electrical Simulations," Proceedings of the 1996 Wroclaw EMC Symposium, pp. 664-668.
- [12] Henry Hungjen Wu, Ken Lee, Alan Barber, "Accurate Power Supply and Ground Plane Pair Models," Proceedings of the 7<sup>th</sup> Topical Meeting on Electrical Performance of Electronic Packaging, October 26-28, 1998, West Point, NY, pp.163-166.
- [13] Richard Charbonneau, "An Overview of the NCMS Embedded Capacitance Project," NCMS Embedded Capacitance Conference, Tempe, AZ, February 28-29, 2000.
- [14] Todd Hubing, "Decoupling Capacitance, Theory and Application," NCMS Embedded Capacitance Conference, Tempe, AZ, February 28-29, 2000.
- [15] Gary Min, et. Al., "Developments of Polyimide-Based Capacitors and resistors for Embedded Passives," IPCExpo2000, April 4-6, 2000, San Diego, CA.
- [16] John Felten, "Embedded Ceramic/PWB Composite Resistors and Capacitors," IPCExpo2000, April 4-6, 2000, San Diego, CA.
- [17] Edward J. Reardon, Richard W. Carpenter, "Novel Thin Film Materials and Processes for Integral (Embedded) Resistors and Capacitors," 8th Circuit World Convention, September 10, 1999, Tokyo, Japan.
- [18] Edward Reardon, "Novel, Practical Materials for Embedded Capacitors and Resistors," IPCExpo2000, April 4-6, 2000, San Diego, CA.