POWERING DIGITAL BOARDS

DISTRIBUTION AND PERFORMANCE

Istvan Novak, Signal Integrity Staff Engineer
SUN Microsystems, Inc.

Meeting of the Greater Boston Chapter
IPC Designer's Council
February 9, 1999
In CMOS devices, at every edge, power is dissipated. The power can be lowered by:

- lower capacitance (smaller feature size)
- lower voltage

With submicron feature sizes, the breakdown voltage is below 5 V. Supply voltages in different circuits (core, IO, memory, etc) drop differently.

\[
E = \frac{1}{2} CV^2 \quad P = fCV^2
\]
Power Distribution Requirements


Powering digital boards - distribution and performance

Vdd
Power
Current
Frequency
Ztarget


Vdd
Power
Current
Frequency
Ztarget
Power-Distribution Hierarchy

Power Supply

Supply filter
Low frequency

Backplane

Printed Circuit Board

Board filter
Medium frequency

Component

Component filter
High frequency

SMPS Output Impedance

Measured output impedance of a 50W SMPS

Log magnitude of impedance [ohms]

Log frequency [Hz]

Output impedance varies with input and output conditions \((V_{in}, I_{load})\)

Powering digital boards - distribution and performance 5

IPC Boston Chapter
Feb. 1999

Istvan Novak
istvan.novak@worldnet.att.net
**DC Resistance**

**Resistance of a homogeneous square conductor:**

\[ R = \rho \frac{l}{A} \quad [\Omega] \]

- \( R \): resistivity of material \([\Omega\text{m}]\)
- \( \rho \): resistivity of material \([\Omega\text{m}]\)
- \( l \): length of conductor \([\text{unit}]\)
- \( w \): width of conductor \([\text{unit}]\)
- \( t \): thickness of conductor \([\text{unit}]\)

**Example:**

2 ounce (2.76mil, 70µm) copper on 6" by 9" PCB:

\[ \sigma = 5.85 \times 10^7 \quad [\text{S/m}] \]

\[ R_{\text{DC}} = 0.00037 \text{ ohms} \]  
(along the 9" side)

Copper sheet resistance:

\[ R_{\text{sheet}} = \frac{679}{T_p} \quad [\mu\Omega] \]

- \( T_p \): sheet thickness \([\text{mils}]\)

\[ R_{\text{DC}} = 370 \text{ microohms} \]  
(along the 9" side)
Simulated DC voltage drop on a pair of 3”x3.6” one ounce copper planes, with single-point feed at the front corner (left graph) and with line feed (right graph). Model: resistive grid with 0.2” grid size, 25A DC current sink at 1.5”x1.5” from upper left corner. The floor grids of graphs represent the simulation grid.
Inductors

Inductors in logic circuits are used for

* decoupling
* EMI filtering

Inductance may appear as side effect:

* inductance of lead-frames
* inductance of connector pins
* inductance of ground returns
* inductance of component leads

There are different selection criteria for

* small-signal filtering
* high-current decoupling
Inductor Parameters

- Nominal inductance
- Tolerance of inductance
- Rated AC and DC current
- Temperature dependence (TC)
- Loss factor
- Packaging, parasitics

Magnetic materials with high $\mu$ are nonlinear, unstable.

For decoupling and EMI filtering applications, lossy inductors are preferable.
Inductor Equivalent Circuit

Linearized model:

\[ \begin{align*} 
C_p & \quad \text{LESR} \\
\text{ESR} & \quad L 
\end{align*} \]

* ESR: Effective series resistance
* L: Nominal inductance
* \( C_p \): Equivalent parallel capacitance

Components in the equivalent circuit are nonlinear.
Inductor Parasitics, Decoupling

Fair-Rite lossy inductors:
three half turns

Single-turn SMD

Impedance magnitude [ohms]

1000

100

10

1M 10M 100M 1G

Frequency [Hz]

Powering digital boards - distribution and performance 11
Powering digital boards - distribution and performance

Measured:

- Impedance magnitude [dBΩ]
- Phase of impedance [deg]
- Frequency [MHz]

Specification:

- Impedance [ohms]
- Log. frequency [MHz]

TDK 70ACC453215T SMD L

IPC Boston Chapter
Feb. 1999
DC Bias, Saturation

Variation of total impedance with DC bias and frequency of a Fair-Rite bead.

Impedance [ohms]

Frequency [MHz]

<table>
<thead>
<tr>
<th>Frequency [MHz]</th>
<th>Impedance [ohms]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>10</td>
</tr>
<tr>
<td>10</td>
<td>30</td>
</tr>
<tr>
<td>30</td>
<td>50</td>
</tr>
<tr>
<td>100</td>
<td>70</td>
</tr>
</tbody>
</table>

0 A
2 A
15 A

Istvan Novak
istvan.novak@worldnet.att.net
Three-node EMI T filters are optimized for 50-ohm operation.

Using EMI T filters in low-Z high-Z bypassing/decoupling may result in peaky response.

Use lossy ferrites instead.

http://www.tdk.com
Capacitor Parameters

- Nominal capacitance
- Tolerance of capacitance
- Rated DC voltage (polarization)
- Quality factor, loss
- Packaging, parasitics

Dielectric materials with high $\varepsilon_r$ have several drawbacks. The capacitance is a function of:
- frequency
- DC and AC voltage
- temperature (TC)
- time (long-term stability)
Capacitor Equivalent Circuit

Simple model:

ESR  C  ESL

Extended model:

\[ R_S \quad L_S \quad C \quad R_P \]

C: Nominal capacitance
ESR: Effective series resistance
L_S: Effective series inductance (ESL)
R_S: Equivalent series resistance
R_P: Equivalent parallel resistance

Components in the equivalent circuit may be frequency dependent and/or nonlinear.
Capacitor Parasitics

1: 1nF chip
ESR = 1Ω ESL = 1.6nH

2: 100nF chip
ESR = 10mΩ ESL = 1nH

3: 220nF foil
ESR = 10mΩ ESL = 8nH

4: 10µF tantalum bead
ESR = 0.2Ω ESL = 6nH

Powering digital boards - distribution and performance 17
Capacitor Banks

Parallel capacitors [ohms]

5 x 1500uF 0.02 ohm 7nH
10 x 10uF 0.035 ohm 1.2nH
25 x 0.22uF 0.1 ohm 0.5nH
OSCON Bulk Capacitors

Impedance of capacitors [ohms]

Standard aluminium:
1500uF 1ohm 20nH

OSCON SP Series:
1500uF 10mohm 5nH

http://134.180.49.67/compo/os-con/index_e.html

IPC Boston Chapter
Feb. 1999

Istvan Novak
istvan.novak@worldnet.att.net
AVX Low Inductance Capacitance LICA

Internal construction:

View of BGA connections:

Interleaved matrix connections

ESL = 100 pH

AVX Corporation: Low Inductance Capacitors, S-LICC5M396-C brochure, 1996.
Technology Trend in Packaging of RLC Components (ESL)

2-5 nH   0.5-2 nH   0.3-1 nH   50-200 pH   10-50 pH

axial    SMD (length)   SMD (width)   SMD (height)   buried

1970s     late 80s      early 90s     late 90s

1206 size 0603 size 0402 size

Powering digital boards - distribution and performance 21
Location of Device Filter

- Bypass loop must be small
- Ground connection must be short
- VCC connection should be inductive and/or lossy (thin trace, ferrite bead)
Integrated Capacitors

Available technologies:
- thin FR4-like cores
- ceramic-filled cores
- TaO thin-film structures

HADCO:

EmCap™

Dk: 20-50
thickness: >=4mil
capacitance: 2.5nF/inch²

http:\www.hadco.com

Dk: 25
thickness: 0.02mil
capacitance: 2.5nF

http:\www.hidec.engr.uark.edu

Powering digital boards - distribution and performance 25
Simulated inductive voltage drop (mV) on a pair of 3”x3.6” copper planes with 1mil separation. Model: Tline grid with 0.2” grid size, 2A/nsec PWL current sink at 1.5”x1.5” from upper left corner. The floor grids of graphs represent the simulation grid.
Developed and licensed by Unysis, Zycon.

Multilayer board

* \( h = 2 \text{ mils} = 51 \text{ microns} \)
* \( \varepsilon_r = 4.5 \) (FR4)
* Low inductance \( \sim \) pH
* No signal trace between
* Layer count increases by two

\[
C_i = \varepsilon_o \varepsilon_r \frac{A}{d} = 78.4 \text{ pF/cm}^2
\]


Istvan Novak
istvan.novak@worldnet.att.net

Powering digital boards - distribution and performance 27

IPC Boston Chapter
Feb. 1999
Multilayer backplane

$h = 0.95 \text{ mm}$

$\varepsilon_r = 4.7$ (FR4)

$C_i = \varepsilon_0 \varepsilon_r \frac{A}{d} = 4.3 \text{ pF/cm}^2$

Correction with pad clearances is needed

Plane Resonances

10”x10”x31mil FR4 planes at 100MHz

Transfer impedance from Node 4,4

Magnitude and imaginary self impedances

Powering digital boards - distribution and performance  29

Istvan Novak
istvan.novak@worldnet.att.net

IPC Boston Chapter
Feb. 1999
Reducing Plane Resonances

Resonances can be suppressed by
- series DC loss (no good)
- series AC loss
- parallel AC loss [1]
- capacitive damping at selected locations [2]
- dissipative edge termination [3]

Reducing EMI by DET

Powering digital boards - distribution and performance 31

Zoomed:
First-cut Lumped Bypass Methodology

Identify target impedance/bandwidth >> bypass capacitance & ESR
Identify dI/dt load, $V_{\text{noise\_max}}$ >> plane and bypass-cap inductance
Identify power-supply response >> bulk capacitance & ESR

For detailed analysis, use SPICE with plane, package, and silicon models.
Correct Frequency Response

Target: 5mohm 10kHz-30MHz

- 5 x 1500uF 0.02 ohm 7nH
- 10 x 10uF 0.035 ohm 1.2nH
- 25 x 0.22uF 0.1 ohm 0.5nH
Correct Time Response

10A 10nsec PWL square current source
Lumped capacitors with ESR & ESL

Powering digital boards - distribution and performance 35
Low-ESR, Frequency Response

Target: 5mohm 10kHz-30MHz

5 x 1500uF 0.02 ohm 7nH
10 x 10uF 0.01 ohm 1.2nH
25 x 0.22uF 0.01 ohm 0.5nH
Low-ESR, Time Response

10A 10nsec PWL square current source
Lumped capacitors with ESR & ESL

Powering digital boards - distribution and performance 37
Summary

* Target impedance is in the mohm range
* Plane DC resistance analysis should be multi point
* Bypass capacitor ESL must be low
* Low-ESR capacitors may resonate
* Power planes have specific resonant frequencies
* Lumped models may be suitable for first-cut PDS design
* Detailed PDS design must include
  - component parasitics (ESL, ESR)
  - detailed plane model
  - power supply and package/silicon models are optional