Tolerance Calculations in Power Distribution Networks

The impedance gradient of power planes around bypass capacitors depends on the impedance of planes and the loss of bypass capacitor.

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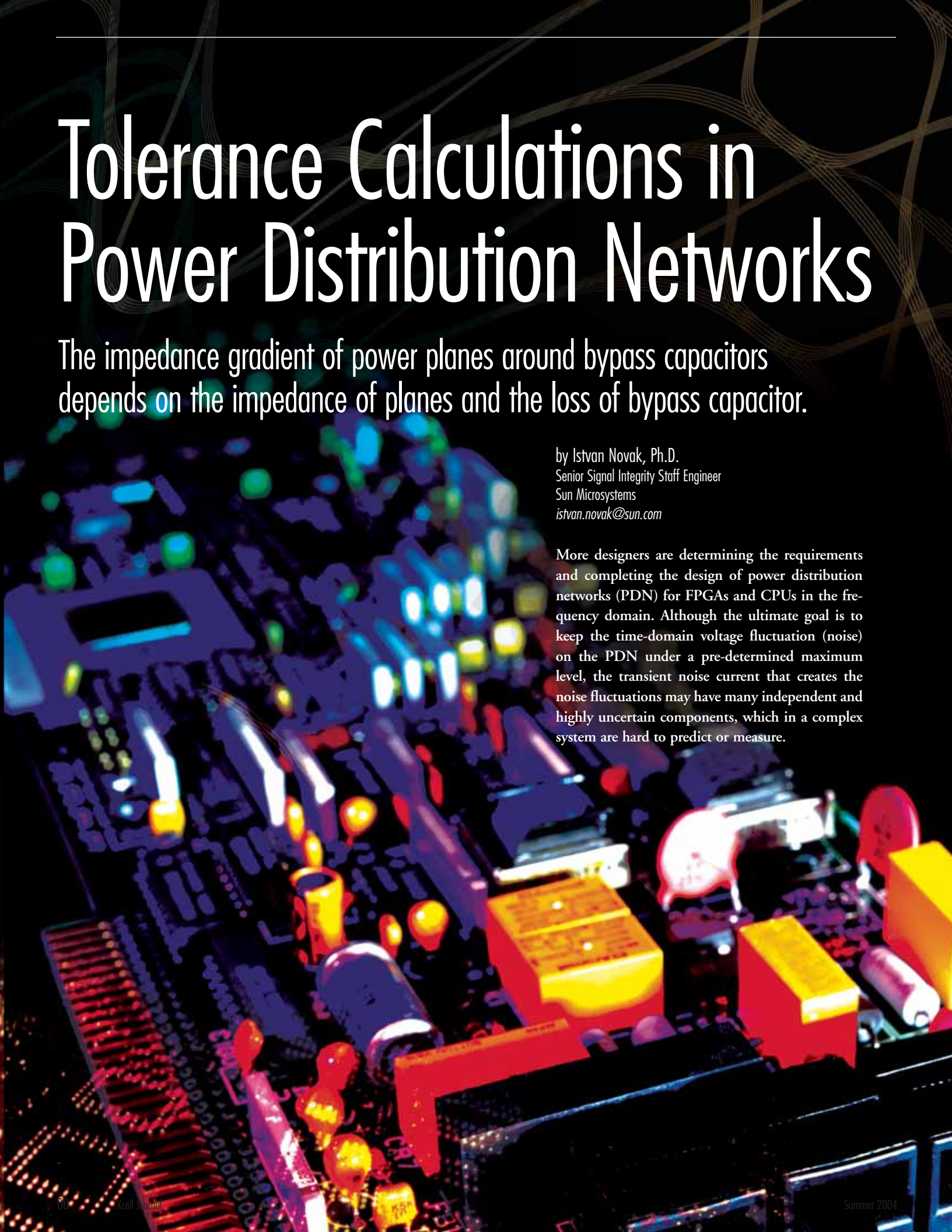
More designers are determining the requirements and completing the design of power distribution networks (PDN) for FPGAs and CPUs in the frequency domain. Although the ultimate goal is to keep the time-domain voltage fluctuation (noise) on the PDN under a pre-determined maximum level, the transient noise current that creates the noise fluctuations may have many independent and highly uncertain components, which in a complex system are hard to predict or measure.



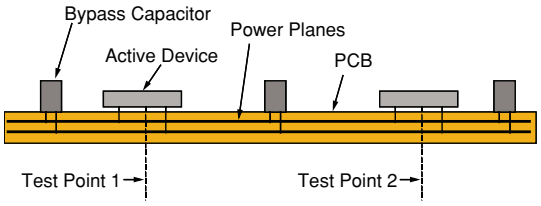


Figure 1 – Simple sketch of a PDN with two active devices, three capacitors, and one pair of power planes

Figure 2 – Three-element equivalent circuit of bypass capacitors

Figure 1 is a simple sketch of a PDN [1] with two test points. In the frequency domain, you can describe this network with a two-by-two impedance matrix, where the indices refer to the test points. Z_{11} and Z_{22} are the self impedances at test points 1 and 2, respectively, and Z_{12} and Z_{21} are the transfer impedances between test points 1 and 2.

With very few exceptions, the PDN components are electrically reciprocal; therefore the two transfer impedances are identical, and can be replaced with a mutual impedance term:

$$Z_{12} = Z_{21} = Z_M.$$

You cannot assume electrical symmetry, however, so Z_{11} and Z_{22} are, in general, different. You can calculate the noise voltages at test points 1 and 2 generated by the noise currents of $I_1(t)$ and $I_2(t)$ of the two active devices with the following formula:

$$V_1(t) = Z_{11}I_1(t) + Z_MI_2(t)$$
$$V_2(t) = Z_MI_1(t) + Z_{22}I_2(t)$$

A PDN comprises power sources (DC/DC, AC/DC converters, batteries); low- and medium-frequency bypass capacitors; PCB planes or other metal structures (a collection of traces or patches); packages with their PDN components; and the PDN elements of the silicon [2]. When dealing with board-level PDN, its impedance contributions to the overall PDN performance are much more stable and predictable, so much so that we often forget to analyze our PDN designs against component tolerances. In this article, we'll show how tolerances of bypass-capacitor parameters, such as capacitance (C), effective series resistance (ESR), effective series inductance (ESL), and capacitor location impact the impedance of PDNs.

C, ESR, and ESL Tolerance Effects

Figure 2 shows the simple equivalent circuit of a bypass capacitor when neglecting the parallel leakage of the capacitor. The series capacitor-resistor-inductor circuit shows a resonance frequency with a given quality factor (Q). You can calculate the series resonance frequency (SRF) and Q from the equations below:

$$SRF = \frac{1}{2\pi\sqrt{C * ESL}};\quad Q = \frac{\sqrt{\frac{ESL}{C}}}{ESR}$$

Although in a general case all three elements in the equivalent circuit are frequency-dependent [3], for the sake of simplicity, and because it would not change the conclusions of this article, we'll use frequency-independent constant parameters.

Figure 3 shows the impedance magnitudes of three different capacitors you could use in a PDN. Each curve has a label, giving the C, ESR, and ESL values assumed for the part. The SRF and Q values are also shown for each part. With these numbers, the 100 uF part could be a tantalum brick; the 1 uF and 0.1 uF parts could be multi-layer ceramic capacitors (MLCC).

When connecting capacitors with different SRFs in parallel, they may create anti-resonance peaks where the impedance magnitude exceeds the lower boundary of the composing capacitors' impedance magnitude values [4] [5]. The impedance penalty gets bigger as the Q of capacitors gets bigger, or as their SRFs are farther apart in frequency.

The anti-resonance peaks get even bigger when you consider the possible tolerances associated with the capacitor parameters. We illustrate this in Figure 4, which shows what happens in typical, best, and worst cases when you connect the three capacitors from Figure 3 in parallel. The plot assumes no connection impedance or delay between the capacitors. You can use this assumption as long as the distance between the capacitors is much less than the wavelength of higher frequency of interest, and the connecting series plane impedance is much less than the impedance of capacitors.

The frequency plot extends up to 100

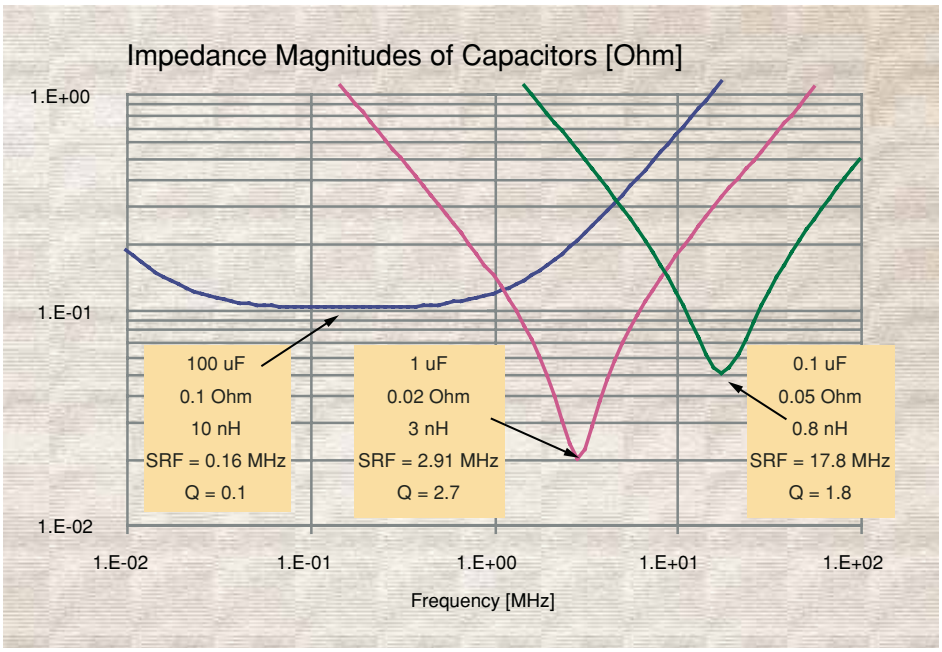


Figure 3 – Impedance magnitudes of three stand-alone bypass capacitors

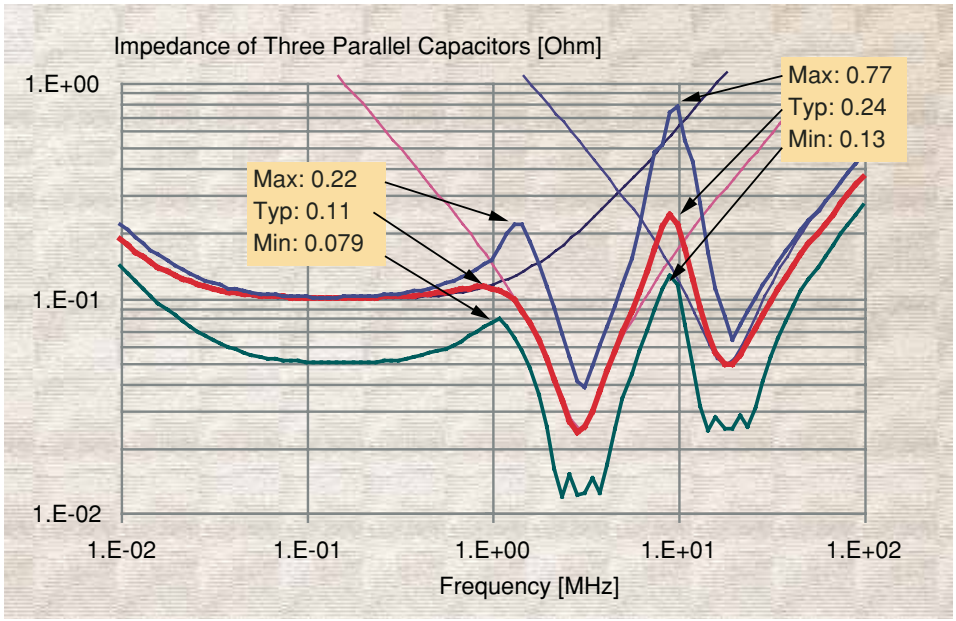


Figure 4 – Typical, highest, and lowest impedance curves of the three parallel connected capacitors shown in Figure 3

MHz, which represents a wavelength of 15 meters in FR4 PCB dielectrics. This tells us that the lumped approximation is valid in this entire frequency range, no matter where we place these capacitors on a typical-size PCB.

Table 1 lists the percentage tolerance ranges for the C, ESR, and ESL values used in Figure 3. We calculated the impedance curves and tolerance analysis with a simple spreadsheet [6]. The spreadsheet calculates the complex impedance resulting from the three parallel connected impedances. During tolerance analysis, the spreadsheet steps each parameter systematically though their minimum and maximum values – specified by the tolerance percentage entered – and accumulates the lowest and highest magnitudes at each frequency point.

For Figure 4, we assume a capacitance tolerance of +-20% for all three capacitors. For ESR, datasheets usually state the maximum value but no minimum, so we can assume a +0 to -50% tolerance around the nominal value. ESL strongly depends on both the capacitor's construction and its mounting geometry. For this example, we assume +-25% inductance variation.

Figure 4 also shows the impedance magnitudes of the individual capacitors with thin lines. The three heavy lines in the figure represent the maximum, typical, and minimum values from all possible tolerance permutations. All three curves exhibit two peaks: the first around 1 MHz and a second around 10 MHz.

The trace representing the typical case has an impedance magnitude of 0.11 Ohms and 0.24 Ohms at these peak frequencies, respectively. Impedance at and around the first peak is mostly below the impedance curves of the 100 uF and 1 uF capacitors. The second peak, however, exceeds the lower boundary of the impedance curves of the 1 uF and 0.1 uF capacitors by about a factor of two. This is a typical anti-resonance scenario.

In a worst-case combination of component tolerances, the second anti-resonance peak increases from 0.24 Ohms to 0.77 Ohms, a 220% increase. The contributors to the second anti-resonance peak are the ESR and ESL of the 1 uF capacitor, and the C and ESR of the 0.1 uF capacitor. The sum of the tolerances of these four parameters is 145%, but they increase the impedance at the peak by 220%. This illustrates that the resonance magnifies the tolerance window.

	C1	tol. [%]	C2	tol. [%]	C3	tol. [%]
Capacitance [uF]:	100	20 -20	1	20 -20	0.1	20 -20
ESR [Ohms]:	0.1	0 -50	0.02	0 -50	0.05	0 -50
ESL [nH]:	10	25 -25	3	25 -25	0.8	25 -25

Table 1 – Parameters used for Figure 4

Bypass Capacitor Range

Bypass capacitors are considered to be charge reservoir components, and common wisdom tells you to put them close to the active device they need to feed. We will show here that when the capacitor and the active device are connected with planes, the ratio of plane impedance and ESR of capacitor will determine the spatial gradient of impedance around the capacitor. Even at low frequencies, the impedance gradient can be significant.

Let's look at the self-impedance distribution over a 2" x 2" plane pair with 50 mil plane separation. You will get this plane separation if you have just a few layers in the board and if they are not placed next to each other in the stack-up. The characteristic impedance of these planes is approximately 1.7 Ohms. You can calculate the approximate plane impedance from our third equation [7]:

$$Z_p = \frac{532}{\sqrt{\varepsilon_r}} \frac{h}{P}$$

where Z_p is the approximate plane impedance in Ohms and h and P are the plane separation and plane periphery, respectively, in the same but arbitrary units.

We assume one piece of capacitor located in the middle of the planes. MLCC capacitors are available with as much as a few hundred uF capacitance in the 1210 case style, and their ESR can be as low as one milliohm. For this example, we use C = 100 uF, ESR = 0.001 Ohm, ESL = 1 nH. The SRF of this part is 0.5 MHz.

The surface plot of Figure 5 shows the variation of self-impedance magnitude over the plane at 0.5 MHz. The gray bottom area of the graph represents the top view of the planes. The grid on the bottom area shows the locations where the impedance was calculated: the granularity was 0.2 inches. The logarithmic vertical scale shows the impedance magnitude between 1 and 10 milliohms.

We calculated the surface impedance with a spreadsheet [8]. The macro in the spreadsheet calculates the impedance matrix by evaluating the double series of cavity resonances. It then combines the complex impedance of plane pair with the complex impedance of the bypass capacitor.

The impedance surface at 0.5 MHz has a sharp minimum in the middle; here the capacitor forces its ESR value over the plane impedance. However, as we move away from the capacitor, the impedance rises very sharply. At 0.2 inches away, the impedance is approximately 50% higher; 0.4 inches away, the impedance magnitude doubles. At the corners of the 2" x 2" plane pair, the impedance magnitude is almost 10 milliohms.

When changing either the plane impedance or the ESR of capacitor so that their values are closer, the variation of impedance over the plane shape gets smaller. Figure 6 shows the impedance surface of the same plane shape and same capacitor in the middle, except we increased ESR from 1 to 7 milliohms and decreased the plane separation from 50 to 20 mils. Now the impedance surface at SRF varies only about 10% over the plane area.

For Figures 5 and 6, you can see the same characteristic behavior if you sweep the frequency over a wider frequency range in the spreadsheet. The impedance surface of Figure 5 changes and fluctuates significantly, while the impedance surface of Figure 6 changes less with frequency.

Note that this trend does not change if we have more capacitors on the board. If we have significantly different plane impedance and cumulative ESR of capacitors, the impedance gradient will be big, and we must use many capacitors to hold the impedance uniformly down over a bigger area even at low frequencies.

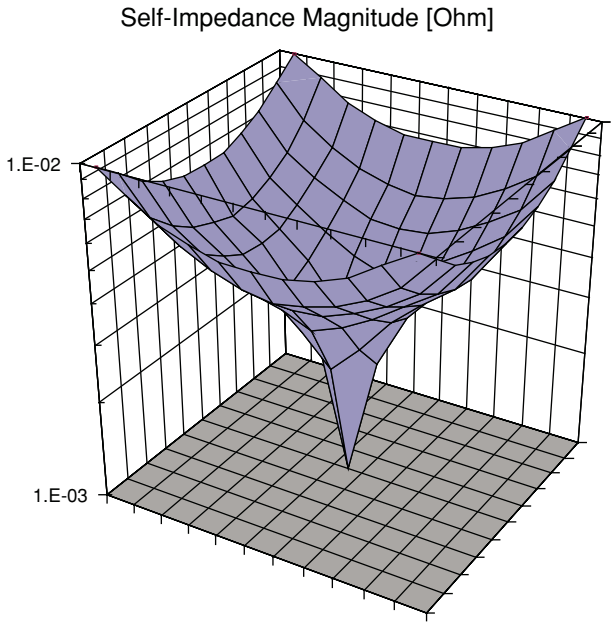


Figure 5 – Self-impedance at 0.5 MHz on a 2" x 2" plane pair with 50 mils dielectric separation, with a 100 uF, 0.001 Ohm, 1 nH capacitor located in the middle

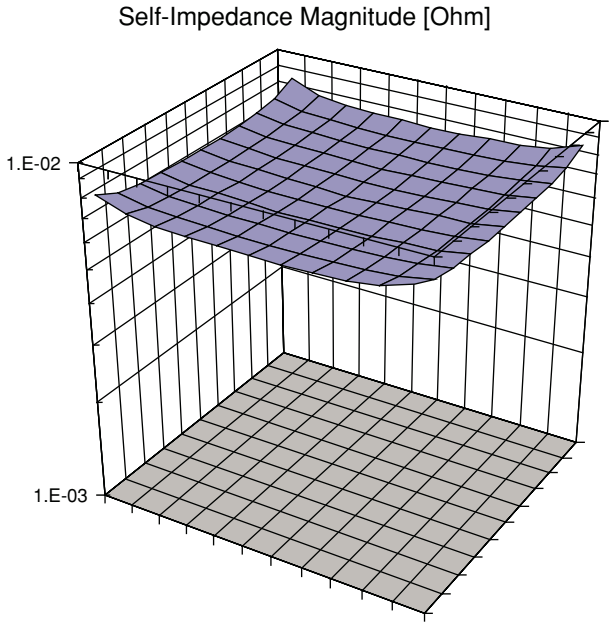


Figure 6 – Self-impedance at 0.5 MHz on a 2" x 2" plane pair with 20 mils dielectric separation, and a 100 uF, 0.007 Ohm, 1 nH capacitor located in the middle

Conclusion

The impedance tolerance window at the anti-resonance peak of paralleled discrete bypass capacitors widens with higher Q capacitors. To keep the impedance window due to tolerances small, you need either many different SRF values tightly spaced on the frequency axis, or the Qs of capacitors must be low.

Contrary to popular belief, the service range of low-ESR capacitors is severely limited when connected to planes of much higher impedance. But you can achieve the lowest spatial impedance gradient if the cumulative ESR of bypass capacitors is close to the characteristic impedance of planes. Σ

References

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[5] Ritchey, Lee W. 2003. *Right the First Time, A Practical Handbook on High Speed PCB and System Design, Volume 1.* Glen Ellen: Speeding Edge.

[6] Download Microsoft™ Excel spreadsheet at *http://home.att.net/~istvan.novak/tools/bypass49.xls*

[7] Novak, I., L. Noujeim, V. St. Cyr, N. Biunno, A. Patel, G. Korony, and A. Ritter. 2002. Distributed Matched Bypasssing for Board-Level Power Distribution Networks. *IEEE Transactions on Advanced Packaging* 25(2):230-243.

[8] Download Microsoft Excel spreadsheet at *http://home.att.net/~istvan.novak/tools/Caprange_rev10.xls*