

Do Not Perforate Planes Unnecessarily

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I take a quick detour from the series of columns about the inductance of bypass capacitors and devote this column to a few comments about via placement and its potentially detrimental impact of signal and power integrity when antipads heavily perforate planes.

My thoughts were triggered by the column of Kate Mayer, CID and CID+ instructor for IPC [1]. In the excellent article Kate argues that vias should be placed along lines, or over a grid, to allow the routing of traces in the ‘streets’ formed by the vias. Nicely arranged vias result in a neat printed circuit board layout and makes routing easier.

During my career I have always listened eagerly to expert technologists, who can tell us the various constraints, Dos and DONTs of practical designs. Layout and PCB design is no exception: we can learn a lot from experienced people in this field. Many years ago I was one of those engineers who drove layout people crazy with last-minute requests to make the PCB layout ‘nicer’ and more regular. Since then in the industry I learned the new competitive art: the design should be ‘good enough’ but not better. Experience also taught me to carefully look at all possible consequences of the various design choices we make, which leads me to the heart of this column.

Lining up vias on a regular grid, though it certainly helps routing, may create unwelcome side effects at high frequencies. One of the possible obvious problems is illustrated in *Figure 1*. The photo shows a small detail of a plug-in module from a personal computer. The photo was taken with a light source behind the module, thus the open via barrels show up as bright spots, and the antipads around the barrels, where copper is removed on all layers, come through as light green circles. You can notice that the antipads are slightly bigger than the via pitch, and therefore the line of vias in this case results in a full cut in the reference planes.

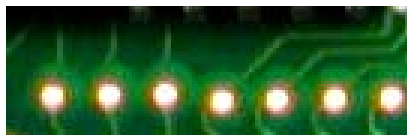


Figure 1: *Photo of a printed circuit board with via antipads cutting through the planes. The vias are lined up and the antipads are as big as the via pitch, thus cutting a continuous slot in the reference plane.*

If there is no need to route traces in between vias, the loss of reference plane may be acceptable. However, we would still need to consider the impact of the slot on the modal resonances of the power-ground plane pairs. You can read more on this in [2].

There are instances in the printed circuit board designs, where we have very little choice, and we have to follow regular component footprints with the vias. This is the case when we use BGA or LGA packages, multi-pin connectors and sockets. These components usually have their pins on a regular grid, and the antipads associated with the vias will create areas of periodical perforations. Plane perforations near high-speed signal traces create a series of miniscule discontinuities, and with a regular via pattern, the reflections from the discontinuities will line up destructively at certain frequencies, creating a strong filtering effect [3].

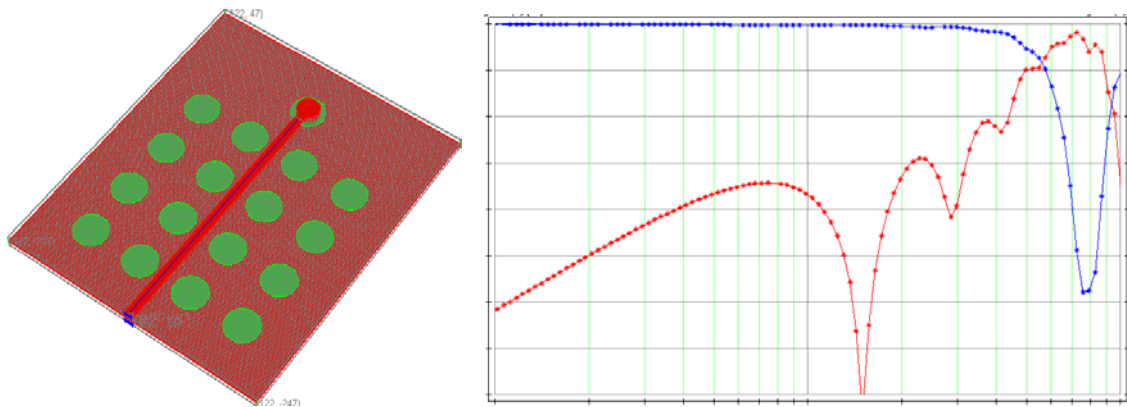


Figure 2: Trace over a perforated plane (left) and its simulated S parameters (right). Red trace: return loss. Blue trace: insertion loss. Horizontal scale: 1-100 GHz, logarithmic. Vertical scale 0 to -40dB.

Figure 2 shows the reflection and insertion loss of a trace over a plane with periodical 30-mil antipads on a 50-mil grid. The structure was simulated with a full-wave field solver [4]. Note that above 30GHz reflection goes up and insertion loss also increases, indicating that the structure behaves like a band-reject filter. With a 50-mil (1.25 mm) via pitch, the first suckout in the transmission occurs above 50GHz, which is probably not a concern except for speeds beyond 20Gbps. However, as it was shown in [5], our printed circuit boards may have several levels of periodicities, and those can push the lowest resonance frequency to much lower values.

Conclusions: Do I suggest not to line up vias in order to create routing channels for signal traces? No, I do not say that. From a layout and routing perspective many times we have no choice but to line up vias. However, the board designers and layout people need to be aware of the consequences. We need to avoid the worst if at all possible: completely cutting through reference planes. We also need to understand the resonances created by the periodical via antipads, which eventually impair signal quality. If plane perforation becomes unavoidable, the extra attenuation and dispersion should be taken into account in the design.

References:

- [1] Kate Mayer, Manage Your Vias, Manage Your Design
<http://www.pcbdesign007.com/pages/zone.cgi?a=72004&artpg=1>
- [2] Istvan Novak, Jason R. Miller, Eric Blomberg, “Simulating Complex Power-Ground Plane Shapes with Variable-Size Cell SPICE Grids,” Proceedings of the the 11th Topical Meeting on Electrical Performance of Electronic Packaging, October 21-23, 2002, Monterey, CA.
Available at <http://www.electrical-integrity.com/>
- [3] Gustavo Blando, Jason R. Miller, Istvan Novak, Jim DeLap, Cheryl Preston, “Attenuation in PCB Traces due to Periodic Discontinuities,” Proceedings of DesignCon 2006, February 6-9, 2006, Santa Clara, CA. Available at <http://www.electrical-integrity.com/>
- [4] www.simbeor.com
- [5] Jason R. Miller, Gustavo Blando, Istvan Novak, “Additional Trace Losses due to Glass-Weave Periodic Loading,” Proceedings of DesignCon 2010, February 1-4, 2010, Santa Clara, CA. Available at <http://www.electrical-integrity.com/>