

Thin Laminates: Buried Capacitance or What?

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After the heated debate about the proper selection of bypass capacitors, probably the next most controversial topic is about thin laminates. Are they really beneficial? Do we really need them?

Since the early 1990s thin laminates have been mostly marketed as buried capacitance, many times also suggesting or at least implying that by using thin laminates we can eliminate many of the high-frequency bypass capacitors on the board. Is it really possible? The answer lies in the electrical properties of thin laminates.

A pair of rectangular parallel sheet conductors – a power/ground layer pair - separated by dielectrics, as shown in *Figure 1*, creates static capacitance.

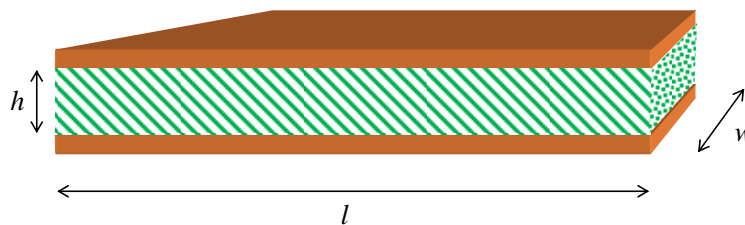


Figure 1: A pair of metal layers forms a parallel-plate capacitor.

The C capacitance is proportional to the dielectric constant of the laminate ($\epsilon_0\epsilon_r$) and area of conductors ($l*w$) and inversely proportional to the dielectric thickness (h):

$$C = \epsilon_0\epsilon_r \frac{l w}{h}$$

The dielectric constant of free space, ϵ_0 is 8.85 pF/m, and the ϵ_r relative dielectric constant is around 4 for many of our printed circuit board laminates. If we plug in l , w and h in meters, we get the capacitance in farads.

The expression tells us where the name ‘Buried Capacitance’ comes from: a pair of power/ground layer pair gives us capacitance buried in the stackup; and we get more capacitance as we use thinner laminates and/or higher dielectric constants. A one-inch square power-ground pair of the popular 50um (2-mil) buried capacitance laminate produces approximately 450 pF of capacitance. If we double the dielectric thickness, the capacitance goes down by a factor of two; if we cut the dielectric thickness in half, the capacitance doubles.

A simple stackup choice, as shown in *Figure 2*, gives us the opportunity to increase the amount of capacitance: by placing the power and ground layers next to each other,

without a signal layer in between, we can place the plane layers much closer and we get more capacitance. When we have a signal layer between power and ground, the minimum separation is limited by how narrow traces we can etch reliably. The closer we put the planes, the narrower traces we would need to use to maintain our impedance target. For 50-ohm traces and assuming regular materials and processes, the plane-to-plane separation is limited to about 10 mils (250 μm) or more. In contrast, if we pair up the power and ground layers, we can put the layers much closer, limited only by the risk of shorting due to finite surface roughness. Note that *Figure 2* shows only part of a multi-layer stackup and during the definition of a full stackup we need to take into account various additional factors, such as symmetry, thickness limitation of the board, etc.

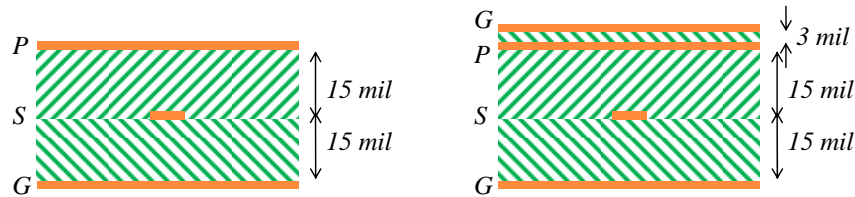


Figure 2: We can get more static capacitance between power and ground planes by placing them next to each other, without a signal layer in between.

So if we use thin laminates for power-ground layers, can we really eliminate many bypass capacitors from the board? The answer is yes, but not because the increased capacitance of the thin laminate, rather due to its lower inductance. *Figure 3* shows the measured impedance on a board similar to the one we showed in *Figures 2 and 3* of the previous column “The Big Bang and the Power Distribution”.

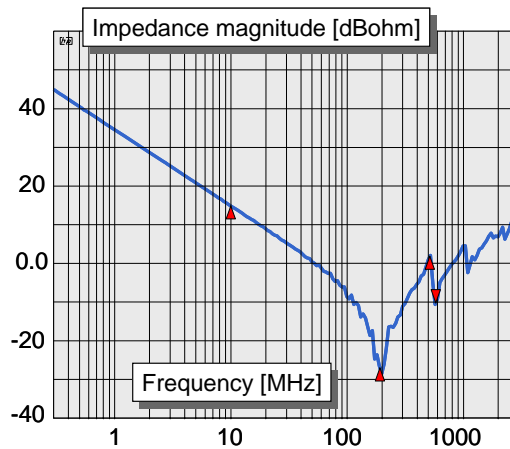


Figure 3: Measured self impedance magnitude of a power rail on a bare PCB with 2-mil dielectric.

The vertical scale of the figure is dBohm. Zero dBohm corresponds to one ohm, -20 dBohm refers to 0.1 ohms, and so on. At low frequencies the curve shows a straight down slope; on a log-log scale this indicates capacitance. We can calculate the static

capacitance for instance from the 60MHz frequency point, where the impedance magnitude is zero dBohm, or one ohm. This value corresponds to about 3nF static capacitance. At 200MHz the curve has a minimum, followed by an upslope, which corresponds to inductance. If for now we neglect the small resonances (we will cover those in later columns), we can approximate the curve with an average line, which goes through the zero dBohm value at 1GHz. This corresponds to about 150pH inductance.

The 3nF static capacitance is not much on a power rail: unless the circuit draws very-very little power, we usually need orders of magnitude more capacitance to keep the impedance below our target value at lower frequencies. The real electrical benefit of the tin laminate comes from its low inductance. The inductance of a plane pair is approximately $L[\text{pH}] = 33 * h[\text{mil}]$, which yields 66pH for our 2 mil plane separation in the above example. As opposed to the static capacitance of the laminate, which stays the same everywhere on the plane, inductance changes with location. It is the lowest in the middle of the plane and goes up rather sharply towards the sides and edges. The impedance of *Figure 3* was measured at one of the corners, this explains the 150pH inductance value (instead of the 66pH value expected from the 2-mil thickness). This inductance, however, even at the corner, is much lower than what we can achieve with a single bypass capacitor. In contrast, the inductance of a single bypass capacitor is usually around 1nH, at least ten times higher than the average inductance of a 2-mil plane pair.

Whether it is a discrete bypass capacitor or a power-ground plane pair, the impedance becomes inductive above the series resonance frequency. At high frequencies all what matters is the inductance, and thin laminates create very low inductance indeed. So when it comes to thin laminates, think about their inductance rather their capacitance.

References:

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- [2] James R. Howard, Gregory L. Lucas, "Capacitor laminate for use in capacitive printed circuit boards and methods of manufacture," US Patent 5,079,069, January 7, 1992.
- [3] Joel S. Peiffer, "The history of embedded distributed capacitance," Printed Circuit Design and Manufacture, August 2004, pp. 32-37.
- [4] TecForum HP-TF2: "Thin PCB Laminates for Power Distribution. How Thin is Thin Enough?" February 2002, DesignCon 2002. Available at www.electrical-integrity.com