PCB Design 007 *QuietPower* column

Will power planes disappear?

Istvan Novak, Oracle, March 2012

In modern multi-layer printed circuit boards power planes can help us to achieve all three possible functions of a power distribution network: a) to provide clean power to the electronics, b) to provide good return path to high-speed signals, and c) to avoid excess electromagnetic radiation. If we look at printed circuit boards from decades ago, they had very few (if any) planes in the stackup. We can ask: are power planes inevitable in modern printed circuit boards? A DesignCon 2012 paper offers an interesting alternative.

As we showed in the first QuietPower column [1], the number of bypass capacitors on our boards depends on the inter-play of various factors. As a result, in the old days it was possible to create good working boards with no bypass capacitors at all, and even though today we have a tendency to use many bypass capacitors, we can predict that in the future this number can –and probably will- decline. Similarly, the inter-play of a set of constraints determines whether or not a printed circuit board needs power planes. As we look at those constraints, we can identify a similar trend: in the future the need for power planes may diminish or go away altogether. The change is already under way, and power planes –at least full-layer planes- are disappearing fast from our boards.

The first figure of [1] showed that early printed circuit boards not only had no bypass capacitors, they had no power planes either. As current consumption and circuit density increased, we had to use bus-bars or wider traces to carry power, eventually turning the power layers into full planes. This actually happened first on the reference (ground) connections: the faster interconnects had to be impedance matched, and a solid reference plane next to the traces is a convenient way to achieve this goal. Power planes followed the trend: first wider traces, then patches and islands, finally full-layer planes. Full-layer planes were and are still used when the entire board needs only one or just a few different supply voltages. However, performance optimization resulted in a rapid increase of independent supply voltages, and with many different supply rails on the board, we simply cannot afford full layers assigned to them. We have to reuse power layers to accommodate a number of power puddles and smaller plane shapes, each serving a different power rail.

An interesting paper at DesignCon 2012 [2] outlines a possible next step, when not only chips are fed with separate supply nets, but also each IO cell in a chip. Instead of combining all supply pins on a chip into a single power rail, each signaling cell in the package has its own power connection, essentially feeding the chip with a number of power traces rather than a power plane.

Figure 1 shows a traditional power distribution scheme based on planes. The signal traces reference the power planes, and cavity modes of planes are excited. Unless the

power distribution network suppresses the resonances, the impedance peaks of the cavities may deteriorate high-speed signaling.

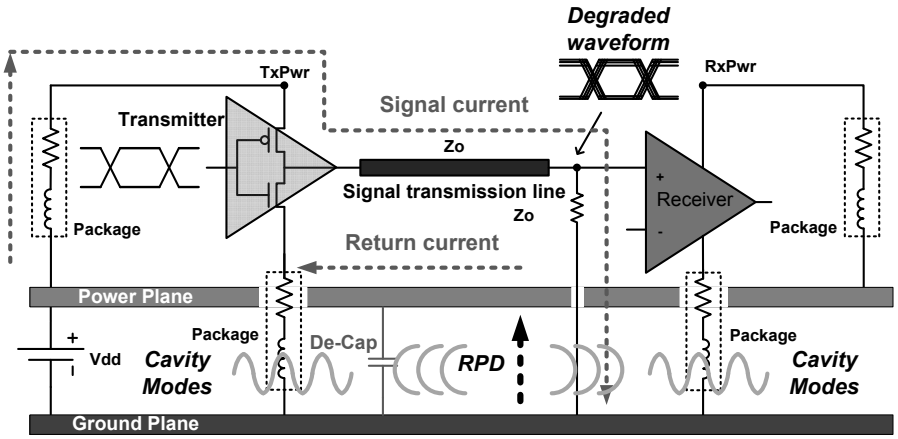

***Figure 1**: Plane-based signaling and power distribution network. (Figure 2 from [2], used with permission)*

If we replace the power planes with Power Transmission Lines (PTL), feeding each IO cell separately, the signaling will become cleaner, because the cavity resonances associated with the planes are eliminated. This scheme is shown in *Figure 2*.

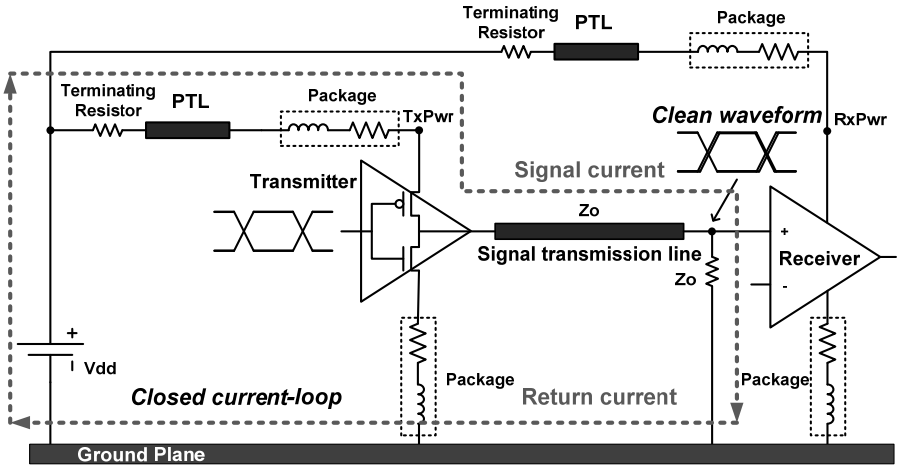

***Figure 2**: PTL-based signaling and power distribution network. (Figure 3 from [2], used with permission)*

Figure 3 compares the insertion loss of a test-board trace with the two alternatives. The PTL-based trace has a nice and smooth insertion loss profile, not disturbed by the power distribution network. The plane-based solution (with no power distribution network to suppress cavity resonances) exhibits a series of dips where the PDN impedance has peaks.

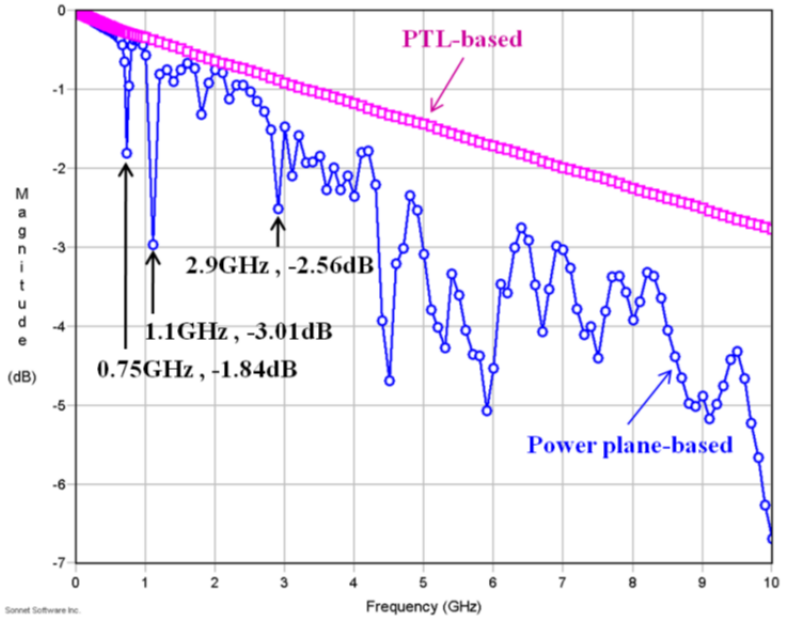

***Figure 3**: Comparison of plane-based and PTL-based insertion loss of a signal line. (Figure 12 from [2], used with permission)*

A PTL-based solution could use one power trace per differential cell. Assuming good symmetry between the positive and negative signals of the differential pair, the sum of the two currents, the supply current to the differential cell, could have very little high-frequency fluctuation. This will minimize the need for local decoupling capacitance at the cell and the resulting eye diagram will be more open (see *Figure 4*).

PTL-based power distribution can reduce the need for power planes and bypass capacitors at the same time. With disappearing planes, on the other hand, the vertical isolation between adjacent signal layers will be also lost, and therefore in high-speed multilayer boards the ground planes will probably stay with us longer.

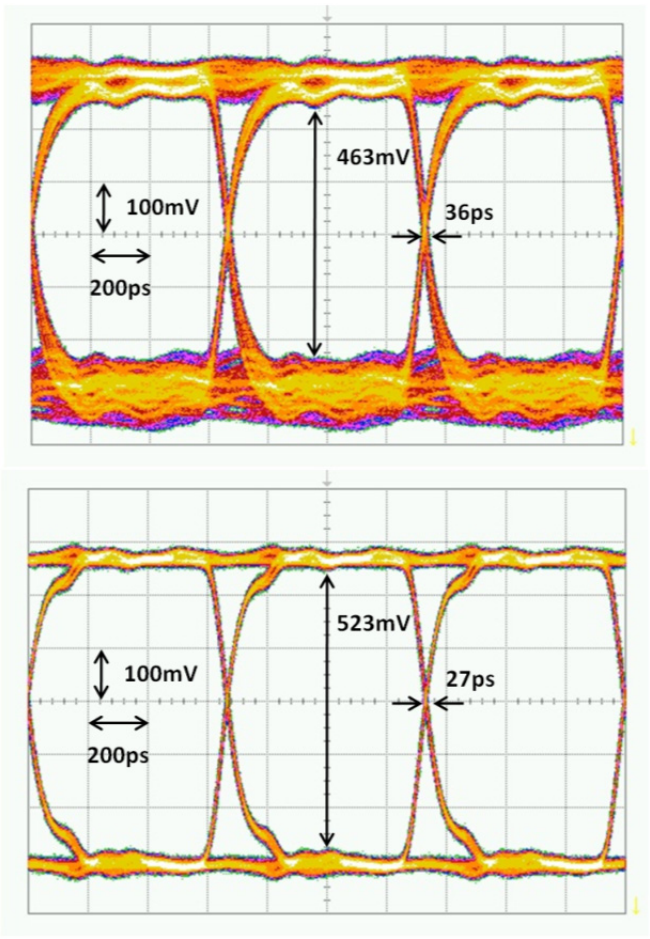

***Figure 4**: Comparison of plane-based (top) and PTL-based (bottom) eye diagram of a signal line. (Figure 14 from [2], used with permission)*

References:

[1] QuietPower column: "How many bypass capacitors do we need?"

[2] "Are Power Planes Necessary for High Speed Signaling?", DesignCon 2012, January 28 – February 1, 2012, Santa Clara, CA. Available at http://www.ece.gatech.edu/research/labs/hppdl/Epsilon2010/index.html