PCB007 QuietPower column

Memories from early years of DesignCon

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DesignCon is a conference in Santa Clara, California, late January or early February each year, attracting signal and power integrity practitioners from around the globe [1]. People who started to attend this conference in recent years, may not know that –even though DesignCon's history is not as long as some other professional conferences, such as the ones sponsored by IEEE- DesignCon started about twenty-five years ago.

My first personal experience with what later became DesignCon as we know it today, was almost exactly twenty years ago to the day when this column goes online. On April 5, 1993, in Budapest, Hungary, there was a High Speed Digital Design Symposium. Figure 1 shows the front page of the flyer.

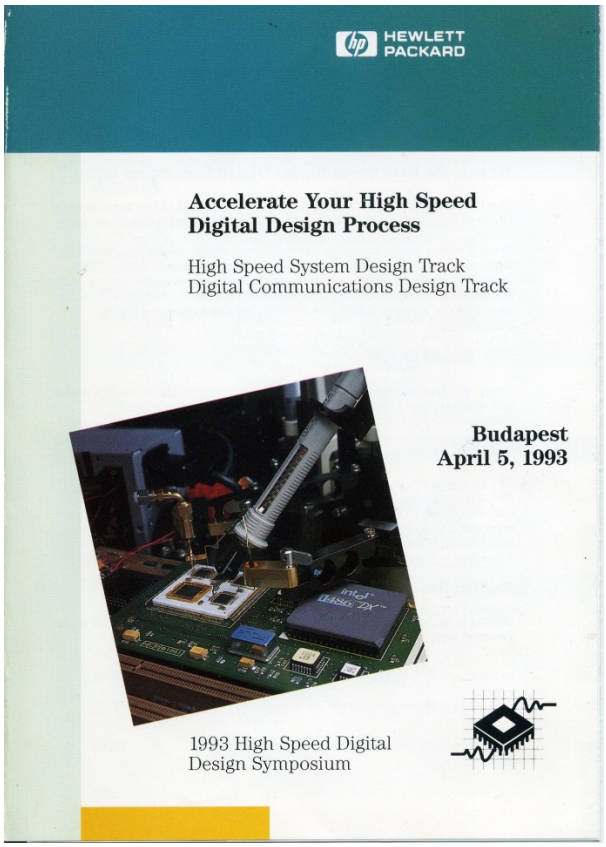
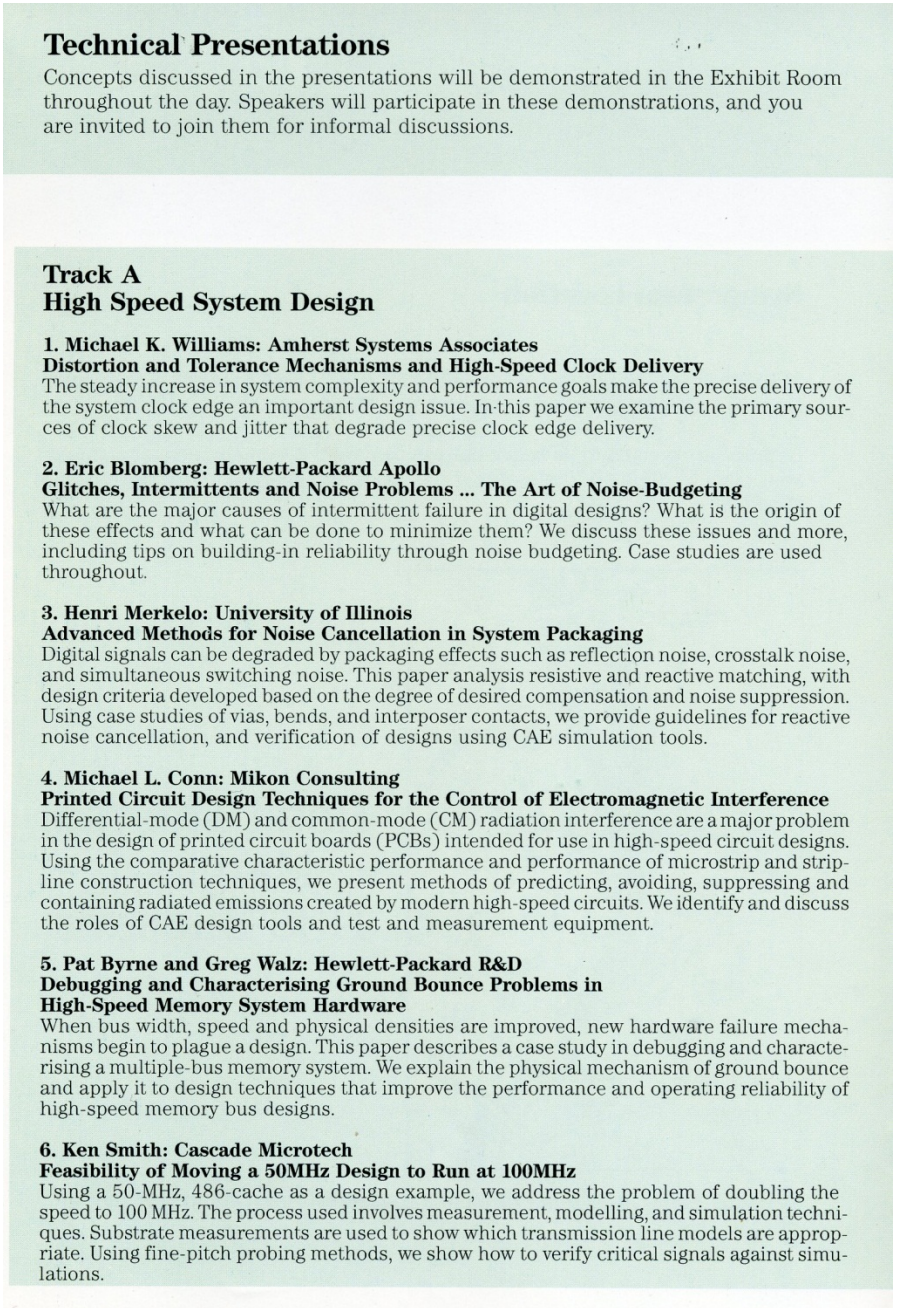


Figure 1: *Front page of the conference flyer for the April 5, 1993 High Speed Digital Design Symposium, sponsored by Hewlett Packard.*

For the younger generation it is worth mentioning that Hewlett Packard in those years was mostly known for their measurement solutions provided by the business unit that later became Agilent. There were two tracks in the symposium: one about High Speed System Design and one for Digital Communications Design. Figure 2 shows the papers, presenters and abstracts of Track A, High Speed Digital Design.



Technical Presentations

Concepts discussed in the presentations will be demonstrated in the Exhibit Room throughout the day. Speakers will participate in these demonstrations, and you are invited to join them for informal discussions.

Track A
High Speed System Design

1. Michael K. Williams: Amherst Systems Associates
Distortion and Tolerance Mechanisms and High-Speed Clock Delivery
The steady increase in system complexity and performance goals make the precise delivery of the system clock edge an important design issue. In this paper we examine the primary sources of clock skew and jitter that degrade precise clock edge delivery.

2. Eric Blomberg: Hewlett-Packard Apollo
Glitches, Intermittents and Noise Problems ... The Art of Noise-Budgeting
What are the major causes of intermittent failure in digital designs? What is the origin of these effects and what can be done to minimize them? We discuss these issues and more, including tips on building-in reliability through noise budgeting. Case studies are used throughout.

3. Henri Merkelo: University of Illinois
Advanced Methods for Noise Cancellation in System Packaging
Digital signals can be degraded by packaging effects such as reflection noise, crosstalk noise, and simultaneous switching noise. This paper analysis resistive and reactive matching, with design criteria developed based on the degree of desired compensation and noise suppression. Using case studies of vias, bends, and interposer contacts, we provide guidelines for reactive noise cancellation, and verification of designs using CAE simulation tools.

4. Michael L. Conn: Mikon Consulting
Printed Circuit Design Techniques for the Control of Electromagnetic Interference
Differential-mode (DM) and common-mode (CM) radiation interference are a major problem in the design of printed circuit boards (PCBs) intended for use in high-speed circuit designs. Using the comparative characteristic performance and performance of microstrip and stripline construction techniques, we present methods of predicting, avoiding, suppressing and containing radiated emissions created by modern high-speed circuits. We identify and discuss the roles of CAE design tools and test and measurement equipment.

5. Pat Byrne and Greg Walz: Hewlett-Packard R&D
Debugging and Characterising Ground Bounce Problems in High-Speed Memory System Hardware
When bus width, speed and physical densities are improved, new hardware failure mechanisms begin to plague a design. This paper describes a case study in debugging and characterising a multiple-bus memory system. We explain the physical mechanism of ground bounce and apply it to design techniques that improve the performance and operating reliability of high-speed memory bus designs.

6. Ken Smith: Cascade Microtech
Feasibility of Moving a 50MHz Design to Run at 100MHz
Using a 50-MHz, 486-cache as a design example, we address the problem of doubling the speed to 100 MHz. The process used involves measurement, modelling, and simulation techniques. Substrate measurements are used to show which transmission line models are appropriate. Using fine-pitch probing methods, we show how to verify critical signals against simulations.

Figure 2: *Presentations in the High Speed Digital Design track.*

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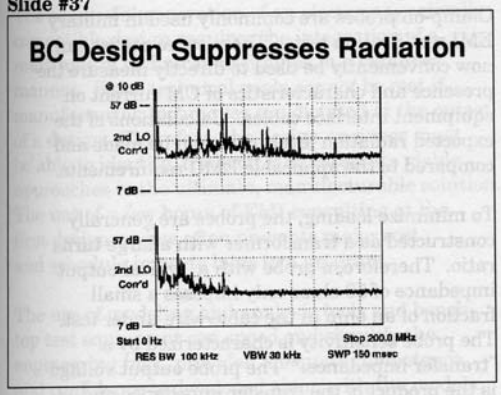
superior EMI performance is critical to the high-speed digital designer. The particular multi-layer PCB configuration shown above carries out those recommendations while adding 2 foil layers (assuming 2 sandwiches for the construction) whose cost is at least partially offset by the reduction in decoupling capacitors required in the final assembly.

For the Mikon-recommended construction, the sandwiches are located on the outside layers of the PCB and offer a *double shield* that should prove superior to a single layer shield of 2-ounce copper.

Slide #37

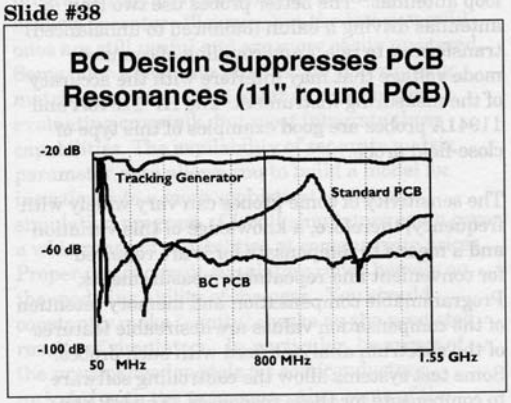


This "Before and After" example of a digital PCB design used in a line of computers is excerpted from the July 1991 issue of *Printed Circuit Design*. The boards used in the test were fabricated with dielectric and copper foils from the same lots, and tested in the same test setup. The standard 11-inch-by-14-inch PCB had 6 layers and the artwork for both boards was identical.

The board circuit contained multiple oscillators ranging from 14.745 MHz to 40 MHz, with the processor clocked at 20 MHz. The standard board was completely loaded and included 141 bypass capacitors. The BC board used only 4 capacitors; namely, two 0.1 µF and two 0.01 µF. Even though low inductance connections were used for the 4 capacitors, their effect was minimal above 30 MHz. The response recorded was located approximately 4 inches from the capacitors; however, the results indicated were reported to be virtually identical to that found at all points on the PCB. Additional capacitors were reported to further reduce the emissions in the 10 MHz to 20 MHz range.

The BC manufacturing process used in the PCB of this example used a dielectric thickness of 2 ± 0.5 mils. Today the process is achieving thicknesses of 2.0 ± 0.25 mils.

Slide #38



This slide provides a good example of resonance effects that occur on standard PCBs versus the same configuration of PCB using buried capacitance.

HEWLETT PACKARD

Figure 3: *Page 21 of Michael Conn's paper describing the benefits of the 2-mil laminates.*

Each paper presentation was an hour-long session, and the day concluded with demonstrations by the presenters in the spacious hallway. I remember among others Michael Williams demonstrating the clock jitter and skew with his custom-built circuit, the demonstration with fine-pitch probes measuring the signals on a multi-chip module (it is also shown on the front page in Figure 1), the close-field probe measurements of PCB radiation by Michael Conn and Henri Merkelo demonstrating the compensation options of via discontinuities. The big news in those days: Is it possible to run a system at 100 MHz clock speed that was designed for 50 MHz.? Most papers focused on signal integrity, though in those years even the term signal integrity was not widely used yet. Power integrity had no dedicated paper at this conference, but if we read the papers carefully, we can find several related topics, which later became important pieces of power integrity. For instance, Michael Conn's paper, Printed Circuit Design Techniques for the Control of Electromagnetic Interference, devoted three pages and five slides to the Buried Capacitance concept from Zycon Corporation. The third of these pages is reproduced in Figure 3. In case you are interested in reading the full paper but can not find it, read on: it will become available.

When I tried to locate proceedings of this conference from earlier years, I came up empty. Unfortunately these conference proceedings did not have an ISBN number, and to confuse things further, there were also other events with similar names. Based on the proceedings I have from 1993, I tried to find at least some of those papers on line. It turns out that there are a few websites dedicated to preserving the technical history of Hewlett Packard, one of them is [2], maintained by Glenn Robb, which under the HP Seminars header had one (and only one) scanned paper from the US version of this High Speed Digital Design Symposium. When I asked around among my friends and colleagues, who had more direct information about the early years of this conference series, Karl Kachigan from Agilent offered a brief summary from first-hand experience. Karl was one of the team that created Design SuperCon, and offered his perspective.

Karl wrote in an e-mail:
"A group in the Americas created the first High Speed Digital Seminar in 1989. It was given in the HP Santa Clara office by HP marketing folks. For the next few years, 1990-2, that seminar evolved using some consultants to create and deliver some presentations, and was delivered at several cities in the US. In 1993, we again ran the seminar tour and first did one in Europe. In 1994, seminar tours focused on ATM/Broadband and Communications. To simplify equipment setup, we created custom carts that could be wheeled into the hotels and back onto a big 18-wheel moving van. The carts stored the equipment beneath, and showcased it on top. There were custom back boards with signage. I remember having to wheel these things around.

At that point, it was getting difficult to coordinate the consultants, equipment, and travel to multiple cities. We had enlisted a moving company to get stuff from city to city, so just getting schedules setup was a challenge. We determined that it would be better to hold a symposium in one city over a few days instead of a seminar tour in 8 cities.

The concept of the HP Design SuperCon was to solicit paper topics from consultants, provide some funding to those that looked best, and have them create a paper and associated demo of HP gear (actually, we used this process for the seminar tours in 1990 and on). The demos were in another area in a trade show format with the movable carts. We aggregated topics into 3 or 4 tracks -- typically high speed design, system design, package design, and ASIC/IC design. In 1995, we held the first HP DesignSuperCon at the Santa Clara Marriott hotel. We had a big tent outside for registration, used a large room for the tradeshow, and several other rooms a bit of a walk away for the papers. Books were printed for each of the tracks. I have one from the system design track. I left many others with someone in EEsof when I left the group. The papers were never available in electronic form, not even pdfs, so if you found anything, it was likely a scan of the pages from the book. I found the 1995 call for papers, which provides some interesting insight into that first DesignSuperCon.

We branched out and held the event in the US and Japan for the next few years. We had easily outgrown the Marriott hotel and looked for another venue, which was the Santa Clara Convention Center. We started there in 1996, and targeting the last week of January for the show each year. In 1998, I think we dropped the "Super" from the name and it was then just called DesignCon.

In 2000, when the Internet bubble burst and HP had to cut expenses, we worked with the IEC for them to own the DesignCon show. They drove the key decisions, solicited people to join the technical review committee, and expanded it from an HP only event to an open event. HP/Agilent continued to be active in many aspects of the show and paid appropriate sponsor fees. I was involved with DesignCon again from 2003 to 2010 as the Agilent liaison. In 2003 we created an Executive Forum aimed at discussing the challenges managers experienced. In 2004, it evolved into a management track, which was quickly embraced by the EDA companies. In 2003, a DesignCon East was started in the Boston area, attempting to appeal to those on the East Coast. Unfortunately, it never had high attendance and last happened in 2005. In 2004, a Euro DesignCon appeared but the costs were high and I think it happened only once.

To this day, DesignCon has been fairly true to its roots -- papers created by experts to train others on leading edge topics with a tradeshow that is fairly tame compared with the big shows like DAC, MTT, etc."

In recent years DesignCon is managed by UBM and the DesignCon East events restarted a few years ago [4]. Unfortunately as Karl confirmed, there is little chance to find the conference proceedings in a public library, but thanks to websites like [2], scanned papers from these conferences will be made available if people who have their own copies of the conference proceedings are willing to scan it and send the files to Glenn Robb. In the coming weeks I am going to scan the proceedings from 1993; you can already read the first scanned item at [5].

If you are interested in the recent activities around DesignCon, you can follow the DesignCon Community website at [6].

References:

[1] www.designcon.com
[2] http://www.hparchive.com/
[3] http://www.hparchive.com/seminar_notes/HP_HighSpeedDigitalSystemsDesign-TestSymp1993_SONETCaseStudy.pdf
[4] http://signal-integrity.tm.agilent.com/2011/design-days-boston-features-designcon-east/
[5] http://www.hparchive.com/seminar_notes/Doubling-the-Clock-Speed-Feasibility_1993.pdf
[6] http://www.designconcommunity.com/