PCB Design 007 *QuietPower* columns, February 2010

PDN Measurements: Reducing Cable-Braid Loop Error

Istvan Novak

There are several reasons why PDN validation is more convenient in the frequency domain rather than in the time domain. We may cover those reasons later in a separate column. When it comes to simulating or measuring PDN components, modules or systems, we usually want to do it as a function of frequency. At low and mid frequencies, where the self-impedance of a DUT may reach milliohm values or even less, a fundamental challenge in measurement is the connection to the Device Under Test (DUT). Unless we measure a single component in a well-constructed fixture, the home-made connections from the instrument to the DUT will introduce too much error. The top scheme of *Figure 1* shows a Vector Network Analyzer (VNA) connecting to the (DUT) with a cable. Our DUT (for instance a DC-DC converter or a populated board) typically do not have connectors and therefore we need to have a short piece of wire (possibly the center wire of the coax cable or connector) to attach to the DUT. However, just 40 milli-inches (1 millimeter) of wire outside of the calibration loop may result in an error as much as 1 milliohm resistance and 1 nH inductance. The solution is to use the AC equivalent of the DC four-wire Kelvin measurement approach, shown on the bottom scheme of *Figure 1*.

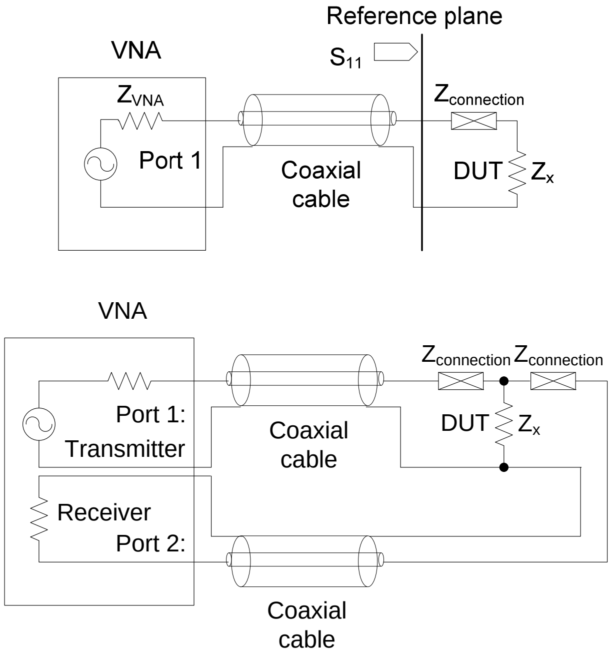


Figure 1: *Illustration of connection error with a single connection to the DUT (on the top), and block schematics of the Two-port Shunt-through measurement (on the bottom).*

The Two-port Shunt-through connection works well for very small impedances. The DUT impedance can be resolved from the measured S_{21} parameter as follows:

$$Z_{DUT} = \frac{Z_{VNA}}{2} \frac{S_{21}}{1 - S_{21}} \qquad (1)$$

where Z_{DUT} is the unknown complex impedance to be measured, Z_{VNA} is the reference impedance of VNA (usually 50 Ohm) and S_{21} is the measured complex response by the VNA.

The Two-port Shunt-through connection is a good fit for Vector Network Analyzers or Frequency Response Analyzers, which inherently have at least two ports, one being the source at any given time. However, by using two connections attached to the same DUT, now we just created a new problem: unless one or both ports are floating, the reference connections going to the two ports form a ground loop and we end up with a significant error floor. This is explained in *Figure 2*. We assume very low frequencies (or DC), so that we need to consider only resistances and ignore inductance. The test current flowing through the DUT (for sake of simplicity, it is represented by a Short) creates a V_e voltage drop across the parallel equivalent of the two cable-braid resistances: R_{b1} x R_{b2}. Therefore, instead of the expected zero value, the reading at Port 2 will be this V_e voltage, which represents the R_{b1} x R_{b2} resistance.

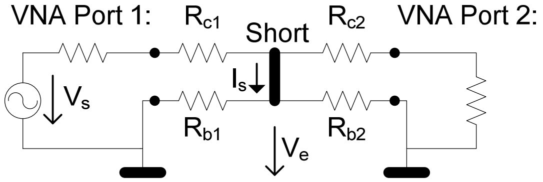


Figure 2: *Illustration of cable-braid loop error.*

This cable-braid error floor gradually diminishes as the inductive reactance of the cable opens up the loop. By the time we get up into the MHz frequency range, this error usually diminishes. At low frequencies, until recently we had to use an external floating-input differential amplifier or had to artificially increase the common-mode inductance of the cable by adding ferrite beads or threading the cable through a ferrite toroid.

The Agilent E5061B LF-RF network analyzer takes a different approach by using semi-floating references for its Gain-Phase port inputs [1]. The equivalent low-frequency impedance is approximately 30 Ohms and this reduces the cable-braid loop's error dramatically. The concept is illustrated in *Figure 3*, and its results are shown in *Figure 4*.

Assuming that the Z_{DUT} impedance is much lower than 50 Ohms, the Va error voltage, created by the test current flowing through the cable-braid impedances, is similar in magnitude to Ve in *Figure 2*. However, the received V_T voltage will contain only a very tiny attenuated portion of this error voltage, V_{b2}.

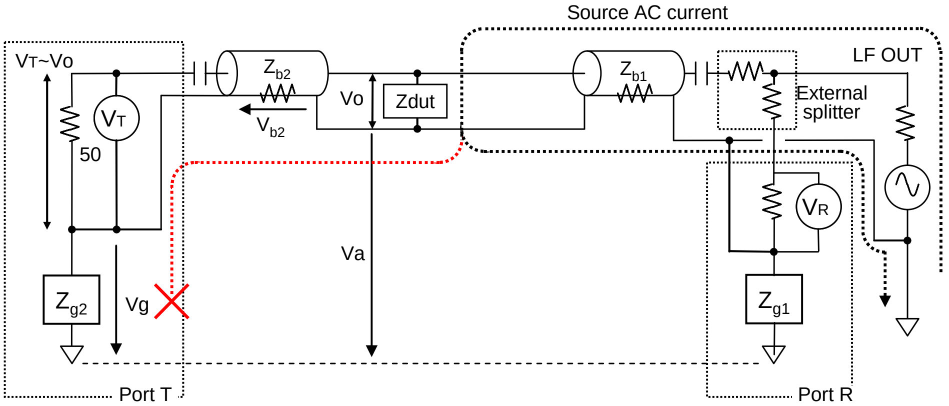
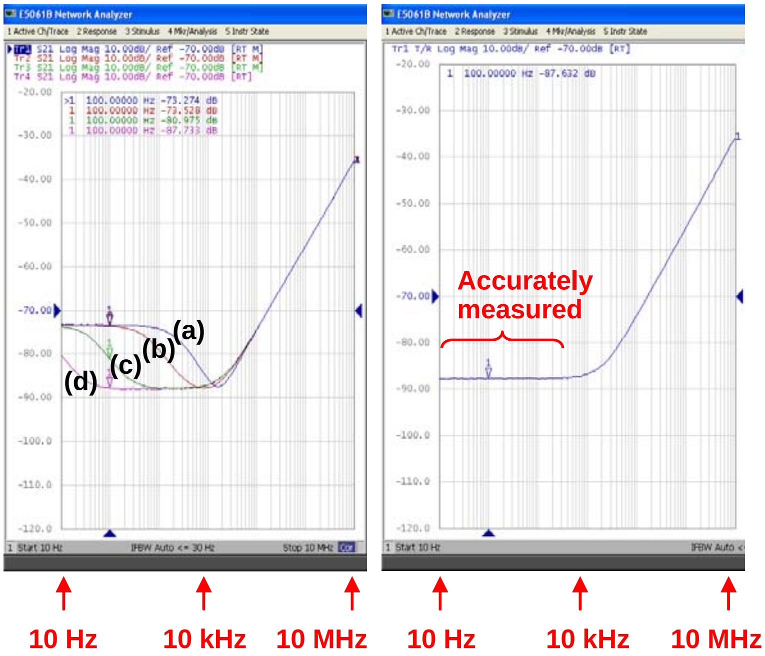


Figure 3: *Concept of semi-floating ground in the Gain-Phase test port of E5061B. Courtesy of Agilent Technologies.*

From the Va = Vg + V_{b2} vector triangle we can calculate the actual V_{b2} error voltage as

$$V_{b2} = V_a \frac{Z_{b2}}{Z_{g2} + Z_{b2}} \tag{2}$$

Since $Z_{g2} >> Z_{b2}$, the voltage at the T input will be very close to the correct value: $V_T \sim Vo$. For instance, assuming 30 milliohm braid resistance, the 30 Ohm semi-floating ground impedance will reduce this error to 30 microOhm.



```
Tr1 S21 Log Mag 10.00dB/ Ref -70.00dB [RT M]
Tr2 S21 Log Mag 10.00dB/ Ref -70.00dB [RT M]
Tr3 S21 Log Mag 10.00dB/ Ref -70.00dB [RT M]
Tr4 S21 Log Mag 10.00dB/ Ref -70.00dB [RT]
>1  100.00000 Hz -73.274 dB
 1  100.00000 Hz -73.528 dB
 1  100.00000 Hz -80.975 dB
 1  100.00000 Hz -87.733 dB
1 Start 10 Hz          IFBW Auto <= 30 Hz          Stop 10 MHz Cor
```

```
Tr1 T/R Log Mag 10.00dB/ Ref -70.00dB [RT]
1  100.00000 Hz -87.632 dB
1 Start 10 Hz          IFBW Auto <
```

Figure 4: *Illustration of effectiveness of semi-floating ground. Courtesy of Agilent Technologies.*

Figure 4 was measured using a home-made reference piece that has one miliOhm DC resistance with some series inductance. The left four traces are measurement results with a conventional grounded receiver. (a) represents the measurement result without attaching anything to the cables, which indicates the measurement error due to the cable braid loop in the low frequency range. The other three traces (b) to (d) show the measurement results by adding an increasing number of ferrite cores to the test cable. The error is reduced by adding inductance, but the result is still not perfect. On the other hand, the right plot shows the low-frequency reading with the semi-floating ground in the E5061B VNA, which is flat at the correct value. This shows the ability of the Agilent E5061B VNA to accurately measure milliohm impedances. More details can be found in [2] about PDN measurements and in [3] about the measurements with E5061B.

[1] http://cp.literature.agilent.com/litweb/pdf/5990-4391EN.pdf
[2] Frequency-Domain Characterization of Power Distribution Networks, Artech House, 2007.
[3] Accuracy Improvements of PDN Impedance Measurements in the Low to Middle Frequency Range, DesignCon 2010, February 1-4, 2010, Santa Clara, CA. Available online at www.electrical-integrity.com