PCB Design 007 *QuietPower* columns

Avoid Overload in Gain-Phase Measurements

Istvan Novak, Oracle, May 2015

Today most of our printed circuit boards have at least a few, some many, DC-DC converters. We have a large choice when it comes to deciding what to use: we can design and build our own converter from discrete parts (called Voltage Regulator Down or VRD) or we can buy one of the off-the-shelf open-frame or fully encapsulated Voltage Regulator Modules (VRM). For low currents we can use linear regulators; for medium and high current we are better off using a switching-mode topology. Whatever circuit suits best our needs, chances are that we want to keep the output voltage regulated against changes in input voltage and load current, which in turn calls for one or more internal control loops. There is a well-established theory to design stable control loops, but in case of power converters, we face a significant challenge: each application may require a different set of output capacitors coming with our loads. Since the regulation feedback loop is directly across our bypass capacitors (shown as a single Cout in *Figure 1*), our application-dependent set of capacitors now become part of the control feedback loop. Certain combination of output capacitors may cause the converter to self-oscillate, something we want to avoid. This raises the need to test, measure and/or simulate the control-loop stability.

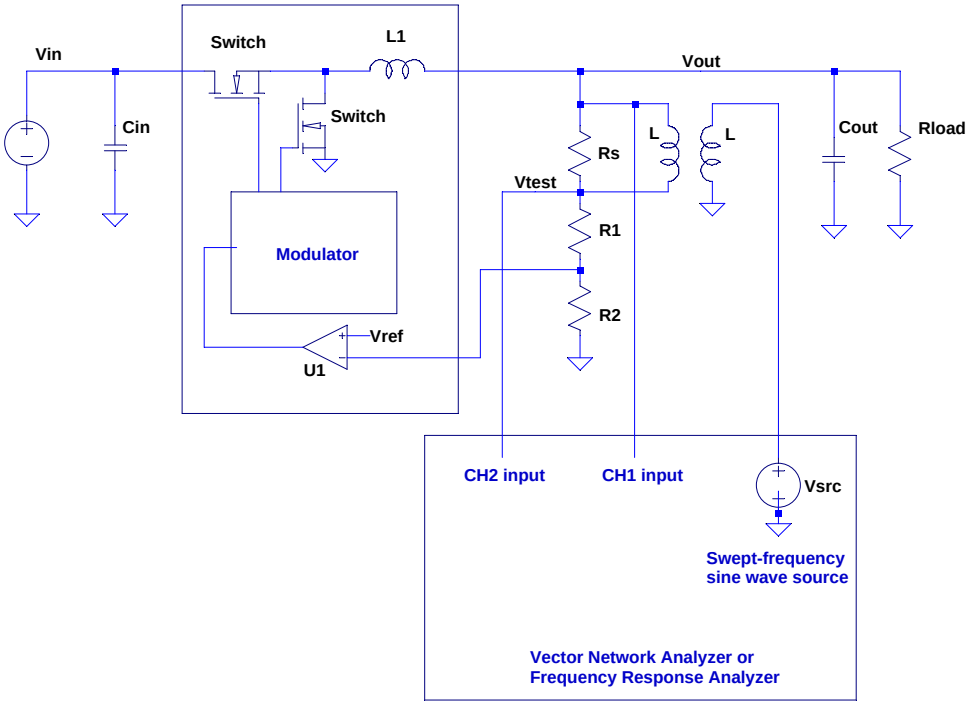

Figure 1.: *Block diagram of DC-DC converter and Gain-Phase test setup.*

Figure 1 shows the block diagram of a switching-mode step-down DC-DC converter (also commonly called as buck converter) together with the usual connections and setup for measuring the loop stability. This is also called the Gain-Phase measurement, because we are mostly interested in the phase of the loop gain at a frequency where the gain magnitude drops to unity. This phase value is also called the *phase margin*. A typical measured data set is shown in *Figure 2*, where the labels identify the *phase margin*.

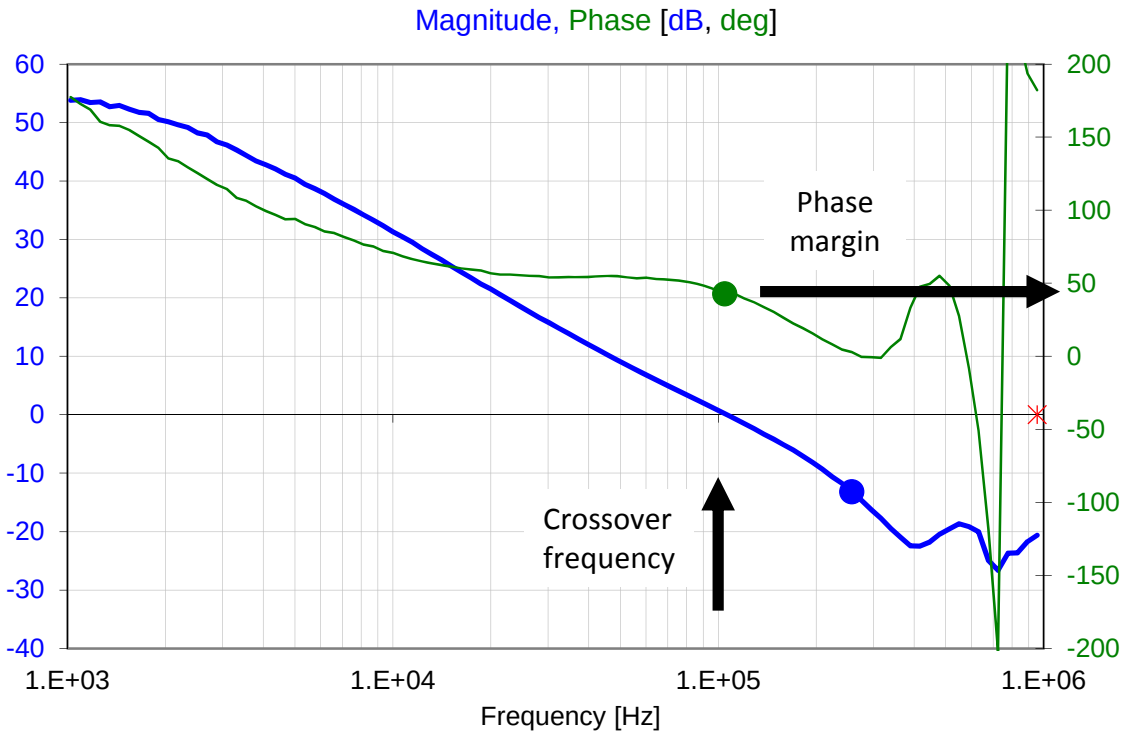

Figure 2.: *Typical Gain-Phase plot with the phase margin identified.*

The heavy blue line on the chart goes with the left vertical axis and it shows the loop gain magnitude in dB. The gain magnitude reaches unity (zero dB) at slightly above 100 kHz. There is a large dot at this frequency on the thin green phase curve, which indicates the crossover frequency on the horizontal axis and the phase margin on the right vertical axis. The phase margin in this case is around 45 degree, which is usually considered as sufficient margin.

To measure the phase margin, we need to inject a test signal into the control loop. A suitable location is the top of the feedback voltage divider, where the top side of the opening faces the converter output, which is low impedance, whereas the low side of the opening faces the voltage divider resistors, which is usually in the hundreds of ohms range or higher. Inserting the test signal in series at such a location guarantees the lowest possible alteration of loop characteristics by the measurement. Since the injection point is at the DC output voltage, we need an isolation transformer as shown in *Figure 1*. By

measuring the complex ratio of the voltages at the two sides of the injection transformer, we measure the loop gain. There are dedicated instruments for this purpose, called Frequency Response Analyzers.

There is one remaining challenge though, which leads us to the title of this article: unless the converter is our design, we may not know exactly what is along the control loop. As you can see on the chart, the loop gain can vary orders of magnitudes as frequency changes. If we are not careful and use too high test signal level, we can easily overload the control loop, which will create invalid results. If, on the other hand, we preemptively try to select a very low injected test signal level, our test data will be buried under noise. How can we maintain the proper injected level to be above the noise floor, yet avoid control-loop saturation, is shown in one of the live demonstrations at the power integrity training courses [2]. It will also be described in one of the upcoming *QuietPower* columns.

References

[1] "Dynamic Characterization of DC-DC Converters," DesignCon 2012, Santa Clara, CA, January 30 - February 2, 2012. Available at http://www.electrical-integrity.com/Paper_download_files/DC12_11-MP2.pdf

[2] Practical Power Distribution Design, Simulations and Measurements. Two-day training course, June 29-30, 2015, University of Oxford, Oxford, UK.