QuietPower column

DesignCon: Personal Reflections on the Past Twenty Years

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DesignCon has been a tremendous source of information for myself and for the team I have been working with at SUN Microsystems, which later became part of Oracle Corporation. This summary is an attempt to capture some of the most influential papers from the past twenty years that made the biggest impact on our work. This compilation is necessarily subjective and vastly incomplete. DesignCon had an enormous number of great presentations and there is no way anyone could create a fair list. What amounts to the 'best' for someone, depends on what we are looking for at any given moment, what is our experience level in the different subject matters and on our own preferences to different styles. Nevertheless this is my very subjective list of gems from DesignCon's past twenty years. One author from each selected paper was contacted and the same question was asked: "If you had to name one DesignCon publication that made the biggest impact on your work, which paper would you name?" The favorites of those authors are also listed here. I also found many of the comments and notes that came with the answers very interesting and telling; some of them are included below with permission. I am hoping that those answers diversify my subjective view and give a broader perspective.

DesignCon is a conference in Santa Clara, California, late January or early February each year, attracting signal and power integrity practitioners from around the globe [1]. People who started to attend this conference in recent years, may not know that –even though DesignCon's history is not as long as some other professional conferences, such as the ones sponsored by IEEE- DesignCon started (under various different names) in the early part of the nineties [2]. I feel very lucky that every year since the late nineties I have had a chance to be part of DesignCon in various capacities: as author and presenter, as panel, TecForum, tutorial and track organizer, as well as during the past sixteen years, as member of the Technical Program Committee.

DesignCon started to hand out the conference proceedings on CD-ROM in year 2000. Earlier proceedings were prints only. From my notes and from the 1999 printed conference proceedings, my favorite was a paper by Dr. Ed Sayre and his co-workers [3]. This paper summarized very nicely the frequency dependent losses, transmission-line attenuation, conductive and dielectric loss crossover frequency and eye diagram fundamentals. *Figure 1* shows page 33 of the proceedings, where attenuation contributors are listed. This great forward-looking summary appeared at a time when causal and frequency dependent models have not been widely and routinely used yet in high-speed interconnect simulations.

The Simulation of Transmission Lines with Dielectric Loss and Conductor Losses

All transmission lines have two lossy elements: series resistive and shunt dielectric losses. Both series resistance and shunt dielectric losses have both a DC loss term and frequency related (AC) losses. The resistive AC skin effect loss is well known to be proportional to :

$$R_{skin} \propto \sqrt{f}$$

The AC dielectric loss will be analyzed in this section. In the high frequency range, the AC dielectric loss will dominate the loss factor and DC dielectric losses can generally be ignored .

Consider a capacitor C, with dielectric losses represented by the shunt conductance G_c. The admittance of this parallel pair is

$$Y(j\omega) = j\omega C + G_c = j\omega\left[C - j\frac{G_c}{\omega}\right] \qquad (1)$$

A lossy capacitor can thus be introduced to any lossless frequency analyses by the substitution

$$C \rightarrow C - j\frac{G_c}{\omega} \qquad (2)$$

The properties of dielectric materials are represented in terms of permittivity and the dielectric loss factor. These are defined in terms of the complex permittivity ε_c,

$$\varepsilon_c = \varepsilon_0(\varepsilon' - j\varepsilon'') \qquad (3)$$

where ε' is the dielectric constant, often refered to as ε_r and the ε'' is the loss factor.

For homogenius materials, equations 2 and 3 lead to the following relation:

$$G_c = \frac{\varepsilon''}{\varepsilon_r} \bullet \omega C \qquad (4)$$

where: ω is the angular frequency. The ratio

$$\tan\delta \approx \delta = \frac{\varepsilon''}{\varepsilon_r} \qquad (5)$$

is defined as loss tangent.

For most materials, the loss tangent is very small and can be well approximated by the radian angle. Then, use of equations 4 and 5 provides the relationship between the losses, the capacitance, and the conductance:

$$G_c = \delta\omega C \qquad (6)$$

For most PCB dielectric materials, δ is given at a specific frequency. If we assume δ is approximately a constant, then the shunt conductance G_c is defined as

$$G_c \equiv G_0 + G_d f \qquad (7)$$

Where G_0 is the DC shunt conductance, f is frequency and G_d is the dielectric loss per unit frequency. This is the model assumed in the Avanti .W lossy line model.

Based on the polymer nature of PCB resins, we can reasonably assume $G_0 \approx 0$ over normal temperature operating ranges, then,

$$G_d = 2\pi\delta C \qquad (8)$$

When the lossy capacitor model is extended to include PCB transmission lines, the conductance and capacitance in Eq. (8) are expressed in per unit length values.

The conductance can then be found directly: δ is given by the vendor and C is computed from any lossless PCB electromagnetic field solver.

Transmission Line Attenuation

The transmission line attenuation can be derived from the theory of transmission lines with small losses and is given by:

$$\frac{Attenuation}{Per\ Unit\ Length}(dB) = 4.35\left[GZ_0 + \frac{R}{Z_0}\right] \qquad (9)$$

where: Z_0 is transmission line impedance, R is the transmission line resistance including the skin effect loss and G is given by (8) above. The series resistive loss R is given by

$$R = R_0 + R_s\sqrt{f} \qquad (10)$$

where: R_0 is the transmission line DC loss, and R_s is a paramater related to the transmission skin effect loss.

***Figure 1**: Elements of frequency dependent losses in interconnect simulations [3].*

From year 2000, my favorite was the paper from Dr. Howard Johnson on multi-level signaling. The presentation was not included in the conference CD, but you can find it on line on Dr. Johnson's webpage [4].

In the paper I loved the most the figure that summarizes the Multi-Amplitude Signaling (MAS) concept and very eloquently tells us when it makes sense to consider using multi-level signaling. The figure is reproduced below in *Figure 2*.

IF your circuits could go as fast as you wanted, and
IF complexity were free, and
IF your SNR slope is at least -40 dB/decade or worse,
THEN try multi-level signaling, where
B = number of informational bits carried per baud
f/B = new signaling rate (where f is the old rate)
$N = 2^B$ number of levels
$1/(N-1) = 1/(2^B-1)$ = reduction in spacing between levels
(simplistic model – things may not be this bad)

***Figure 2**: Multi-Amplitude Signaling (MAS) concept from [4]. What you GAIN by reduction in baud rate (log(B)*[SNR slope]) exceeds what you LOSE by reduced level spacing $20*\log(2^B-1)$*

Dr. Johnson's favorite was one of Ed Sayre's paper, and he wrote:

> *"Regarding your question, I can't find a date or reference for this paper, but at some point between 1993 (when my first book was published) and 1995 (when I became heavily involved in Ethernet standards) I saw a presentation by Ed Sayre, I believe it was at DesignCon, about dielectric absorption in long transmission media. Ed explained how dielectric losses in a long cable, if measured in dB/meter, would increase in direct proportion to frequency. It was just one slide in a long presentation. That was my first introduction to the topic of dielectric loss. Realizing its importance, and projecting forward to the speeds that I envisioned we would ultimately reach, I was inspired to study the matter quite thoroughly. The results of my study heavily influenced the signal modelling for Ethernet at both 100 and 1000 Mbps, and the standards for category 5e and category 6 cabling, both widely used today. I was by no means the first to understand these effects, nor was Ed. There were people working for data cabling manufacturers who had been studying dielectric loss for decades, as it was vital to the performance of radar and other microwave techniques, but I do think that Ethernet was the first computer networking standard to embody, at least in the committee work, a comprehensive time-domain model that fully incorporated resistive loss, skin-effect loss, and dielectric losses. Such modelling is now commonplace for many high-speed printed circuit board connections."*

This was a reoccurring theme in many of the e-mail exchanges: most of us considers a presentation or paper memorable if it either spurs new ideas or sheds light on something that we have been battling with for some time without finding a solution.

From DesignCon 2002 my favorite article was from John Patrin and Mike Li: "Comparison and Correlation of Signal Integrity Measurement Techniques". This was the time when jitter became important to understand and to measure and this was the great paper from which I learned more about the dual-Dirac model, tail-fit algorithm and bath-tub curves.

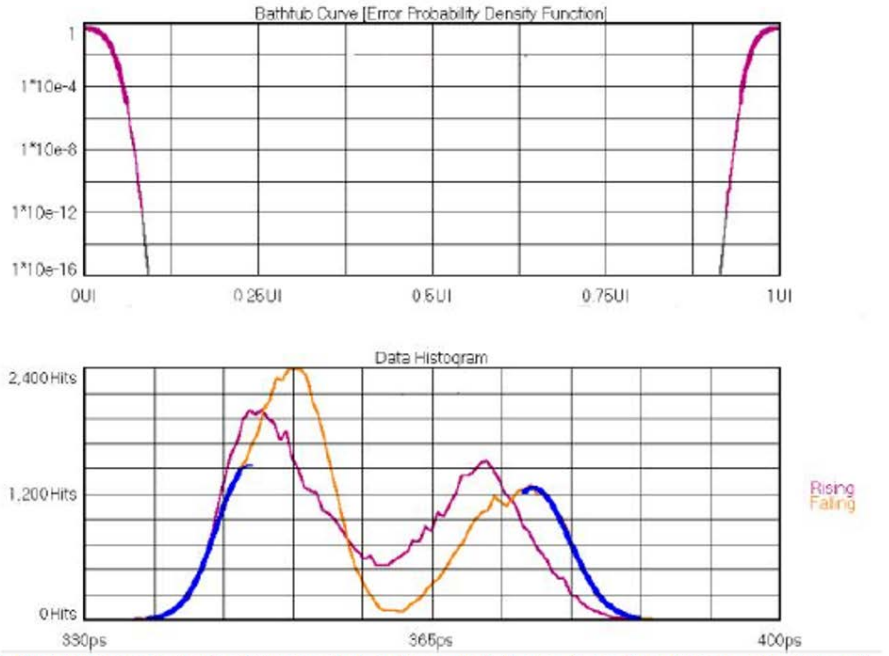

Figure 9. Typical data acquired with a TIA using clock-to-data method. Bottom figure shows histograms for rising and falling data edges. This view enables the user to determine the jitter contribution from the polarity of edges. The right and left most portion of the histograms are fitted with Gaussian tails in order to determine the 1σ for RJ, the difference between the means of the Gaussian distributions is the DJ value. The top figure shows the bathtub curve.

***Figure 3**: The bathtub curve and tail-fit illustration from [5].*

From DesignCon 2004 my absolute favorite was a presentation by John Grabenkemper from Hewlett Packard: "Modeling Noise on Printed Circuit Board Power Planes." You can find the paper on the conference CD [6], but the real jaw-dropping part was the animated wave propagation illustrations during the presentation. Back then the presentation slides were not distributed as part of the conference proceedings. The room on the second floor of the Santa Clara Convention Center was packed, there was not even standing room; I was peeking into the room through the open door above peoples' shoulders. The animations showed the propagation of an injected noise transient on a power-ground plane pair under various conditions. John graciously offered his original set of presentation files that I managed to reformat to a slide show that plays properly in today's PowerPoint. With John's permission, the file is now available [7]. If you look at the slides and animations (note: you have to click on the plots to start each of the

animations), you may say that with today's tools we probably could get more accurate or even different results. Nevertheless this groundbreaking presentation drew the attention to some of the non-trivial and very counter-intuitive phenomena about power distribution design. It showed that noise pulses can easily propagate past beyond the barrier of a row of bypass capacitors and that low-ESR capacitors may actually result in bigger overall noise. *Figure 4* is a static screen capture of the animated noise pulse, comparing 4-mil laminates (green trace) and 2-mil laminates (red trace).

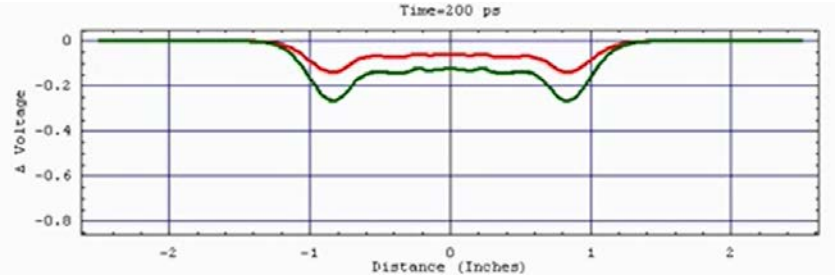

Figure 4: *Screen capture of animated power-ground plane noise from [6]. Slides with embedded animated waveforms are available at [7].*

From 2005 one of my favorite papers was the Eye Patterns in Scopes paper by Peter J. Pupalaikis and Eric Yudin from LeCroy [8]. This paper appeared at a time when different oscilloscope vendors were engaged in a fierce bandwidth race to catch up with the exploding data rates of SerDes signaling. The major message of the very well-illustrated paper was that the absolute bandwidth number gives us little guidance when for signal integrity we have to look at very fine details of complex high-speed waveforms: group delay and overall time-domain response shape are more important.

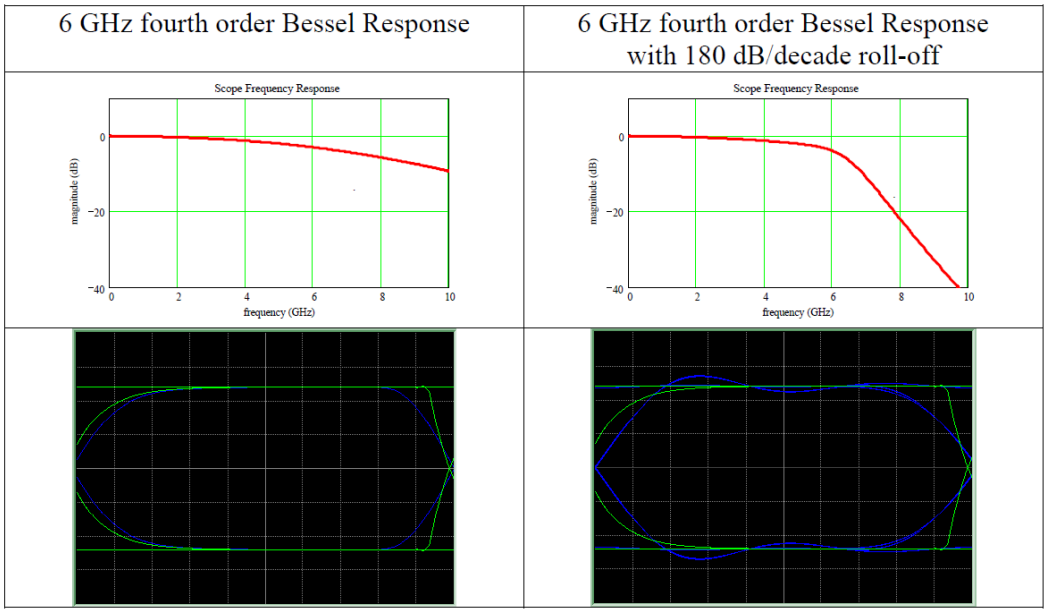

Figure 5*: Comparison of eye patterns with different front-end response shapes [8].*

For years, there was a free little utility illustration software available on the LeCroy website, which allowed the user to visualize the time and frequency-domain behavior of different bandwidth oscilloscopes over a range of data rates and with user-adjustable roll-off and group delays of the anti-aliasing filter. With permission, the illustration tool is now posted at [9].

Peter's pick was the series of presentations that the late Dima Smolyansky did on TDR measurements and modeling, for instance his DesignCon 2000 paper "High-Speed Digital Interconnect Modeling from TDR Measurements". Among others, Peter said:

> *"…when I first saw those and what could be done with TDR, I was totally amazed - like a kid at a magic show. And I guess a lot of the stuff he showed, I've expanded quite a bit on over the years. Too bad he's not with us anymore."*

2006 was an exceptional year of great papers, at least as far as my own learning was concerned. I simply could not distill it down to a single paper; there was a tie between two. Both papers were about vias. One paper was presented by Bruce Archambeault from IBM [10]: "Full Wave Simulation and Validation of a Simple Via Structure". This paper showed the non-trivial detail that above 10 GHz the entry/exit angle of traces connecting to a via can make a big difference in the overall transfer function. *Figure 6* is the reproduction of a very telling figure from the paper.

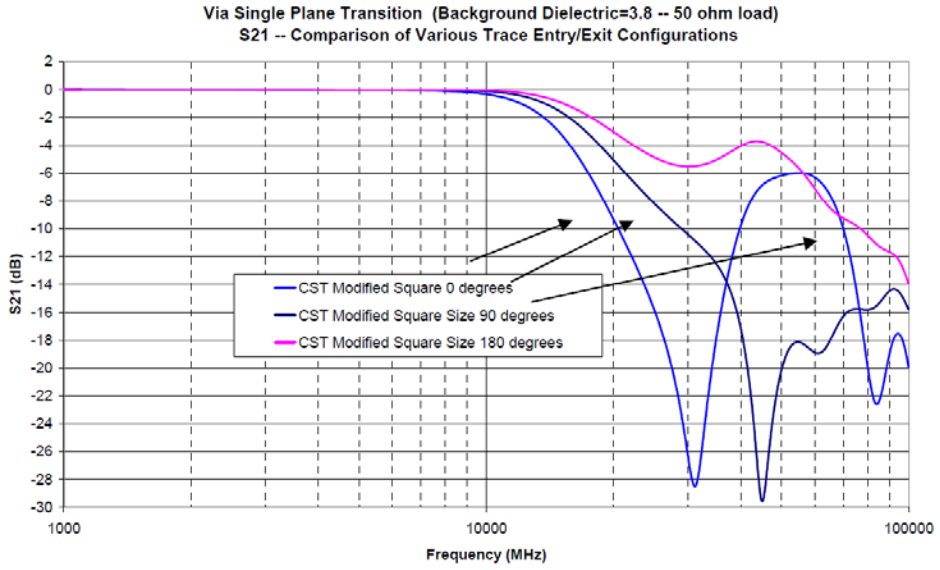

Figure 6: *Comparison of various angle of entry/exit to via (copy of Figure 4 from [10].)*

My other favorite from 2006 was presented by Christian Schuster, also with IBM at that time: Developing a "Physical Model for Vias [11]. The reason why this paper is very memorable for me because it finally gave a very simple and elegant answer to a question that I remember we tried to figure out for years. Since the late 90s at every conference I

attended this topic came up among experts and we brainstormed and tried to get a solution to the question: how do we take the PCB structure into account in the return current model of the via. This paper finally gave us a straightforward solution!

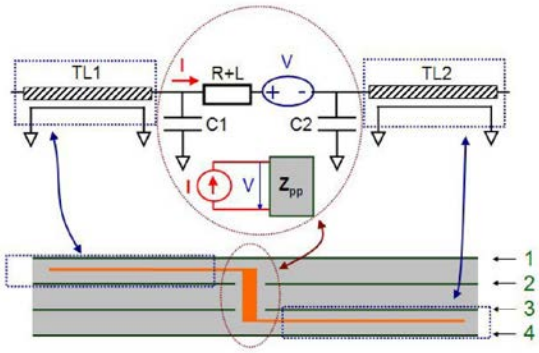

Figure 7: *Relating equivalent circuit elements to geometrical features. (copy of Figure 11 from [11]).*

Christian's favorite pick was a paper from DesignCon 2005 presented by Ravi Kollipara, Rambus (and co-authored by Ben Chia, Qi Lin, Jared Zerbe) "Impact of Manufacturing Parametric Variations on Backplane System Performance." Christian said:

> *"The study is very well done and Ravi is/was a very good presenter….*
> *In hindsight I think this study was ahead of its time."*

At DesignCon 2008 my favorite was "Analyzing the Impact of Simultaneous Switching Noise on System Margin in Gigabit Single-Ended Memory Systems" by the RAMBUS team of Ralf Schmitt, Joong-Ho Kim, Woopong Kim, Dan Oh, June Feng and Chuck Yuan. This was an excellent overview of SI-PI co-simulation, and it illustrated very nicely how the SI noise margin gets degraded by PI noise.

Ralf's favorite pick from the DesignCon papers was [13] and this is how he explained why:

> *"This particular paper was published during the time when we were developing our own PDN modeling methodology, and it came just in time for us to test new modeling approaches and verify them with actual measurements on test and product boards. Getting good correlation of very low impedances over a broad frequency range was a serious challenge. On the other hand, modeling without the verification through correlation to actual physical implementation was not trustworthy enough to use it for crucial design decisions. Following the methods described in this paper we pushed down the noise floor of our correlation measurements significantly, giving us reliable and reproducible results for our PDN implementations and invaluable confidence in our modeling methodology."*

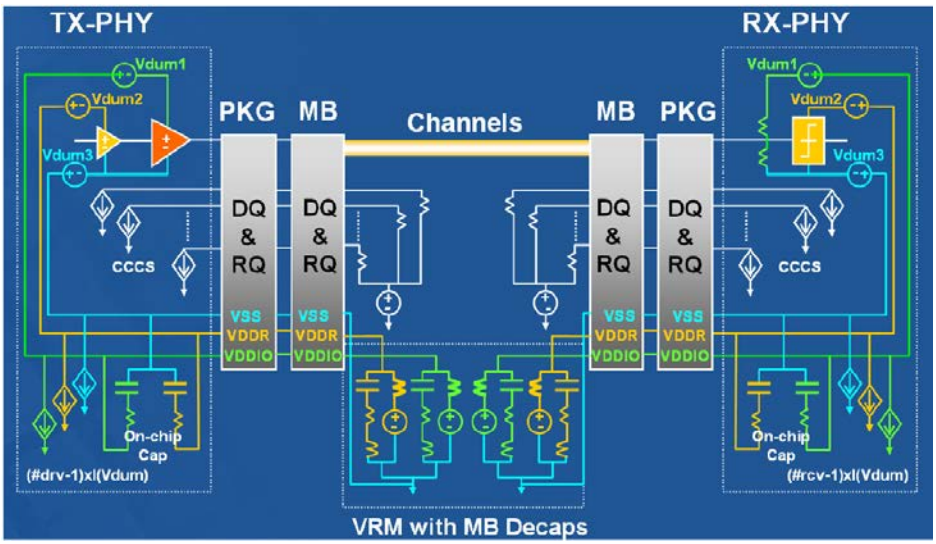

***Figure 8**: Schematics of SI/PI Co-Simulation Model (copy of Figure 2 from [12]).*

From DesignCon 2010 a real eye-opener for me was the Generalized Modal S-parameter presentation from Yuriy Shlepnev, Simberian, and the TeraSpeed team [14]. This paper came along when many of us in the industry were busy characterizing low-loss high-speed laminates. This presentation offered a unified view and a complete theory-to-validation process for laminate characterization. *Figure 9* summarizes the model identification.

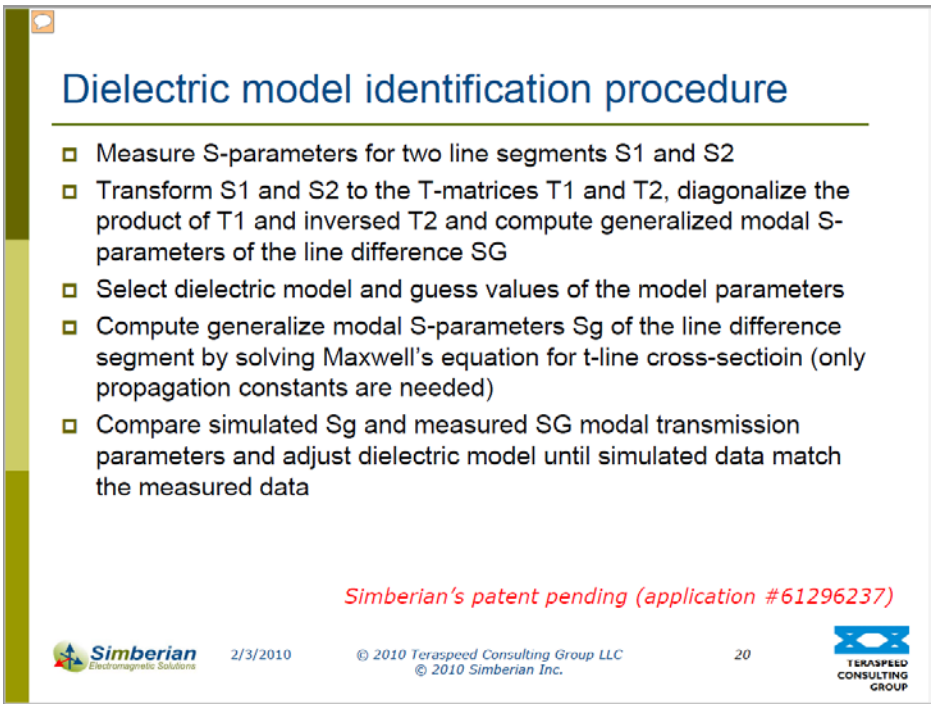

***Figure 9:** Dielectric model identification procedure. Copy of Slide 18 from [14]*

About DesignCon papers that shaped his view and influenced his work, this is what Yuriy said:

> *Here is the list of some DesignCon papers that I carefully studied and revisit from time to time (in chronological order, cannot select just one):*
>
> - *S. McMorrow, C. Heard, The Impact of PCB Laminate Weave on the Electrical Performance of Differential Signaling at Multi-Gigabit Data Rates, DesignCon 2005.*
> - *G. Blando, J. R. Miller, I. Novak, Losses induced by asymmetry in differential transmission lines, DesignCon 2007*
> - *J. R. Miller, G. J. Blando, I. Novak, Additional Trace Losses due to Glass-Weave Periodic Loading, DesignCon 2010*
> - *L. Ritchey, J. Zasio, R. Pangier, G. Partida, High speed signal path losses as related to PCB laminate type and copper roughness, DesignCon 2013.*

From DesignCon 2011, a real gem for me was the presentation by Eric Bogatin and Mike Resso on automatic fixture removal [15]. The presentation guided the audience through the theory and implementation with a series of simulated and measured examples. *Figure 10* summarizes some of the practical considerations to keep in mind.

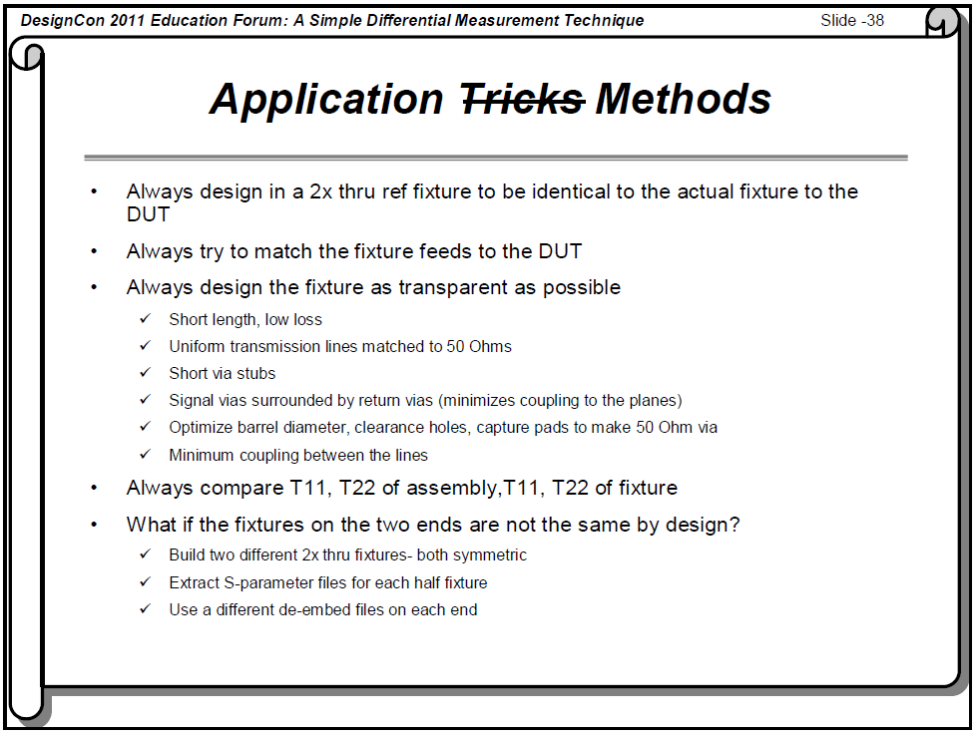

Figure 10: *Practical considerations for the automatic fixture removal, copy of slide 38 from [15].*

Eric and Mike mentioned the following two papers:

- Measuring MilliOhms and PicoHenrys in Power- Distribution Networks, [13]
- Bypass Capacitor Selection Based on Time Domain and Frequency Domain Performances, SUN Microsystems presentation in TF-MP3 "Comparison of Power Distribution Network Design Methods" at DesignCon 2006

Eric said:

> *"The first is the one in around 2001 on low impedance 2-port methods. I learned this technique from you and have been applying it for the last 17 years. The second panel that had an impact was the one on which approach to use for capacitor selection: the big V, the multipole or the FDTIM. I think this might have been around 2005 or 2006. This panel discussion got me thinking about what's really important in the PDN and how important the impedance profile of not just the capacitors on the board is, but how it fits with the rest of the PDN ecology. It had the biggest impact on changing my way of thinking about PDN- that its about the system, not just the components."*

From DesignCon 2014 the presentation that had the biggest impact on me was "De-Mystifying the 28 Gb/s PCB Channel: Design to Measurement", by Jack Carrel, Heidi Barnes, Robert Sleigh, Hoss Hakimi and Mike Resso [16].

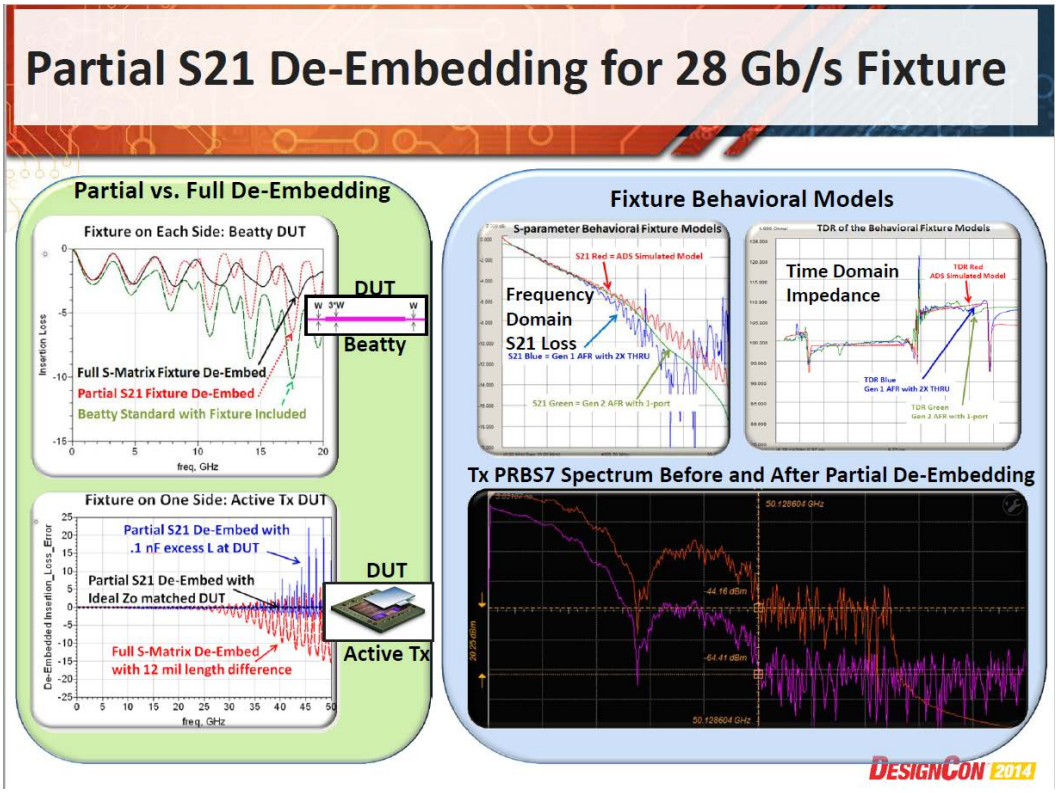

***Figure 11**: Explaining the differences and risks between partial and full de-embedding. Copy of Slide 17 from [16].*

This paper had a very wide scope from various aspects of the design flow to nuances of validation. In fact it was a test-related slide (*Figure 11*) that had the biggest impact on my way of thinking. It explains and illustrates that while full de-embedding (using both reflection and transmission terms) has the potential of giving us more accurate results by eliminating reflection-related errors as well, it also carries the risk of actually making the end-result much worse if there are slight shifts in the reference planes during the process. The take-away for me was that in general, partial de-embedding (using only transmission terms) is a more robust process.

This is what Heidi said about her favorite DesignCon paper(s):

> *"As for which paper made the biggest impact... I would probably say the first one on ATE loadboard design and the inspiration that I have gotten from working with Jose Moreira over the past 12 years to co-author so many papers with him. It was the first paper Jose and I did together for DesignCon which also set a precedence for always trying to co-author with more than one company on the paper. Jose is also the inspiration behind the Non-Destructive Analysis paper this year, and it is very rewarding to see how the Plug-n-Play fixtures are bringing educational as well as technical value to the process of fixture removal."*

From DesignCon 2016 my favorite presentation was "Killing the Bode Plot" by Steve Sandler. Though we may not agree on all of the details, this excellent and thought-provoking paper drew the attention to the various stability metrics of voltage regulators and inspired multiple follow-up studies in our team. *Figure 12* shows some of the arguments and points Steve made.

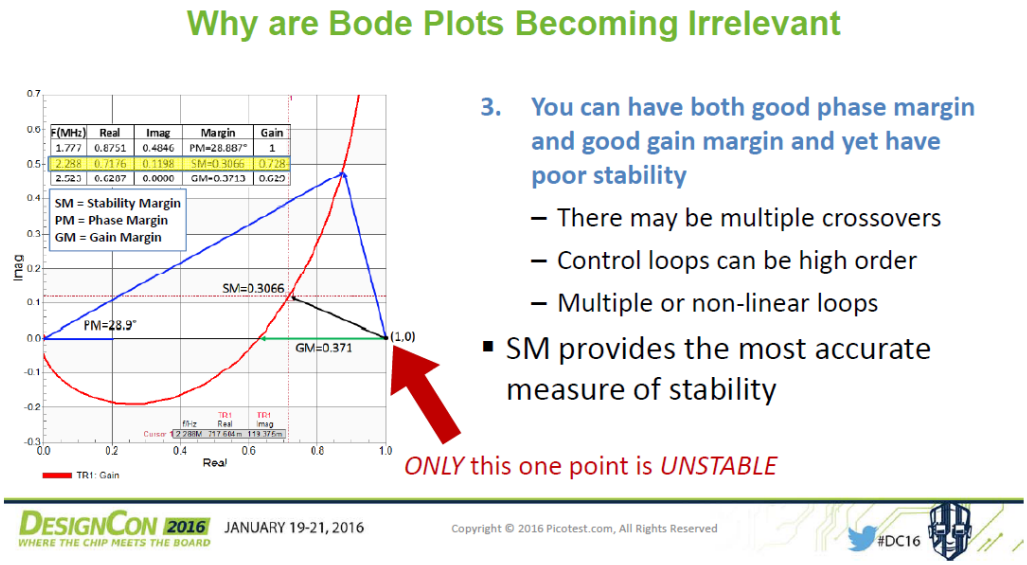

Figure 12: *Reasoning why bode plots become irrelevant. Copy of Slide 10 from [17].*

Steve's choice was also the SUN Microsystems presentation "Bypass Capacitor Selection Based on Time Domain and Frequency Domain Performances," in TecForum-MP3 "Comparison of Power Distribution Network Design Methods" from DesignCon 2006.

Among others, Steve said

> *"I have to pick this one, because I reference it very frequently. For me this was the clearest illustration of the flat impedance goal."*

As reviewers of conference tracks have a chance to see the full papers before the conference, I already made up my mind about a couple of papers that I am going to follow at DesignCon 2018 with particular attention:

- Jonathan L. Fasig, Christopher K. White, Barry K. Gilbert, Clifton R. Haider, "Introduction to Non-Invasive Current Estimation (NICE)," DesignCon 2018
- Larry D. Smith, Yi Cao, "A Convolution Technique for Verifying Acceptable PTPX Current Waveforms for PDN Voltage Droops," DesignCon 2018

Though this brings us to the present, by far this is not the end of the list of the excellent entertaining and educating papers that I liked over the past twenty years. A short list of my additional favorites are in the Appendix.

At the end I want to emphasize again that I understand that this list is very subjective. Also, in retrospect, all of these papers speak about something that feels very simple and obvious today, but was important, novel or groundbreaking at the time of their publication. You may see from the personal reflections shared here that sometimes years later we may not even remember the exact date or title of the paper; all what gets burnt into our memory is the idea that we understood a problem or found a solution. This could not happen without the great authors and presenters who come to DesignCon each year and share the result of their work, and the track and conference organizers who make this series of events possible. I am looking forward to learn new exciting things at DesignCon in the years ahead.

If you have your special favorite DesignCon presentation that you found very useful for your own work, share your story on the DesignCon community or SI Journal sites.

References:

[1] www.designcon.com

[2] http://www.electrical-integrity.com/Quietpower_files/QuietPower-25.pdf

[3] Dr. Edward P. Sayer, Dr. Jinhua Chen, Mr. Michael A. Baxter, "OC-48/2.5 Gbps Interconnect Engineering Design Rules," High-performance System Design Conference, January 1999, Santa Clara, CA.

[4] Dr. Howard Johnson, "Multi-Level Signaling," DesignCon 2000. Available at http://sigcon.com/Pubs/misc/mls.htm

[5] John Patrin, Mike Li, "Comparison and Correlation of Signal Integrity Measurement Techniques," DesignCon 2002.

[6] John Grabenkemper, “Modeling Noise on Printed Circuit Board Power Planes,” DesignCon 2004, January 2004.
[7] http://electrical-integrity.com/Quietpower_files/QP43_extras/DC04_PowerPlaneNoise.ppsx
[8] Peter J. Pupalaikis, Eric Yudin, “Eye Patterns in Scopes,” DesignCon 2005.
[9] http://electrical-integrity.com/Quietpower_files/QP43_extras/Iris.exe
[10] Bruce Archambeault, Samuel Connor, Daniel N. de Araujo, M.R.Hashemi, R. Mittra, C. Schuster, A. Ruehli, “Full Wave Simulation and Validation of a Simple Via Structure,” DesignCon 2006.
[11] Christian Schuster, Young Kwark, Giuseppe Selli, Prathap Muthana,” Developing a “Physical” Model for Vias,” DesignCon 2006.
[12] Ralf Schmitt, Joong-Ho Kim, Woopong Kim, Dan Oh, June Feng and Chuck Yuan, “Analyzing the Impact of Simultaneous Switching Noise on System Margin in Gigabit Single-Ended Memory Systems,” DesignCon 2008
[13] I. Novak, "Measuring milliohms and picohenrys in power distribution networks," DesignCon 2000.
[14] Y. Shlepnev, A. Neves, T. Dagostino, S. McMorrow, “Practical Identification of Dispersive Dielectric Models with Generalized Modal S-parameters for Analysis of Interconnects in 6-100 Gb/s Applications,” DesignCon 2010.
[15] Eric Bogatin, Mike Resso, “A Simple, Yet Powerful Method to Characterize Differential Interconnects,” DesignCon 2011.
[16] Jack Carrel, Heidi Barnes, Robert Sleigh, Hoss Hakimi, Mike Resso, “De-Mystifying the 28 Gb/s PCB Channel: Design to Measurement,” DesignCon 2014.
[17] Steve Sandler, “Killing the Bode Plot,” DesignCon 2016.
[18] DesignCon 2001 flyer, courtesy of Julian Ferry, http://electrical-integrity.com/Quietpower_files/QP43_extras/ Designcon2001.pdf

APPENDIX

- Timothy Hochberg, Henri Merkelo, Mike Resso, “Advances in High-Speed Design in Dispersively Attenuating Environments Such as Cables and Backplanes,” DesignCon 2001
- Tom Cohen, “Practical Guidelines for the Implementation of Back Drilling Plated Through Hole Vias in Multi-Gigabit Board Applications,” DesignCon 2003
- Brian Vicich, Scott McMorrow, Rob Hinz, “Advances in Design, Modeling, Simulation and Measurement Validation of High Performance Board-to-Board 5-to-10 Gbps Interconnects,” DesignCon 2004
- Robert Schaefer, “Discussing the limitations and accuracies of time and frequency domain analysis of physical layer devices,” DesignCon 2005
- Ken Willis, Joel Martinez, Mike Resso, “Multi-Gigabit Serial Channel Design Methodology – From Architecture, Through Prototype, to Physical Measurement Verification,” DesignCon 2005
- James L. Drewniak, Bruce Archambeault, James Knighten, Giuseppe Selli, “Comparing Time-Domain and Frequency Domain Techniques for Investigation on Charge Delivery and Power-Bus Noise for High-Speed Printed Circuit Boards,” DesignCon 2007
- Jeff Loyer, Richard Kunze, Xiaoning Ye, “Fiber Weave Effect: Practical Impact Analysis and Mitigation Strategies,” DesignCon 2007
- Richard I. Mellitz, Michael Tsuk, Tony Donisi, Steve Pytel, “Strategies for Coping with Nonlinear and Time Variant Behavior for High Speed Serial Buffer Modeling,” DesignCon 2008
- Vishram Pandit, “Crosstalk Amplification by Resonance,” DesignCon 2009
- Cosmin Jorga, “Active Cancellation of Noise Coupling in Mixed-Signal Integrated Circuits: Methodology, Design Examples, and Experimental Results,” DesignCon 2009
- Ransom Stephens, Marcus Muller, “Analysis of Random Noise and the Effect of Band-Limited Noise on Stressed-Eye Receiver Tolerance Tests,” DesignCon 2009
- Paul Huray, Olufemi Oluwafemi, Jeff Loyer, Eric Bogatin, Xiaoning Ye,” Impact of Copper Surface Texture on Loss: A Model that Works,” DesignCon 2010
- Jeff Loyer, Richard Kunz, “SET2DIL: Method to Derive Differential Insertion Loss from Single-Ended TDR/TDT Measurements,” DesignCon 2010
- Steve Weir, “PDN Application of Ferrite Beads,” DesignCon 2011
- Mike Steinberger, “How to Avoid Butchering S Parameters,” DesignCon 2011
- Peter J. Pupalaikis, “Wavelet Denoising For TDR Dynamic Range Improvement,” DesignCon 2011
- Larry D. Smith, Sishuang Sun, Mayra Sarmiento, Zhe Li, Karthik Chandrasekar, “On-Die Capacitance Measurements in the Frequency and Time Domains,” DesignCon 2011
- Larry D. Smith, “PDN Resonance Calculator for Chip, Package and Board,” DesignCon 2012
- John Martens, Al Neves, Orlando Bell, “High-confidence S-parameter Measurement Methodologies for 15-28 Gbps,” DesignCon 2012
- Adam Haley, Chad Morgan, Megha Shanbhag, “Beyond 25 Gbps: A Study of NRZ & Multi-Level Modulation in Alternative Backplane Architectures, DesignCon 2013
- Daniel Dvorscak, Michael Tsuk, “A Reverse Nyquist Approach to Understanding the Importance of Low Frequency Information in Scattering Matrices,” DesignCon 2013
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