Measurement to Simulation Correlation on Thin Laminate Test Boards

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A year ago, I introduced causal and frequency-dependent SPICE grid models for simulating power-ground plane impedance [1]. The idea behind the solution was to calculate the actual R, L, G and C parameters for each of the plane segments separately at every frequency point, run a single-point AC simulation and then stitch the data together to get the frequency-dependent AC response. Here, using the measured and simulated data on test boards with four different thin laminates and a regular reference laminate, I will show you how that simple model correlates to measured data and simulation results from other tools.

A number of different test boards were fabricated, tested and simulated. The active area of all boards was 6" x 6" square, and all boards had the same four-layer construction as shown in *Figure 1*.

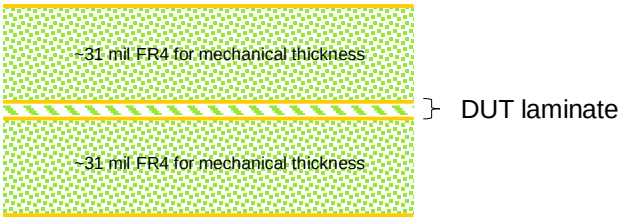

***Figure 1**: Stackup construction of test boards.*

The Device Under Test (DUT) laminate is centered in the middle and had five variants as shown in *Table 1*.

Reference laminate: FR406, 4-mil thickness, 1ou ED copper
HK04J 2536E, 1-mil thickness, 1ou ED coppers
HK04J 7423E, 0.5-mil thickness, 1ou ED copper
HK04J 0.35-mil ED, 0.35-mil thickness, 2ou ED copper
HK04J 0.35-mil RA, 0.35-mil thickness, 2ou RA copper

***Table 1**: Variants of DUT laminates.*

The 4-mil thick regular FR406 laminate served as a baseline, since it is common in low-coast printed circuit boards as power-ground sandwich. The other four options represent

thin laminates in the range of 1-mil down to 0.35 mils thickness. To check for the effect of copper weight and type, the 1-mil and 0.5-mil laminates had one-ounce electro-deposited (ED) copper, the thinnest option used two-ounce copper with ED and rolled-annealed (RA) variants. To attach probes of measuring instruments and/or various bypass components to the board, there are 121 via pairs arranged as test points on a 0.5-inch grid. You can see the close-up of cross-sectional view of the test points and the board top view sketches in *Figures 2* and *3*, respectively.

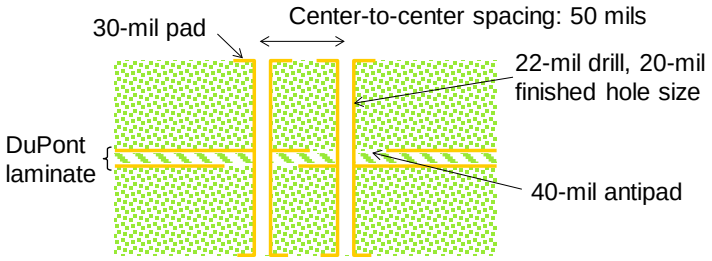

***Figure 2**: Cross-section view of test point via pairs.*

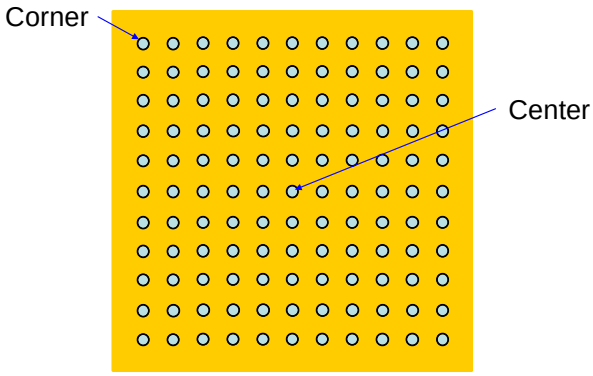

***Figure 3:** Top view of test boards showing the grid of connection points for probes and/or components. Each circle represents two vias as shown in Figure 2. The via pairs are arranged on a 0.5" grid, centered on the board. The Corner and Center labels mark the test points where I measured and simulated the planes.*

Test boards with each laminate flavor had two additional sub-variants: one with the board and plane edges left open (which is the typical case in our boards) and another one where the board edges had vias along the board edge, shorting the DUT laminate. The shorting vias have a center-to-center spacing of 50 mils. You can see photos of the open-edge and shorted-edge 1-mil test boards in *Figure 4*.

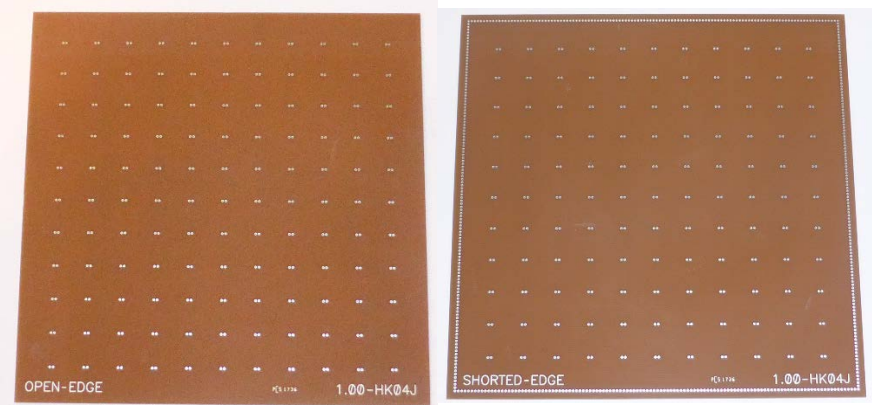

Figure 4: *Test boards with 1-mil DUT laminate, open-edge version on the left, shorted-edge version on the right. Due to the tight spacing, the shorting vias along the board edge blend together and look like a trace.*

These test boards have been measured and simulated in a large number of different configurations. In this article you can read the summary of data referring to two locations, *Corner* and *Center*, as marked in *Figure 3*.

For data shown here, I did not attach any component to the boards. The measurement setup for the open-edge boards is shown in *Figure 5*. I used a Keysight E5061B vector network analyzer in two-port shunt-through connection. On the left, you can see the semirigid probes with red heat-shrink tube and on the right the full setup. For shorted-edge boards the setup is the same, except I also added a common-mode toroid [2] to reduce the cable-braid error (see *Figure 17*).

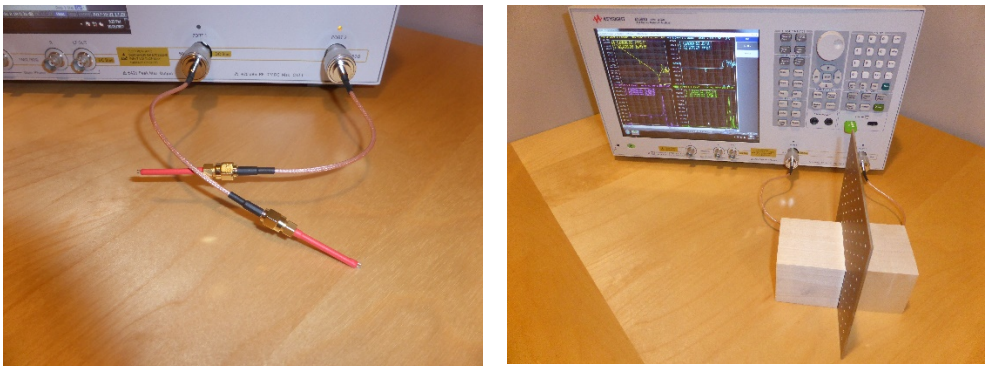

Figure 5*: Test setup for the open-edge test boards.*

The first pass of simulations on the open-edge test boards started out with nominal or estimated values. The boards were also cross sectioned so that we can use the actual geometry in the second pass of simulations. Based on the measured dielectric thickness and measured capacitance, the dielectric constant and dielectric loss numbers were also

updated. You can see representative cross section photos in *Figure 6* and the nominal and actual simulation parameters in *Table 2*.

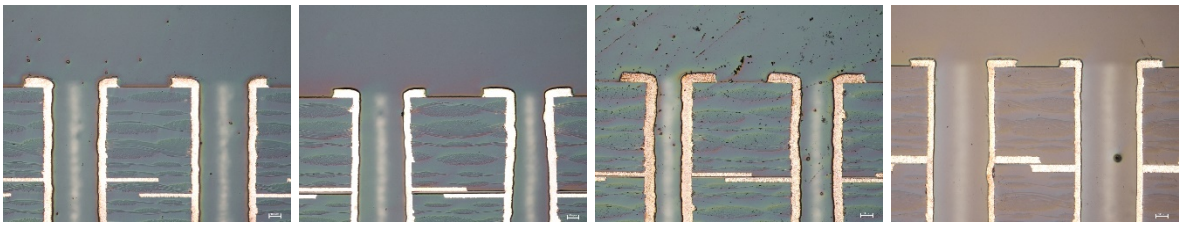

Figure 6: *Cross section photos of the test board with four different laminate thickness: from left to right, 4 mil, 1 mil, 0.5 mil and 0.35 mil. Only the upper half of the stackup is shown; the DUT laminate is towards the bottom of the photos.*

	4mil nom	4mil act.	1mil nom	1mil act.	0.5mil nom	0.5mil act.	0.35mil nom	0.35mil act.
Dielectric thickness [um]	101.6	100	25.4	25.6	12.7	13.6	8.89	9.22
Dielectric constant at Fo [-]	4.3	4.49211	3.3	3.254612829	3.3	3.687295468	3.3	4.096994964
Dielectric loss tangent at Fo [-]	0.02	0.01638	0.01	0.000500367	0.01	0.000500367	0.01	0.000500367
Fo [Hz]	1.00E+07	1.00E+07	1.00E+07	1.00E+07	1.00E+07	1.00E+07	1.00E+07	1.00E+07
Copper thickness [um]	35	29.1	35	33.6	35	32.6	70	69.3
Copper conductivity [S/m]	5.80E+07	46400000	5.80E+07	46400000	5.80E+07	46400000	5.80E+07	46400000
Copper type	ED	ED	ED	ED	ED	ED	ED	ED

Table 2: *Nominal and actual simulation parameters.*

For the open-edge test boards three different simulators were used: a simple analytical solution based on loss-less cavity models implemented in Excel macros [3], a causal SPICE grid model solved by Berkeley SPICE [1], and a professional hybrid solver, Cadence PowerSI [4].

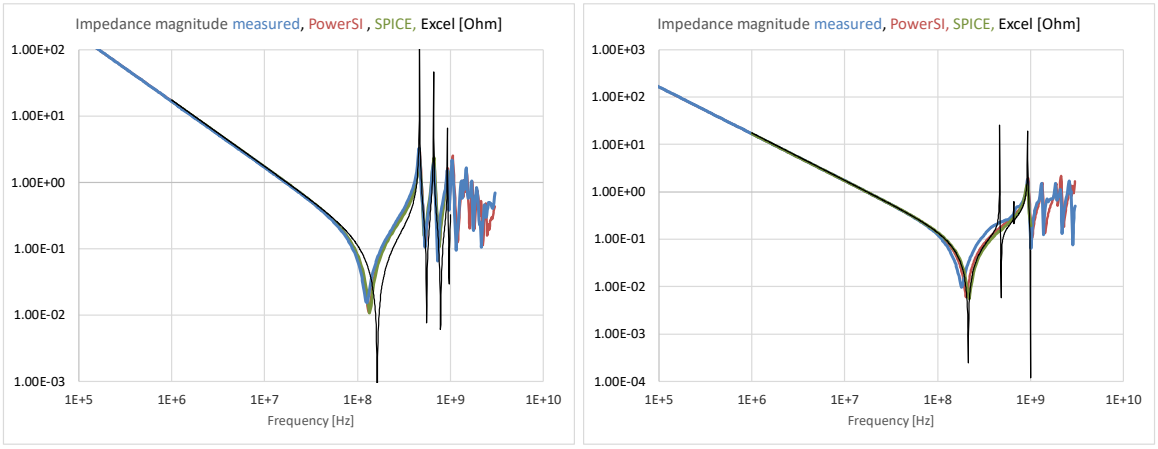

Figure 7*: Impedance magnitude correlation of the 4-mil laminate data at the corner (left) and center (right).*

You can see the correlation for the 4-mil laminate in open-edge test boards in *Figures 7* and *8*. The impedance magnitude correlation is quite good. Even the loss-less analytical formulas (black trace, labeled Excel) capture correctly the capacitive downslope and the overall inductive upslope as well as the anti-resonance peak frequencies. What it can not capture properly is the loss-related items: magnitudes of the modal resonance peaks and valleys and the frequencies of the minima (which shift with losses). You can see the same effect in *Figure 8*, which shows the extracted capacitance at the corner (the plots look the same at the center as well and therefore not shown). Note the slight tilt of capacitance versus frequency curves, which is due to the dielectric loss. We see this tilt in the measured data and simulated data alike, except the loss-less simulation (black trace), which ignores losses.

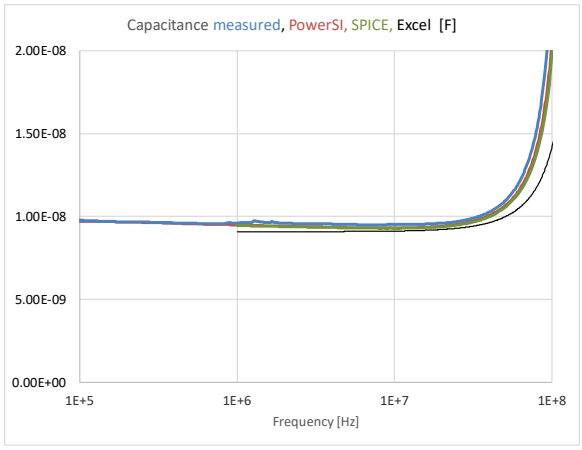

***Figure 8**: Capacitance extracted from the imaginary part of impedance of the 4-mil open-edge board data.*

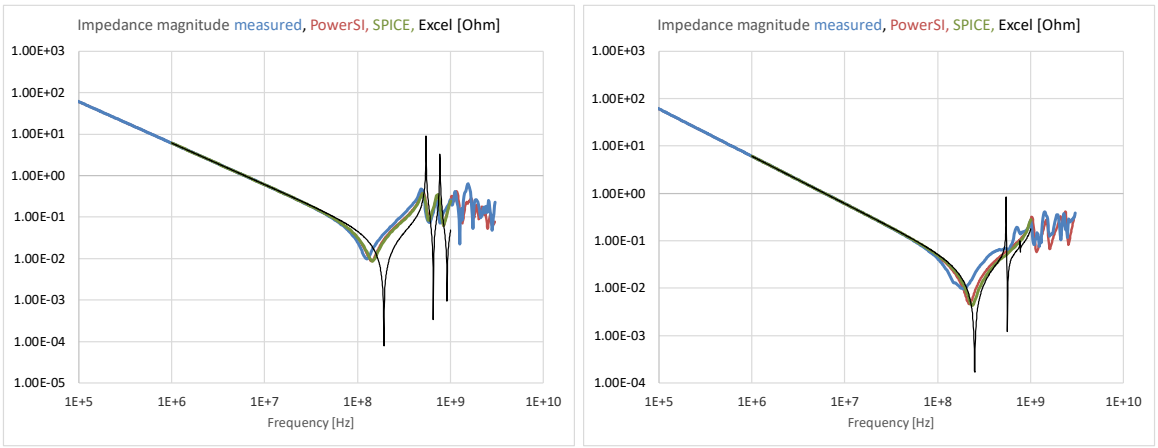

***Figure 9**: Impedance magnitude correlation of the 1-mil laminate data at the corner (left) and center (right).*

You can see the impedance magnitude and capacitance correlation for the 1-mil laminate in *Figures 9* and *10*.

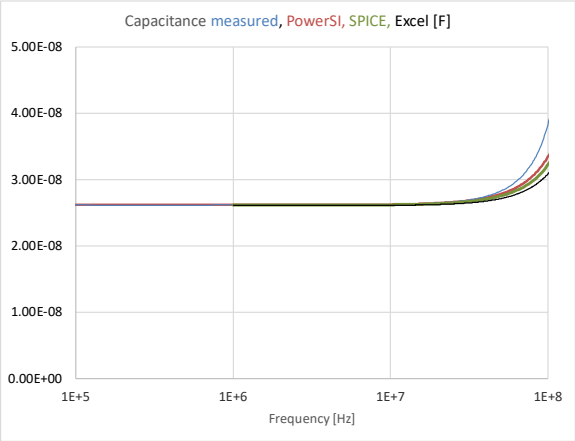

***Figure 10**: Capacitance extracted from the imaginary part of impedance of the 1-mil open-edge board data.*

You can observe the expected trend: the reduced dielectric thickness comes with an overall lower impedance and higher capacitance. The conductive losses start to attenuate the modal resonance peaks. Also, the extracted capacitance curve is flat, indicating very low dielectric losses, and therefore even the loss-less analytical Excel model correlates well. This trend continues as we switch to the 0.5-mil and 0.35-mil laminates: overall impedance drops, resonance peaks and valleys get less pronounced and capacitance goes up. The data for the 0.35-mil laminates are shown for the RA copper, though there was no measurable difference between the board impedances with ED or RA copper. Also, you don't see the effect of copper weight on these plots; it will show up in the data of shorted-edge boards.

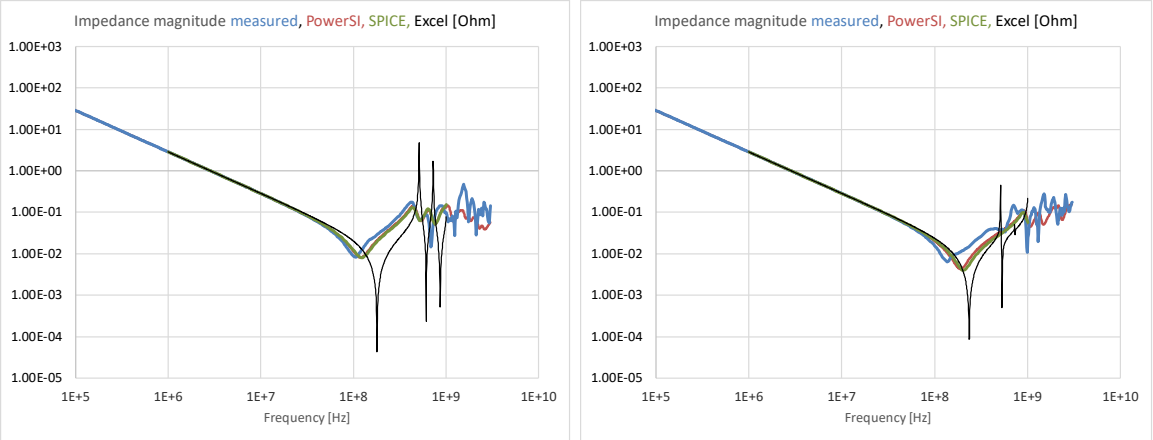

***Figure 11**: Impedance magnitude correlation of the 0.5-mil laminate data at the corner (left) and center (right).*

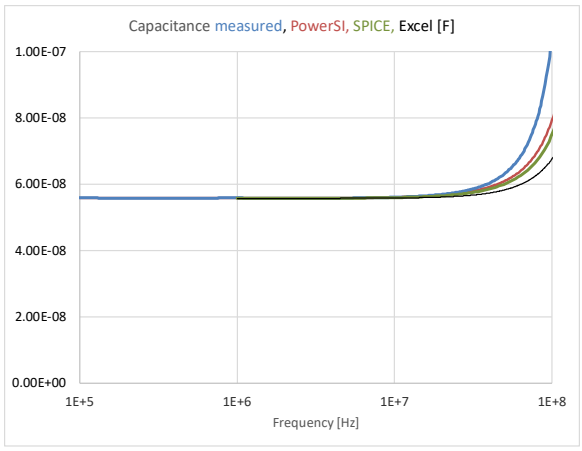

***Figure 12**: Capacitance extracted from the imaginary part of impedance of the 0.5-mil open-edge board data.*

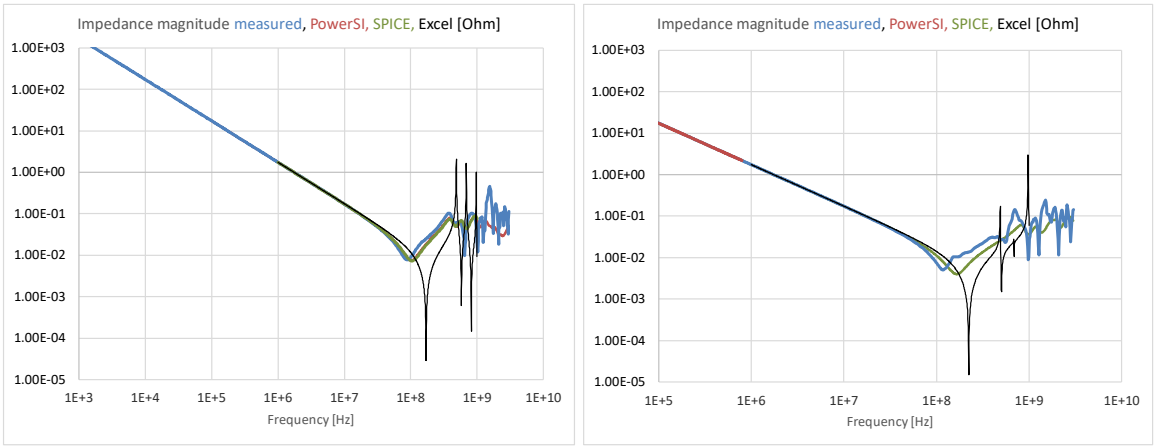

***Figure 13**: Impedance magnitude correlation of the 0.35-mil laminate data at the corner (left) and center (right).*

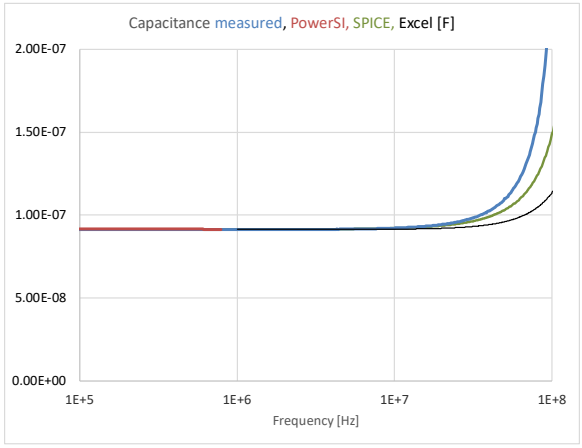

***Figure 14**: Capacitance extracted from the imaginary part of impedance of the 0.35-mil open-edge board data.*

Now that we showed good correlation between measured and simulated data, we can do the comparison of different laminates with the clean simulated data from PowerSI. *Figure 15* shows the impedance magnitude, *Figure 16* shows the capacitance comparison.

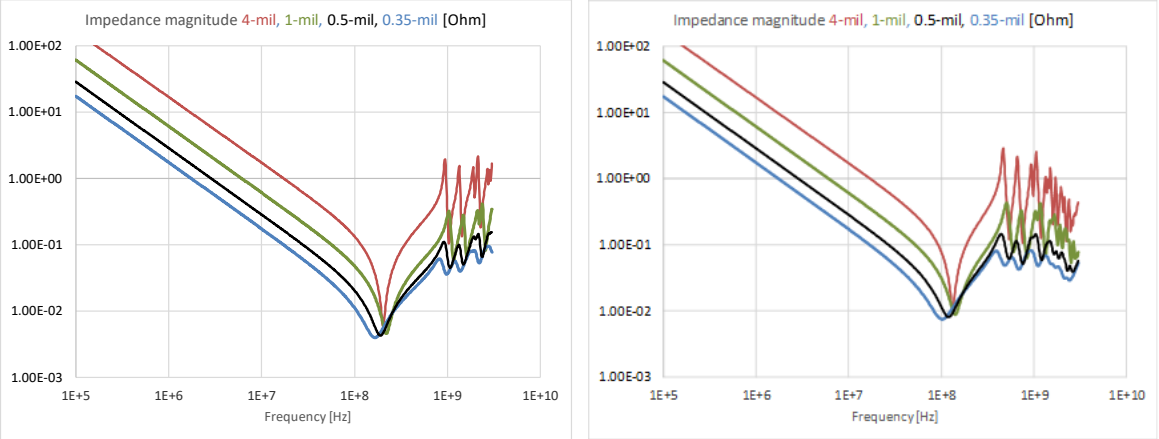

***Figure 15**: Comparison of PowerSI simulated impedance magnitude with different laminate thicknesses at the center (on the left) and corner (on the right) of boards.*

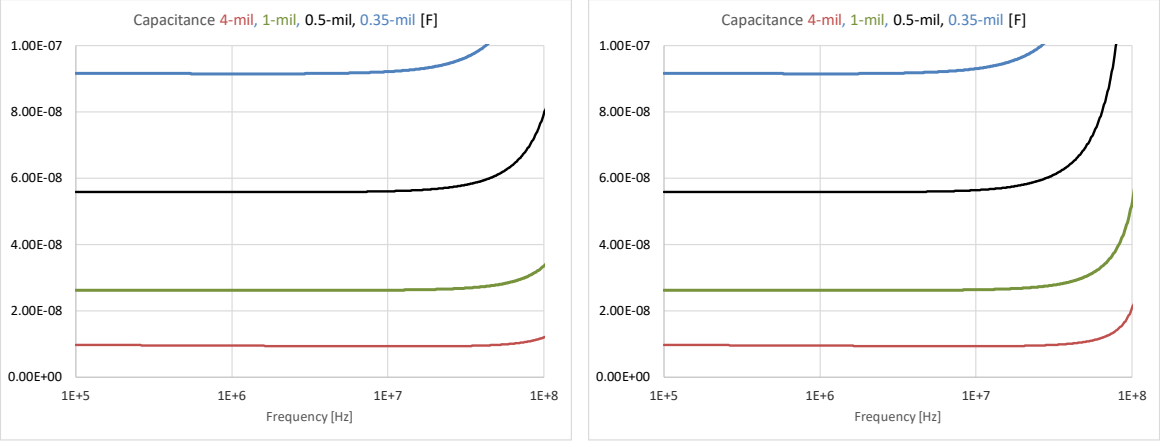

***Figure 16**: Comparison of PowerSI simulated capacitance with different laminate thicknesses at the center (on the left) and corner (on the right) of boards.*

On the comparison plots we see that as the laminate gets thinner, the peak-valley ratio of modal resonances goes down, making it less likely that noise at the peaks would get too big causing power or signal integrity issues, which is a clear signal-integrity benefit of thin laminates. You can also see that dependent on the location where we look at the board, we may see different resonant frequencies: in the center, reflected waves coming back from the open edges cancel for the first two resonant peaks below one gigahertz and therefore we do not see those peaks at the center. Also note that the capacitance curves have very little dependence on location: at low frequencies the static plane capacitance is the same at every location. However, approaching 100 MHz, all traces curve up and this

is where we see slight differences, because the series resonance frequency varies a little with laminate thickness. We need to remember that the uptick of extracted capacitance is not real, it is just a side-effect of the approaching series resonance, which happens at slightly different frequencies with different laminate thicknesses.

The main takeaway from *Figure 16* is that the static capacitance of power-ground laminates is inversely proportional to the laminate thickness. With thinner laminates we get more capacitance, which is the reason why you may hear thin laminates called buried capacitance. However, while for nano-power circuits the plane capacitance itself may be sufficient for bypassing, in medium and high-power circuits the big help is the lower inductance and lower resonance peaks. To see clearly how the inductance of laminates depend on dielectric thickness, next we look at the data on shorted-edge test boards.

The measurement setup for the shorted-edge test boards is similar to what we had for open-edge boards, but we have to reduce the low-frequency error caused by the cable-braid resistance. This is not an issue when we measure open-edge boards, because their impedance at low frequencies is much higher than the cable-braid resistance. With shorted-edge boards, we have to measure milliohms or less impedance at low frequencies, which is practically the resistance of plane loops, and cable braid resistances in the same order of magnitude would create too much error. There are different ways of reducing this error, here we used common-mode toroids on the measurement cable. You can see the setup in *Figure 17*.

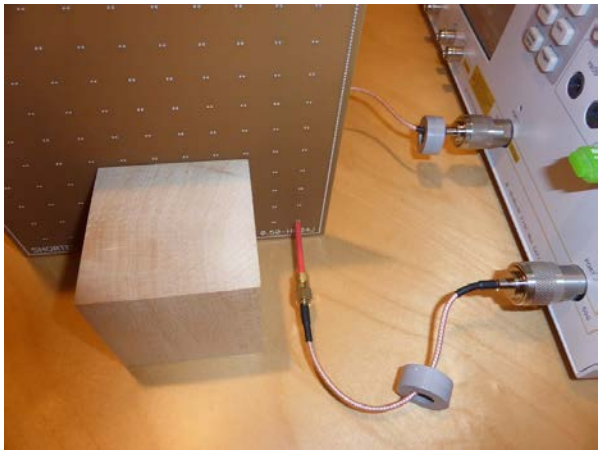

Figure 17: *Setup for measuring shorted-edge boards. Note the grey high-permeability toroids on each of the cables.*

For shorted-edge test boards the simulations were done with PowerSI. You can see the correlation for the 4-mil laminate shorted-edge boards in *Figures 18* and *19*. Up to about 1 MHz, the impedance magnitude is flat, because we measure the resistance of shorted planes. Above 1 MHz the impedance slopes upwards, indicating a combination of increasing skin resistance and inductive reactance. The impedance magnitude plots at the center have resonance peaks and valleys at high frequency. You don't see those resonance

peaks at the corner, because the wall of shorting vias is just a quarter of an inch away, forcing the impedance low. We see the same trend on *Figure 19* as well: as opposed to the static capacitance, which is the same at the center and at the corner, the extracted inductance does depend on the location. Of course, as we go closer to the wall of shorting vias, the loop inductance gets lower. This tells us that if we want inductance values representative to the laminate, we have to take the inductance at the center. The inductance is around 100 pH, which correlates approximately with the spreading inductance estimate of planes, which is 33 pH for each mil dielectric spacing. The inductance curves are relatively flat, though you can notice an ever so small downslope starting around 10 MHz.

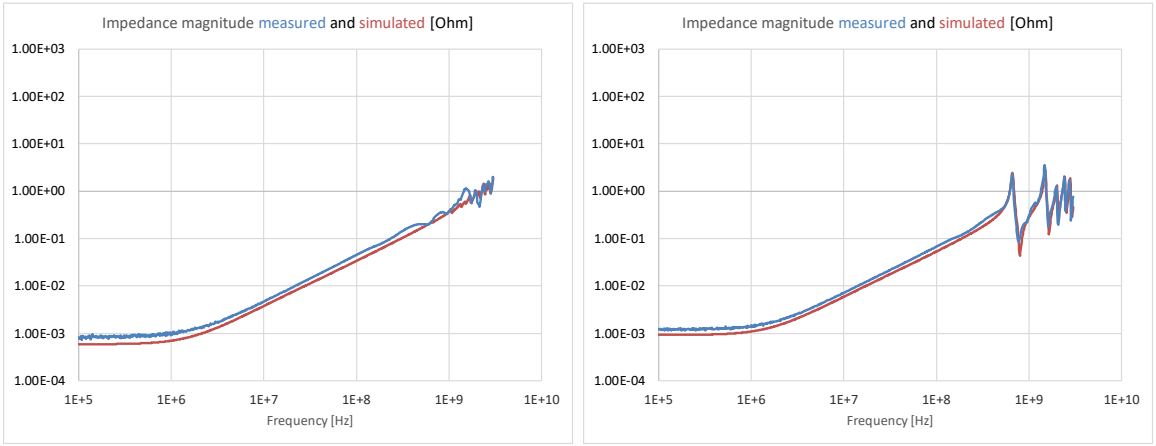

***Figure 18**: Impedance magnitude correlation of the 4-mil laminate data at the corner (left) and center (right).*

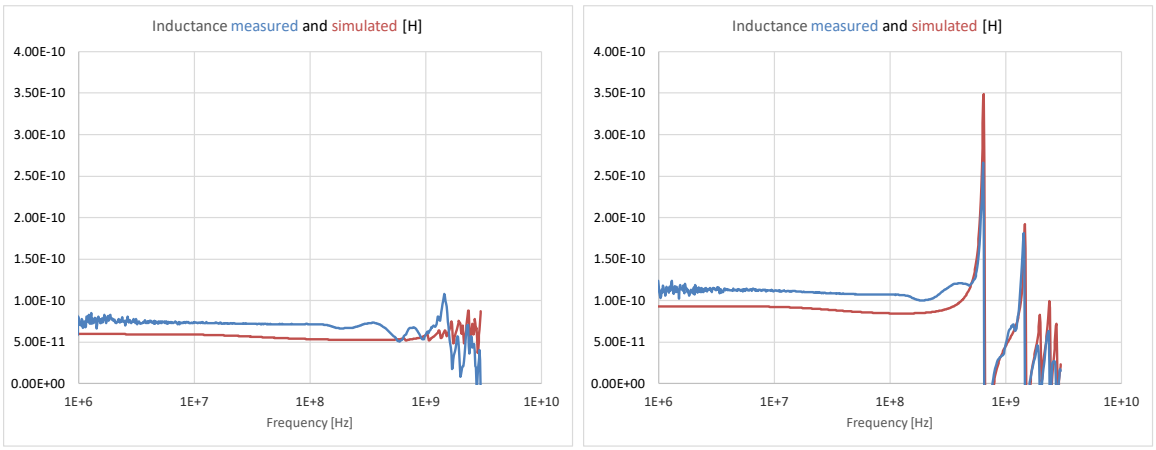

***Figure 19**: Inductance extracted from the imaginary part of impedance of the 4-mil shorted-edge board data at the corner (left) and center (right).*

You can see the correlation for the 1-mil laminate in *Figures 20* and *21*. It follows the same basic signature and the primary difference is the lower inductance. Not only the entire curve runs lower, but we see a more pronounced change of inductance with frequency. The inductance starts to drop at 10 MHz, which is commonly considered the skin corner frequency of one-ounce copper.

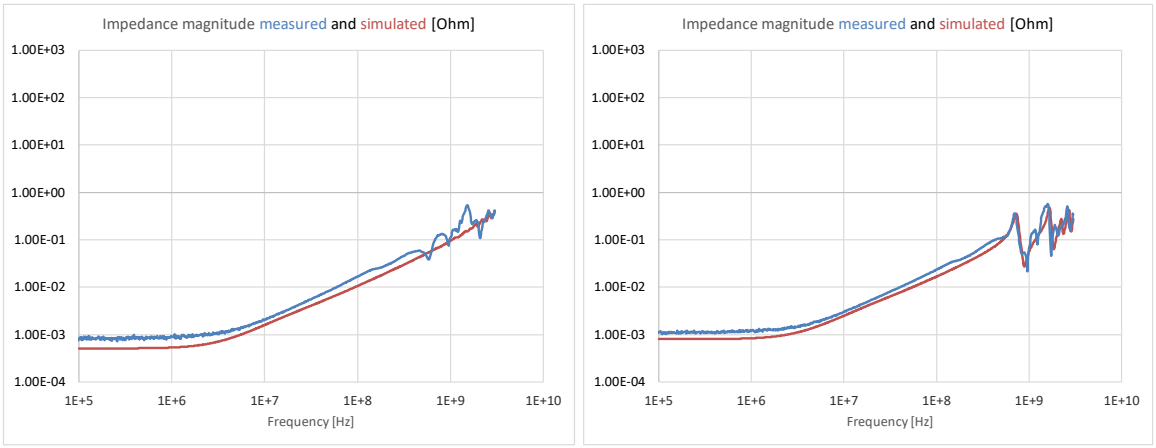

***Figure 20**: Impedance magnitude correlation of the 1-mil laminate data at the corner (left) and center (right).*

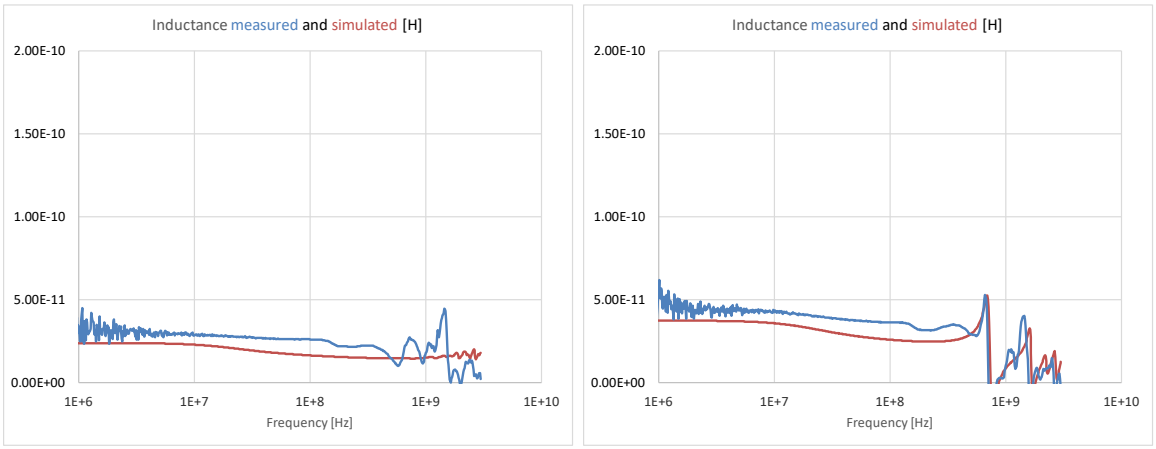

***Figure 21**: Inductance extracted from the imaginary part of impedance of the 1-mil shorted-edge board data at the corner (left) and center (right).*

I show the 0.5-mil correlation in *Figures 22* and *23*. The data follows the same trend: lower inductance, though here you can notice that the inductance did not drop by a factor of two. The reason is that the inductance of the unavoidable antipad opening around the test vias penetrate the plane that they do not connect to. Unless we use smaller vias and antipads, this eventually becomes a limiting factor for utilizing the full low-inductance benefits of thin laminates.

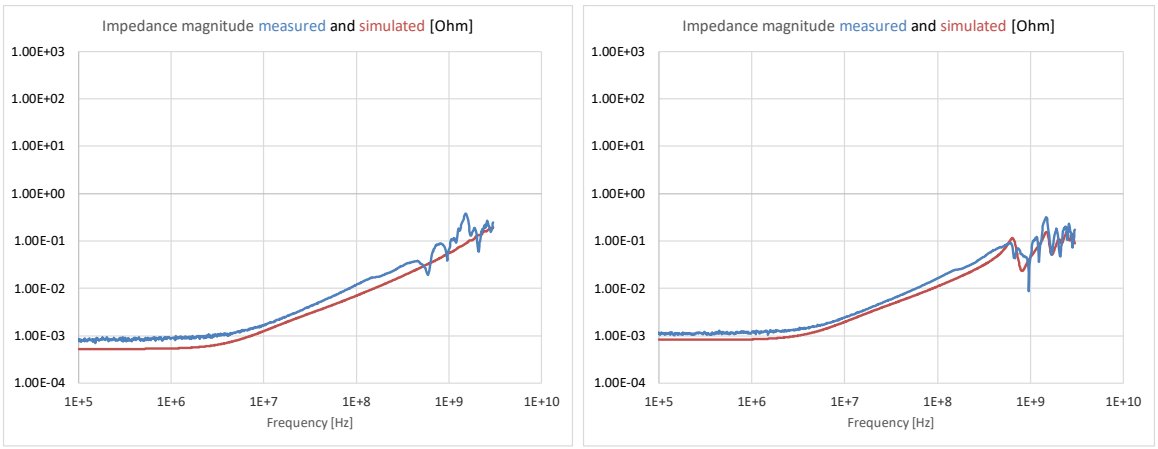

***Figure 22**: Impedance magnitude correlation of the 0.5-mil laminate data at the corner (left) and center (right).*

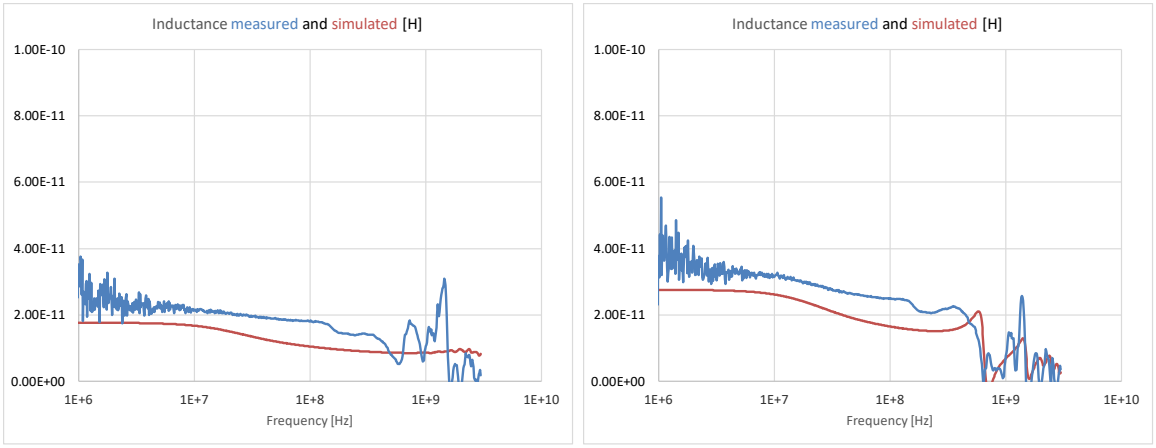

***Figure 23**: Inductance extracted from the imaginary part of impedance of the 0.5-mil shorted-edge board data at the corner (left) and center (right).*

Figures 24 and *25* show the correlation with 0.35-mil laminate with two-ounce copper. Here we see that at low frequencies the impedance magnitude curves start out at lower values because of the lower resistance of the two-ounce copper planes. The thicker copper allows for more vertical spreading of the current loop, which results in a higher inductance at low frequencies. The low inductance originating from the thin laminate kicks in at higher frequencies.

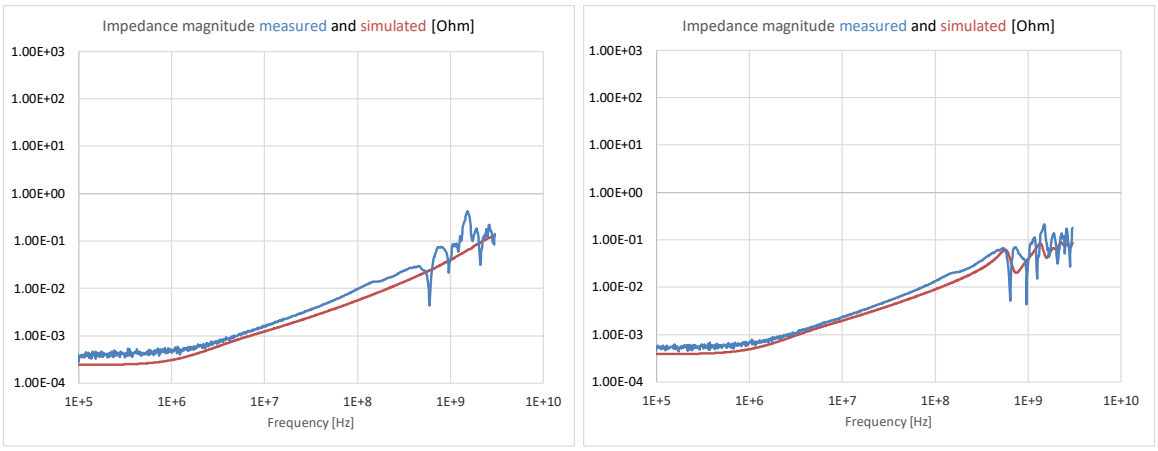

***Figure 24**: Impedance magnitude correlation of the 0.35-mil laminate data at the corner (left) and center (right).*

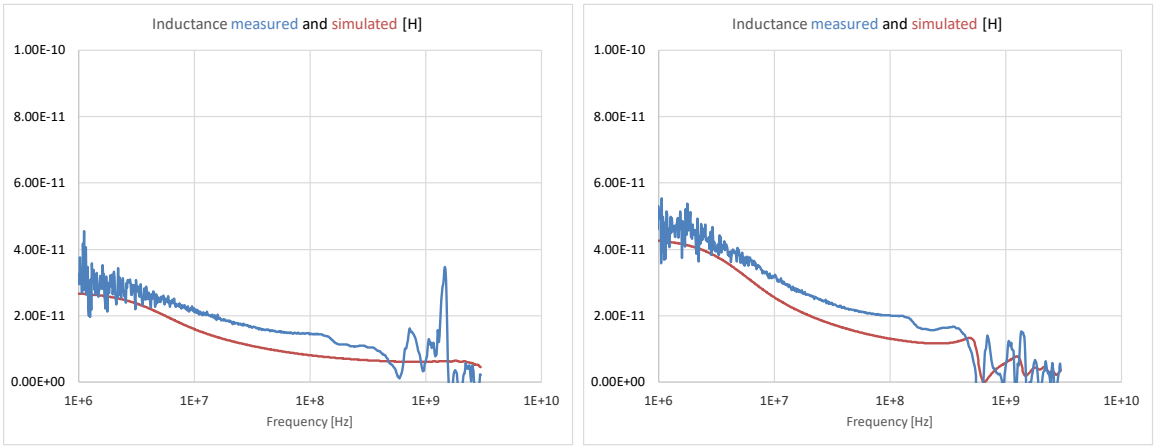

***Figure 25**: Inductance extracted from the imaginary part of impedance of the 0.35-mil shorted-edge board data at the corner (left) and center (right).*

The next two figures show the overall comparison of the shorted laminates: you can see the impedance magnitude comparison in *Figure 26* and the inductance comparison in *Figure 27*. Below one MHz the impedance magnitude plots follow the DC resistance of the planes: the three boards with one ounce copper run around one mOhm, the 0.35-mil test board using two-ounce copper runs at 0.5 mOhm. In the inductive upslope region the order of curves follow the laminate thickness values: thinner laminates produce lower impedance. The inductance comparison in *Figure 27* tells you visually how the different laminates compare in the different frequency ranges. In the entire frequency range, the 4-mil laminate produces the highest inductance. With thinner laminates and also because the copper thickness now becomes comparable to the dielectric thickness, the order of inductance depends not only on the laminate thickness, but also on the copper weight and frequency. Below 1 MHz the highest inductance comes from the thinnest dielectric, but only because this laminate had two-ounce copper. Above 10 MHz the order of curves follows the laminate thickness.

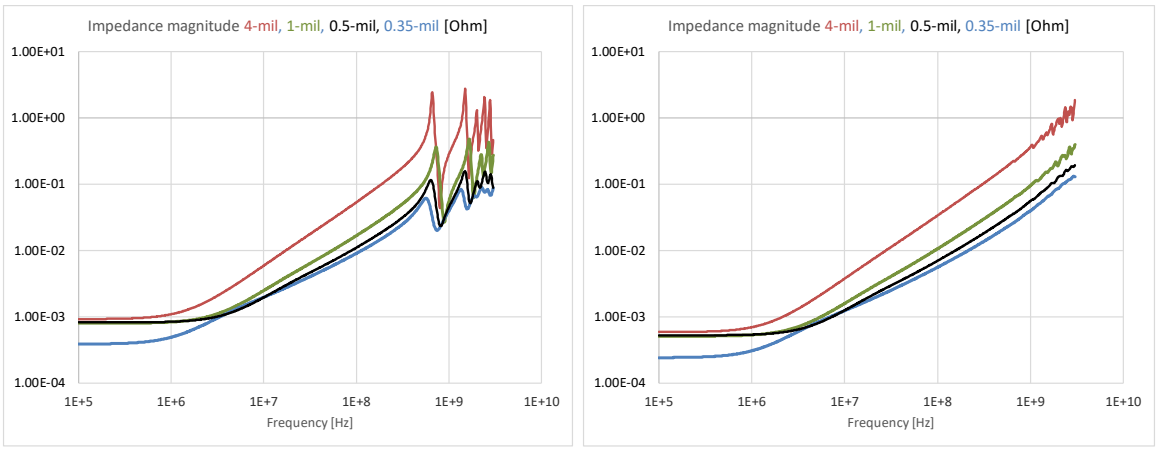

***Figure 26**: Comparison of PowerSI simulated impedance magnitude with different laminate thicknesses at the center (on the left) and corner (on the right) of boards.*

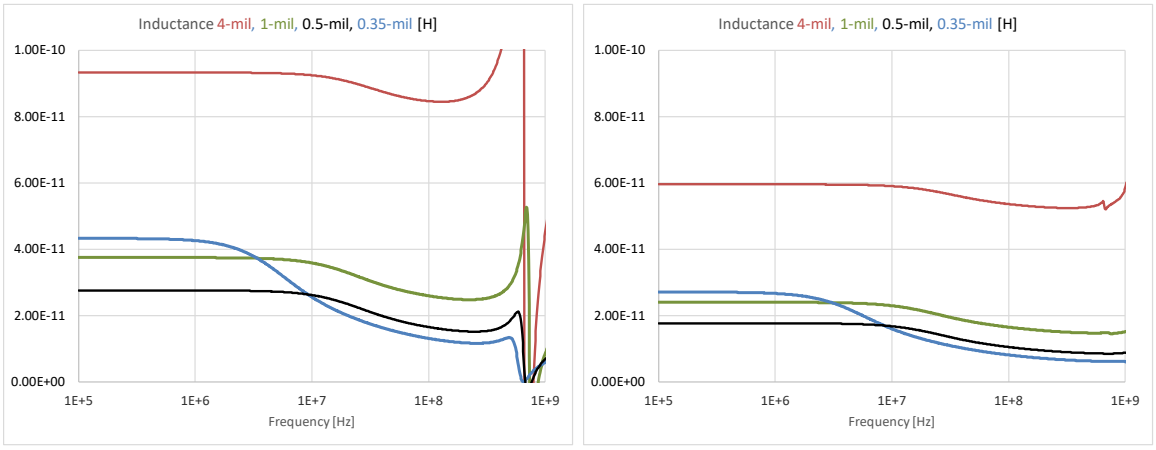

***Figure 27**: Comparison of PowerSI simulated inductance with different laminate thicknesses at the center (on the left) and corner (on the right) of boards.*

Summary and conclusions

I showed the correlation of impedance and extracted capacitance/inductance values of 6” x 6” laminate test boards with open and shorted edges. The correlation was shown with three different simulation tools for the open-edge boards: loss-less analytical formulas capture the capacitive downslope of impedance magnitude curve, but without the small tilt due to dielectric losses. They also capture properly the peak frequencies of resonances, but due to ignoring losses, the peak/valley values and valley frequencies are off. The causal SPICE models and professional hybrid solvers capture all of those effects correctly. The inductance of laminates depends on the combination of laminate and copper thicknesses and frequency. At high frequencies the inductance is clearly proportional to dielectric thickness, which is the primary power distribution benefit. Below the skin cutoff frequency, the inductance gets bigger with heavier copper. Thin laminates also naturally suppress plane resonances. The correlation is somewhat worse for shorted-edge

test cases because the causal SPICE models ignore and hybrid solvers only approximate for the impact of test-via antipads. To get that level of correlation, we have to use 3D solvers [5].

Acknowledgement
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