EDN SI/PI Masterclass

Co-Planar Fixtures for Bypass Capacitor Testing

Istvan Novak, Oracle, August 2018

In the previous blog posts we introduced two very simple home-made fixtures made out of solder wick and SMA connectors. In this article you can learn about co-planar fixtures.

Co-planar PCB fixtures

Generic PCB fixtures can be created from small co-planar 50-ohm traces that have exposed trace and ground next to each other on the same side of the little board. The DUT can be connected between the trace and the ground shape, allowing us to use the Two-Port Shunt-Through connection topology. Having a sufficiently large ground shape next to the trace, we can accommodate a large number of different case styles and sizes. Having connectors at the ends of the through trace will allow for quick connections, though we could also use permanently attached (soldered) cables. Soldered cables would eliminate the need for separate cables with connectors at both ends, but would make the calibration a little bit more involved. The photo in *Figure 2* shows the un-assembled panel of fixture boards available from [4]. On one panel we get eight identical fixture boards (though they carry different labels) that we can break away. Three of them labeled for calibration (OPEN, SHORT, LOAD) and five are labeled for measuring components (DUT). The panels are available with SMA male-female connectors attached, or with the loose connectors shipped in the same package for us to solder them on. The coplanar traces are very close to 50 ohms and have only 160 ps delay, which means for a lot of measurements up to 10 MHz a simple Response Through calibration is enough.

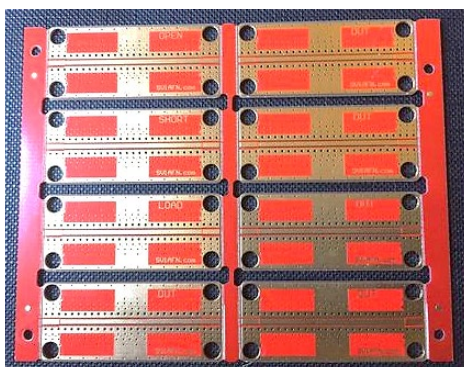

Figure 2: A full panel of test fixtures from [4].

If we are willing to do more complex calibrations, this setup now can be used reliably up to higher frequencies as well. The tradeoff is between the start and stop frequencies of the measurement range and the nature of components we want to measure. If we want to start the sweep anywhere below a few times ten kilohertz ***and*** we want to measure components that have low impedance at low frequencies, such as low-ESR high-capacitance components, we run up against the cable-braid loop error, described in Section 7.1.1 of

[3]. Dependent on how we reduce the cable-braid loop error, the chosen solution may come with its own limitations at high frequencies. For this article a home-made common-mode choke was used to reduce the effect of the cable braid resistance, with an upper bandwidth of approximately 50 MHz and the data was collected in the 300 Hz to 30 MHz frequency range.

These fixtures can take any component size from 0402 (1 mm long) to D-size (7.3 mm long). The DUT sample in *Figure 3* was a 1210-size ceramic capacitor. With these fixtures we also have the option of connecting the DUT in different ways. Mechanically and electrically we get the most robust and most reliable connection if we solder the part to the fixture. If we want to re-use the fixture and want to speed up the swapping of components, we can opt to use simple pressure mount, like we do with the solder-wick fixture, and maybe we can reduce the contact resistance and improve consistency of our collected data by applying a dot of silver paste each to the component terminals. If we decide to solder the component, we can improve the repeatability of the measurement by slightly pushing down the parts on the pads during soldering, which guarantees that the different components sit at the same height above the fixture.

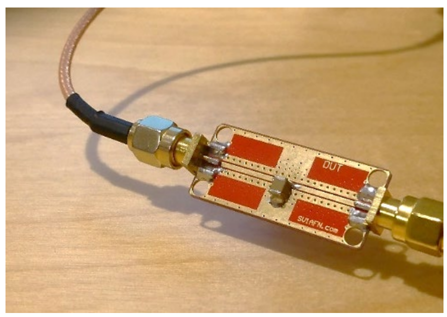

Figure 3: Fixture with a 1210-size capacitor soldered on.

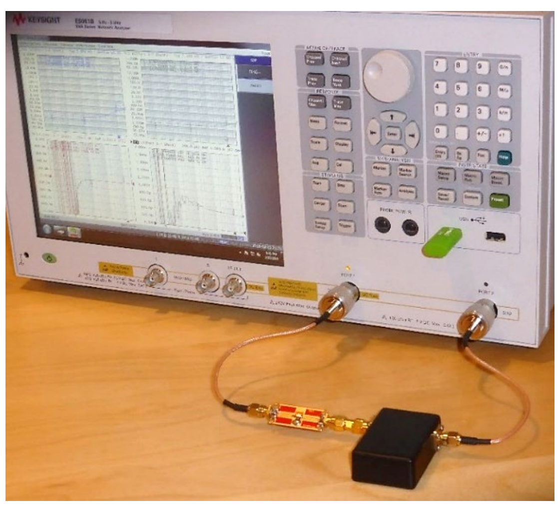

Figure 4.: *Measurement setup with network analyzer and common-mode toroid. E5061B loaner VNA is courtesy of Keysight.*

Figure 5 shows the measurement result from the setup and DUT shown in *Figure 4*. We make use of the Impedance Analysis Option [5] and the screen is set up with four simultaneous traces: Impedance magnitude (upper left), Effective Series Resistance, Rs (upper right), Equivalent Series Capacitance, Cs (lower left) and Equivalent Series Inductance, Ls (lower right). The logarithmic horizontal scale starts at 300 Hz and ends at 30 MHz. The 70 Hz IFBW setting provides a good compromise between sweep speed and noise floor.

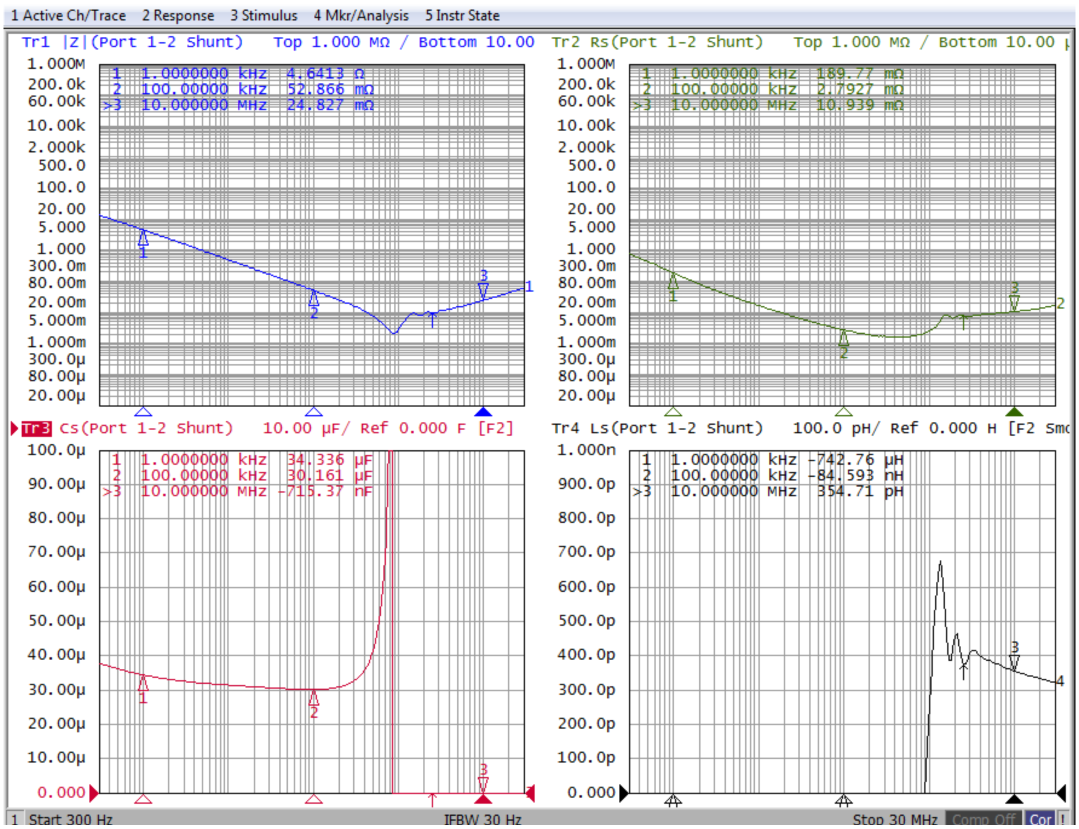

Figure 5.: Measurement data of a 47 uF 1210 size ceramic multi-layer capacitor taken in a co-planar fixture. E5061B loaner VNA is courtesy of Keysight.

References

[1] Solder-wick trick characterizes bypass caps, EDN, May 9, 2018, https://www.edn.com/electronics-blogs/signal-integrity-collection/4460638/Solder-wick-trick-characterizes-bypass-caps

[2] "Accuracy Improvements of PDN Impedance Measurements in the Low to Middle Frequency Range," DesignCon2010, Santa Clara, CA, February 1-4, 2010, available at http://www.electrical-integrity.com/Paper_download_files/DC10_12-TH3_Novak-Mori-Resso.pdf

[3] Istvan Novak, Jason R. Miller: Frequency Domain Characterization of Power Distribution Networks. Artech House, Boston, 2007.

[4] RF Experimenter's PCB Panel, https://www.sv1afn.com/rf-experimenter-s-pcb-panel.html

[5] Impedance Analysis for the E5061B ENA LF-RF Vector Network Analyzer (Option 005), http://literature.cdn.keysight.com/litweb/pdf/5991-0213EN.pdf