Be Aware of Default Values in Circuit Simulators

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Simulators are very convenient for getting quick answers without lengthy, expensive and time-consuming measurements. Simulators range from simple spreadsheet-based illustration tools, like [1], to very sophisticated 3D field solvers, like [2]. Somewhere in the middle we have the generic circuit simulators, the most well known among them SPICE. Berkeley SPICE has been the grand-daddy of all SPICE tools [3] and in these days there are many professional SPICE variants available. These tools have been around for a long time and usually we take the validity of their output for granted. While the tools may be bug free, no tool can give us perfect answers for just any arbitrary numerical input: sometimes we can be up to surprises if we forget about the numerical limits and the limitations imposed by internal default values.

As an example, I show a few simulation results on a simple ladder-like power distribution network, all done with the free LTSPICE simulator [4] from Linear Technologies, now part of Analog Devices.

Figure 1 shows the schematic diagram of a simplified ladder model of a point-of-load power distribution network (PDN). The PDN is represented by four cascaded blocks: on the left an ideal voltage source with series resistance and inductance modeling the DC source. To its right is a PI model of the printed circuit board with plane resistance and inductance as well as bulk and ceramic capacitors. The next block describes the package with its series resistance, inductance and its capacitance. The 10 uF capacitance value suggests that this is not only the static capacitance of the package planes, but it also represents package capacitors. The last block on the right describes the die with a series RL term, a parallel capacitance and a parallel load resistance, which is determined by the nominal voltage and the average power consumption. Outside of these blocks is a 1A AC current source injecting test current into the silicon node. Since here all elements are linear and time invariant models, the actual current value does not matter, but the 1A value is convenient because the simulated V(load) output voltage directly gives us impedance without the need for further scaling.

Figure 2 shows the result. The heavier line is the impedance magnitude with its scale on the left, the phase is the thin line with its scale on the right. We see four resonance peaks and one sharp dip on the plot. The peaks labeled 1, 2 and 3 come from the antiresonances of neighboring capacitor banks. For instance, the first peak is formed by Lsrc and Cbulk, and the LC parallel resonance of the 100 nH and 10000 uF values produce the 5 kHz

resonance peak. To find the second peak, which comes from the series inductance of the Cbulk capacitor and the capacitance of Cceramic, we need to know what is the assumed inductance of Cbulk. You can notice that there are no series resistance and inductance symbols in series to the capacitors, so does it mean the simulation assumes zero values for those parasitics? In this regard LTSPICE is unique among the SPICE circuit simulators: we can specify the usual simple parasitics without adding the corresponding schematic elements. The equivalent circuit as defined in LT Wiki [5] is shown in *Figure 3*. We can specify not only the equivalent series resistance and inductance, but also two parallel loss elements and a body capacitance. These parameters will be frequency independent entries. But how do we enter these parameters if we don't want to type up the SPICE deck manually? LTSPICE makes it easy, offering multiple options. *Figure 4* on the left shows what happens if we move the cursor over a capacitor in the schematic diagram and right click. A window pops up where we can manually enter various attributes. On the right you see the window which pops up when you hold the CTRL key while you right click.

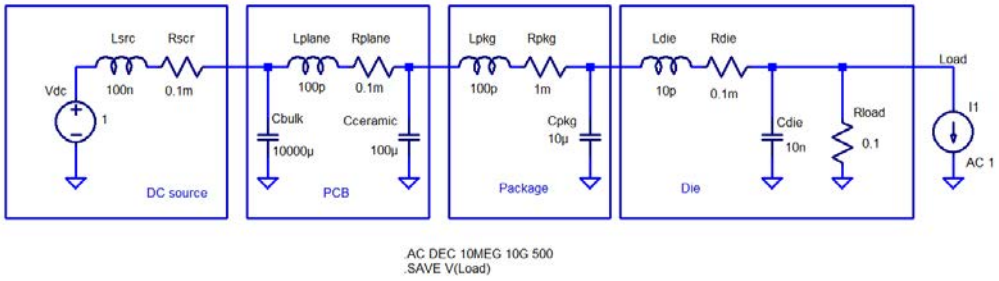

Figure 1.: *LTSPICE schematics of a simple PDN.*

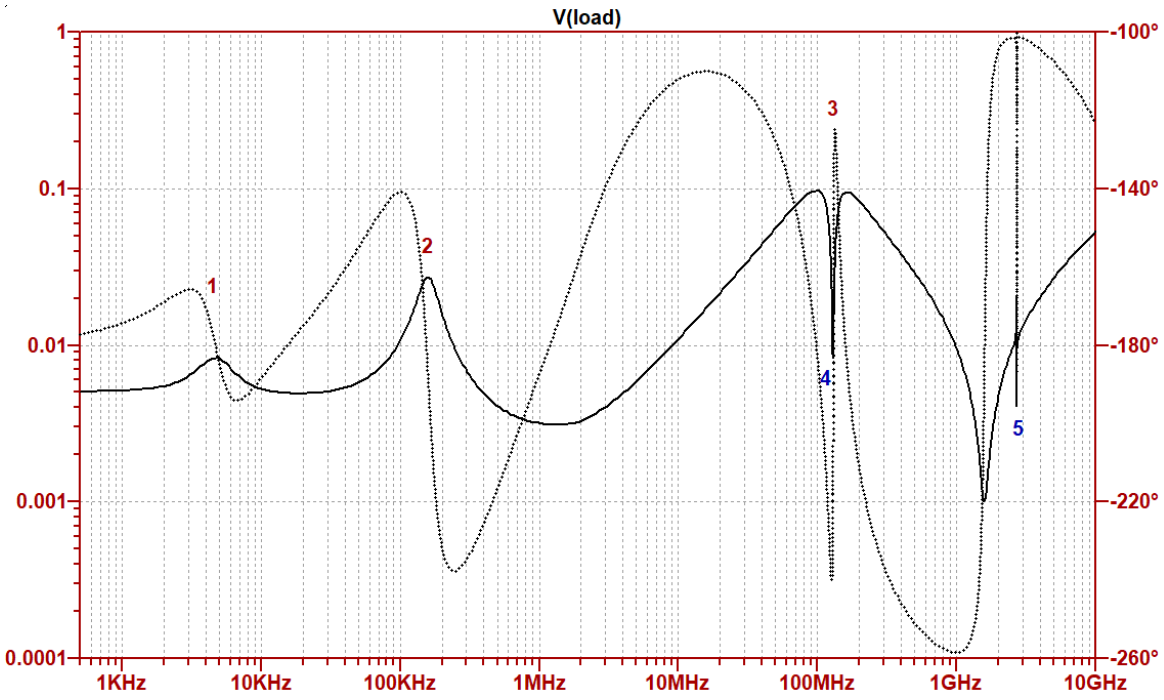

Figure 2.: *Impedance magnitude and phase of the simple PDN showed in Figure 1.*

C. Capacitor

Symbol names: CAP, POLCAP

```
Syntax: Cnnn n1 n2 <capacitance> [ic=<value>]
+ [Rser=<value>] [Lser=<value>] [Rpar=<value>]
 + [Cpar=<value>] [m=<value>]
 + [RLshunt=<value>] [temp=<value>]
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It is possible to specify an equivalent series resistance, series inductance, parallel resistance and parallel shut capacitance. The equivalent circuit is given below:

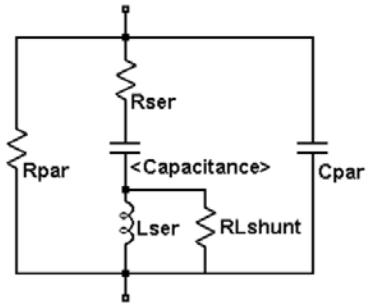

Figure 3.: *Screen shot explaining the capacitor equivalent circuit in LTSPICE.*

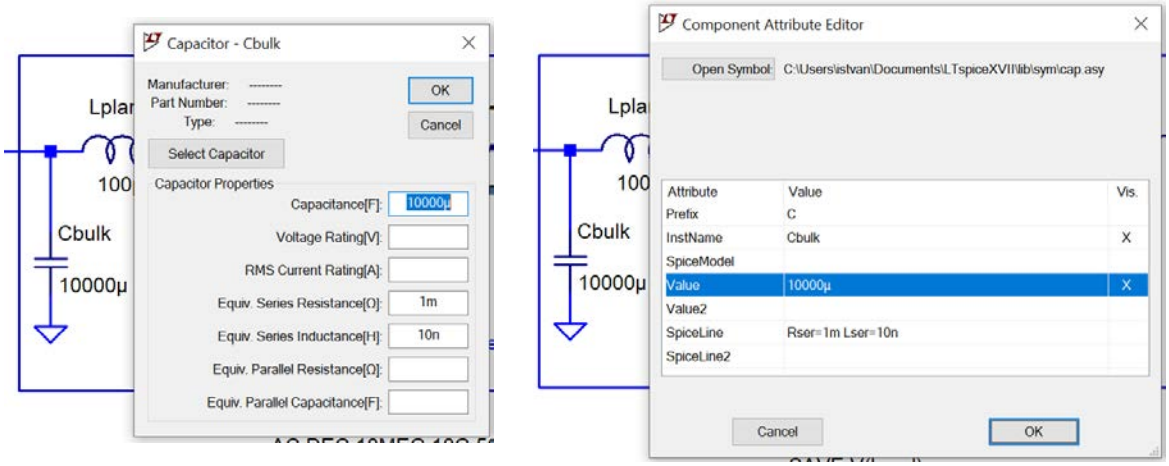

Figure 4.: *Options to enter parasitic values for capacitors in LTSPICE.*

The two windows offer somewhat different choices. On the left, in addition to the equivalent series resistance, inductance and body capacitance, we have only one parallel resistance entry. On the right, we can enter every parameter listed in *Figure 3*, including the initial condition, temperature and the multiplier (m or x), which is a convenient way to simplify the schematics if we have *m* number of identical capacitors connected in parallel. We can also hide parameters or make them visible on the schematic using the checkmark in the last column. For the schematics shown here, I turned on the feature only for the capacitance value, otherwise the view would become very crowded. Notice that in *Figure 4* I show the actual parasitic values that were used to generate *Figure 2*. Now we see that the series inductance of the bulk capacitor is 10 nH and this creates the antiresonance with

the 100 uF ceramic capacitor. From these two values we get a 150 kHz antiresonance frequency, and that is exactly where *peak 2* is. *Peak 3* is at 150 MHz and it appears to be split by the sharp and deep *notch 4*. *Table I* summarizes the capacitor parasitic values for all four capacitors.

	Cbulk	***Cceramic***	***Cpkg***	***Cdie***
C [F]	10000u	100u	10u	10n
ESR [Ohm]	1m	0.5m	10m	1m
ESL [H]	10n	100p	1n	1p

Table I.: *Parasitic values of capacitors that were used to generate Figure 2.*

We may wonder if the values in *Table I* represent reality, because ESR and ESL for the ceramic capacitor appear to be unrealistically low. Yes, it would be unrealistic to expect these values from a single capacitor, but if we imagine that these values represent ten pieces of 10uF ceramic capacitor with 5 mOhm ESR and 1nH ESL in each, it then looks reasonable.

If we move on to look at the resonance at *peak 3*, we realize that it is formed by the 10 nF Cdie capacitance and the equivalent inductance of the entire network looking back from the silicon, which is the well-known die-package resonance. By the time we add up properly all series and parallel inductances, it comes out around 160 pH. The antiresonance with the 10 nF Cdie value comes out close to 100 MHz, where the split antiresonance peak happens.

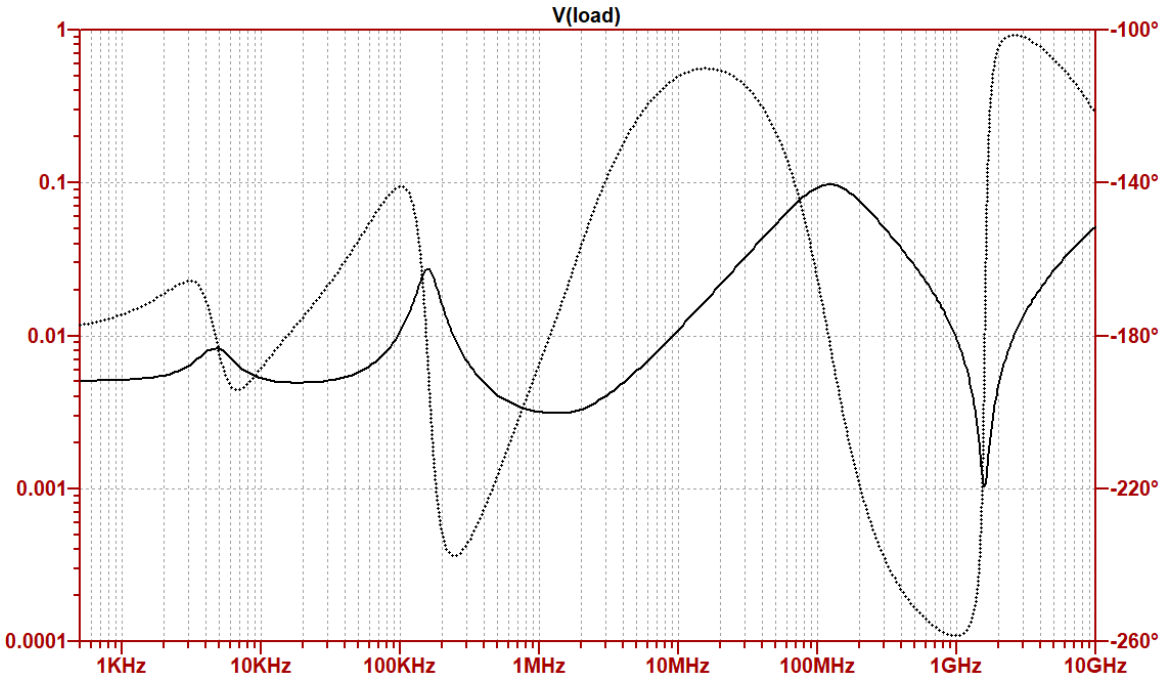

Figure 5.: *Impedance magnitude and phase of the simple PDN showed in Figure 1, but all parallel body capacitance is set to zero.*

We still need to understand where the two extra resonances, *notch 4* and *peak 5* come from. To get the answer, we need to go back to *Figure 4* and check what happens with the parameters that we ***did not*** fill out. On the left there are two parameters we left empty: parallel capacitance and parallel resistance. What happens if we explicitly set the body capacitance to zero? The result is shown in *Figure 5*: *notch 4* and *peak 5* disappeared, the rest remained practically unchanged.

Now the resonance pattern makes sense, but there is still something going on: why do we have 5 mOhm impedance at low frequencies, when the circuit calls out only 1 mOhm and three times 0.1 mOhm resistor values in the series path, altogether 1.3 mOhm series resistance? We need to look at the definitions of the inductors. The definition of inductor attributes is shown in *Figure 6* [5].

L. Inductor

Symbol Names: IND, IND2

Syntax: Lxxx n+ n- <inductance> [ic=<value>]
+ [Rser=<value>] [Rpar=<value>]
+ [Cpar=<value>] [m=<value>] [temp=<value>]

It is possible to specify an equivalent series resistance, series inductances, parallel resistance and parallel shut capacitance. The equivalent circuit is given below:

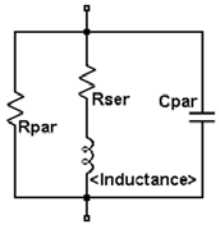

Figure 6.: *Equivalent circuit of inductor parasitics and attribute list.*

The same way how we did it for the capacitors, we can call up the parameter-entry windows for the inductors as well. In *Figure 7* we see two parasitic components listed: series resistance and parallel capacitance. We also see a note at the bottom of the left window: there is a 1 mOhm default value for the series resistance. This means if we do not make an entry there, the tool will automatically add a 1 mOhm value (but this automatically added value does not show up in the Series Resistance input field). This explains the low-frequency value on *Figure 2*, since we have four series inductors, each will have 1 mOhm series resistance by default.

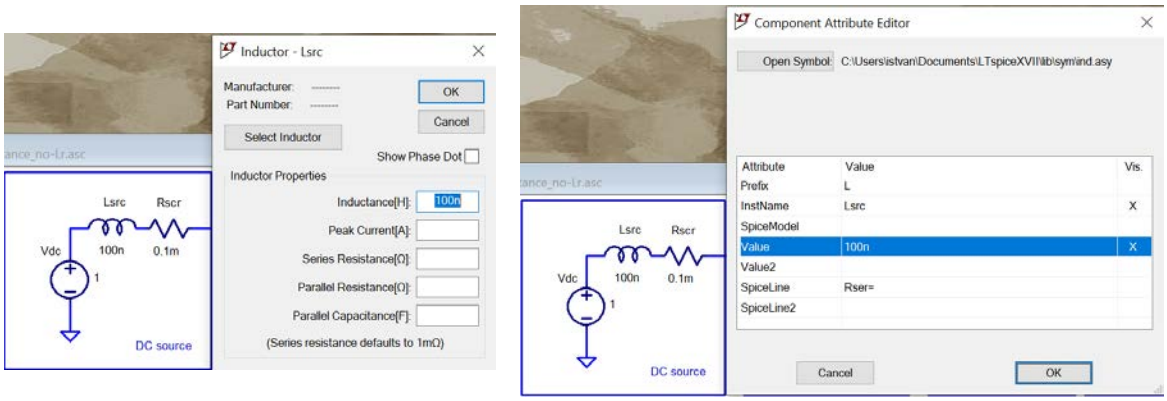

Figure 7.: *Parasitic definitions of the Lsrc inductor.*

If we explicitly call out zero for the series resistance parasitics on all inductors, we get *Figure 8.* Now the low-frequency value starts at the correct 1.3 mOhm value, but we can also notice that the first two peaks got a little bigger. This is happening because we removed the extra series resistances, which helped to lower the antiresonance peaks. Note that with the circuit values used in this example, explicitly calling out zero body capacitance for the inductors will not change the result.

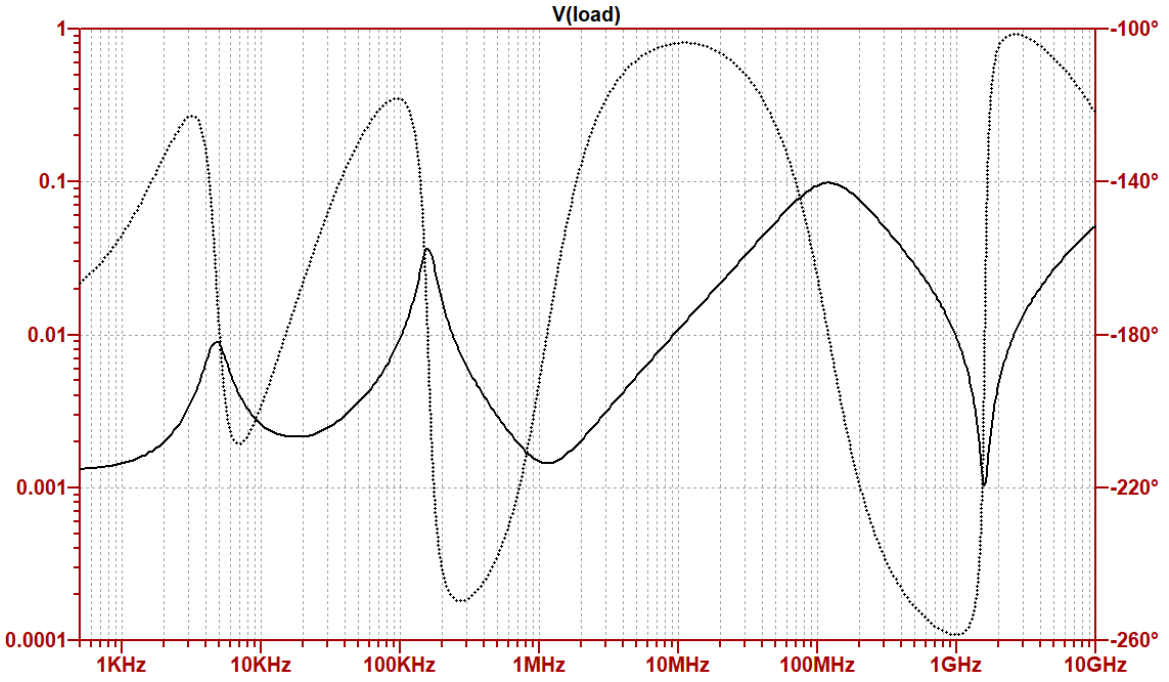

Figure 8.: *Impedance magnitude and phase of the simple PDN showed in Figure 1, with forcing zero body capacitance of capacitors and zero series resistance of inductors.*

This is eventually what we expect: smooth impedance profile, no unexpected and 'unexplained' sharp resonances, asymptotic low-frequency impedance matches the sum of series resistance values.

We are almost done, but it still would be useful to check the capacitor's equivalent circuit one more time and take another look at the body capacitance. To make it simple, we look at a single capacitor as shown in *Figure 9*. We set the main capacitance as a parameter so that we can step it and set the ESR and ESL to fixed values, 10 mOhm and 1 nH, respectively. To see what happens, intentionally we do not specify the parallel body capacitance; the entry is left blank. We step the capacitance from 1 pF to 1F in four large logarithmic steps and sweep the frequency from 1 mHz to 1 THz. The result shows that in fact a parallel body capacitance is added by the simulator, but its value is not fixed, it depends on the other parameters. With the values used here, the body capacitance seems to be approximately one million times smaller than the main capacitance. While this looks like a huge ratio (and it is!), we see that if we simulate our circuit over many decades of frequencies, this small default body capacitance value still can cause unexpected artifacts. The good news is that it is easy to deal with, we just have to remember to call out specifically zero body capacitance, unless, of course, when we know its correct value and want to simulate the effect of the body capacitance.

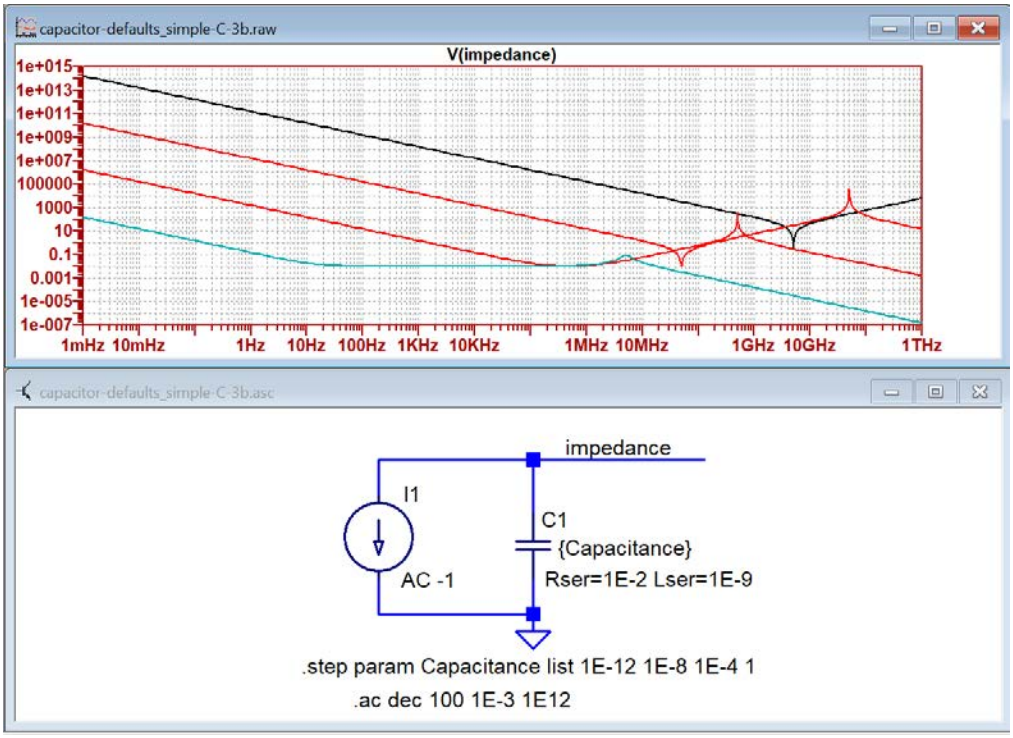

Figure 9.: *Checking the body capacitance default value for the capacitor model.*

And a final note: remember that all numerical tools have to set limits to the input numbers they can accept and can process, whether the tools will tell you and remind you or not. So

next time when you see unexpected things in circuit-simulation results, make sure first that the input numbers, including potential defaults, are set correctly.

References:

[1] Parallel Impedance of Four Groups of Capacitors, http://www.electrical-integrity.com/Tool_download_files/Bypass_four-banks_v-w04.xls

[2] High Frequency Structure Simulator, https://www.ansys.com/products/electronics/ansys-hfss

[3] Berkeley SPICE, http://bwrcs.eecs.berkeley.edu/Classes/IcBook/SPICE/

[4] LTSPICE, https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html

[5] LT wiki, http://ltwiki.org/