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Uncompensated DC Drop in Power Distribution Networks

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One reoccurring question I get is how to factor the DC drop into the power distribution network design process. Whether you prefer time-domain based or frequency-domain based design approach, the DC drop on the distribution path has to be taken into account. This article walks you through some of the important options and considerations.

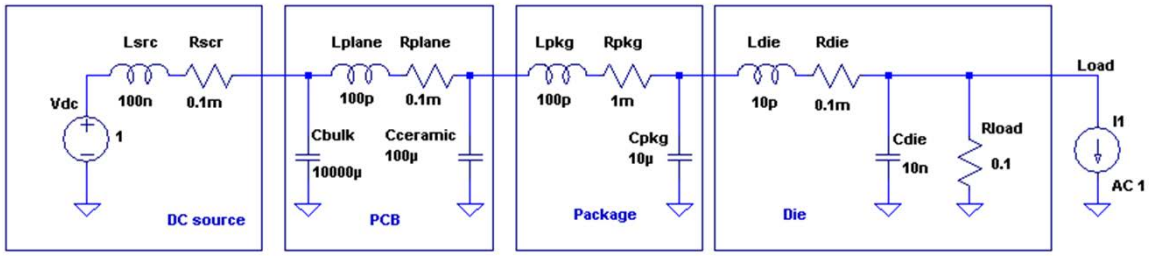

Figure 1.: *Simplified block schematics of a 1V 10W point-of-load (POL) power distribution network.*

To connect the source to the load, the power distribution network has series conductive elements (connectors, cables, PCB planes, traces and potentially also inductors, ferrite beads, current-sense and current-limiting devices) and parallel bypass capacitors. In our typical electronic circuit we feed our load with clean DC power with a known, regulated voltage. The active DC source in the example of *Figure 1* could be a linear or switching regulator, monitoring and keeping its average output voltage constant across its output connections. In such a scenario, as shown in *Figure 2*, due to the uncompensated voltage drop across the resistances of the series elements between the source and load, the voltage across the load will be less than what we wanted.

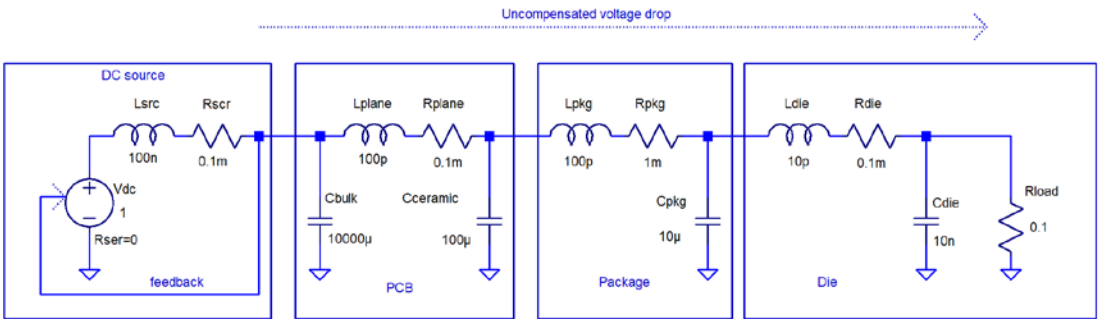

Figure 2.: *Voltage regulator with feedback loop monitoring the output connections of the regulator.*

For our power distribution networks we need to start a systematic design by finding the noise budget. *Figure 3* shows its elements. The vertical height of each line represents voltage with respect to the reference (we may call it ground), which is not shown; if drawn proportionally for a supply rail where the maximum voltage deviation is just a few percent of the nominal voltage, the reference line would be a few pages further down. The $V_{max} – V_{min}$ range is what our load can tolerate at any given moment. If the load current changes with time, we will have some transient noise; it is represented by ΔV on the sketch. The purpose of the sketch is to illustrate the process how we can calculate the ΔV range that is allowed for transient noise.

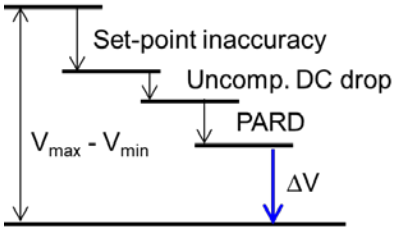

Figure 3.: *Components of the noise budget.*

The $V_{max} – V_{min}$ range is not entirely available for the ΔV transients. The linear and switching regulators have a finite accuracy how accurately their nominal voltage can be set and how much it may drift over time, over the specified temperate range, due to unit-to-unit variations, changes of input voltage, etc. We call that range the Set-point inaccuracy. PARD stands for Periodic and Random Deviation and it captures any self-generated AC fluctuation of the DC source itself. In switching regulators, it is primarily the switching ripple on the output. In linear regulators we don't have switching ripple, but the electronics in the regulators still has some random noise, which may be important to know for very sensitive loads. And we also have the Uncompensated DC drop. We have to subtract all of these from the $V_{max} – V_{min}$ range to get ΔV.

There are several details that are useful to keep in mind when we consider uncompensated voltage drop. The first is the obvious complication when we think about the entire flow of the design from beginning to end: when we start our design process, we don't have any details worked out yet and still we need an input number – the uncompensated DC drop- which eventually will depend on the stackup, material choice (remember: electro-deposited and rolled-annealed coppers have slightly different conductivity!), component placement and layout. We need to accept the inevitable: if we try to push the envelope and make a cost-effective, lean and optimized design, the design process will be iterative. There is one trick though that may help us under some circumstances: if we know that the load current is not changing much with time, with temperature and due to unit-to-unit differences, we can easily remove most of the uncompensated voltage drop even if the regulator sense point is monitoring the voltage before the voltage drop happens. As long as the voltage drop is not so huge that the regulator could not compensate for it, for the design process we can assume zero uncompensated voltage drop. With this assumption we complete the entire design and once we figure out what is the actual voltage drop beyond the sense point, we just statically raise the regulator's output voltage by that amount.

For cases when the DC load current may change a lot, we can use regulators with an external sense connection and route it on the board close to the load, as shown in *Figure 4*.

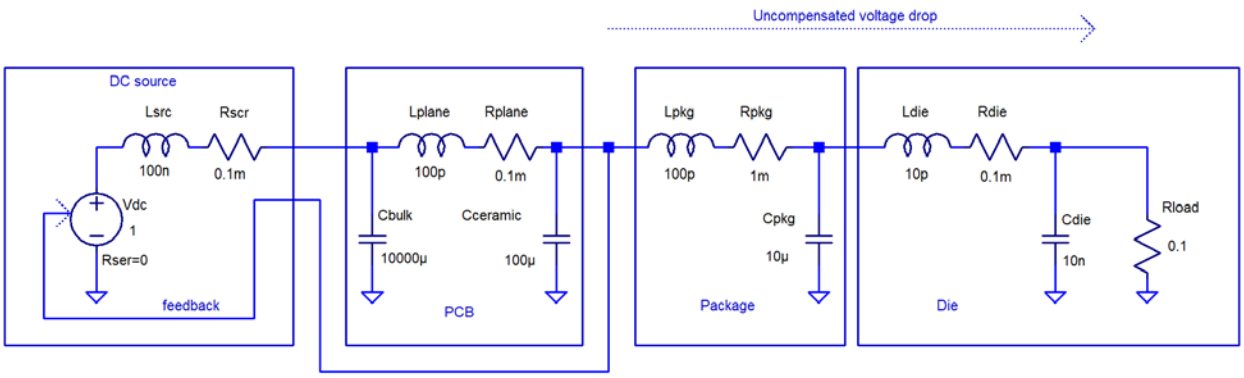

Figure 4.: *Voltage regulator with sense connection at the board-package interface.*

If our design process does not include the package and our design requirements are formulated at the board-package interface, we are all set: connecting the voltage regulator sense point on the board under the package removes the majority of the uncompensated voltage drop.

Some chips have sense-point connection pins, which route out sensitive silicon areas so that we can connect to them the voltage regulator's sense line, thus removing the uncompensated voltage drop all the way to the targeted silicon cells. This case is shown in *Figure 5*.

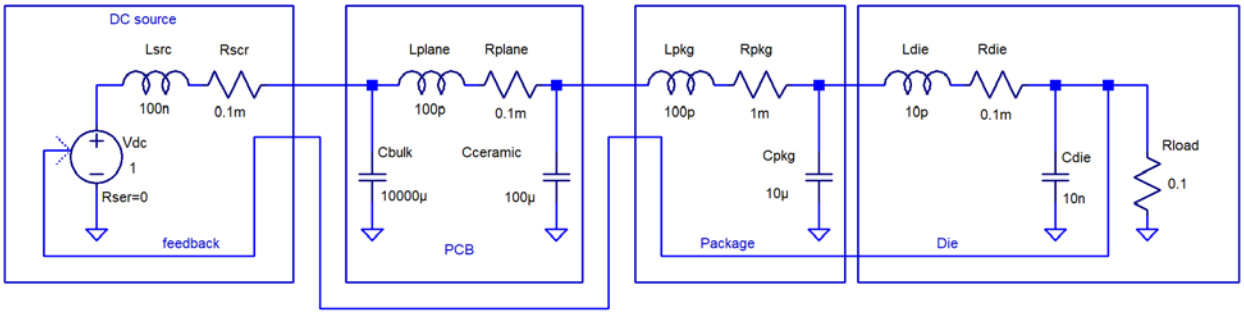

Figure 5.: *Voltage regulator's sense point connected to the load's sense line allows the removal of the entire uncompensated voltage drop.*

There is one more case worth mentioning. Sometimes the switching regulator's output ripple is too big for a sensitive load and lowering the switching ripple magnitude just by adding more capacitance on the regulator's output is not a good option. In such cases a downstream linear regulator or a series LC filter may be the best solution. *Figure 6* shows this case. The LC filter

usually adds to the DC voltage drop, so we may need to connect the regulator's sense point further downstream after the LC filter.

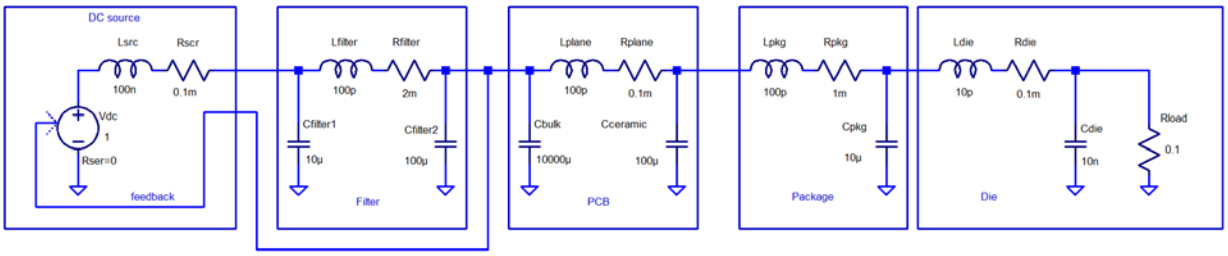

Figure 6.: *Power distribution network with a single-stage LC filter to reduce the switching ripple of the regulator.*

In all of these cases the lowering of the uncompensated DC drop comes with a potential problem: if we connect the regulator's sense point further away from the regulator, the phase shift along that path may reduce the stability margin of the regulator's feedback loop. In extreme cases this can also happen even if we do not have an additional LC filter. As it was shown in [1], the DC resistance of a power rail with the bulk capacitors may produce noticeable phase shift near the crossover frequency of typical regulators. *Figure 7* shows the sketch of the board layout from [1], *Figure 8* shows the resulting difference caused by miniscule layout differences between the two PDN rails layouts.

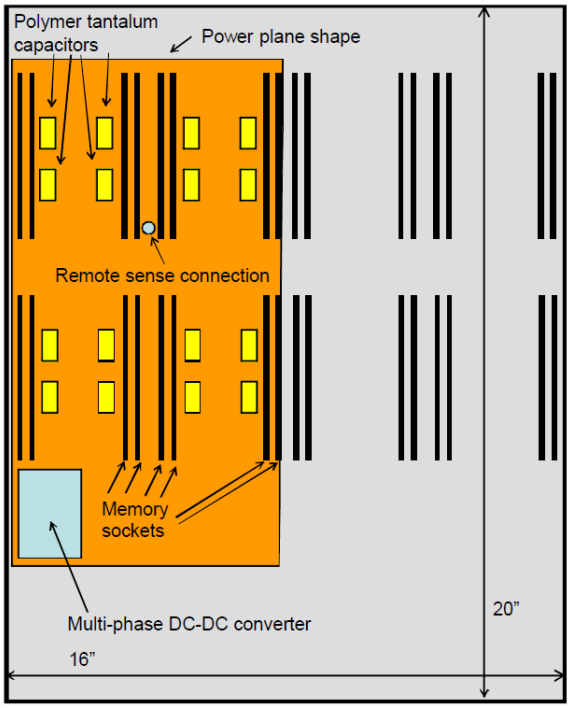

Figure 7.: *Layout sketch of a large memory board with two PDN rails with mirror-image component placement and layout.*

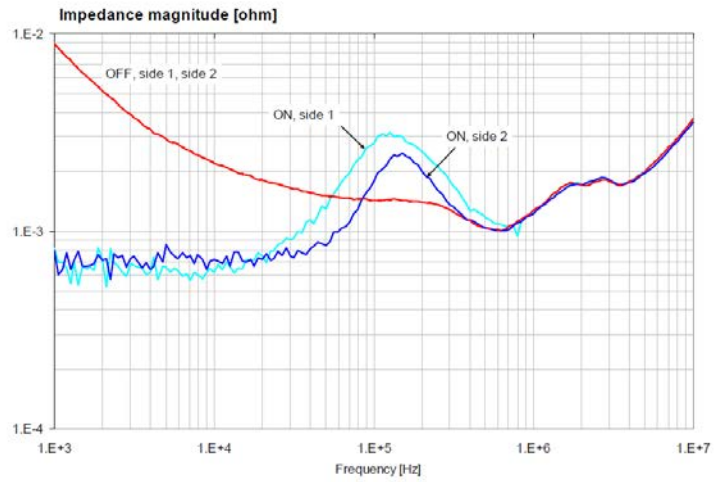

Figure 8.: *Measured impedance profiles of the two PDN rails.*

Note the marked difference in the two impedance profiles. Follow-on tests and analysis showed that the two power rails had systematically different phase shift at the converter's crossover frequency due to very minor layout differences between the two sides.

If we need to supply power to more than one load with the same regulator, in lucky cases may have two nominally identical chips, drawing approximately the same current. If we have to position them far enough so that routing power through them sequentially would leave too much uncompensated voltage drop, a symmetric fork may be our best option. Such a case is shown from [2] in *Figure 9*. A single sense point symmetrically between the two loads will eliminate most of the uncompensated voltage drop.

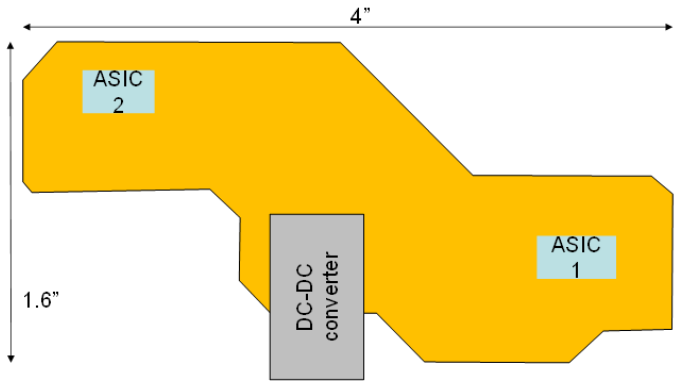

Figure 9.: *Suggested layout if the voltage regulator has to feed two identical loads.*

In these days professional tools can do a good job to simulate the DC voltage drop on power planes, vias and traces, so after completing the layout, it is always a good idea to check the DC drop to make sure that our design meets the requirements.

When it comes to the very fine details, several other factors may need to be considered. For instance, how dop we deal with the voltage drop across a large pin field connecting a power-hungry chip? Do we need to consider the micro detail of the voltage drop across large pads of power connections? How would the simulated DC drop change if we take the non-vertical sidewalls of copper etching of printed circuit boards into account? Those could be important aspects in a high-end design and may be the subject of future articles.

And a final closing thought. For sake of simplicity, the voltage diagram of *Figure 3* does not include margin: however, in a real design it is always a good idea to add the typical 10-20% margin for any unaccounted contributor.

References, further reading:

[1] Impact of Regulator Sense-point Location on PDN Response. DesignCon 2015. Available at: http://www.electrical-integrity.com/Paper_download_files/DC15_11_FR1_Paper_ImpactofRegulatorSense_point.pdf

[2] How Spatial Variation of Voltage Regulator Output Impedance Depends on Sense Point Location. DesignCon 2018. Available at: http://www.electrical-integrity.com/Paper_download_files/DC18_PAPER_Track11_HowSpatialVariationofVoltage_Miranda_updated__.pdf