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Noise Mitigation in Power Planes

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Inductive kick has been a well-known phenomenon in the electronic industry from very early on. First associated with motors, AC-mains transformers and mechanical relays, people noticed large voltage spikes when the current-carrying circuit was opened. Later as more sophisticated electronic circuits emerged, the same thing was noticed any time when current was changing through an inductor, or for that matter, through any inductance, whether it was an intentionally placed discrete inductor piece or just the parasitic inductance associated with a current path. This phenomenon is captured by the third Maxwell equation, which describes Farady's Law. For an introductory overview and summary, see for instance [1]. In its simple form we know this rule from signal integrity as it describes the Δv ground bounce as a function of the dI/dt rate of change of current through an inductance of L:

$$\Delta v = L\frac{dI}{dt}$$

In today's electronics, the components are held and connected by printed circuit boards, which have been around for several decades. The front and back side of a small printed circuit board I designed, etched and populated in the late 1960s, are shown in *Figure 1*.

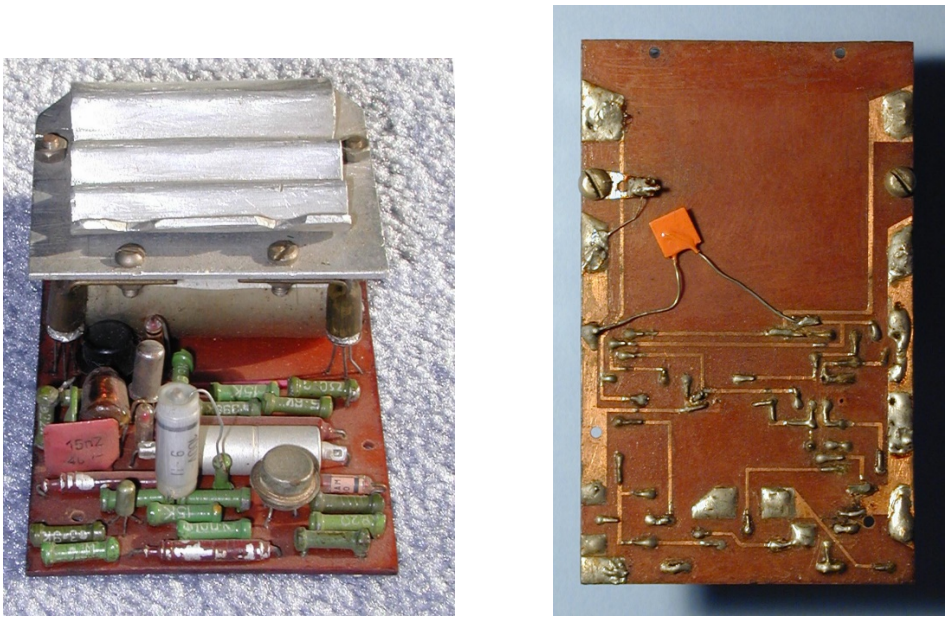

Figure 1: *Small battery-powered audio amplifier on a single-sided printed circuit board from the late 1960s.*

It was the audio amplifier for a battery-powered portable radio, using all Germanium transistors. The printed circuit board dielectric was unreinforced, fairly brittle, and to connect all components it was enough to use copper traces only on the back side of the board. The power and ground nets were carried by the wider etches near the two edges of the board. Being an analog audio amplifier using low-frequency transistors with a transit frequency in the order of a megahertz, the circuit did not create high-frequency or high-speed noise and to carry power around simple traces with no special high-frequency bypassing were sufficient. Though the L inductance of the widely-spaced power and ground traces must have been very high, possibly in the tens of nHs, the noise across it was low because the dI/dt rate of current change was even smaller.

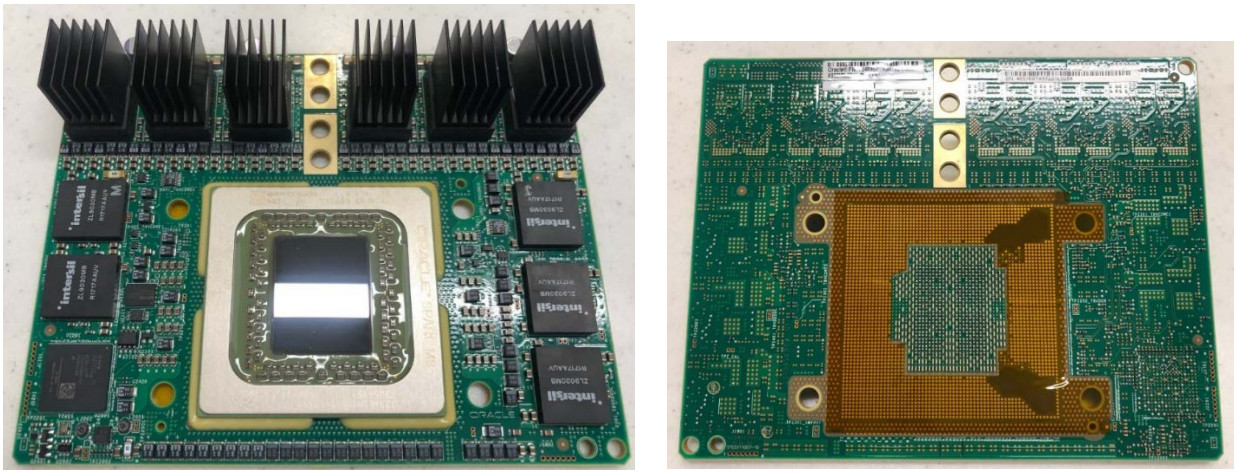

Figure 2: *CPU module from the late 2010s.*

Fast-forward about fifty years; *Figure 2* shows the front and back of a CPU module from the late 2010s [2]. I designed the power distribution network for this board that consumed hundreds of watts, had 20+ layers and used several hundred bypass capacitors. The board had multiple solid ground layers and multiple power planes for the high-current supply rails. The power and ground planes in close proximity produced very low inductance in the tens of pH range, which was necessary to counter the high dI/dt of the chip.

Large power planes provide not only lower inductance, they are also necessary to keep the DC voltage drop low. However, power planes come with some downsides: they do produce resonances that can interfere with both the power delivery or most likely, with our high-speed signaling. We know that signal traces will resonate if we don't terminate them properly. Even with proper terminations at the ends, additional reactances along the signaling channel can create quarter-wave or half-wave resonances [3]. Traces are one-dimensional transmission lines, exhibiting a series of modal resonances associated with their length. Traces are one-dimensional, because we have to keep the trace width and dielectric separation much smaller than the shortest wavelength of interest. In contrast, planes are two-dimensional resonators and rectangular plane pairs exhibit modal resonances both along their length and width [4]. As an illustration, *Figure 3* shows a simulated impedance surface created by the standing-wave pattern on a 2:1 aspect ratio rectangular plane pair.

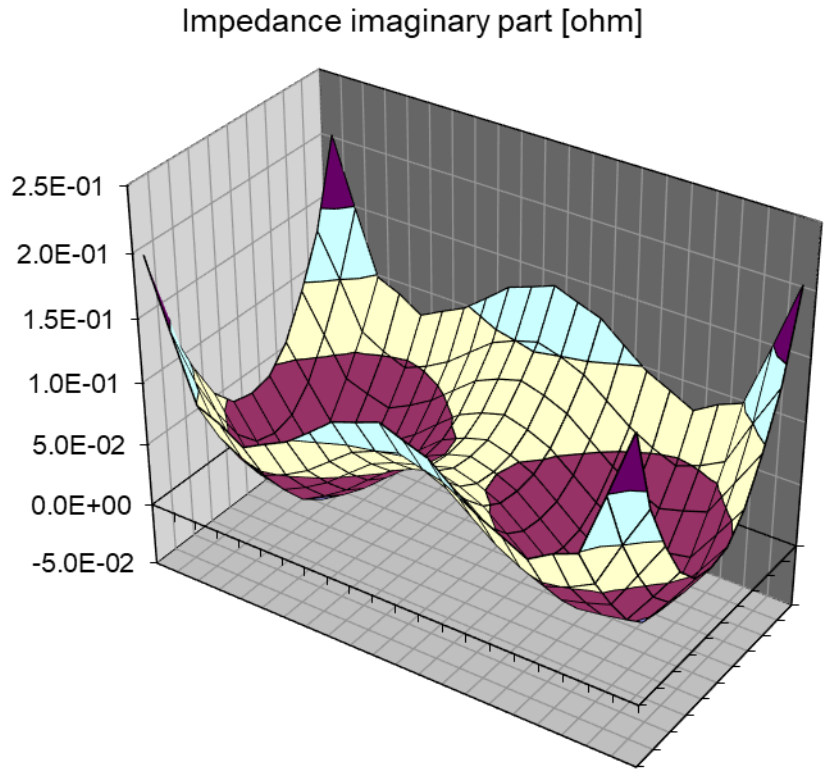

Figure 3: *Impedance magnitude showing two-dimensional standing-wave pattern on a rectangular pair of power ground planes.*

Depending on the resonance frequencies and the functionality of our circuit on the board, the standing waves and resonances can create issues in any of our major disciplines: signal integrity, power integrity or electromagnetic compatibility. At locations and frequencies where the impedance is high, a signal via going through the power-ground plane cavity will introduce a dip in the trace's transfer function (S_{21}), which could be a signal-integrity problem. At the same locations and frequencies power noise will also be higher and if at those frequencies there is sufficient excitation energy from our circuit, the conducted noise can create power integrity issues and the circuit potentially could also radiate enough to create electromagnetic compatibility issues.

If we determine that the resonances could impose a risk to the operation of our circuit, we have a few options to deal with it. One possibility is to push the resonance frequencies high enough that our high-speed signals or power noise from our circuit will not excite them. Since we often use power planes to feed multiple electronic devices on our boards, this possible solution depends on

how may devices we need to feed and what are our constraints for their placement. If this mitigation does not work, we have to find a way to suppress the modal resonances. One 'easy' solution is if the density of our bypass capacitors is so high that eventually the cumulative impedance of bypass capacitors become dominant at the resonance frequencies. While this is a practical possibility and may often happen in very dense and physically small applications, large boards may require too many components to make this a viable option. Another alternative is to use power-ground plane pairs on thin enough laminates that naturally will suppress modal resonances. As it was explained and documented in [6], the natural attenuation of a power-plane pair increases with decreasing dielectric thickness. With medium and large size boards, a dielectric thickness of 25um (one mil) or less greatly suppresses the resonances. As an illustration, *Figure 4* shows measured transfer impedance plots on the same board design manufactured with different dielectric thickness values.

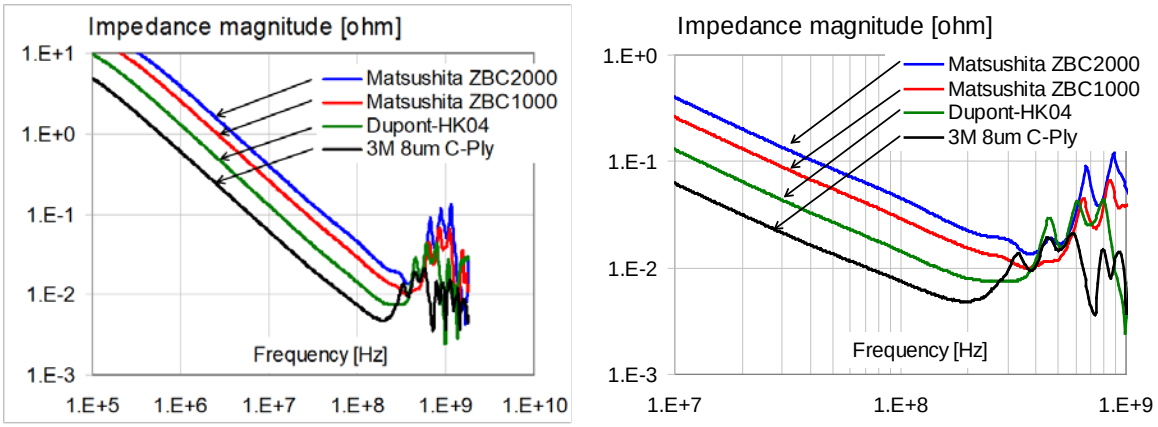

Figure 4: *Transfer impedance plots of measured transfer impedances with different laminate thickness values. Reproduced from [6].*

However, laminates thinner than 75um (3mils) come with a price premium and we also need to consider the usual stackup requirements calling for symmetry. This means we can not just use one thin laminate layer, we need to use them in pairs in the stackup, even if the circuit would otherwise require only one. Also, in case only a smaller portion of a larger board would require the suppression of plane resonances, we will end up with the same thin laminate horizontally everywhere on the board, also where do don't really need it. In those applications we can consider another potential solution: terminating the planes (see for instance [7]), just as we reduce trace resonances by connecting the proper termination resistance to both ends. Since planes do not have well-defined 'ends;' as traces do, we need to connect termination components along their periphery. Power-plane pairs, except for a few special shapes, do not have a specific characteristic impedance and therefore we need to rely on approximations, such as this approximation of a rectangular plane pair with x and y horizontal dimensions:

$$Z_p = \frac{266\left(\frac{h}{x}\right)}{\sqrt{\varepsilon_r}\left(1+\frac{y}{x}\right)} = \frac{532}{\sqrt{\varepsilon_r}}\frac{h}{P}$$

Where

Z_p is the approximate characteristic impedance of the plane pair in ohms

ε_r is the relative dielectric constant of the laminate

h and P are the laminate thickness and periphery in arbitrary, but identical units.

With typical plane sizes and laminate thickness values we use today, the impedance comes out in the tens to hundreds of milliohms range. We need to match this impedance with a number of termination elements, placed around the plane periphery. The number of elements depends on our frequency of interest. We need to make sure that up to the highest frequency of interest, often chosen as the tenth harmonic in the modal resonance series, the phase difference between adjacent termination components is much less than 90 degrees. As a result, we typically end up with a centimeter or so spacing. We then take the P periphery of plane shape and divide by the spacing between adjacent elements and it gives us the N number of terminations. Each termination resistor has to have an $N*Z_p$ value, many times it comes out as a few ohms. We also add a small series capacitor in series to each termination resistor to avoid 'shorting' the power-ground plane pair with the termination resistance. Terminating power planes was an attractive and viable solution a couple of decades ago when computer systems still had a lot of single-ended signaling and fewer supply rails with larger planes. In these days it still could be a viable alternative if system constraints prevent us from placing bypass capacitors to their optimum location. An example of plane termination on a recent computer board in volume production was described in [8]. In this case the very high density of memory sockets ruled out the placement of bypass capacitors next to the power pins of memory sockets. The simulated and measured impedance of that supply rail is reproduced from [8] in *Figure 5*. Note the logarithmic vertical scale; using the proper termination components, the peak impedance was reduced by at least a factor of two.

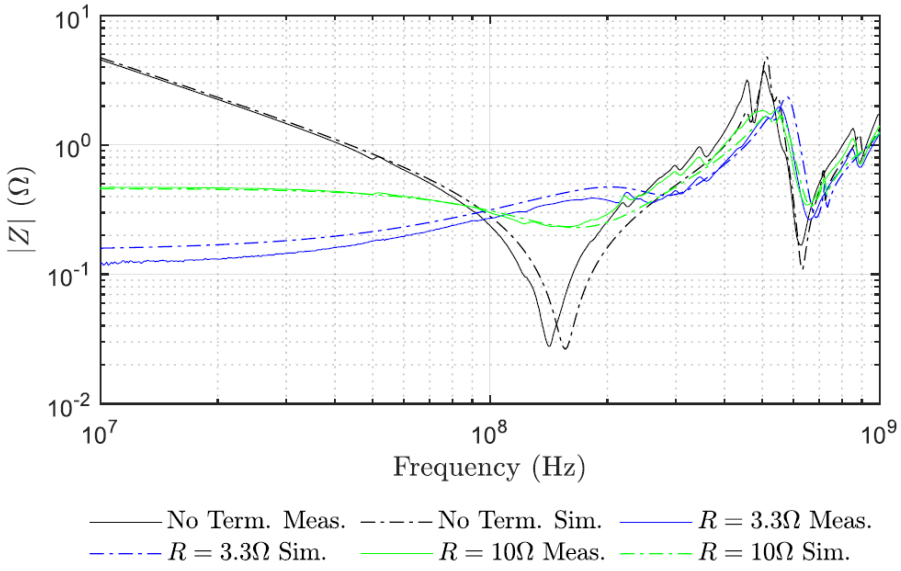

***Figure 5**: Simulated and measured power rail impedance on a production board with and without resistive edge termination.*

Conclusions

Power planes provide a convenient means to connect multiple loads to a single power rail, but they introduce a series of modal resonances. The resonances can be suppressed by a large number of bypass capacitors, or by using sufficiently thin dielectrics or by placing termination components along the plane periphery.

References, further reading:

[1] https://byjus.com/physics/maxwells-equations/

[2] Is Power Integrity the Next Black Magic? Keynote webinar talk at E-learning By Cadence, April 12, 2021

[3] Gustavo Blando, “Those Pesky Half-Wave Resonances,” Signal Integrtity Journal, October 19, 2021

[4] Carver, K. R., and Mink, J. W., "Microstrip antenna technology," IEEE Transactions on Antennas and Propagation, AP-29, 1981, pp. 2-24.

[5] Frequency Domain Characterization of Power Distribution Networks. Artech House, July 2007. ISBN-13: 978-1-59693-200-5

[6] “SUN’s Experience with Thin and Ultra Thin Laminates for Power Distribution Applications,” DesignCon2006, Santa Clara, CA, February 6-9, 2006

[7] “Distributed Matched Bypassing for Power Distribution Network,” IEEE Tr. CPMT, August 2002

[8] “Impact of Power Plane Termination on System Noise,” DesignCon 2021, San Jose, CA, August 16 - 18, 2021