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3D Effects in Power Distribution Networks

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Signal integrity (SI) gradually became a topic on its own right and grew out of the electromagnetic compatibility (EMC) discipline in the early 90s. In fact, the book that in my personal opinion was really the first on signal integrity, did not even have signal integrity in its title: it was called Introduction to Electromagnetic Compatibility, by Clayton Paul. And then about a decade later power integrity (PI) also became a hot topic and created a separate discipline with multitude of books and conference sessions devoted to it.

Originally, SI was based on high-frequency RF and microwave knowledge, whereas PI tasks in those days were handled primarily by AC-DC and DC-DC power supply designers, who care for the low-frequency behavior of circuits. Though it has been understood all along that the same basic physics rules and principles apply to both SI and PI, the separate high-frequency and low-frequency considerations led to seemingly disconnected design rules.

Take for instance three-dimensional (3D) effects. We usually associate 3D effects with high-frequency SI problems, where the full-wave solution of Maxwell equations becomes necessary. This can happen for instance when we analyze a right-angle turn in a printed-circuit board (PCB) trace or look at the high-speed behavior of a plated through hole (PTH). In SI, the full-wave effects become more noticeable at higher frequencies, where the physical dimensions are not negligibly small any more compared to the wavelength. Based on all this it may be surprising to realize that in power integrity 3D effects can equally show up at very low frequencies, sometimes in the kHz region, even at DC. These 3D effects are created by specific patterns and changes in the current density in conductors. As shown in Figure 1, the density of DC current at a sharp right-angle turn of a power strip will be very small at the outer point of the corner and could be very high at the inner corner.

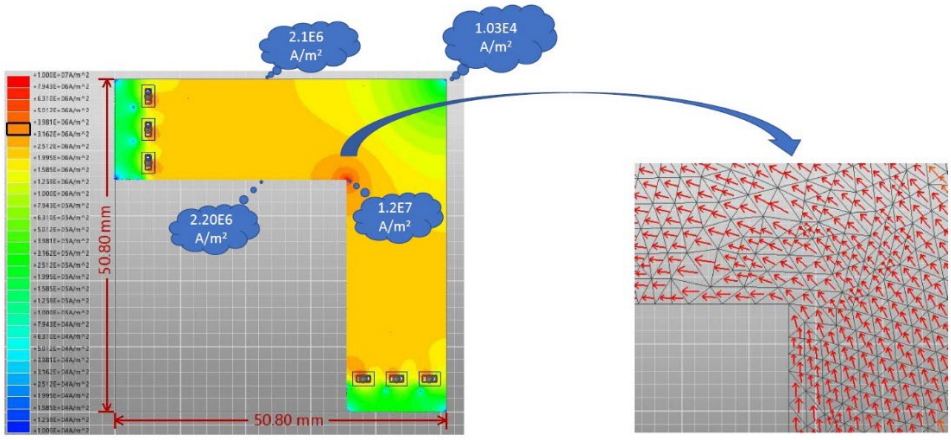

Figure 1: Simulated DC current density of a power strip making a right-angle sharp turn, as described in detail in [1]. There is a total of 1A through a one-oz half-inch wide copper strip.

We know that high-speed traces with a sharp bend will suffer from the capacitive loading at the outer 'unused' portion of the turning trace. We see in Figure 1 that at DC the outer corner is equally 'unused', except at DC it does not cause problems, it is just not necessary to have copper there. Instead, the problem at DC shows up at the opposite side of the power strip, at the inner corner, where the current density may exceed the safe limit.

Another example of complex three-dimensional behavior at low frequencies was documented by measured and simulated data in [2], where the conductor geometry and the component placement interacted in a way that created a negative phase and negative slope of the magnitude of impedance. Shown in Figure 2, the circuit in question was a small fixture, consisting of two back-to-back SMA edge-mount coaxial connectors and four 10 mOhm surface-mount resistors.

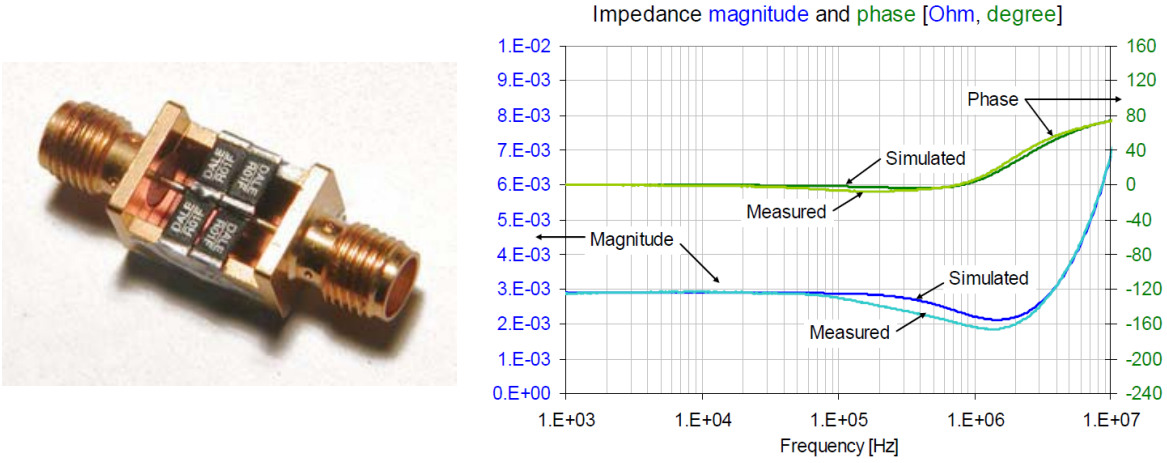

Figure 2: Small fixture with two coaxial connectors and resistors on the left, measured and simulated impedances on the right (after [2])

With just metal pieces and resistors, we would expect an R-L like impedance profile. But the frequency dependency in this case looks like as if we had the series resonance of a low-Q bulk capacitor at around 1.5 MHz. However, there is no capacitor in this circuit, not one that could create a series resonance at 1.5 MHz. Instead, as explained and correlated in [2], the reason for the impedance dip is the distributed nature of the resistance and inductance of the ground pegs of the SMA connectors interacting with the multiple pieces of R-L parallel shunt elements created by the four resistors.

As detailed in [3], 3D effects at relatively low frequencies also show up in wafer-probe PDN measurements. Figure 3 on the left shows a computer rendering of two wafer probes measuring a chip's core power supply across two adjacent power-ground via pairs in a 1-mm array. The inductive coupling between the two loops formed by the probe tips has to be removed from the measured data, either by deembedding or by calibration. The coupling can be characterized on appropriate calibration substrates; the mutual inductance between the probe tip loops is shown on the right for three different probe tip geometries. Note that the mutual inductance has different frequency dependency at low frequencies for the three probe geometries.

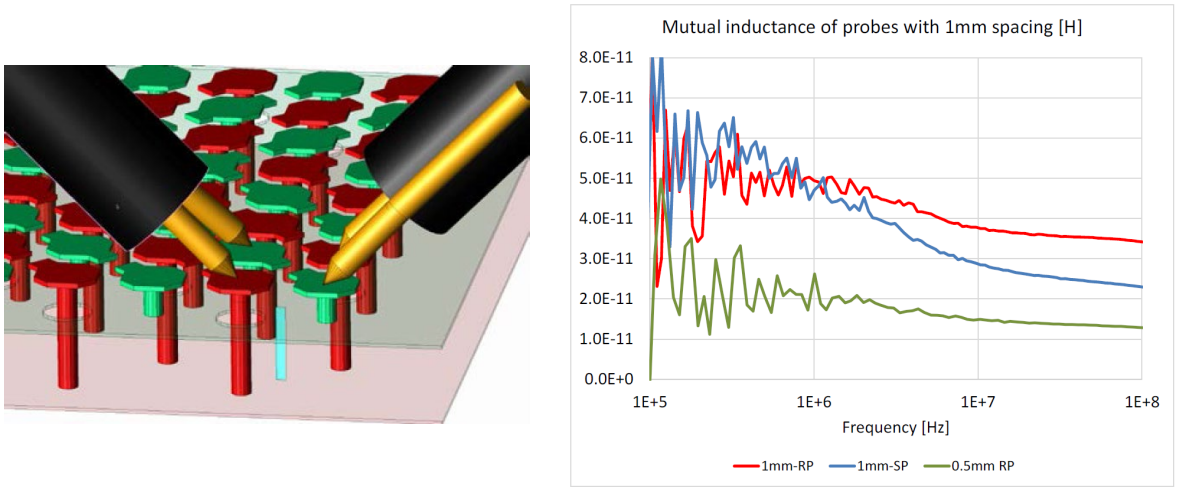

Figure 3: Wafer probe landing on a via-grid array (on the left) and the mutual inductance between the probe-tip loops as a function of frequency (on the right).

Conclusions

Regardless of the frequency, three-dimensional interactions among electrically small features noticeably impact the PI simulations and measurements as well.

References:

[1] "The Perils of Right-Angle Turns at DC," gEEk spEEk, May 14, 2020, available at https://blog.samtec.com/05_14_2020_geek_speek_perils_ra_turns/

[2] "Accuracy Improvements of PDN Impedance Measurements in the Low to Middle Frequency Range," DesignCon 2010, February 1-4, 2010, Santa Clara, CA

[3] "3D Connection Artifacts in PDN Measurements," DesignCon 2023, January 30 – February 2, 2023, Santa Clara, CA